LH79524/LH79525 (A.1)
System-on-Chip

Preliminary data sheet

FEATURES

- Highly Integrated System-on-Chip
- High Performance: 76.205 MHz CPU Speed, 50.803 MHz maximum AHB clock (HCLK)
- 32-bit ARM720T™ RISC Core
  - LH79524: 32-bit External Data Bus
    - 208 LFBGA package
  - LH79525: 16-bit External Data Bus
    - 176 LQFP package
- 8 kB Cache with Write Back Buffer
- MMU (Windows CE™ Enabled)
- 16 kB On-Chip SRAM
- Flexible, Programmable Memory Interface
  - SDRAM Interface
    - 512 MB External Address Space
    - 32-bit External Data Bus (LH79524)
    - 16-bit External Data Bus (LH79525)
  - SRAM/Flash/ROM Interface
    - 15-bit External Address Bus
    - 32-bit External Data Bus (LH79524)
    - 16-bit External Data Bus (LH79525)
- Multi-stream DMA Controller
  - Four 32-bit Burst-Based Data Streams
- Clock and Power Management
  - 32.768 kHz Oscillator for Real Time Clock
  - 10 MHz to 20 MHz Oscillator and On-chip PLL
  - Active, Standby, Sleep, Stop1, and Stop2 Modes
  - Externally-supplied Clock Options
- On-Chip Boot ROM
  - Allows Booting from 8-, 16-, or 32-bit Devices
  - NAND Flash Boot
- Low Power Modes
  - Active Mode: 85 mA (MAX.)
  - Standby Mode: 50 mA (MAX.)
  - Sleep Mode: 3.8 mA (TYP.)
  - Stop Mode 1: 420 μA (TYP.)
  - Stop Mode 2: 25 μA (TYP.)
- USB Device
  - Compliant with USB 2.0 Specifications (Full Speed)
  - Four Endpoints
- Ethernet MAC, with MII and MDIO Interfaces
  - IEEE 802.3 Compliant
  - 10 and 100 Mbit/s Operation
- Analog-to-Digital Converter/Brownout Detector
  - 10-bit ADC
  - Pen Sense Interrupt
  - Integrated Touch Screen Controller (TSC)
- I^2C Module
- Integrated Codec Interface Support Features (I^2S)
- Watchdog Timer
- Vectored Interrupt Controller
  - 16 Standard and 16 Vectored IRQ Interrupts
  - Interrupts Individually Configurable as IRQ or FIQ
- Three UARTs
  - 16-entry FIFOs for Rx and Tx
  - IrDA SIR Support on all UARTs
- Three 16-bit Timers with PWM capability
- Real Time Clock
  - 32-bit Up-counter with Programmable Load
  - Programmable 32-bit Match Compare Register
- Programmable General Purpose I/O Signals
  - LH79524: 108 available pins on 14 ports
  - LH79525: 86 available pins on 12 ports
- Programmable Color LCD Controller
  - 16 (LH79524) or 12 (LH79525) Bits-per-Pixel
  - Up to 800 × 600 resolution
  - STN, Color STN, HR-TFT, AD-TFT, TFT
  - TFT: Supports 64 k (LH79524) or 4 k (LH79525) Direct Colors or 256 colors selected from a Palette of 64 k Colors; 15 Shades of Gray
  - Color STN: Supports 3,375 Direct Colors or 256 Colors Selected from a Palette of 3,375 Colors
- Synchronous Serial Port
  - Supports Data Rates Up to 1.8452 Mbit/s
  - Compatible with Common Interface Schemes
- JTAG Debug Interface and Boundary Scan
- 5 V Tolerant Digital Inputs (excludes oscillator pins)
  - XTALIN and XTAL32IN pins are 1.8 V ± 10%
- On-Chip regulator allows single 3.3 V supply

DESCRIPTION

The LH79524/LH79525, powered by an ARM720T, is a complete System-on-Chip with a high level of integration to satisfy a wide range of requirements and applications**.** The SoC has a fully static design, power management unit, and low voltage operation (1.8 V Core, 3.3 V I/O). With the on-chip voltage regulator, a single 3.3 V supply can be used as well. Robust peripherals and a low-power RISC core provide high performance at a reasonable price.

ORDERING INFORMATION

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
LH79524N0F100A0	LFBGA208	plastic low profile fine-pitch ball grid array package; 208 balls	SOT1019-1
LH79524N0F100A1	LFBGA208	plastic low profile fine-pitch ball grid array package; 208 balls	SOT1019-1
LH79525N0Q100A0	LQFP176	plastic low profile quad flat package; 176 leads; body 20 x 20 x 1.4 mm	SOT1017-1
LH79525N0Q100A1	LQFP176	plastic low profile quad flat package; 176 leads; body 20 x 20 x 1.4 mm	SOT1017-1

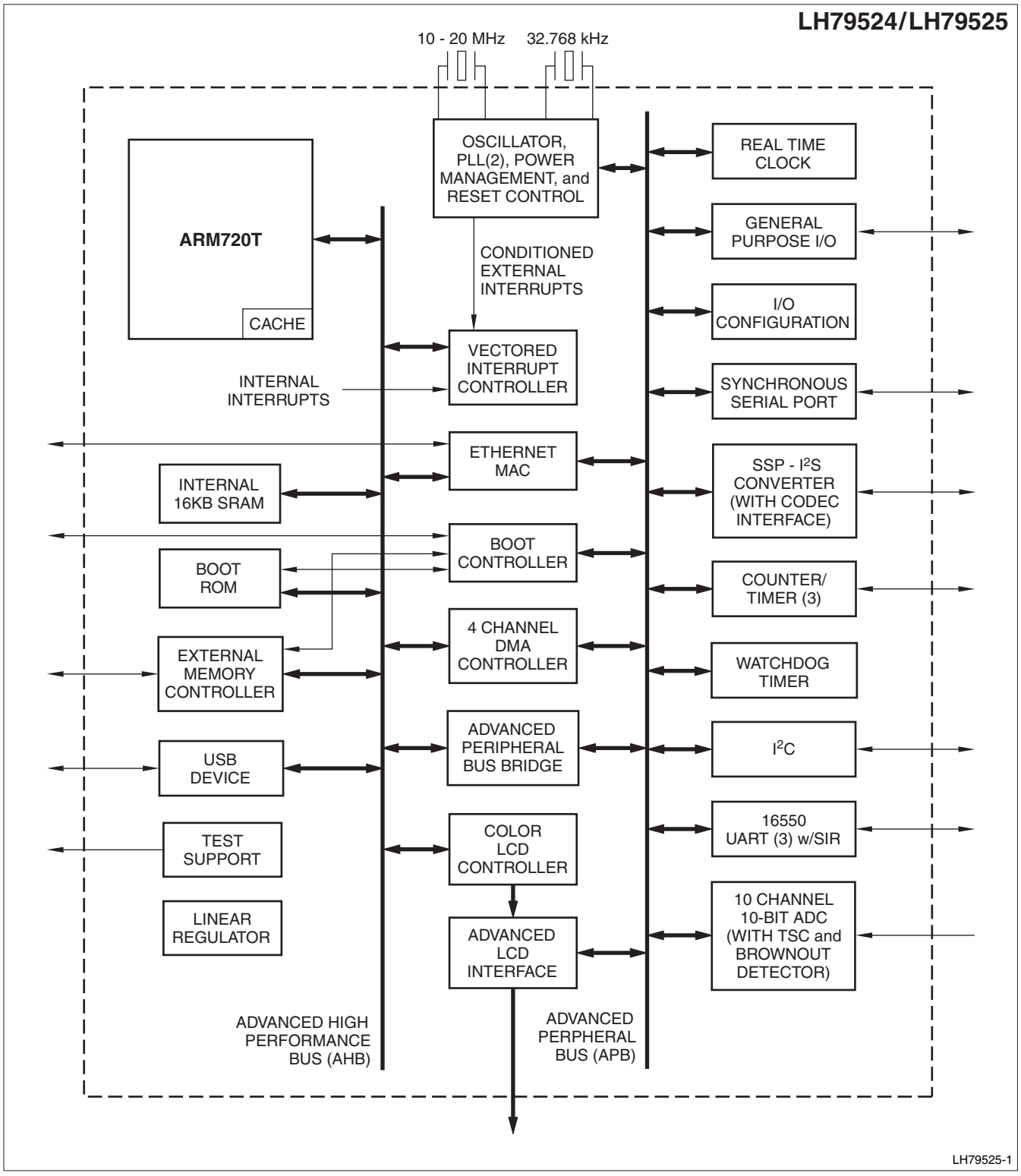


Figure 1. LH79524/LH79525 block diagram

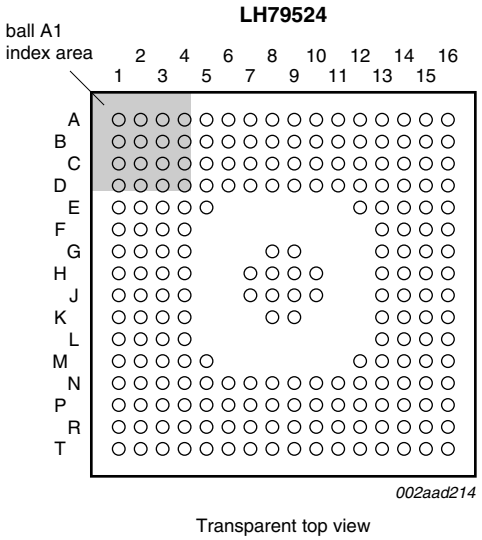


Figure 2. LH79524 pin configuration (LFBGA208)

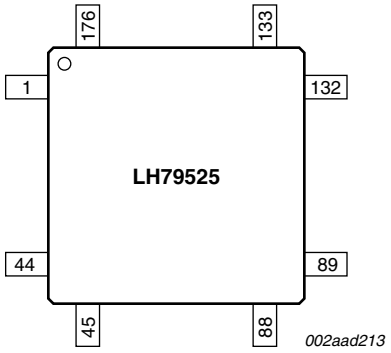


Figure 3. LH79525 pin configuration (LQFP176)

SIGNAL DESCRIPTIONS

Table 2. LH79524 Pin Descriptions

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
T12	A0	O	External Address Bus
R11	A1		
T11	A2		
P10	A3		
R10	A4		
T10	A5		
P9	A6		
R9	A7		
T9	A8		
T8	A9		
R8	A10		
P8	A11		
T7	A12		
R7	A13		
P7	A14		
T6	A15		
M15	D0	I/O	External Data Bus
N16	D1		
L13	D2		
M14	D3		
N15	D4		
P16	D5		
M13	D6		
N14	D7		
F14	SDCLK	O	SDRAM Clock
G15	SDCKE	O	SDRAM Clock Enable
D13	DQM0	O	Data Mask Output to SDRAMs
E13	DQM1		
E14	DQM2		
G14	DQM3		
G16	nDCS0	O	SDRAM Chip Select
H14	nDCS1	O	SDRAM Chip Select
H15	nRAS	O	Row Address Strobe
H16	nCAS	O	Column Address Strobe
L16	nCS0/PM0	O	Static Memory Chip Select; multiplexed with GPIO Port M[3:0] (output only)
L15	nCS1/PM1		
M16	nCS2/PM2		
L14	nCS3/PM3		
J15	nBLE0/PM4	O	Static Memory Byte Lane Enable / Byte Write Enable; multiplexed with GPIO Port M[7:4] (output only)
J14	nBLE1/PM5		
K16	nBLE2/PM6		
K15	nBLE3/PM7		

Table 2. LH79524 Pin Descriptions (Cont'd)

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
K14	nOE	O	Static Memory Output Enable
J16	nWE	O	Static Memory Write Enable
A16	USBDN	I/O	USB Data Negative (Differential Pair output, single ended and Differential pair input)
A15	USBDP	I/O	USB Data Positive (Differential Pair output, single ended and Differential pair input)
E2	AN0/UL/X+	I	ADC Input 0, 4-wire touch screen Upper Left, 5-wire touch screen X+
F2	AN1/UR/X–	I	ADC Input 1, 4-wire touch screen Upper Right, 5-wire touch screen X–
G2	AN2/LL/Y+/PJ3	I	ADC Input 2, 4-wire touch screen Lower Left, 5-wire touch screen Y+; multiplexed with GPIO Port J3 (input only)
H2	AN3/LR/Y–/PJ0	I	ADC Input 3, 4-wire touch screen Upper Right, 5-wire touch screen Y–; multiplexed with GPIO Port J0 (input only)
H3	AN4/WIPER/PJ1	I	ADC Input 4, 5-wire touch screen Wiper input; multiplexed with GPIO Port J1 (input only)
F1	AN5/PJ5/INT5	I	ADC Input 5; multiplexed with GPIO Port J5 (input only) and External Interrupt 5
F3	AN6/PJ7/INT7	I	ADC Input 6; multiplexed with GPIO Port J7 (input only) and External Interrupt 7
E1	AN7/PJ6/INT6	I	ADC Input 7; multiplexed with GPIO Port J6 (input only) and External Interrupt 6
G3	AN8/PJ4	I	ADC Input 8; multiplexed with GPIO Port J4 (input only)
G1	AN9/PJ2	I	ADC Input 9; multiplexed with GPIO Port J2 (input only)
J3	CTCLK/INT4/BATCNTL	I/O	Timer[2:0] External Clock input; muxed with External Int 4 and Battery Control
N1	PA0/INT2/UARTRX2/ UARTIRRX2	I/O	General Purpose I/O Signal — Port A0; multiplexed with UART2 Received Serial Data Input, UART2 Infrared Received Serial Data In, and External Interrupt 2
M2	PA1/INT3/UARTTX2/ UARTIRTX2	I/O	General Purpose I/O Signal — Port A1; multiplexed with UART2 Transmitted Serial Data Output, UART2 Serial Transmit Data Out, and External Interrupt 3
L3	PA2/CTCAP0A/ CTCMP0A	I/O	General Purpose I/O Signal — Port A2; multiplexed with Counter/Timer 0 Capture A input and Counter/Timer 0 Compare A output
M1	PA3/CTCAP0B/ CTCMP0B	I/O	General Purpose I/O Signal — Port A3; multiplexed with Counter/Timer 0 Capture B input and Counter/Timer 0 Compare B output
L2	PA4/CTCAP1A/ CTCMP1A	I/O	General Purpose I/O Signal — Port A4; multiplexed with Counter/Timer 1 Capture A input and Counter/Timer 1 Compare A output
L1	PA5/CTCAP1B/ CTCMP1B	I/O	General Purpose I/O Signal — Port A5; multiplexed with Counter/Timer 1 Capture B input and Counter/Timer 1 Compare B output
K3	PA6/CTCAP2A/ CTCMP2A/SDA	I/O	General Purpose I/O Signal — Port A6; multiplexed with Counter/Timer 2 Capture A input, Counter/Timer 2 Compare A output, I^2C Bus Data (open drain)
K2	PA7/CTCAP2B/ CTCMP2B/SCL	I/O	General Purpose I/O Signal — Port A7; multiplexed with Counter/Timer 2 Capture B input, Counter/Timer 2 Compare B output, I^2C Bus Clock (open drain)
R2	PB0/nDACK/ nUARTCTS0	I/O	General Purpose I/O Signal — Port B0; multiplexed with DMA Acknowledge and UART0 CTS
R1	PB1/DREQ/ nUARTRTS0	I/O	General Purpose I/O Signal — Port B1; multiplexed with DMA Request and UART0 RTS
P2	PB2/SSPFRM/I2SWS	I/O	General Purpose I/O Signal — Port B2; multiplexed with SSP Serial Frame Output and I^2S Frame Output
N3	PB3/SSPCLK/I2SCLK	I/O	General Purpose I/O Signal — Port B3; multiplexed with SSP Clock and I^2S Clock
M4	PB4/SSPRX/I2SRXD/ UARTRX1/ UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
P1	PB5/SSPTX/I2STXD/ UARTTX1/UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
N2	PB6/INT0/UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0

Table 2. LH79524 Pin Descriptions (Cont'd)

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
M3	PB7/INT1/UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1.
N7	PC0/A16	I/O	General Purpose I/O Signal — Port C0; multiplexed with Address A16
R6	PC1/A17	I/O	General Purpose I/O Signal — Port C1; multiplexed with Address A17
T5	PC2/A18	I/O	General Purpose I/O Signal — Port C2; multiplexed with Address A18
P6	PC3/A19	I/O	General Purpose I/O Signal — Port C3; multiplexed with Address A19
R5	PC4/A20	I/O	General Purpose I/O Signal — Port C4; multiplexed with Address A20
T4	PC5/A21	I/O	General Purpose I/O Signal — Port C5; multiplexed with Address A21
P5	PC6/A22/nFWE	I/O	General Purpose I/O Signal — Port C6; multiplexed with Address A22 and NAND Flash Write Enable
R4	PC7/A23/nFRE	I/O	General Purpose I/O Signal — Port C7; multiplexed with Address A23 and NAND Flash Read Enable
P15	PD0/D8	I/O	General Purpose I/O Signal — Port D0; multiplexed with Data D8
P14	PD1/D9	I/O	General Purpose I/O Signal — Port D1; multiplexed with Data D9
N13	PD2/D10	I/O	General Purpose I/O Signal — Port D2; multiplexed with Data D10
T15	PD3/D11	I/O	General Purpose I/O Signal — Port D3; multiplexed with Data D11
N12	PD4/D12	I/O	General Purpose I/O Signal — Port D4; multiplexed with Data D12
T14	PD5/D13	I/O	General Purpose I/O Signal — Port D5; multiplexed with Data D13
P12	PD6/D14	I/O	General Purpose I/O Signal — Port D6; multiplexed with Data D14
T13	PD7/D15	I/O	General Purpose I/O Signal — Port D7; multiplexed with Data D15
B12	PE0/LCDLP/ LCDHRLP	I/O	General Purpose I/O Signals — Port E0; multiplexed with LCD Line Pulse and AD-TFT/HR-TFT Line Pulse
D11	PE1/LCDDCLK	I/O	General Purpose I/O Signals — Port E1; multiplexed with LCD Data Clock
B13	PE2/LCDPS	I/O	General Purpose I/O Signals — Port E2; multiplexed with LCD Power Save
C13	PE3/LCDCLS	I/O	General Purpose I/O Signals — Port E3; multiplexed with LCD Row Driver Clock
D12	PE4/LCDDSPLEN/ LCDREV	I/O	General Purpose I/O Signals — Port E4; multiplexed with LCD Panel Power Enable and LCD Reverse
B16	PE5/LCDVDDEN	I/O	General Purpose I/O Signals — Port E5; multiplexed with LCD VDD Enable
B15	PE6/LCDVEEN/ LCDMOD	I/O	General Purpose I/O Signals — Port E6; multiplexed with LCD Analog Power Enable and MOD
D14	PE7/nWAIT/nDEOT	I/O	General Purpose I/O Signals — Port E7; multiplexed with nWAIT and DMA End of Transfer
A8	PF0/LCDVD6	I/O	General Purpose I/O Signals — Port F0; multiplexed with LCD Video Data bit 6
A9	PF1/LCDVD7	I/O	General Purpose I/O Signals — Port F1; multiplexed with LCD Video Data bit 7
B9	PF2/LCDVD8	I/O	General Purpose I/O Signals — Port F2; multiplexed with LCD Video Data bit 8
C9	PF3/LCDVD9	I/O	General Purpose I/O Signals — Port F3; multiplexed with LCD Video Data bit 9
B10	PF4/LCDVD10	I/O	General Purpose I/O Signals — Port F4; multiplexed with LCD Video Data bit 10
A11	PF5/LCDVD11	I/O	General Purpose I/O Signals — Port F5; multiplexed with LCD Video Data bit 11
B11	PF6/LCDEN/LCDSPL	I/O	General Purpose I/O Signals — Port F6; multiplexed with LCD Start Pulse Left
A12	PF7/LCDFP/LCDSPS	I/O	General Purpose I/O Signals — Port F7; multiplexed with LCD Row Driver Counter reset
A5	PG0/ETHERTXEN	I/O	General Purpose I/O Signals — Port G0; multiplexed with Ethernet TX Enable
B6	PG1/ETHERTXCLK	I/O	General Purpose I/O Signals — Port G1; multiplexed with Ethernet TX Clock
A6	PG2/LCDVD0	I/O	General Purpose I/O Signals — Port G2; multiplexed with LCD Video Data bit 0
C7	PG3/LCDVD1	I/O	General Purpose I/O Signals — Port G3; multiplexed with LCD Video Data bit 1
B7	PG4/LCDVD2	I/O	General Purpose I/O Signals — Port G4; multiplexed with LCD Video Data bit 2

Table 2. LH79524 Pin Descriptions (Cont'd)

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
A7	PG5/LCDVD3	I/O	General Purpose I/O Signals — Port G5; multiplexed with LCD Video Data bit 3
C8	PG6/LCDVD4	I/O	General Purpose I/O Signals — Port G6; multiplexed with LCD Video Data bit 4
B8	PG7/LCDVD5	I/O	General Purpose I/O Signals — Port G7; multiplexed with LCD Video Data bit 5
C4	PH0/ETHERRX3	I/O	General Purpose I/O Signals — Port H0; multiplexed with Ethernet Receive Channel 3
A3	PH1/ETHERRXDV	I/O	General Purpose I/O Signals — Port H1; multiplexed with Ethernet Data Valid
B4	PH2/ETHERRXCLK	I/O	General Purpose I/O Signals — Port H2; multiplexed with Ethernet Receive Clock
C5	PH3/ETHERTXER	I/O	General Purpose I/O Signals — Port H3; multiplexed with Ethernet Transmit Error
D6	PH4/ETHERTX0	I/O	General Purpose I/O Signals — Port H4; multiplexed with Ethernet Transmit Channel 0
A4	PH5/ETHERTX1	I/O	General Purpose I/O Signals — Port H5; multiplexed with Ethernet Transmit Channel 1
B5	PH6/ETHERTX2	I/O	General Purpose I/O Signals — Port H6; multiplexed with Ethernet Transmit Channel 2
C6	PH7/ETHERTX3	I/O	General Purpose I/O Signals — Port H7; multiplexed with Ethernet Transmit Channel 3
D3	PI0/ETHERMDC	I/O	General Purpose I/O Signals — Port I0; multiplexed with Ethernet Management Data Clock
B1	PI1/ETHERMDIO	I/O	General Purpose I/O Signals — Port I1; multiplexed with Ethernet Management Data I/O
B2	PI2/ETHERCOL	I/O	General Purpose I/O Signals — Port I2; multiplexed with Ethernet Collision Detect
D4	PI3/ETHERCRS	I/O	General Purpose I/O Signals — Port I3; multiplexed with Ethernet Carrier Sense
C3	PI4/ETHERRXER	I/O	General Purpose I/O Signals — Port I4; multiplexed with Ethernet Receive Error
A1	PI5/ETHERRX0	I/O	General Purpose I/O Signals — Port I5; multiplexed with Ethernet Receive Channel 0
A2	PI6/ETHERRX1	I/O	General Purpose I/O Signals — Port I6; multiplexed with Ethernet Receive Channel 1
B3	PI7/ETHERRX2	I/O	General Purpose I/O Signals — Port I7; multiplexed with Ethernet Receive Channel 2
R16	PK0/D16	I/O	General Purpose I/O Signals — Port K0; multiplexed with data bit D16
M12	PK1/D17	I/O	General Purpose I/O Signals — Port K1; multiplexed with data bit D17
T16	PK2/D18	I/O	General Purpose I/O Signals — Port K2; multiplexed with data bit D18
R15	PK3/D19	I/O	General Purpose I/O Signals — Port K3; multiplexed with data bit D19
P13	PK4/D20	I/O	General Purpose I/O Signals — Port K4; multiplexed with data bit D20
R14	PK5/D21	I/O	General Purpose I/O Signals — Port K5; multiplexed with data bit D21
R13	PK6/D22	I/O	General Purpose I/O Signals — Port K6; multiplexed with data bit D22
N11	PK7/D23	I/O	General Purpose I/O Signals — Port K7; multiplexed with data bit D23
C1	PL0/LCDVD14	I/O	General Purpose I/O Signals — Port L0; multiplexed with LCD Video Data bit 14
C2	PL1/LCDVD15	I/O	General Purpose I/O Signals — Port L1; multiplexed with LCD Video Data bit 15
A10	PL2/LCDVD12	I/O	General Purpose I/O Signals — Port L2; multiplexed with LCD Video Data bit 12
C10	PL3/LCDVD13	I/O	General Purpose I/O Signals — Port L3; multiplexed with LCD Video Data bit 13
C12	PL4/D28	I/O	General Purpose I/O Signals — Port L4; multiplexed with Data bit D28
A14	PL5/D29	I/O	General Purpose I/O Signals — Port L5; multiplexed with Data bit D29
B14	PL6/D30	I/O	General Purpose I/O Signals — Port L6; multiplexed with Data bit D30
C14	PL7/D31	I/O	General Purpose I/O Signals — Port L7; multiplexed with Data bit D31
C11	PN0/D26	I/O	General Purpose I/O Signals — Port N0; multiplexed with Data bit D26
A13	PN1/D27	I/O	General Purpose I/O Signals — Port N1; multiplexed with Data bit D27
R12	PN2/D24	I/O	General Purpose I/O Signals — Port N2; multiplexed with Data bit D24

Table 2. LH79524 Pin Descriptions (Cont'd)

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
P11	PN3/D25	I/O	General Purpose I/O Signals — Port N3; multiplexed with Data bit D25
J2	nRESETIN	I	Reset Input
H1	nRESETOUT	O	Reset Output
C16	XTALIN	I	Crystal Input
C15	XTALOUT	O	Crystal Output
D16	XTAL32IN	I	32.768 kHz Crystal Oscillator Input
D15	XTAL32OUT	O	32.768 kHz Crystal Oscillator Output
K1	CLKOUT	O	Clock Out (selectable from the internal bus clock or 32.768 kHz crystal)
D2	nTRST	I	JTAG Test Reset Input
P4	TMS	I	JTAG Test Mode Select Input
T3	TCK	I	JTAG Test Clock Input
T1	TDI	I	JTAG Test Serial Data Input
P3	TDO	O	JTAG Test Data Serial Output
T2	TEST1	I	Tie HIGH for Normal Operation; pull LOW to enable Embedded ICE Debugging
R3	TEST2	I	Tie HIGH for Normal Operation; pull HIGH to enable Embedded ICE Debugging
E3	LINREGEN	I	Linear Regulator Enable
D5, E4, E5, H13, N5	VDDC	Power	Core Power Supply
D10, F4, J13, N4	VSSC	Ground	Core GND
D7, D8, D9, F13, G4, G13, H4, J4, K4, K13, L4, N6, N8, N9, N10	VDD	Power	Input/Output Power Supply
E12, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, M5	VSS	Ground	Input/Output GND
D1	VDDA0	Power	Analog Power Supply for Analog-to-Digital Converter
F16	VDDA1	Power	Analog Power Supply for the USB PLL
E16	VDDA2	Power	Analog Power Supply for System PLL
J1	VSSA0	Ground	Analog GND for Analog-to-Digital Converter
F15	VSSA1	Ground	Analog GND for the USB PLL
E15	VSSA2	Ground	Analog GND for System PLL

Table 3. LH79524 Numerical Pin List

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
A1	PI5	ETHERRX0	8 mA	1
A2	PI6	ETHERRX1	8 mA	1
A3	PH1	ETHERRXDV	8 mA	1
A4	PH5	ETHERTX1	8 mA	1
A5	PG0	ETHERTXEN	8 mA	1
A6	PG2	LCDVD0	8 mA	1
A7	PG5	LCDVD3	8 mA	1
A8	PF0	LCDVD6	8 mA	1
A9	PF1	LCDVD7	8 mA	1
A10	PL2	LCDVD12	8 mA	1
A11	PF5	LCDVD11	8 mA	2
A12	PF7	LCDFP/LCDSPS	8 mA	1
A13	PN1	D27	8 mA	1
A14	PL5	D29	8 mA	1
A15	USBDP			3
A16	USBDN			3
B1	PI1	ETHERMDIO	8 mA	2
B2	PI2	ETHERCOL	8 mA	1
B3	PI7	ETHERRX2	8 mA	1
B4	PH2	ETHERRXCLK	8 mA	1
B5	PH6	ETHERTX2	8 mA	1
B6	PG1	ETHERTXCLK	8 mA	1
B7	PG4	LCDVD2	8 mA	1
B8	PG7	LCDVD5	8 mA	1
B9	PF2	LCDVD8	8 mA	2
B10	PF4	LCDVD10	8 mA	2
B11	PF6	LCDEN/LCDSPL	8 mA	1
B12	PE0	LCDLP/LCDHRLP	8 mA	1
B13	PE2	LCDPS	8 mA	1
B14	PL6	D30	8 mA	1
B15	PE6	LCDVEEN/ LCDMOD	8 mA	1
B16	PE5	LCDVDDEN	8 mA	1
C1	PL0	LCDVD14	8 mA	1
C2	PL1	LCDVD15	8 mA	1
C3	PI4	ETHERRXER	8 mA	1
C4	PH0	ETHERRX3	8 mA	1
C5	PH3	ETHERTXER	8 mA	1
C6	PH7	ETHERTX3	8 mA	1
C7	PG3	LCDVD1	8 mA	1
C8	PG6	LCDVD4	8 mA	1
C9	PF3	LCDVD9	8 mA	2
C10	PL3	LCDVD13	8 mA	1
C11	PN0	D26	8 mA	1
C12	PL4	D28	8 mA	1

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
C13	PE3	LCDCLS	8 mA	1
C14	PL7	D31	8 mA	1
C15	XTALOUT			4
C16	XTALIN			5
D1	VDDA0			
D2	nTRST			2, 6
D3	PI0	ETHERMDC	8 mA	1
D4	PI3	ETHERCRS	8 mA	1
D5	VDDC			
D6	PH4	ETHERTX0	8 mA	1
D7	VDD			
D8	VDD			
D9	VDD			
D10	VSSC			
D11	PE1	LCDDCLK	8 mA	1
D12	PE4	LCDDSPLEN/ LCDREV	8 mA	1
D13	DQM0		8 mA	
D14	PE7	nWAIT/nDEOT	8 mA	2, 6
D15	XTAL32OUT			4
D16	XTAL32IN			5
E1	AN7	PJ6/INT6		
E2	AN0/UL/X+			
E3	LINREGEN			
E4	VDDC			
E5	VDDC			
E12	VSS			
E13	DQM1		8 mA	
E14	DQM2		8 mA	
E15	VSSA2			
E16	VDDA2			
F1	AN5	PJ5/INT5		
F2	AN1/UR/X-			
F3	AN6	PJ7/INT7		
F4	VSSC			
F13	VDD			
F14	SDCLK		12 mA	
F15	VSSA1			
F16	VDDA1			
G1	AN9	PJ2		
G2	AN2/LL/Y+	PJ3		
G3	AN8	PJ4		
G4	VDD			
G8	VSS			
G9	VSS			

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
G13	VDD			
G14	DQM3		8 mA	
G15	SDCKE		8 mA	
G16	nDCS0		8 mA	
H1	nRESETOUT		8 mA	
H2	AN3/LR/Y-	PJ0		
H3	AN4/WIPER	PJ1		
H4	VDD			
H7	VSS			
H8	VSS			
H9	VSS			
H10	VSS			
H13	VDDC			
H14	nDCS1		8 mA	
H15	nRAS		8 mA	
H16	nCAS		8 mA	
J1	VSSA0			
J2	nRESETIN			2, 6
J3	CTCLK	INT4/BATCNTL	8 mA	2, 6
J4	VDD			
J7	VSS			
J8	VSS			
J9	VSS			
J10	VSS			
J13	VSSC			
J14	nBLE1	PM5	8 mA	
J15	nBLE0	PM4	8 mA	
J16	nWE		8 mA	
K1	CLKOUT		8 mA	
K2	PA7	CTCAP2B/ CTCMP2B/SCL	8 mA	2, 6
K3	PA6	CTCAP2A/ CTCMP2A/SDA	8 mA	2, 6
K4	VDD			
K8	VSS			
K9	VSS			
K13	VDD			
K14	nOE		8 mA	
K15	nBLE3	PM7	8 mA	
K16	nBLE2	PM6	8 mA	
L1	PA5	CTCAP1B/ CTCMP1B	8 mA	1, 6
L2	PA4	CTCAP1A/ CTCMP1A	8 mA	1, 6
L3	PA2	CTCAP0A/ CTCMP0A	8 mA	1, 6

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
L4	VDD			
L13	D2		8 mA	1
L14	nCS3	PM3	8 mA	
L15	nCS1	PM1	8 mA	
L16	nCS0	PM0	8 mA	
M1	PA3	CTCAP0B/ CTCMP0B	8 mA	1, 6
M2	PA1	INT3/UARTTX2/ UARTIRTX2	8 mA	1, 6
M3	PB7	INT1/UARTTX0/ UARTIRTX0	8 mA	1, 6
M4	PB4	SSPRX/I2SRXD/ UARTRX1/ UARTIRRX1	8 mA	2
M5	VSS			
M12	PK1	D17	8 mA	1
M13	D6		8 mA	1
M14	D3		8 mA	1
M15	D0		8 mA	1
M16	nCS2	PM2	8 mA	
N1	PA0	INT2/UARTRX2/ UARTIRRX2	8 mA	1, 6
N2	PB6	INT0/UARTRX0/ UARTIRRX0	8 mA	1, 6
N3	PB3	SSPCLK/I2SCLK	8 mA	1
N4	VSSC			
N5	VDDC			
N6	VDD			
N7	PC0	A16	8 mA	1
N8	VDD			
N9	VDD			
N10	VDD			
N11	PK7	D23	8 mA	1
N12	PD4	D12	8 mA	1
N13	PD2	D10	8 mA	1
N14	D7		8 mA	1
N15	D4		8 mA	1
N16	D1		8 mA	1
P1	PB5	SSPTX/I2STXD/ UARTTX1/ UARTIRTX1	8 mA	1
P2	PB2	SSPFRM/I2SWS	8 mA	2
P3	TDO		4 mA	
P4	TMS			2, 6
P5	PC6	A22/nFWE	8 mA	1
P6	PC3	A19	8 mA	1
P7	A14		8 mA	

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
P8	A11		8 mA	
P9	A6		8 mA	
P10	A3		8 mA	
P11	PN3	D25	8 mA	1
P12	PD6	D14	8 mA	1
P13	PK4	D20	8 mA	1
P14	PD1	D9	8 mA	1
P15	PD0	D8	8 mA	1
P16	D5		8 mA	1
R1	PB1	DREQ/ nUARTRTS0	8 mA	2
R2	PB0	nDACK/ nUARTCTS0	8 mA	2
R3	TEST2			2, 6
R4	PC7	A23/nFRE	8 mA	1
R5	PC4	A20	8 mA	1
R6	PC1	A17	8 mA	1
R7	A13		8 mA	
R8	A10		8 mA	
R9	A7		8 mA	
R10	A4		8 mA	
R11	A1		8 mA	
R12	PN2	D24	8 mA	1
R13	PK6	D22	8 mA	1
R14	PK5	D21	8 mA	1
R15	PK3	D19	8 mA	1
R16	PK0	D16	8 mA	1
T1	TDI			2, 6
T2	TEST1			2, 6
T3	TCK			2, 6

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
T4	PC5	A21	8 mA	1
T5	PC2	A18	8 mA	1
T6	A15		8 mA	
T7	A12		8 mA	
T8	A9		8 mA	
T9	A8		8 mA	
T10	A5		8 mA	
T11	A2		8 mA	
T12	A0		8 mA	
T13	PD7	D15	8 mA	1
T14	PD5	D13	8 mA	1
T15	PD3	D11	8 mA	1
T16	PK2	D18	8 mA	1

NOTES:
1. Internal pull-down. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
2. Internal pull-up. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
3. USB Inputs/outputs are tristated.
4. Output is for crystal oscillator only, no drive capability.
5. Crystal Oscillator Inputs should be driven to a maximum of 1.8 V ± 10%.
6. Input with Schmitt Trigger.
7. Output Drive Values are MAX. See 'DC Specifications'.
8. All unused analog pins, and XTAL32IN (if unused) should be tied to ground through a 33KΩ resistor.

Table 4. TESTx PIN FUNCTION

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

Table 5. LH79525 Pin Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
80	A0	O	External Address Bus
79	A1		
78	A2		
77	A3		
76	A4		
74	A5		
73	A6		
72	A7		
71	A8		
70	A9		
69	A10		
67	A11		
65	A12		
63	A13		
62	A14		
61	A15		
99	D0	I/O	External Data Bus
98	D1		
97	D2		
96	D3		
95	D4		
94	D5		
93	D6		
91	D7		
117	SDCLK	O	SDRAM Clock
116	SDCKE	O	SDRAM Clock Enable
119	DQM0	O	Data Mask Output to SDRAMs
118	DQM1		
115	nDCS0	O	SDRAM Chip Select
114	nDCS1	O	SDRAM Chip Select
113	nRAS	O	Row Address Strobe
112	nCAS	O	Column Address Strobe
104	nCS0/PM0	O	Static Memory Chip Select; multiplexed with GPO Port M[3:0]
103	nCS1/PM1		
102	nCS2/PM2		
100	nCS3/PM3		
110	nBLE0/PM4	O	Static Memory Byte Lane Enable / Byte Write Enable; multiplexed with GPIO Port M[5:4]
109	nBLE1/PM5		
106	nOE	O	Static Memory Output Enable
111	nWE	O	Static Memory Write Enable
130	USBDN	I/O	USB Data Negative (Differential Pair output, single ended and Differential input)
131	USBDP	I/O	USB Data Positive (Differential Pair output, single ended and Differential input)
11	AN0/UL/X+	I	ADC Input 0, 4 wire touch screen Upper Left, 5 wire touch screen X+
14	AN1/UR/X–	I	ADC Input 1, 4 wire touch screen Upper Right, 5 wire touch screen X–
17	AN2/LL/Y+/PJ3	I	ADC Input 2, 4 wire touch screen Lower Left, 5 wire touch screen Y+; multiplexed with GPIO Port J3 (input only)

Table 5. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
20	AN3/LR/Y–/PJ0	I	ADC Input 3, 4 wire touch screen Upper Right, 5 wire touch screen Y–; multiplexed with GPIO Port J0 (input only)
19	AN4/WIPER/PJ1	I	ADC Input 4, 5 wire touch screen Wiper input; multiplexed with Port J1 (input only)
15	AN5/PJ5/INT5	I	ADC Input 5; multiplexed with GPIO Port J5 (input only) and External Interrupt 5
12	AN6/PJ7/INT7	I	ADC Input 6; multiplexed with GPIO Port J7 (input only) and External Interrupt 7
13	AN7/PJ6/INT6	I	ADC Input 7; multiplexed with GPIO Port J6 (input only) and External Interrupt 6
16	AN8/PJ4	I	ADC Input 8; multiplexed with GPIO Port J4 (input only)
18	AN9/PJ2	I	ADC Input 9; multiplexed with GPIO Port J2 (input only)
25	CTCLK/INT4/ BATCNTL	I/O	Timer[2:0] External Clock input; multiplexed with Battery Control and Interrupt 4
36	PA0/UARTRX2/ UARTIRRX2/INT2	I/O	General Purpose I/O Signal — Port A0; multiplexed with UART2 Received Serial Data Input, UART2 Infrared Received Serial Data In, and External Interrupt 2
35	PA1/UARTTX2/ UARTIRRX2/INT3	I/O	General Purpose I/O Signal — Port A1; multiplexed with UART2 Transmitted Serial Data Output, UART2 Serial Transmit Data Out, and External Interrupt 3
34	PA2/CTCAP0A/ CTCMP0A	I/O	General Purpose I/O Signal — Port A2; multiplexed with Counter/Timer 0 Capture A input and Counter/Timer 0 Compare A output
32	PA3/CTCAP0B/ CTCMP0B	I/O	General Purpose I/O Signal — Port A3; multiplexed with Counter/Timer 0 Capture B input and Counter/Timer 0 Compare B output
31	PA4/CTCAP1A/ CTCMP1A	I/O	General Purpose I/O Signal — Port A4; multiplexed with Counter/Timer 1 Capture A input and Counter/Timer 1 Compare A output
30	PA5/CTCAP1B/ CTCMP1B	I/O	General Purpose I/O Signal — Port A5; multiplexed with Counter/Timer 1 Capture B input and Counter/Timer 1 Compare B output
29	PA6/CTCAP2A/ CTCMP2A/SDA	I/O	General Purpose I/O Signal — Port A6; multiplexed with Counter/Timer 2 Capture A input, Counter/Timer 2 Compare A output, and I^2C Bus Data (open drain)
28	PA7/CTCAP2B/ CTCMP2B/SLC	I/O	General Purpose I/O Signal — Port A7; multiplexed with Counter/Timer 2 Capture B input, Counter/Timer 2 Compare B output, and I^2C Bus Clock (open drain)
44	PB0/nDACK/ nUARTCTS0	I/O	General Purpose I/O Signal — Port B0; multiplexed with DMA Acknowledge and UART0 CTS
43	PB1/DREQ/ nUARTRTS0	I/O	General Purpose I/O Signal — Port B1; multiplexed with DMA Request and UART0 RTS
42	PB2/SSPFRM/ I2SWS	I/O	General Purpose I/O Signal — Port B2; multiplexed with SSP Serial Frame Output and I^2S Frame Output
41	PB3/SSPCLK/ I2SCLK	I/O	General Purpose I/O Signal — Port B3; multiplexed with SSP Clock and I^2S Clock
40	PB4/SSPRX/ I2SRXD/UARTRX1/ UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
39	PB5/SSPTX/ I2STXD/UARTTX1/ UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
38	PB6/INT0/ UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0
37	PB7/INT1/ UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1
60	PC0/A16	I/O	General Purpose I/O Signal — Port C0; multiplexed with Address A16
59	PC1/A17	I/O	General Purpose I/O Signal — Port C1; multiplexed with Address A17
58	PC2/A18	I/O	General Purpose I/O Signal — Port C2; multiplexed with Address A18
56	PC3/A19	I/O	General Purpose I/O Signal — Port C3; multiplexed with Address A19
55	PC4/A20	I/O	General Purpose I/O Signal — Port C4; multiplexed with Address A20
54	PC5/A21	I/O	General Purpose I/O Signal — Port C5; multiplexed with Address A21

Table 5. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
53	PC6/A22/nFWE	I/O	General Purpose I/O Signal — Port C6; multiplexed with Address A22 and NAND Flash Write Enable
52	PC7/A23/nFRE	I/O	General Purpose I/O Signal — Port C7; multiplexed with Address A23 and NAND Flash Read Enable
90	PD0/D8	I/O	General Purpose I/O Signal — Port D0; multiplexed with Data D8
89	PD1/D9	I/O	General Purpose I/O Signal — Port D1; multiplexed with Data D9
88	PD2/D10	I/O	General Purpose I/O Signal — Port D2; multiplexed with Data D10
87	PD3/D11	I/O	General Purpose I/O Signal — Port D3; multiplexed with Data D11
85	PD4/D12	I/O	General Purpose I/O Signal — Port D4; multiplexed with Data D12
84	PD5/D13	I/O	General Purpose I/O Signal — Port D5; multiplexed with Data D13
83	PD6/D14	I/O	General Purpose I/O Signal — Port D6; multiplexed with Data D14
82	PD7/D15	I/O	General Purpose I/O Signal — Port D7; multiplexed with Data D15
141	PE0/LCDLP/ LCDHRLP	I/O	General Purpose I/O Signals — Port E0; multiplexed with LCD Line Pulse and AD-TFT/HR-TFT Line Pulse
139	PE1/LCDDCLK	I/O	General Purpose I/O Signals — Port E1; multiplexed with LCD Data Clock
138	PE2/LCDPS	I/O	General Purpose I/O Signals — Port E2; multiplexed with LCD Power Save
137	PE3/LCDCLS	I/O	General Purpose I/O Signals — Port E3; multiplexed with LCD Row Driver Clock
136	PE4/LCDDSPLEN/ LCDREV	I/O	General Purpose I/O Signals — Port E4; multiplexed with LCD Panel Power Enable and LCD Reverse
134	PE5/LCDVDDEN	I/O	General Purpose I/O Signals — Port E5; multiplexed with LCD VDD Enable
133	PE6LCDVEEN/ LCDMOD	I/O	General Purpose I/O Signals — Port E6; multiplexed with LCD Analog Power Enable and MOD
120	PE7/nWAIT/nDEOT	I/O	General Purpose I/O Signals — Port E7; multiplexed with nWAIT and DMA End of Transfer
153	PF0/LCDVD6	I/O	General Purpose I/O Signals — Port F0; multiplexed with LCD Video Data bit 6
151	PF1/LCDVD7	I/O	General Purpose I/O Signals — Port F1; multiplexed with LCD Video Data bit 7
149	PF2/LCDVD8	I/O	General Purpose I/O Signals — Port F2; multiplexed with LCD Video Data bit 8
147	PF3/LCDVD9	I/O	General Purpose I/O Signals — Port F3; multiplexed with LCD Video Data bit 9
146	PF4/LCDVD10	I/O	General Purpose I/O Signals — Port F4; multiplexed with LCD Video Data bit 10
145	PF5/LCDVD11	I/O	General Purpose I/O Signals — Port F5; multiplexed with LCD Video Data bit 11
143	PF6/LCDEN/ LCDSPL	I/O	General Purpose I/O Signals — Port F6; multiplexed with LCD Start Pulse Left
142	PF7/LCDFP/ LCDSPS	I/O	General Purpose I/O Signals — Port F7; multiplexed with LCD Row Driver Counter reset
162	PG0/ETHERTXEN	I/O	General Purpose I/O Signals — Port G0; multiplexed with Ethernet Transmit Enable
161	PG1/ETHERTXCLK	I/O	General Purpose I/O Signals — Port G1; multiplexed with Ethernet Clock
159	PG2/LCDVD0	I/O	General Purpose I/O Signals — Port G2; multiplexed with LCD Video Data bit 0
158	PG3/LCDVD1	I/O	General Purpose I/O Signals — Port G3; multiplexed with LCD Video Data bit 1
157	PG4/LCDVD2	I/O	General Purpose I/O Signals — Port G4; multiplexed with LCD Video Data bit 2
156	PG5/LCDVD3	I/O	General Purpose I/O Signals — Port G5; multiplexed with LCD Video Data bit 3
155	PG6/LCDVD4	I/O	General Purpose I/O Signals — Port G6; multiplexed with LCD Video Data bit 4
154	PG7/LCDVD5	I/O	General Purpose I/O Signals — Port G7; multiplexed with LCD Video Data bit 5
171	PH0/ETHERRX3	I/O	General Purpose I/O Signals — Port H0; multiplexed with Ethernet Receive Channel 3
170	PH1/ETHERRXDV	I/O	General Purpose I/O Signals — Port H1; multiplexed with Ethernet Data Valid
169	PH2/ETHERRXCLK	I/O	General Purpose I/O Signals — Port H2; multiplexed with Ethernet Receive Clock
167	PH3/ETHERTXER	I/O	General Purpose I/O Signals — Port H3; multiplexed with Ethernet Transmit Error
166	PH4/ETHERTX0	I/O	General Purpose I/O Signals — Port H4; multiplexed with Ethernet Transmit Channel 0
165	PH5/ETHERTX1	I/O	General Purpose I/O Signals — Port H5; multiplexed with Ethernet Transmit Channel 1
164	PH6/ETHERTX2	I/O	General Purpose I/O Signals — Port H6; multiplexed with Ethernet Transmit Channel 2

Table 5. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
163	PH7/ETHERTX3	I/O	General Purpose I/O Signals — Port H7; multiplexed with Ethernet Transmit Channel 3
4	PI0/ETHERMDC	I/O	General Purpose I/O Signals — Port I0; multiplexed with Ethernet Management Data Clock
2	PI1/ETHERMDIO	I/O	General Purpose I/O Signals — Port I1; multiplexed with Ethernet Management Data I/O
1	PI2/ETHERCOL	I/O	General Purpose I/O Signals — Port I2; multiplexed with Ethernet Collision Detect
176	PI3/ETHERCRS	I/O	General Purpose I/O Signals — Port I3; multiplexed with Ethernet Carrier Sense
175	PI4/ETHERRXER	I/O	General Purpose I/O Signals — Port I4; multiplexed with Ethernet Receive Error
174	PI5/ETHERRX0	I/O	General Purpose I/O Signals — Port I5; multiplexed with Ethernet Receive Channel 0
173	PI6/ETHERRX1	I/O	General Purpose I/O Signals — Port I6; multiplexed with Ethernet Receive Channel 1
172	PI7/ETHERRX2	I/O	General Purpose I/O Signals — Port I7; multiplexed with Ethernet Receive Channel 2
24	nRESETIN	I	Reset Input
22	nRESETOUT	O	Reset Output
127	XTALIN	I	Crystal Input, or external clock input
128	XTALOUT	O	Crystal Output
125	XTAL32IN	I	32.768 kHz Crystal Oscillator Input, or external clock input,
126	XTAL32OUT	O	32.768 kHz Crystal Oscillator Output
23	CLKOUT	O	Clock Out (selectable from the internal bus clock or 32.768 MHz)
8	nTRST	I	JTAG Test Reset Input
50	TMS	I	JTAG Test Mode Select Input
51	TCK	I	JTAG Test Clock Input
46	TDI	I	JTAG Test Serial Data Input
45	TDO	O	JTAG Test Data Serial Output
47	TEST1	I	Tie HIGH for Normal Operation; pull LOW to enable embedded ICE Debugging
48	TEST2	I	Tie HIGH for Normal Operation; pull HIGH to enable embedded ICE Debugging
9	LINREGEN	I	Linear Regulator Enable (Requires pull-up. See User's Guide)
6, 66, 107, 150	VDDC	Power	Core Power Supply
7, 64, 105,148	VSSC	Ground	Core GND
3, 26, 33, 57, 75, 86, 101, 129, 135, 144, 160	VDD	Power	Input/Output Power Supply
5, 27, 49, 68, 81, 92, 108, 132, 140, 152, 168	VSS	Ground	Input/Output GND
10	VDDA0	Power	Analog Power Supply for Analog-to-Digital Converter
122	VDDA1	Power	Analog Power Supply for the USB PLL
123	VDDA2	Power	Analog Power Supply for System PLL
21	VSSA0	Ground	Analog GND for Analog-to-Digital Converter
121	VSSA1	Ground	Analog GND for the USB PLL
124	VSSA2	Ground	Analog GND for System PLL

Table 6. LH79525 Numerical Pin List

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
1	PI2	ETHERCOL	8 mA	1

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
2	PI1	ETHERMDIO	8 mA	2

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
3	VDD			
4	PI0	ETHERMDC	8 mA	1
5	VSS			
6	VDDC			
7	VSSC			
8	nTRST			2, 3
9	LINREGEN			
10	VDDA0			
11	AN0/UL/X+			
12	AN6	PJ7/INT7		
13	AN7	PJ6/INT6		
14	AN1/UR/X-			
15	AN5	PJ5/INT5		
16	AN8	PJ4		
17	AN2/LL/Y+	PJ3		
18	AN9	PJ2		
19	AN4/WIPER	PJ1		
20	AN3/LR/Y-	PJ0		
21	VSSA0			
22	nRESETOUT		8 mA	
23	CLKOUT		8 mA	
24	nRESETIN			2, 3
25	CTCLK	INT4/BATCNTL	8 mA	2, 3
26	VDD			
27	VSS			
28	PA7	CTCAP2B/CTCMP2B/ SCL	8 mA	2, 3
29	PA6	CTCAP2A/CTCMP2A/ SDA	8 mA	2, 3
30	PA5	CTCAP1B/CTCMP1B	8 mA	1, 3
31	PA4	CTCAP1A/CTCMP1A	8 mA	1, 3
32	PA3	CTCAP0B/CTCMP0B	8 mA	1, 3
33	VDD			
34	PA2	CTCAP0A/CTCMP0A	8 mA	1, 3
35	PA1	INT3/UARTTX2/ UARTIRTX2	8 mA	1, 3
36	PA0	INT2/UARTRX2/ UARTIRRX2	8 mA	1, 3
37	PB7	INT1/UARTTX0/ UARTIRTX0	8 mA	1, 3
38	PB6	INT0/UARTRX0/ UARTIRRX0	8 mA	1, 3
39	PB5	SSPTX/I2STXD/ UARTTX1/UARTIRTX1	8 mA	1
40	PB4	SSPRX/I2SRXD/ UARTRX1/UARTIRRX1	8 mA	2
41	PB3	SSPCLK/I2SCLK	8 mA	1
42	PB2	SSPFRM/I2SWS	8 mA	2
43	PB1	DREQ/nUARTRTS0	8 mA	2
44	PB0	nDACK/nUARTCTS0	8 mA	2
45	TDO		4 mA	
46	TDI			2, 3

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
47	TEST1			2, 3
48	TEST2			2, 3
49	VSS			
50	TMS			2, 3
51	TCK			2, 3
52	PC7	A23/nFRE	8 mA	1
53	PC6	A22/nFWE	8 mA	1
54	PC5	A21	8 mA	1
55	PC4	A20	8 mA	1
56	PC3	A19	8 mA	1
57	VDD			
58	PC2	A18	8 mA	1
59	PC1	A17	8 mA	1
60	PC0	A16	8 mA	1
61	A15		8 mA	
62	A14		8 mA	
63	A13		8 mA	
64	VSSC			
65	A12		8 mA	
66	VDDC			
67	A11		8 mA	
68	VSS			
69	A10		8 mA	
70	A9		8 mA	
71	A8		8 mA	
72	A7		8 mA	
73	A6		8 mA	
74	A5		8 mA	
75	VDD			
76	A4		8 mA	
77	A3		8 mA	
78	A2		8 mA	
79	A1		8 mA	
80	A0		8 mA	
81	VSS			
82	PD7	D15	8 mA	1
83	PD6	D14	8 mA	1
84	PD5	D13	8 mA	1
85	PD4	D12	8 mA	1
86	VDD			
87	PD3	D11	8 mA	1
88	PD2	D10	8 mA	1
89	PD1	D9	8 mA	1
90	PD0	D8	8 mA	1
91	D7		8 mA	1
92	VSS			
93	D6		8 mA	1
94	D5		8 mA	1
95	D4		8 mA	1
96	D3		8 mA	1

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
97	D2		8 mA	1
98	D1		8 mA	1
99	D0		8 mA	1
100	nCS3	PM3	8 mA	
101	VDD			
102	nCS2	PM2	8 mA	
103	nCS1	PM1	8 mA	
104	nCS0	PM0	8 mA	
105	VSSC			
106	nOE		8 mA	
107	VDDC			
108	VSS			
109	nBLE1	PM5	8 mA	
110	nBLE0	PM4	8 mA	
111	nWE		8 mA	
112	nCAS		8 mA	
113	nRAS		8 mA	
114	nDCS1		8 mA	
115	nDCS0		8 mA	
116	SDCKE		8 mA	
117	SDCLK		12 mA	
118	DQM1		8 mA	
119	DQM0		8 mA	
120	PE7	nWAIT/nDEOT	8 mA	2, 3
121	VSSA1			
122	VDDA1			
123	VDDA2			
124	VSSA2			
125	XTAL32IN			5
126	XTAL32OUT			6
127	XTALIN			5
128	XTALOUT			6
129	VDD			
130	USBDN			4
131	USBDP			4
132	VSS			
133	PE6	LCDVEEN/ LCDMOD	8 mA	1
134	PE5	LCDVDDEN	8 mA	1
135	VDD			
136	PE4	LCDDSPLEN/LCDREV	8 mA	1
137	PE3	LCDCLS	8 mA	1
138	PE2	LCDPS	8 mA	1
139	PE1	LCDDCLK	8 mA	1
140	VSS			
141	PE0	LCDLP/LCDHRLP	8 mA	1
142	PF7	LCDFP/LCDSPS	8 mA	1
143	PF6	LCDEN/LCDSPL	8 mA	1
144	VDD			
145	PF5	LCDVD11	8 mA	2

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
146	PF4	LCDVD10	8 mA	2
147	PF3	LCDVD9	8 mA	2
148	VSSC			
149	PF2	LCDVD8	8 mA	2
150	VDDC			
151	PF1	LCDVD7	8 mA	1
152	VSS			
153	PF0	LCDVD6	8 mA	1
154	PG7	LCDVD5	8 mA	1
155	PG6	LCDVD4	8 mA	1
156	PG5	LCDVD3	8 mA	1
157	PG4	LCDVD2	8 mA	1
158	PG3	LCDVD1	8 mA	1
159	PG2	LCDVD0	8 mA	1
160	VDD			
161	PG1	ETHERTXCLK	8 mA	1
162	PG0	ETHERTXEN	8 mA	1
163	PH7	ETHERTX3	8 mA	1
164	PH6	ETHERTX2	8 mA	1
165	PH5	ETHERTX1	8 mA	1
166	PH4	ETHERTX0	8 mA	1
167	PH3	ETHERTXER	8 mA	1
168	VSS			
169	PH2	ETHERRXCLK	8 mA	1
170	PH1	ETHERRXDV	8 mA	1
171	PH0	ETHERRX3	8 mA	1
172	PI7	ETHERRX2	8 mA	1
173	PI6	ETHERRX1	8 mA	1
174	PI5	ETHERRX0	8 mA	1
175	PI4	ETHERRXER	8 mA	1
176	PI3	ETHERCRS	8 mA	1

NOTES:
1. Internal pull-down. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
2. Internal pull-up. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
3. Input with Schmitt Trigger.
4. USB Inputs/outputs are tristated.
5. Crystal Inputs should be driven to a maximum of 1.8 V ± 10%.
6. Output is for crystal oscillator only, no drive capability.
7. Output Drive Values shown are MAX. See 'DC Specifications'.
8. All unused analog pins, and XTAL32IN (if unused) should be tied to ground through a 33KΩ resistor.

Table 7. TESTx PIN FUNCTION

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

Table 8. LH79524 LCD Data Multiplexing

LFBGA BALL NO.	LFBGA BALL NAME	STN						TFT
		MONO 4-BIT		MONO 8-BIT		COLOR		COLOR
		SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL
C2	LCDVD15	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	INTENSITY
C1	LCDVD14	X	X	X	MLSTN4	X	CLSTN4	BLUE4
C10	LCDVD13	X	X	MUSTN6	MUSTN6	CUSTN6	CUSTN6	BLUE3
A10	LCDVD12	X	X	X	MLSTN7	X	CLSTN7	BLUE2
A11	LCDVD11	X	X	X	MLSTN6	X	CLSTN6	BLUE1
B10	LCDVD10	X	X	X	MLSTN5	X	CLSTN5	BLUE0
C9	LCDVD9	X	MLSTN3	X	MLSTN3	X	CLSTN3	GREEN4
B9	LCDVD8	X	MLSTN2	X	MLSTN2	X	CLSTN2	GREEN3
A9	LCDVD7	X	MLSTN1	X	MLSTN1	X	CLSTN1	GREEN2
A8	LCDVD6	X	MLSTN0	X	MLSTN0	X	CLSTN0	GREEN1
B8	LCDVD5	X	X	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN0
C8	LCDVD4	X	X	MUSTN5	MUSTN5	CUSTN5	CUSTN5	RED4
A7	LCDVD3	X	X	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED3
B7	LCDVD2	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED2
C7	LCDVD1	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED1
A6	LCDVD0	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED0

NOTES:
1. Recommended hookups for TFT 5:5:5 + Intensity and 5:6:5 are shown.
2. The Intensity bit is identically generated for all three colors.
3. Connect to the LSB of the Red, Green, and Blue inputs of a 6:6:6 panel.
4. CLSTN = Color Lower data bit for STN panel.
5. CUSTN = Color Upper data bit for STN panel.
6. MLSTN = Monochrome Lower data bit for STN panel.
7. MUSTN = Monochrome Upper data bit for STN panel.

Table 9. LH79525 LCD Data Multiplexing

PIN NO.	PIN NAME	STN MONO 4-BIT	
		SINGLE PANEL	DUAL PANEL
145	LCDVD11	MUSTN1	MUSTN1
146	LCDVD10	MUSTN0	MUSTN0
147	LCDVD9		
149	LCDVD8		
151	LCDVD7		MLSTN3
153	LCDVD6		MLSTN2
154	LCDVD5		MLSTN1
155	LCDVD4		MLSTN0
156	LCDVD3		

Table 9. LH79525 LCD Data Multiplexing

PIN NO.	PIN NAME	STN MONO 4-BIT	
		SINGLE PANEL	DUAL PANEL
157	LCDVD2		
158	LCDVD1	MUSTN3	MUSTN3
159	LCDVD0	MUSTN2	MUSTN2

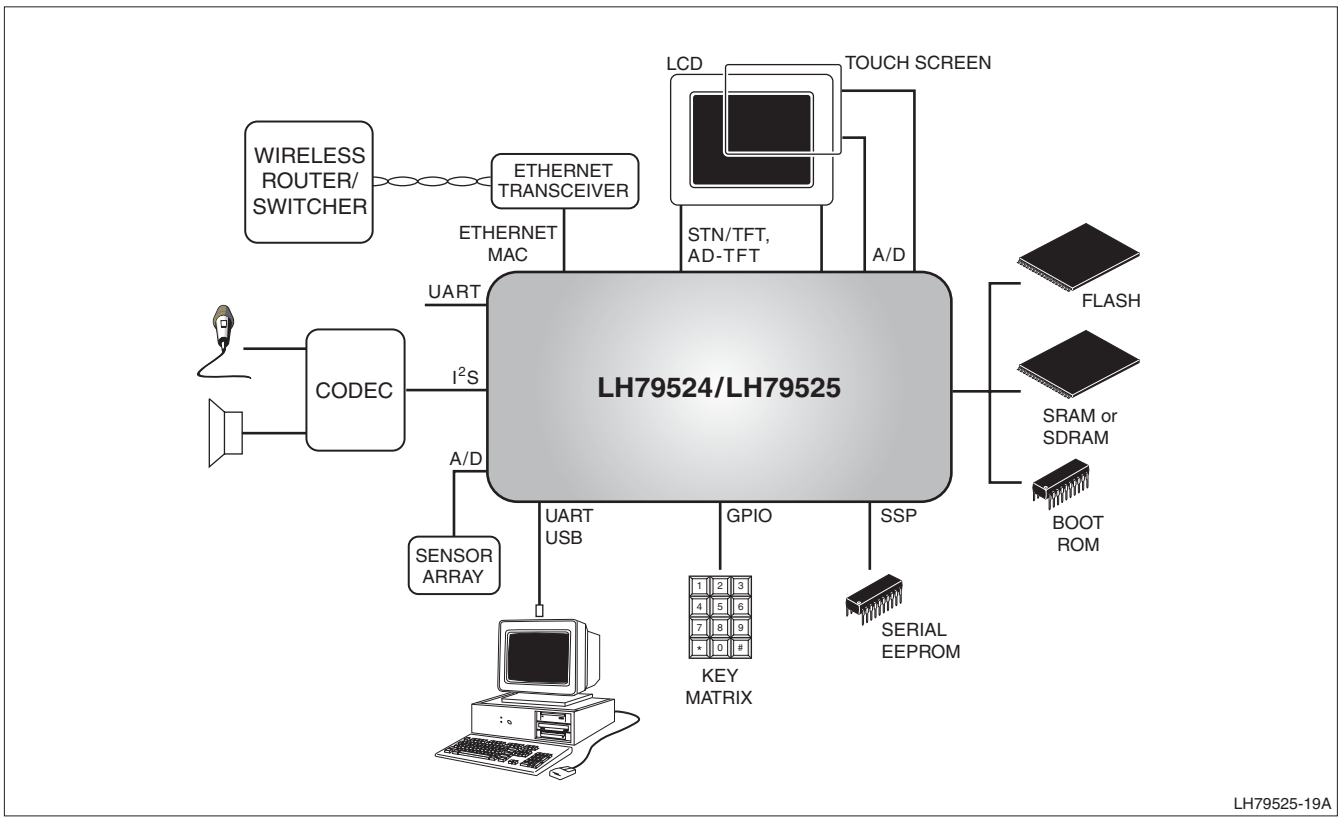


Figure 4. LH79524/LH79525 Application Diagram Example

SYSTEM DESCRIPTIONS

ARM720T Processor

The LH79524/LH79525 microcontrollers feature the ARM720T cached core with an Advanced High-Performance Bus (AHB) interface. The ARM720T features:

- 32-bit ARM720T RISC Core
- 8 kB Cache
- MMU (Windows CE enabled)

The core processor for both is a member of the ARM7T family of processors. For more information, see the ARM document, 'ARM720T (Rev 3) Technical Reference Manual', available on ARM's website at www.ARM.com.

The LH79524/LH79525 MMU allows mapping Physical Memory (PA) addresses to virtual memory addresses. This allows physical memory, which is constrained by hardware to specific addresses, to be reorganized at addresses identified by the user. These user identified locations are called Virtual Addresses (VA). When the MMU is enabled, Code and Data must be built, loaded, and executed using Virtual Addresses which the MMU translates to Physical Addresses. In addition, the user may implement a memory protection scheme by using the features of the MMU. Address translation and memory protection services provided by the MMU are controlled by the user. The MMU is directly controlled through the System Control Coprocessor, Coprocessor 15 (CP15). The MMU is indirectly controlled by a Translation Table (TT) and Page Tables (PT) prepared by the user and established using a portion of physical memory dedicated by the user to storing the TT and PT's.

External Memory Controller

An integrated External Memory Controller (EMC) provides a glueless interface to external SDRAM, Low Power SDRAM, Flash, SRAM, ROM, and burst ROM. Three remap options for the physical memory are selectable by software, as shown in Figure 5 through Figure 8.

The EMC supports six banks of external memory. Two chip selects for synchronous memory, and either two (LH79525) or four (LH79524) static memory chip selects are available. The static interface also includes two (LH79525) or four (LH79524) byte lane enable signals.

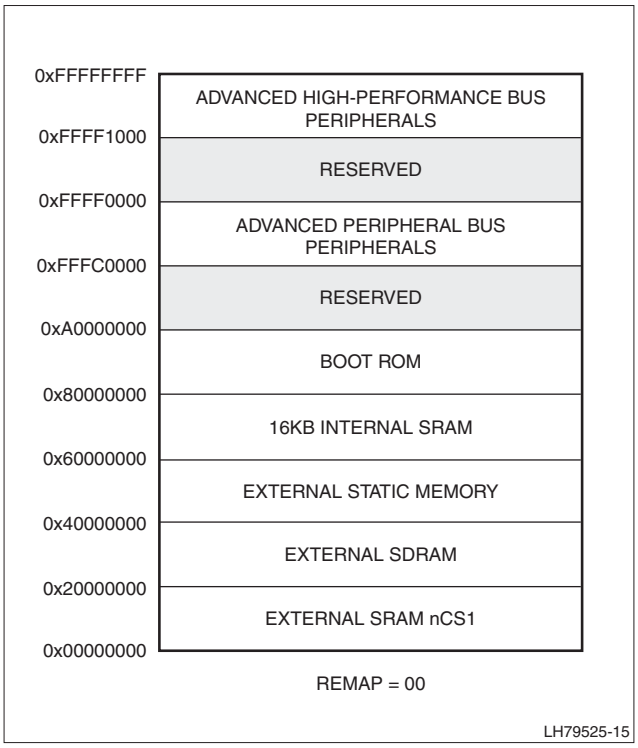


Figure 5. Memory Remap ‘00’

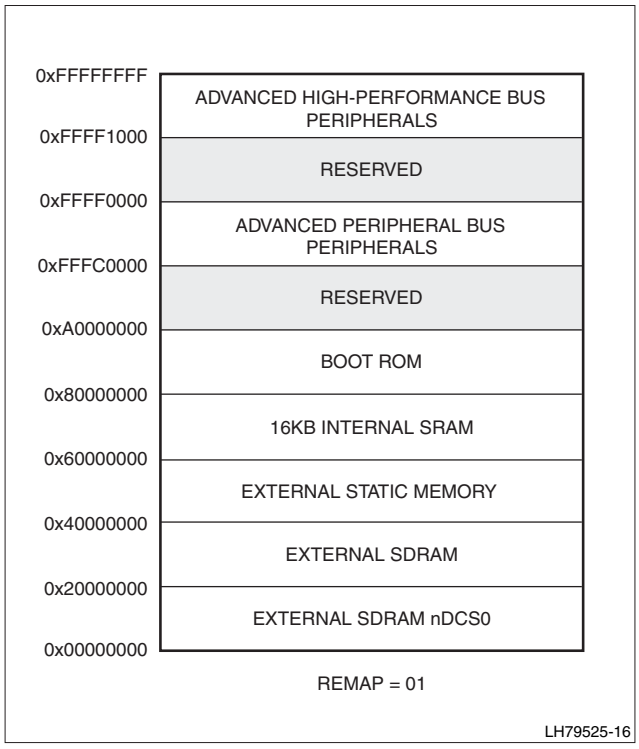


Figure 6. Memory Remap ‘01’

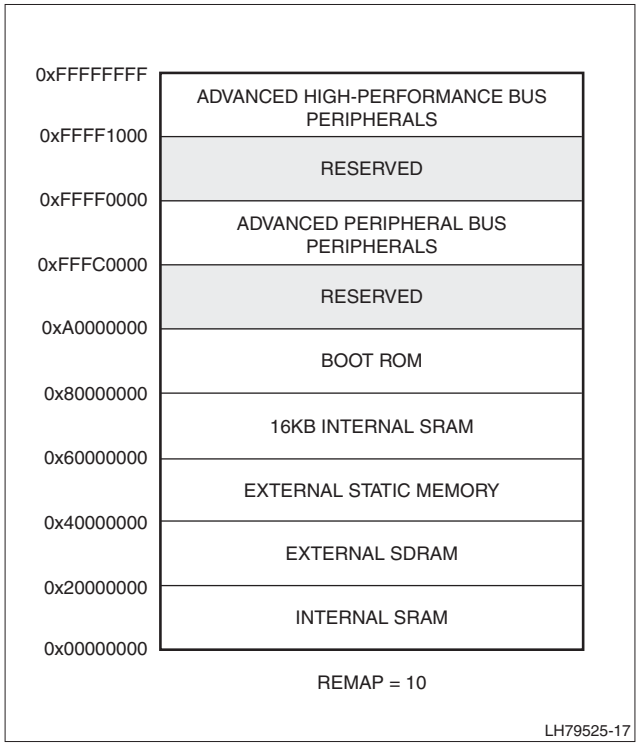


Figure 7. Memory Remap ‘10’

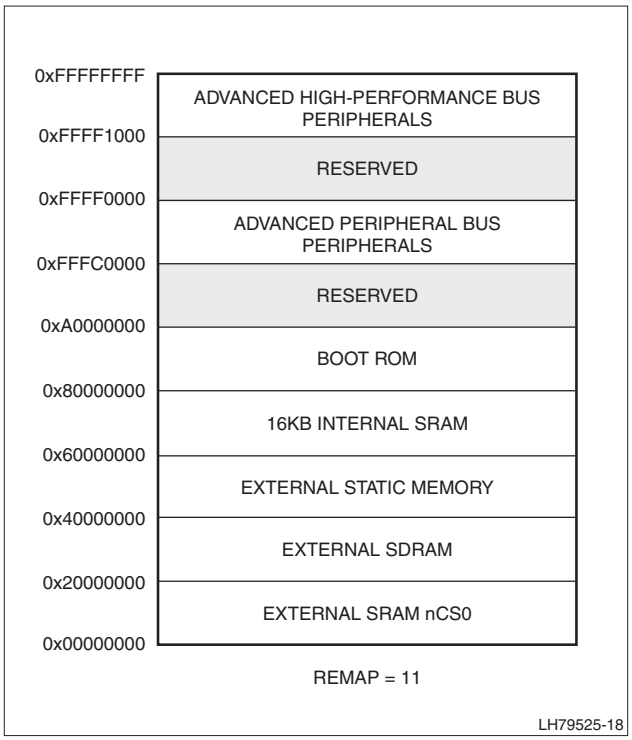


Figure 8. Memory Remap '11'

DMA Controller

The DMA Controller provides support for DMA-capable peripherals. The LCD controller uses its own DMA port, connecting directly to memory for retrieving display data.

- Simultaneous servicing of up to 4 data streams
- Three transfer modes are supported:
  - Memory to Memory
  - Peripheral to Memory
  - Memory to Peripheral
- Identical source and destination capabilities
- Transfer Size Programmable (byte, half-word, word)
- Burst Size Programmable
- Address Increment or Address Freeze
- Transfer Error interrupt for each stream
- 16-word FIFO array with pack and unpack logic

Handles all combinations of byte, half-word or word transfers from input to output.

Color LCD Controller (CLCDC)

The CLCDC provides all the necessary control and drive signals to interface directly with a variety of color and monochrome LCD panels.

- LH79524 has 16 LCD Data bits; LH79525 has 12 LCD Data bits.
- Supports single and dual scan color and monochrome Super Twisted Nematic (STN) displays with 4- or 8-bit interfaces (LH79524 only)
- Supports Thin Film Transistor (TFT) color displays
- Programmable resolution up to 1,024 × 1,024
- 15 gray-level mono, 3,375 color STN, and 64 k color TFT support
- 1, 2, or 4 bits-per-pixel (BPP) for monochrome STN
- 1-, 2-, 4-, or 8-BPP palettized color displays for color STN and TFT (1-, 2-, or 4-bit only on LH79525)
- True-color non-palettized, for color STN and TFT
- Programmable timing for different display panels
- 256-entry, 16-bit palette fast-access RAM
- Frame, line and pixel clock signals
- AC bias signal for STN or data enable signal for TFT panels
- Patented grayscale algorithm
- Interrupt Generation Events
- Dual 16-deep programmable 32-bit wide FIFOs for buffering incoming data.

ADVANCED LCD INTERFACE

The Advanced LCD Interface (ALI) allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The Advanced LCD Interface peripheral also provides a bypass mode that allows the LH79524/LH79525 to interface to the built-in timing ASIC in standard TFT and STN panels.

Synchronous Serial Port (SSP)

The SSP is a master or slave interface for synchronous serial communication with master or slave peripheral devices that support protocols for Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Interface.

- Master or slave operation
- Programmable clock rate
- Separate transmit FIFO and receive FIFO buffers, 16 bits wide, 8 locations deep
- DMA for transmit and receive
- Programmable interface protocols: Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Port
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts
- Available internal loopback test mode.

Universal Asynchronous Receiver Transmitter (UART)

The LH79524/LH79525 incorporates three UARTs. UART0, UART1, and UART2 offer similar functionality to the industry-standard 16C550. They perform serial-to-parallel conversion on data received from a peripheral device and parallel-to-serial conversion on data transmitted to the UART. The CPU reads and writes data and control status information through the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories that support programmable-service 'trigger levels', and overrun protection. These FIFO memories enable up to 32 characters to be stored independently in both transmit and receive modes.

- Programmable bits-per-character (5, 6, 7, or 8)
- Optional nine-bit mode to tag and recognize characters as either data or address
- Nine-bit Transmit FIFO and 12-bit Receive FIFO
- Programmable FIFO trigger points
- DMA support for UART0
- Programmable IrDA SIR input/output for each UART
- Separate 16-byte transmit and receive FIFOs to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Independent masking of transmit FIFO, receive FIFO, receive timeout and modem status interrupts
- False start bit detection
- Line break generation and detection
- Fully-programmable serial interface characteristics:
  - 5-, 6-, 7-, or 8-bit data word length
  - Even-, odd-, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
- IrDA SIR Encode/Decode block, providing:
  - Programmable use of IrDA SIR or UART input/output
  - Supports data rates up to 115.2 kbit/s half-duplex
  - Programmable internal clock generator, allowing division of the Reference clock in increments of 1 to 512 for low-power mode bit durations.
  - Loopback for testing

Vectored Interrupt Controller (VIC)

The Vectored Interrupt Controller combines the interrupt request signals from 20 internal and eight external interrupt sources and applies them, after masking and prioritization, to the IRQ and FIQ interrupt inputs of the ARM7TDMI processor core.

The Interrupt Controller incorporates a hardware interrupt vector logic with programmable priority for up to 16 interrupt sources. This logic reduces the interrupt response time for IRQ type interrupts compared to solutions using software polling to determine the highest priority interrupt source. This significantly improves the real-time capabilities of the LH79524/LH79525 in embedded control applications.

- 20 internal and eight external interrupt sources
  - Individually maskable
  - Status accessible for software polling
- IRQ interrupt vector logic for up to 16 channels with programmable priorities
- All of the interrupt channels, with the exception of the Watchdog Timer interrupt, can be programmed to generate:
  - FIQ interrupt request
  - Non-vectored IRQ interrupt request (software to poll IRQ source)
  - Vectored IRQ interrupt request (up to 16 channels total)
- The Watchdog timer can only generate FIQ interrupt requests
- External interrupt inputs programmable
  - Edge triggered or level triggered
  - Rising edge/active HIGH or falling edge/active LOW

The 32 interrupt channels are shown in Table 10.

Table 10. Interrupt Channels

CHANNEL	INTERRUPT SOURCE
0	WDT
1	Not Used
2	COMRX (used for debug)
3	COMTX (used for debug)
4	Counter/Timer0 Combined
5	Counter/Timer1 Combined
6	Counter/Timer2 Combined
7	External Interrupt 0
8	External Interrupt 1
9	External Interrupt 2
10	External Interrupt 3
11	External Interrupt 4
12	External Interrupt 5
13	External Interrupt 6
14	External Interrupt 7
15	RTC_ALARM
16	ACD TSIRQ Combined
17	ADC Brown Out INTR

Table 10. Interrupt Channels (Cont'd)

CHANNEL	INTERRUPT SOURCE
18	ADC Pen IRQ
19	CLCD Combined Interrupt
20	DMA Stream 0
21	DMA Stream 1
22	DMA Stream 2
23	DMA Stream 3
24	SSP I^2S Interrupt
25	Ethernet Interrupt
26	USB Interrupt
27	UART 0 Interrupt
28	UART 1 Interrupt
29	UART 2 Interrupt
30	USB DMA Interrupt
31	I^2C Interrupt

Reset, Clock, and Power Controller (RCPC)

The RCPC generates the various clock signals for the operation of the LH79524/LH79525 and provides for an orderly start-up after power-on and during a wake-up from one of the power saving operating modes. The RCPC allows the software to individually select the frequency of the various on-chip clock signals as required to operate the chip in the most power-efficient mode. The maximum speeds of the various clocks in the SoC are shown in Table 11. More detailed descriptions of each clock appear in the User's Guide.

The RCPC features:

- 10 - 20 MHz crystal oscillator and PLL for on-chip Clock generation (11.2896 MHz recommended)
- External Clock input if on-chip oscillator and PLL are not used
- 32.768 kHz crystal oscillator generating 1 Hz clock for Real Time Clock
- Individually controlled clocks for peripherals and CPU
- Programmable clock prescalers for UARTs and PWMs
- Five global power control modes are available:
  - Active
  - Standby
  - Sleep
  - Stop1
  - Stop2
- CPU/Bus clock frequency can be changed on the fly
- Selectable clock output
- Hardware reset (nRESETIN) and software reset.

Table 11. Maximum Clock Speeds

NAME	FREQUENCY (MAX.)
Oscillator Clock (CLK OSC)	20.0 MHz
PLL System Clock (CLK PLL)	304.819 MHz
PLL USB Clock	48.0 MHz
32.768 kHz Oscillator Clock	32.768 kHz
AHB Clock (HCLK)	50.803 MHz
AHB Fast CPU Clock (FCLK CPU)	76.205 MHz
Ethernet Clock	50.803 MHz
DMA Clock	50.803 MHz
External Memory Controller Clock	50.803 MHz
SSP Clock	50.803 MHz
CLCD Clock	50.803 MHz
UART[2:0] Clock	20.0 MHz
RTC Clock	1.0 Hz

Table 12. Clock Activity for Different Power Modes

DEVICE	ACTIVE	STANDBY	SLEEP	STOP1	STOP2
RTC 32 kHz Oscillator	ON	ON	ON	ON	ON
10 - 20 MHz Oscillator	ON	ON	ON	ON	OFF
PLL	ON	ON	ON	OFF	OFF
Peripheral Clock	ON	ON	OFF	OFF	OFF
CPU Clock	ON	OFF	OFF	OFF	OFF

Real Time Clock

The RTC provides an alarm or long time base counter. An interrupt is generated following counting a programmed number of one-second periods. The 1 Hz RTC clock is internally derived. The RTC features:

- 32-bit up counter with programmable load
- Programmable 32-bit match compare register
- Software maskable interrupt when counter and compare registers are identical.

RTC input clock sources:

- PLL clock
- 32.768 kHz clock
- 1 Hz clock (default).

Watchdog Timer

The Watchdog Timer provides hardware protection against malfunctions. It is a programmable timer to be reset by software at regular intervals. Failure to reset the timer will cause a FIQ interrupt. Failure to service the FIQ interrupt will then generate a System Reset. The features of the Watchdog Timer are:

- Driven by the bus clock
- 16 programmable time-out periods: 2^{16} through 2^{31} clock cycles
- Generates a reset or an FIQ Interrupt whenever a time-out period is reached
- Software enable, lockout, and counter-reset mechanisms add security against inadvertent writes
- Protection mechanism guards against interrupt-service failure:
  - The first WDT time-out triggers FIQ and asserts nWDFIQ status flag
  - If FIQ service routine fails to clear nWDFIQ, then the next WDT time-out triggers a system reset.

Timers

The LH79524 and LH79525 incorporate three 16-bit independently programmable Timer modules. The timers are clocked by the system clock, but have an internal scaled-down system clock that is used for the Pulse Width Modulator (PWM) and compare functions.

All counters are incremented by an internal prescaled counter clock or external clock and can generate an overflow interrupt. All three timers have separate internal prescaled counter clocks, with either a common external clock or a prescaled version of the system clock.

- Timer 0 has five Capture Registers and two Compare Registers.
- Timer 1 and Timer 2 have two Capture and two Compare Registers each.

The Capture Registers have edge-selectable inputs and can generate an interrupt. The Compare Registers can force the compare output pin either HIGH or LOW upon a match.

The timers support a PWM Mode that uses the two Timer Compare Registers associated with a timer to create a PWM. Each timer can generate a separate interrupt. The interrupt becomes active if any enabled compare, capture, or overflow interrupt condition occurs. The interrupt remains active until all compare, capture, and overflow interrupts are cleared.

General Purpose Input/Output (GPIO)

The LH79524 provides up to 108 bits of programmable input/output, and the LH79525 provides 86 bits. Many of the GPIO pins are multiplexed with other signals. All GPIO feature:

- Individually programmable input/output pins
- All default to Input on power-up.
- LH79524
  - Ports A-I, K, L, and N: Bidirectional I/O (Port N is 4 bits wide)
  - Port J: Input only
  - Port M: Output only
- LH79525
  - Ports A-I: Bidirectional I/O
  - Port J: Input only
  - Port M: Output only (6 bits wide)

Boot Controller

The boot controller allows selection of the hardware device to be used for booting.

- Supports booting from 8-, 16-, or 32-bit devices, selectable via external pins at power-on reset
- Configures the byte lane boot state for nCS1, selectable via external pins at power-on reset.
- Supports booting from alternate external devices (e.g., NAND flash) via external pins on power-on reset
- Glueless interface to external NAND flash.

USB Device

The USB Device integrated into the LH79524/LH79525 is compliant with the USB 1.1 and 2.0 specification, and compatible with both the OpenHCI and Intel UHCI standards. The USB Device:

- Supports Full-Speed (12 Mbit/s) operation, and suspend and resume signaling
- Four Endpoints
- Bulk/Interrupt or Isochronous Transfers
- FIFO for each Endpoint direction (except EP0 which shares a FIFO between IN/OUT). FIFOs exist in 2464 × 8 RAM
- Supports DMA accesses to FIFO.

Ethernet MAC Controller

The on-board Ethernet MAC Controller (EMAC) is compatible with IEEE 802.3, and has passed the University of New Hampshire (UNH) testing. It supports both 10- and 100-Mbit/s, and full and half duplex operation. Other features include:

- Statistics counter registers for RMON/MIB
- MII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- Transmit and receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific (hardware) 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Supports physical layer management through MDIO interface
- Supports serial network interface operation
- Support for:
  - Half duplex flow control by forcing collisions on incoming frames
  - Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
  - 802.Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Software configures the MAC address
- Jumbo frames of up to 10,240 bytes supported.

I^2C Controller

The I^2C Controller includes a two-wire I^2C serial interface capable of operating in either Master or Slave mode. The block conforms to the I^2C 2.1 Bus Specification for data rates up to 400 kbit/s. The two wires are SCL (serial clock) and SDA (serial data). The I^2C module provides the following features:

- Two-wire synchronous serial interface
- Operates in both the standard mode, for data rates up to 100 kbit/s, and the fast mode, with data rates up to 400 kbit/s
- Communicates with devices in the fast mode as well as the standard mode if both are attached to the bus.

SSP To I^2S Converter

The SSP to I^2S converter is an interface that converts a synchronous serial communication stream in TI DSP-compatible mode into an I^2S compliant synchronous serial stream. The I^2S converter operates on serial data in both master and slave mode.

The I^2S converter provides:

- Programmable Word Select (WS) delay
- Left/right channel information:
  - Current WS value at the pin
  - WS value associated with next entry written to TX FIFO
  - WS value associated with next entry read from RX FIFO
- Ability to invert WS state
- Ability to invert the bit clock
- Supports frame size of 16 bits only. Any other frame size will result in a frame size error. Each frame transmits starting with the most-significant bit.
- Master and slave modes supported
- As with the SSP, a single combined interrupt is generated as an OR function of the individual interrupt requests. This interrupt replaces the SSP interrupt, which is used solely as an input to the I^2S converter.
- Additional interrupts:
  - Transmit FIFO underrun
  - Transmit frame size error
  - Receive frame size error
- A set of Interrupt registers contain all the information in the SSPIMSC, SSPRIS, and SSPMIS registers, plus the transmit underrun error and frame size errors
- Additional status bits:
  - Transmit FIFO Full
  - Receive FIFO Empty
- Passes SSP data unaltered when module is not enabled
- Loopback Test Mode support.

ADC and Brownout Detector

The ADC block consists of an 10-channel, 10-bit Analog-to-Digital Converter with integrated Touch Screen Controller (TSC). The complete touch screen interface is achieved by combining the front-end biasing, control circuitry with analog-to-digital conversion, reference generation, and digital control.

The ADC has a bias-and-control network that allows correct operation with both 4- and 5-wire touch panels. A 16-entry × 16-bit wide FIFO holds a 10-bit ADC output and a 4-bit tag number.

When the screen is touched, it pushes the conductive coating on the coversheet against the coating on the glass, making electrical contact. The voltages produced are the analog representation of the position touched. The voltage level of the coversheet is converted continuously by the ADC and monitored by the system.

Other features include:

- 10-bit fully differential Successive Approximation Register (SAR) with integrated sample/hold
- A 10-channel multiplexer that routes user-selected inputs to the ADC in single-ended and differential modes
- A 16-entry × 16-bit wide FIFO that holds the 10-bit ADC output
- Front bias-and-control network for touch screen interface and support functions, which are compatible with industry-standard 4- and 5-wire touch-sensitive panels
- Touch-pressure sensing circuits
- Pen-down sensing circuit and interrupt generator
- Independent voltage reference generator
- Conversion automation function to minimize interrupt overhead
- Brownout Detector
- Battery Control Signal.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
DC Core Supply Voltage	VDDC	-0.3 to 2.4	V
DC I/O Supply Voltage	VDD	-0.3 to 4.6	V
DC Analog Supply Voltage for ADC	VDDA0	-0.3 to 4.6	V
	VDDA1	-0.3 to 2.4	V
	VDDA2	-0.3 to 2.4	V
Storage Temperature	TSTG	-55 to +125	°C

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Recommended Operating Conditions

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	1.7 V	1.8 V	1.9 V	1, 4
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	4
DC Analog Supply Voltage (VDDA0)	3.0 V	3.3 V	3.6 V	
DC Analog Supply Voltage (VDDA1)	1.7 V	1.8 V	1.9 V	
DC Analog Supply Voltage (VDDA2)	1.7 V	1.8 V	1.9 V	
Clock Frequency	3.27 MHz		76.205 MHz	2
Crystal Frequency	10.0 MHz	11.2896 MHz	20.0 MHz	3
Operating Temperature (Industrial)	-40°C	25°C	+85°C	

NOTES:
1. Linear Regulator disabled.
2. With PLL enabled. Without PLL, minimum frequency is 0 MHz. Some peripherals may not operate at minimum frequency.
3. Choose 11.2896 MHz to ensure proper operation of the I^2S, USB, and UART peripherals.
4. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 28.

Power Supply Sequencing

When the linear regulator is *not* enabled, NXP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 μs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up. To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

DC/AC Specifications

Unless noted, all data provided are based on:

- -40°C to +85°C (Industrial temperature range)
- VDDC = 1.7 V to 1.9 V
- VDD = 3.0 V to 3.6 V, VDDA = 1.7 V to 1.9 V.

DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIH	CMOS input HIGH voltage	2.0		5.5	V	CEN = 1
VIL	CMOS input LOW voltage			0.8	V	CEN = 1
VIT+	Positive Input threshold voltage (Schmitt pins)	2.0			V	CSEN = 1
VIT-	Negative Input threshold voltage (Schmitt pins)			0.8	V	CSEN = 1
VHYST	Schmitt trigger hysteresis		0.35		V	CSEN = 1
VOH[1]	Output drive (2 mA type)	2.6			V	IOH = -2 mA
	Output drive (4 mA type)	2.6			V	IOH = -4 mA
	Output drive (8 mA type)	2.6			V	IOH = -8 mA
	Output drive (12 mA type)	2.6			V	IOH = -12 mA
VOL[1]	Output drive (2 mA type)			0.4	V	IOL = 2 mA
	Output drive (4 mA type)			0.4	V	IOL = 4 mA
	Output drive (8 mA type)			0.4	V	IOL = 7 mA
	Output drive (12 mA type)	2.6			V	IOH = 12 mA
RIN	Input leakage pull-up/pull-down resistors		40		kΩ	VIN = VDD or GND (Calculate input leakage current at desired VDD)
IACTIVE	Active current		85		mA	Note 2
ISTANDBY	Standby current		50		mA	Notes 2, 3
ISLEEP	Sleep current		3.8		mA	
ISTOP1	Stop1 current		420		μA	
ISTOP2	Stop2 current		115		μA	RTC ON, Linear Regulator ON
ISTOP2	Stop2 current		95		μA	RTC OFF, Linear Regulator ON
ISTOP2	Stop2 current		45		μA	RTC ON, Linear Regulator OFF
ISTOP2	Stop2 current		25		μA	RTC OFF, Linear Regulator OFF

NOTES:

1. Table 2 details each pin's buffer type.
2. Running Typical Application over operating range.
3. Current measured with CPU stopped and all peripherals enabled

Linear Regulator DC Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		μA
ISLEEPLR	Current with Linear Regulator disabled		8		μA
IOLR	Output Current Range	0.0		200	mA
VOLR	Output Voltage, Linear Regulator		1.84		V

AC Test Conditions

PARAMETER	RATING	UNIT
Supply Voltage (VDD)	3.0 to 3.6	V
Core Voltage (VDDC)	1.7 to 1.9	V
Input Pulse Levels	VSS to VDD	V
Input Rise and Fall Times	2	ns
Input and Output Timing Reference Levels	VDD/2	V

Power Consumption By Peripheral Device

Table 13 shows the typical power consumption by individual peripheral device.

Table 13. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
ADC/TSC	590	μA
Counter/Timers	203	μA
DMA	4.2	mA
Ethernet Controller	670	μA
I^2S	200	μA
LCD Controller	2.2	mA
RTC	5.1	μA
SSP	508	μA
UARTs	203	μA
USB Device (+PLL)	5.6 (+3.3)	mA

AC Specifications

All signals described in Table 14 relate to transitions after a reference clock signal. The illustration in Figure 9 represents all cases of these sets of measurement parameters; except for the Asynchronous Memory Interface — which are referenced to Address Valid.

The reference clock signals in this design are:

- HCLK, the System Bus clock
- PCLK, the Peripheral Bus clock (locked to HCLK in the LH79524/LH79525)
- SSPCLK, the Synchronous Serial Interface clock
- UARTCLK, the UART Interface clock
- LCDDCLK, the LCD Data clock from the LCD Controller
- and SDCLK, the SDRAM clock.

All signal transitions are measured from the 50% point of the clock to the 50% point of the signal. See Figure 9.

For outputs from the LH79524/LH79525, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from the rising edge of the reference clock signal. Maximum requirements for tOVXXX are shown in Table 14.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output will be held valid from the rising edge of the reference clock signal. Minimum requirements for tOHXXX are listed in Table 14.

For Inputs, tISXXX (e.g. tISD) represents the amount of time the input signal must be valid before the rising edge of the clock signal. Minimum requirements for tISXXX are shown in Table 14.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid from the rising edge of the reference clock signal. Minimum requirements are shown in Table 14.

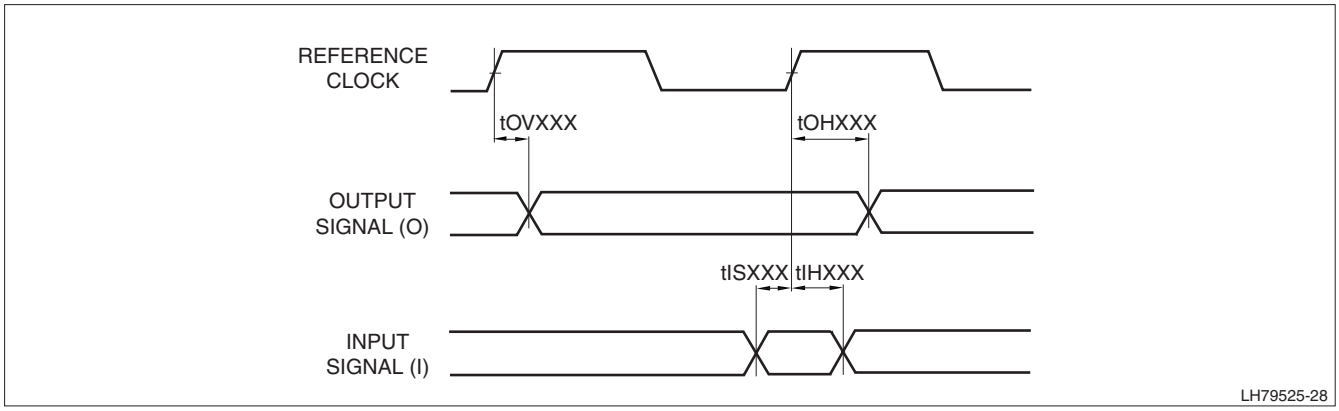


Figure 9. LH79524/LH79525 Signal Timing

Table 14. AC Signal Characteristics

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
ASYNCHRONOUS MEMORY INTERFACE SIGNALS						
A[27:0]	Output	50 pF	tWC	3 × tHCLK – 5.0 ns		Write Cycle time
	Input		tRC	2 × tHCLK – 5.0 ns		Read Cycle time
D[31:0]	Output	50 pF	tDHWE	tHCLK – 5.5 ns		Data out hold to nWE release
			tDWE	tHCLK – 4.5 ns		Data out valid to nWE release
			tDSCS	14.0 ns		Data valid to nCSx release
			tDSOE	12.5 ns		Data valid to nOE release
			tDSB	12.0 ns		Data valid to nBLEx release
			tDHCS	0.0 ns		nCSx release to data invalid
			tDHOE	0.0 ns		nOE release to data invalid
nCS[3:0]	Output	50 pF	tAV		2.5 ns	nCSx valid to Address valid
			tAHCS	tHCLK – 3.0 ns		Address hold after nCSx release
			tAHOE	tHCLK - 1.0 ns		Address hold after nOE release
			tASCS		2.5 ns	Address valid to nCSx valid
			tCW		2 × tHCLK + 3.0 ns	nCSx valid to nWE release
			tCB		2 × tHCLK	nCSx valid to nBLE release
			tCS	tHCLK – 3.5 ns		nCSx width
nBLE	Output	50 pF	tBV		1.5 ns	nCSx valid to nBLE valid
			tAHB	tHCLK – 2.0 ns		Address hold after nBLE release
			tDB	tHCLK – 6.0 ns		Data out valid to nBLE release
			tDHBR	0.0 ns		Data in hold to nBLE release
			tDHBW	tHCLK + 9 ns		Data out hold to nBLE release
			tBR	–2.0 ns		Address hold to nBLE release
			tAB		2 × tHCLK ns	Address valid to nBLE release
			tASB		1.0 ns	Address valid to nBLE valid
			tBLE	tHCLK – 4.5 ns		nBLE width (read)
			tBP	tHCLK – 4.5 ns		nBLE width (write)
nWE	Output	50 pF	tASWE		tHCLK + 1.5 ns	Address valid to nWE valid
			tAW		2 × tHCLK + 0.5 ns	Address valid to nWE release
			tWR	tHCLK – 3.0 ns		Address Hold to nWE release
			tWP	tHCLK – 1 ns		Write Enable width
nOE	Output	50 pF	tOE	tHCLK – 1 ns		Ouput Enable width
			tOEV		– 0.5 ns	nOE valid after nCSx valid
SYNCHRONOUS MEMORY INTERFACE SIGNALS						
A[23:0]	Ouput	50 pF	tOVA		tSDCLK/2 + 4.5 ns	Address Valid
D[31:0]	Output	50 pF	tOVD		tSDCLK/2 + 7.0 ns	Output Data Valid
			tOHD	tSDCLK/2 – 4.0 ns		Output Data Hold
	Input		tISD	5.0 ns		Input Data Setup
			tIHD	1.5 ns		Input Data Hold
nCAS	Output	50 pF	tOVCA		tSDCLK/2 + 4.0 ns	CAS Valid
			tOHCA	tSDCLK/2 – 4.0 ns		CAS Hold
nRAS	Output	50 pF	tOVRA		tSDCLK/2 + 4.5 ns	RAS Valid
			tOHRA	tSDCLK/2 – 4.0 ns		RAS Hold

Table 14. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
nWE	Output	30 pF	tOVSDW		tSDCLK/2 + 4.5 ns	SDWE Write Enable Valid
			tOHSDW	tSDCLK/2 – 4.0 ns		SDWE Write Enable Hold
SDCKE	Output	30 pF	tOVC0		tSDCLK/2 + 4.5 ns	SDCKE Clock Enable Valid
			tOHC0	tSDCLK/2 – 4.0 ns		SDCKE Clock Enable Hold
DQM[3:0]	Output	30 pF	tOVDQ		tSDCLK/2 + 5.0 ns	DQM Data Mask Valid
			tOHDQ	tSDCLK/2 – 4.0 ns		DQM Data Mask Hold
nSDCS[1:0]	Output	30 pF	tOVSC		tSDCLK/2 + 4.5 ns	SDCS Data Mask Valid
			tOHSC	tSDCLK/2 – 4.0 ns		SDCS Data Mask Hold
SDCLK	Output	30 pF	tSDCLK	19.37 ns		SDRAM Clock Period
SYNCHRONOUS SERIAL PORT (SSP)						
SSPFRM	Output	50 pF	tOVSSPFRM		14 ns	tOVSSPFRM Output Valid, Referenced to SSPCLK
SSPTX	Output	50 pF	tOVSSPTX		14 ns	SSP Transmit Valid
SSPRX	Input		tISSPRX	20 ns		SSP Receive Setup
ETHERNET MAC CONTROLLER (EMC)						
ETHERTXER	Output	50 pF	tOVTXER		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXER	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERTX[3:0]	Output	50 pF	tOVTXD		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXD	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERTXEN	Output	50 pF	tOVTXEN		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXEN	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERRXDV	Input		tISRXDV	10 ns		Receive Data Setup prior to ETHERRXCLK
			tIHRXDV	10 ns		Receive Data Hold prior to ETHERRXCLK
ETHERRX[3:0]	Input		tISRXD	10 ns		Receive Data Setup prior to ETHERRXCLK
			tIHRXD	10 ns		Receive Data Hold prior to ETHERRXCLK

Analog-To-Digital Converter Electrical Characteristics

Table 15 shows the ADC electrical characteristics. See Figure 10 for the ADC transfer characteristics.

Table 15. ADC Electrical Characteristics

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Data Format		binary			
CLK Frequency	500		5,000	ns	
Differential Non-Linearity	-0.99		3.0	LSB	
Integral Non-Linearity	-3.0		+3.0	LSB	
Offset Error	-10		+10	mV	
Gain Error	-2.0		+2.0	LSB	
Reference Voltage Output	1.85	2.0	2.15	V	
VREF-	VSSA	VSSA	(VREF+) -1.0 V	V	2
VREF+	(VREF-) +1.0 V	VREF	VDDA	V	2
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDA	V	3
Analog Input Current			5	μA	
Reference Input Current			5	μA	
Analog input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDA0		590	1000	μA	
Powerdown Current, VDDA0		1	10	μA	
Standby Current		180	300	μA	4
Brown Out Trip Point (falling point)	2.36	2.63	2.9	V	
Brown Out Hysterisis		120		mV	
Operating Temperature	-40		85	°C	

NOTES:

1. The analog section of the ADC takes 16 × A2DCLK cycles per conversion plus 1 × A2DCLK cycles to be made available in the PCLK domain. An additional 3 × PCLK cycles are required before being available on the APB.
2. The internal voltage reference is driven to nominal value VREF = 2.0 V. Using the Reference Multiplexer, alternative low impedance (RS < 500) voltages can be selected as reference voltages. The range of voltages allowed are specified above. However, the on-chip reference cannot drive the ADC unless the reference buffer is switched on.
3. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds VREF+ or is below VREF-, the A/D result will saturate appropriately at positive or negative full scale. Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
4. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.

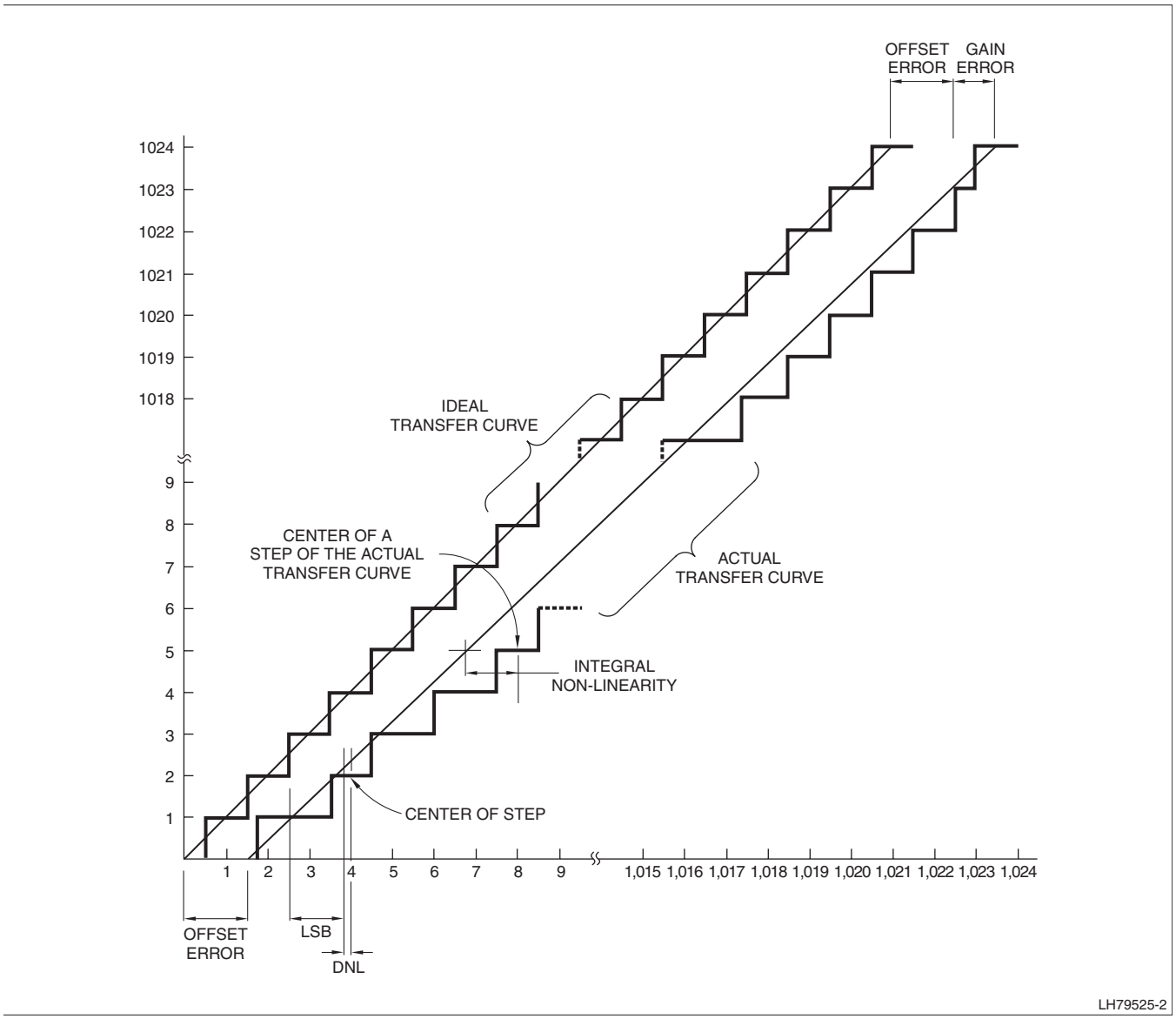


Figure 10. ADC Transfer Characteristics

External Memory Controller Waveforms

The External Memory Controller (EMC) handles transactions with both static and dynamic memory.

STATIC MEMORY WAVEFORMS

This section illustrates static memory transaction waveforms. Each wait state is one HCLK period.

nWAIT Input

The EMC's Static Memory Controller supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 11 through Figure 20.

Read and Write Waveforms

Figure 17 shows the Read cycle with zero wait states. As shown in the figure, SWAITOENx and SWAITRDx are programmed to 0 for minimum Read cycle time.

The zero programmed into the SWAITRDx indicates that the read occurs with zero wait states, on the first rising edge following Address Valid. After a small propagation delay, nOE is deasserted (as is nCSx), latching the data into the SoC. The address line is held valid one more HCLK period ('C' in the figure). Thus, the minimum Read cycle is two HCLK periods.

Figure 18 shows the minimum write cycle time with both SWAITWRx and SWAITWENx programmed to zero. The write access time is determined by the number of wait states programmed in the SWAITWRx register.

In Figure 18, nCSx is asserted coincident (following a small propagation delay) with Valid Address. Data becomes valid another small propagation delay later. Unlike Read transactions, nWE (or nBLEx) assertion is always delayed one HCLK cycle. The nBLEx signal has the same timing as nWE for write to 8-bit devices that use the byte lane enables instead of the write enables.

The nWE (or nBLEx) signal remains asserted for one HCLK cycle when the nWE (or nBLEx) signal is deasserted and the data is latched into the external memory device. Valid address is held for one additional cycle before deassertion ('C' in the figure), as is the Chip Select. The minimum Write cycle is three HCLK periods.

Read wait state programming uses the SWAITRDx register. Figure 19 shows the results of programming SWAITRDx to 0x3, setting the EMC for three wait states. The deassertion of nOE is delayed from the first rising HCLK edge following Valid Address, as in Figure 17, to the fourth rising edge, a delay of 3 HCLK periods.

Figure 20 shows the results of programming the SWAITWRx and SWAITWENx registers for two Write wait states: register SWAITWENx = 0x0, and SWAITWRx = 0x2. Assertion of nCSx precedes nWE (nBLEx) by one HCLK period. Then, instead of the nWE (nBLEx) signal deasserting one HCLK period after assertion, it is delayed two wait states and the signal deasserts on the rising edge following two wait states.

Chapter 7 of the User's Guide has detailed register descriptions and additional programming examples.

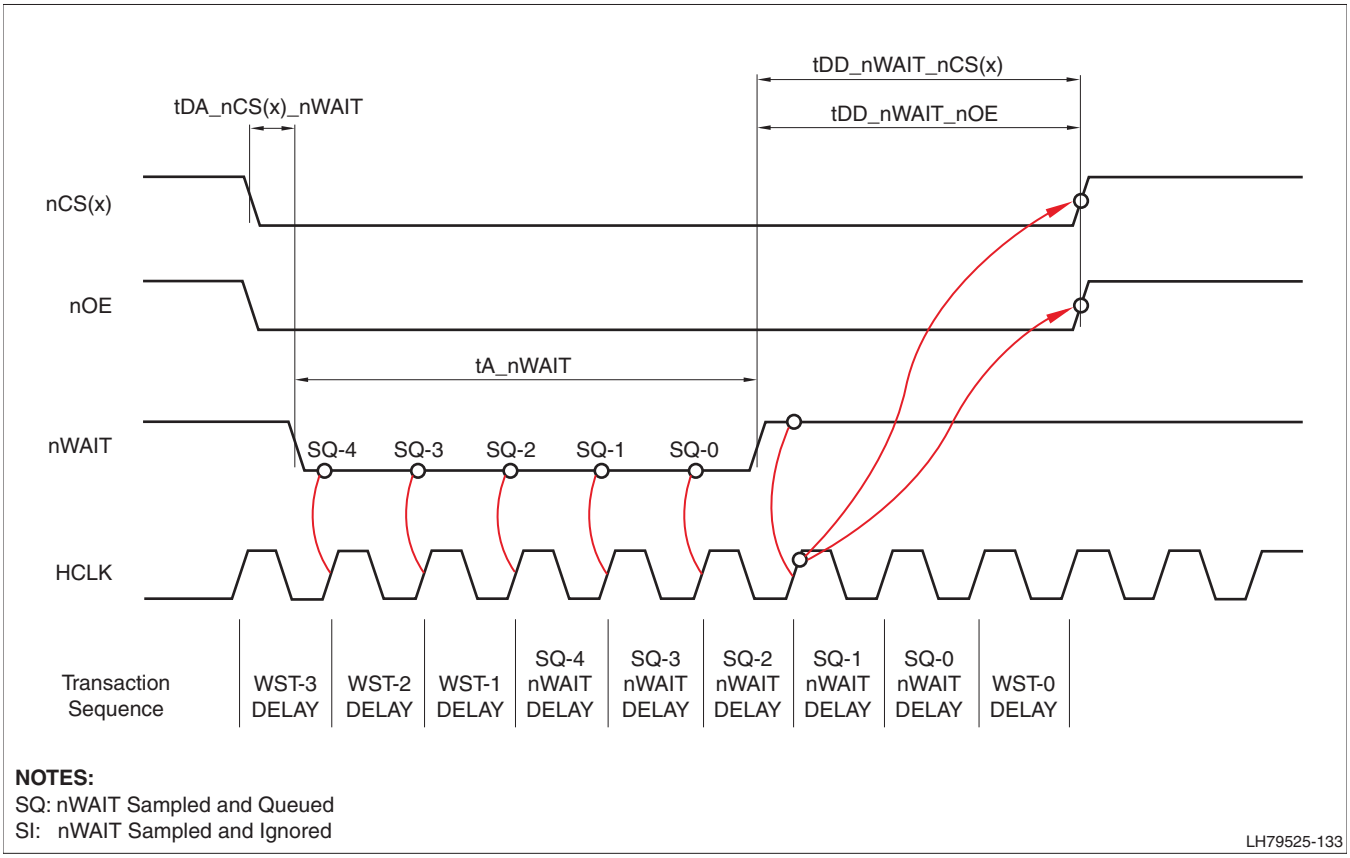


Figure 11. nWAIT Read Sequence (SWAITRDx = 3)

Table 16. nWAIT Read Sequence Parameter Definitions

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT [1]
tDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	16,365	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		4	HCLK periods
tDD_nWAIT_nOE	Delay from nWAIT deassertion to nOE deassertion		4	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:
1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O conditioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Read Wait States register (SWAITRDx) must be set to a minimum value of 3.
3. For each rising clock edge (HCLK) that the assertion of nWAIT lags the assertion of nCSx, another read wait state (SWAITRDx) must be added to the minimum requirement.
4. nWAIT delay cycles are *not* added for all nWAIT assertions sampled prior to WST-3. These nWAIT assertions are ignored.
5. nWAIT delay cycles are added for all nWAIT assertions sampled from WST-3 until the de-assertion of nWAIT. nWAIT delay cycles are added once the wait state countdown has reached WST-1.
6. Once nWAIT is sampled high, the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, any prolonged access (either due to nWAIT or the Extended Wait Register) that causes an SDRAM refresh failure may cause SDRAM data to be lost.
8. Timing assumes Output Enable Delay register (SWAITOENx) is programmed to 0.

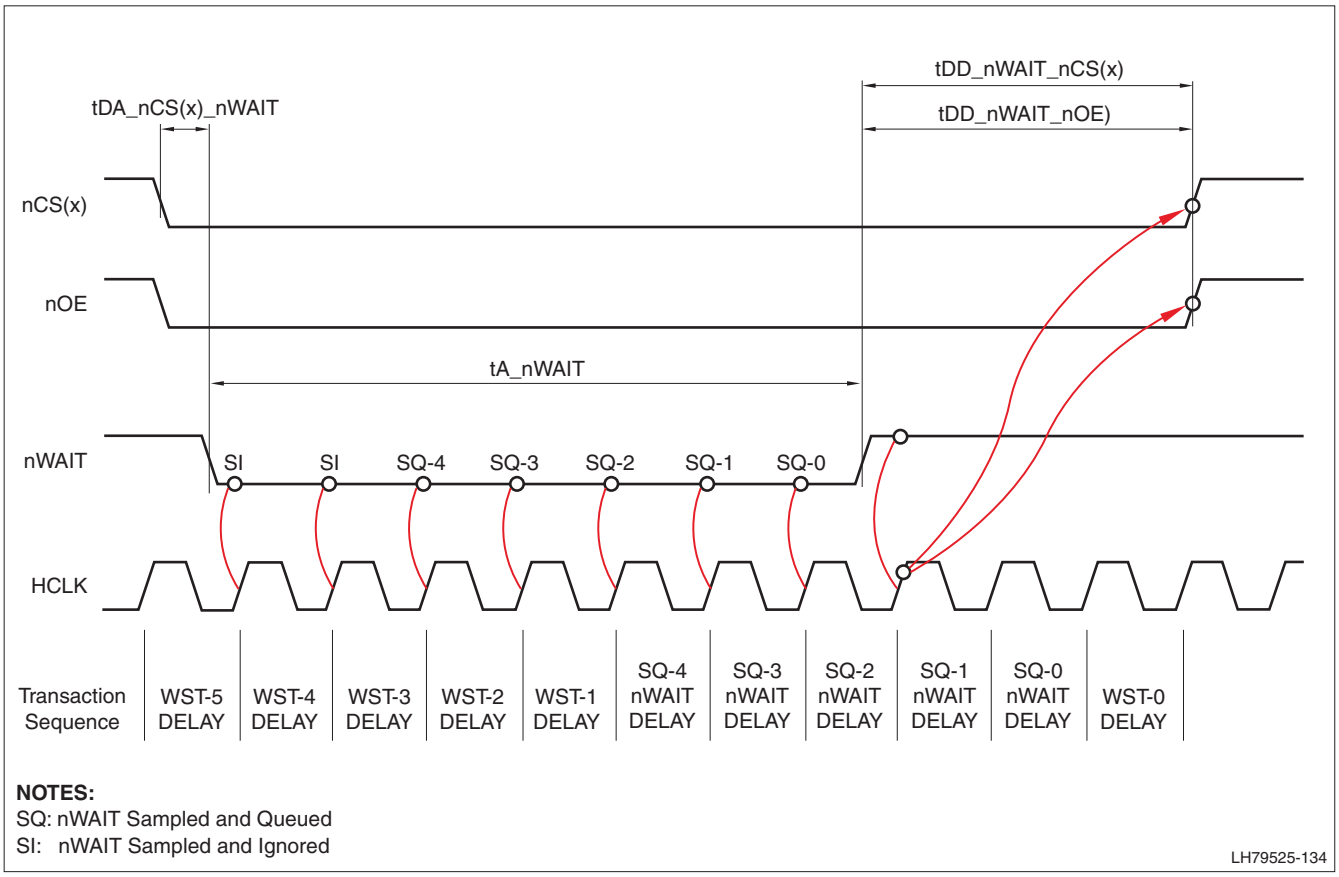


Figure 12. nWAIT Read Sequence (SWAITRDx = 5)

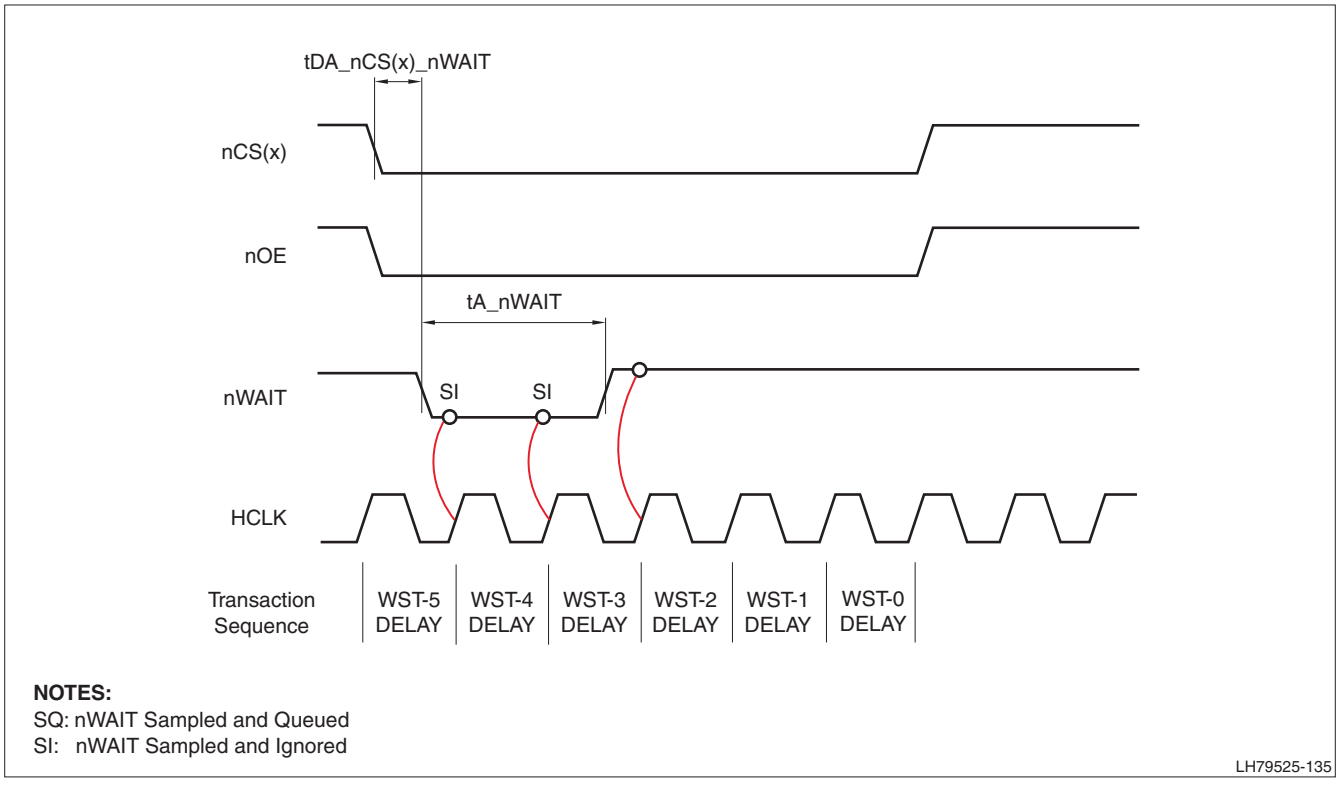


Figure 13. nWAIT Read Sequence (SWAITRDx = 5): nWAIT has no effect on the current transaction

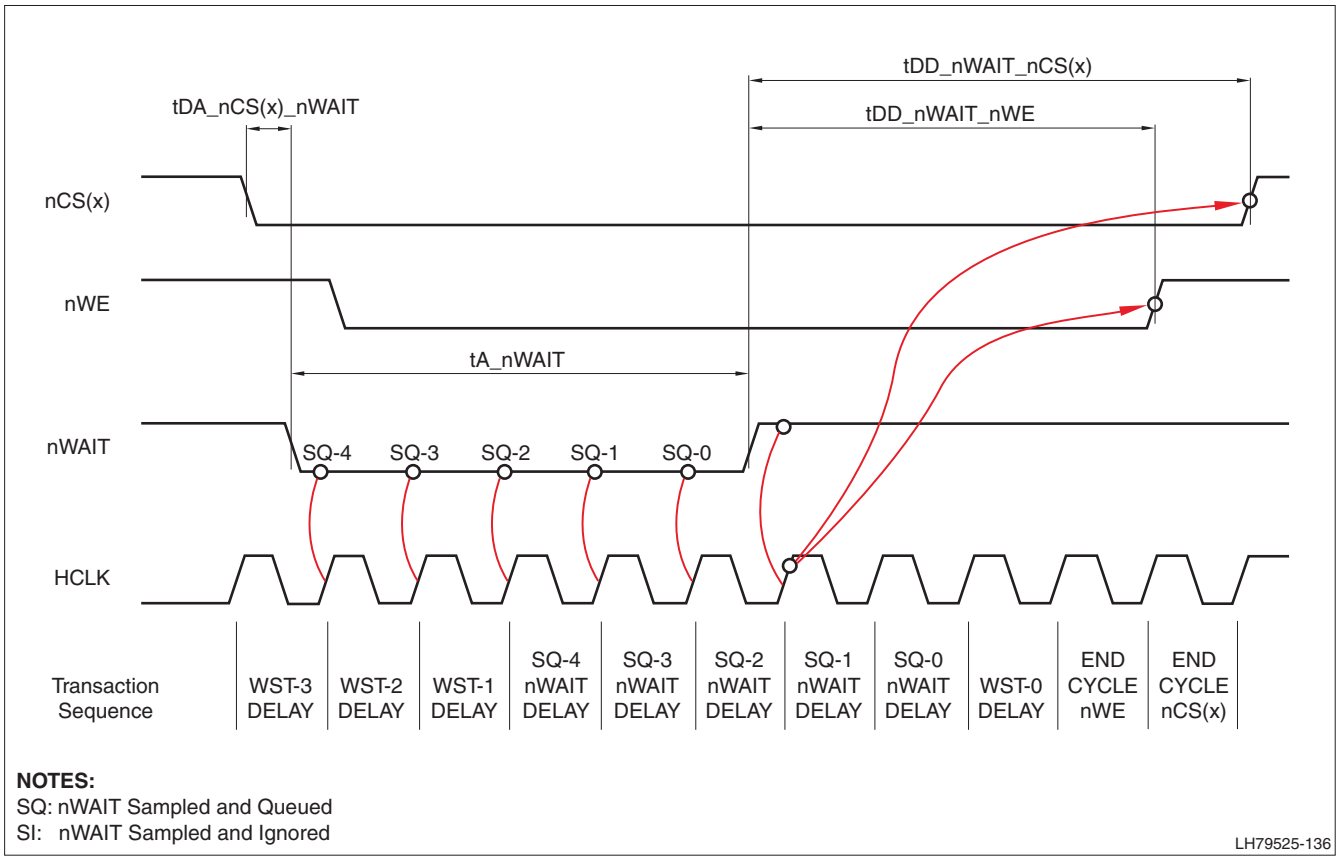


Figure 14. nWAIT Write Sequence (SWAITWRx = 3)

Table 17. nWAIT Write Sequence Parameter Definitions

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT[1]
tIDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	16,365	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		6	HCLK periods
tDD_nWAIT_nWE	Delay from nWAIT deassertion to nWE deassertion		5	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:

1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O conditioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Write Wait States register (SWAITWRx) must be set to a minimum value of 3.
3. For each rising clock edge (HCLK) that the assertion of nWAIT lags the assertion of nCSx, another write wait state (SWAITRDx) must be added to the minimum requirement.
4. nWAIT delay cycles are *not* added for all nWAIT assertions sampled prior to WST-3. These nWAIT assertions are ignored.
5. nWAIT delay cycles are added for all nWAIT assertions sampled from WST-3 until the de-assertion of nWAIT. nWAIT delay cycles are added once the wait state countdown has reached WST-1.
6. Once nWAIT is sampled high, the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, any prolonged access (either due to nWAIT or the Extended Wait Register) that causes an SDRAM refresh failure may cause SDRAM data to be lost.
8. Timing assumes Write Enable Delay register (SWAITWENx) is programmed to 0.

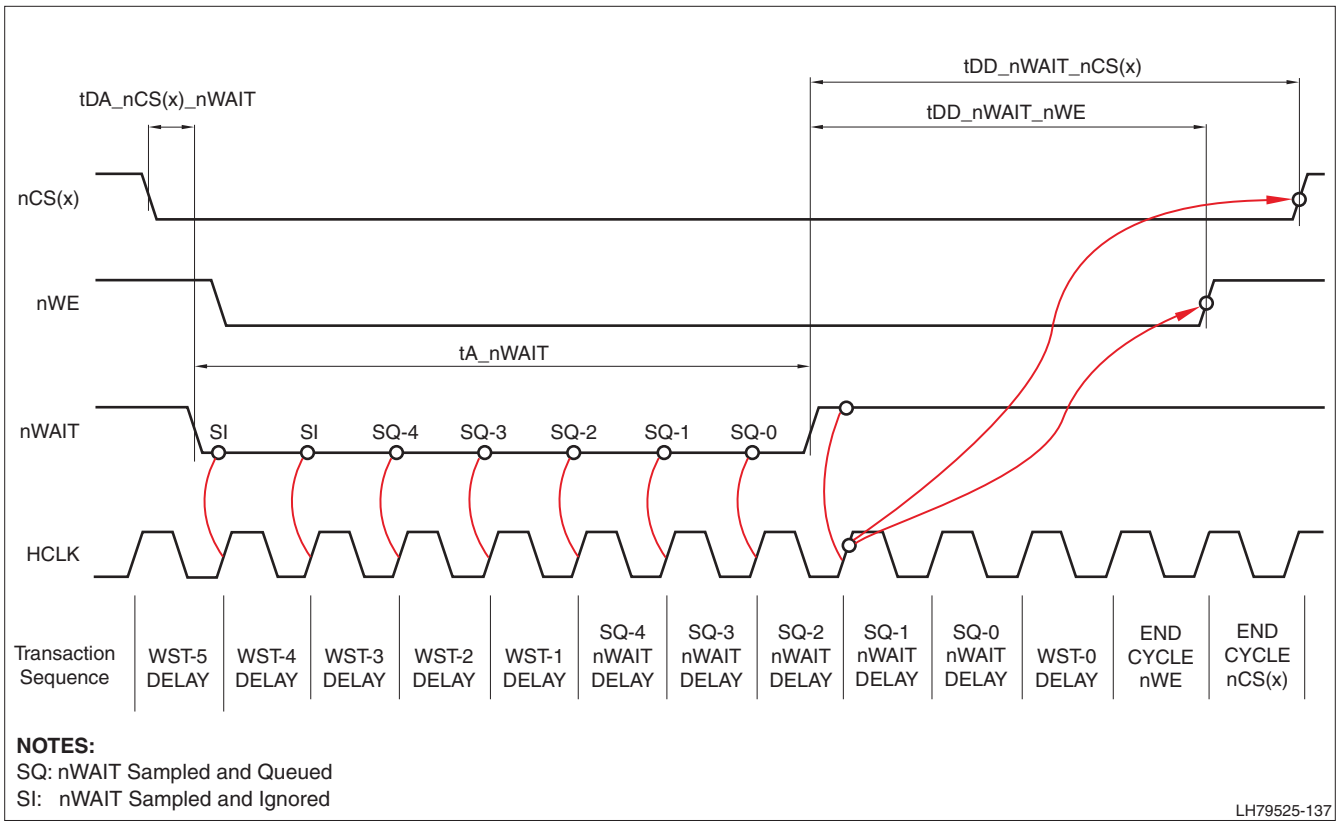


Figure 15. nWAIT Write Sequence (SWAITWRx = 5)

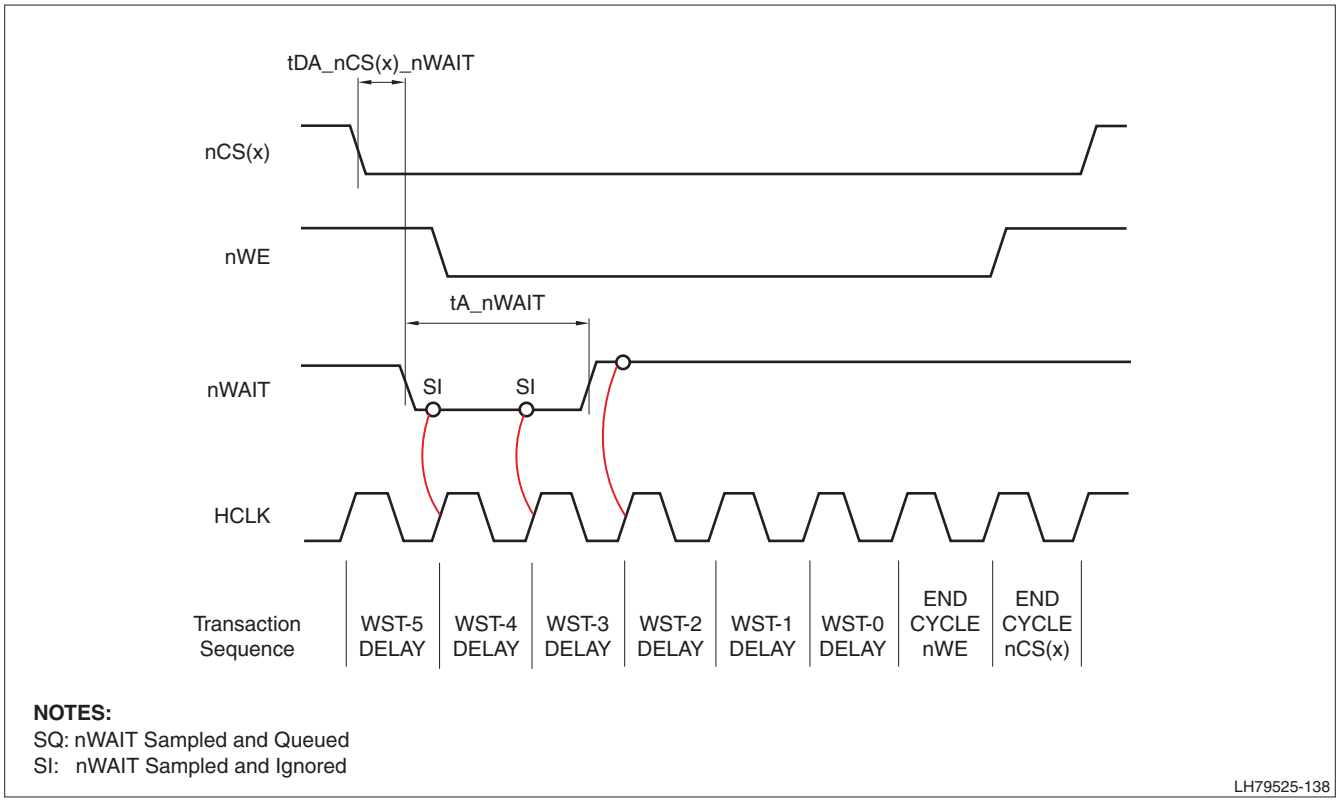


Figure 16. nWAIT Write Sequence (SWAITWRx = 5): nWAIT has no effect on the current transaction

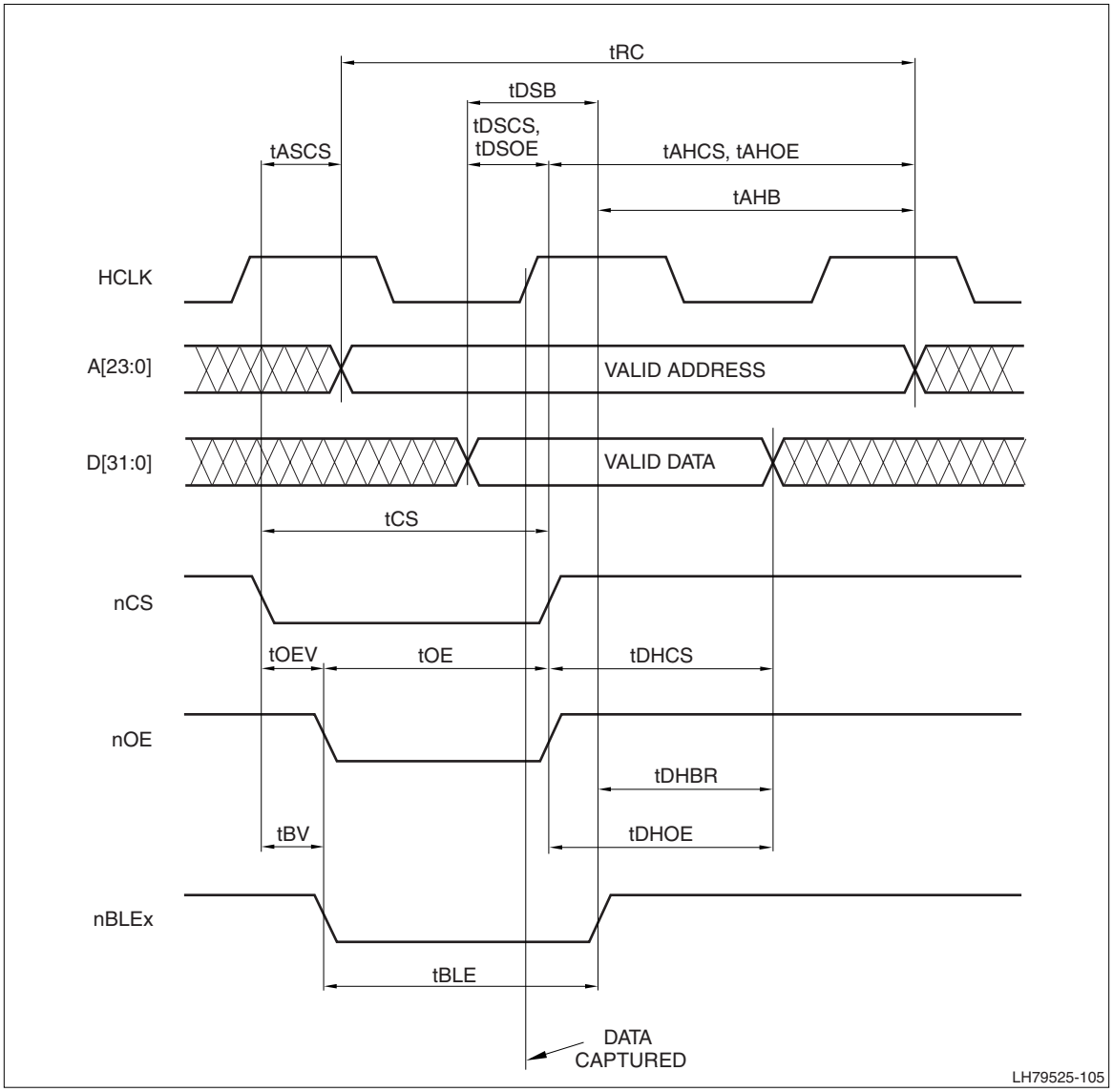


Figure 17. External Static Memory Read, Zero Wait States

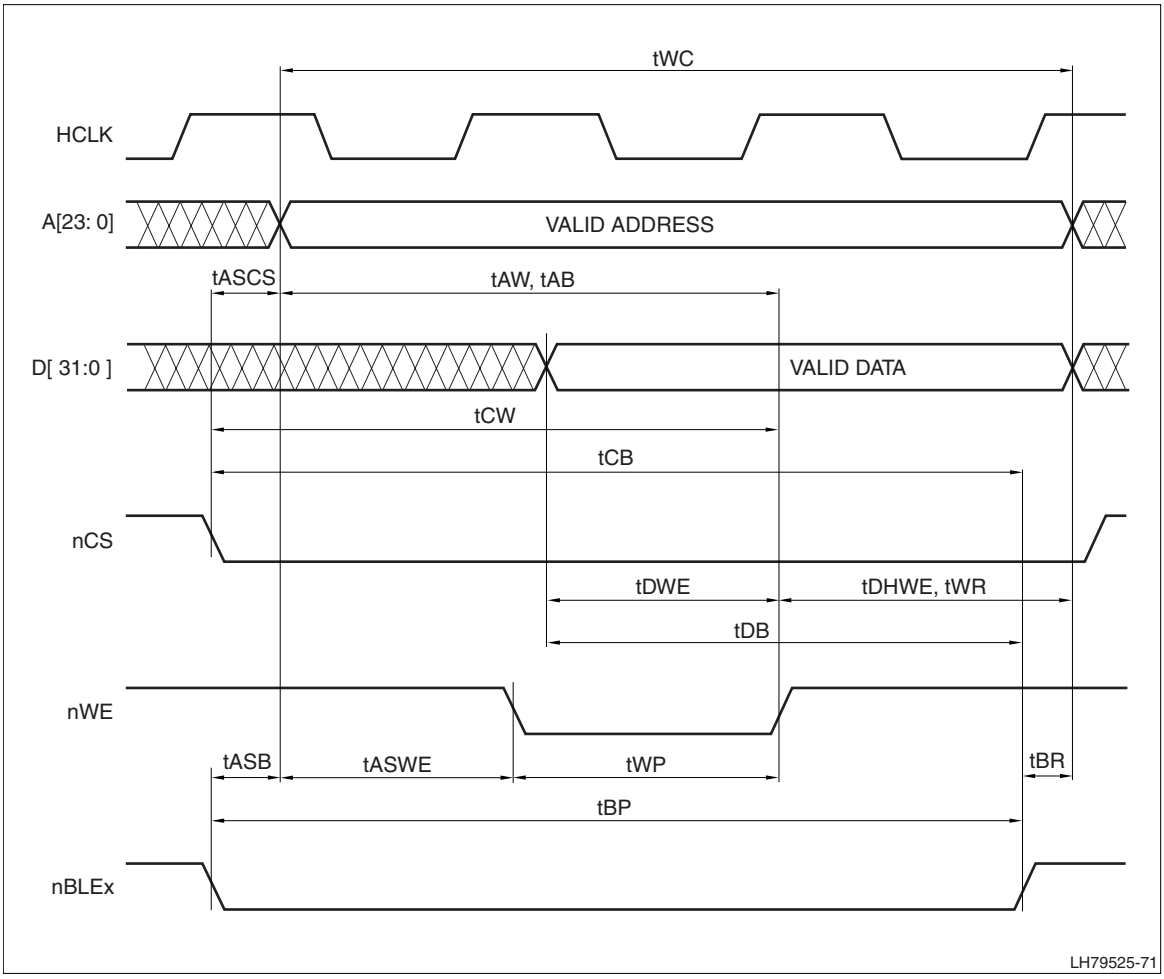


Figure 18. External Static Memory Write, Zero Wait States

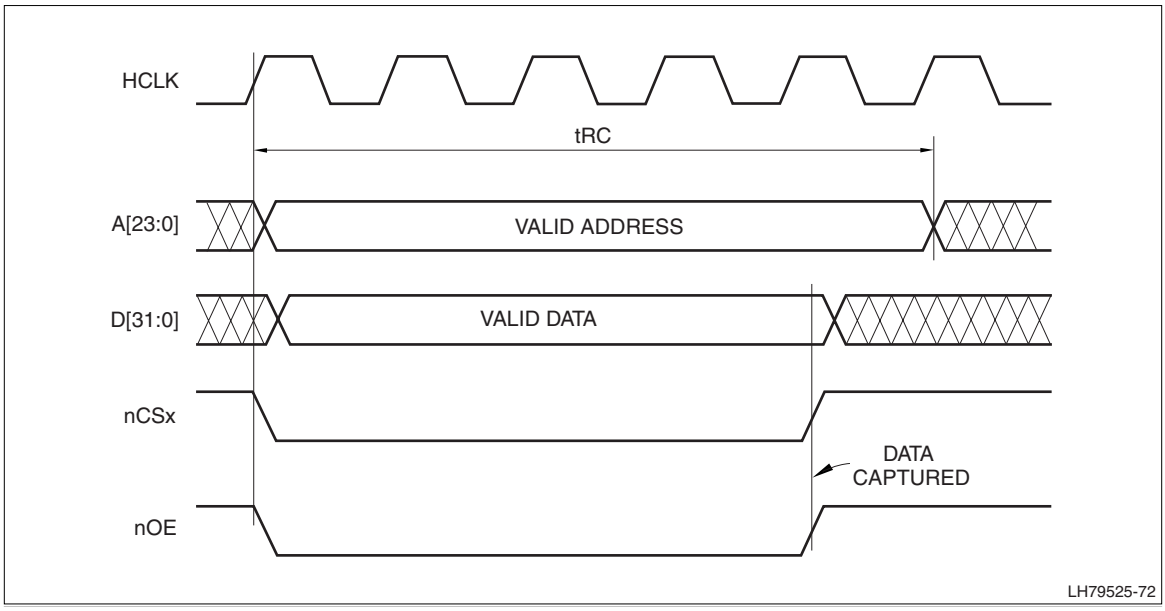


Figure 19. External Static Memory Read with Three Wait States

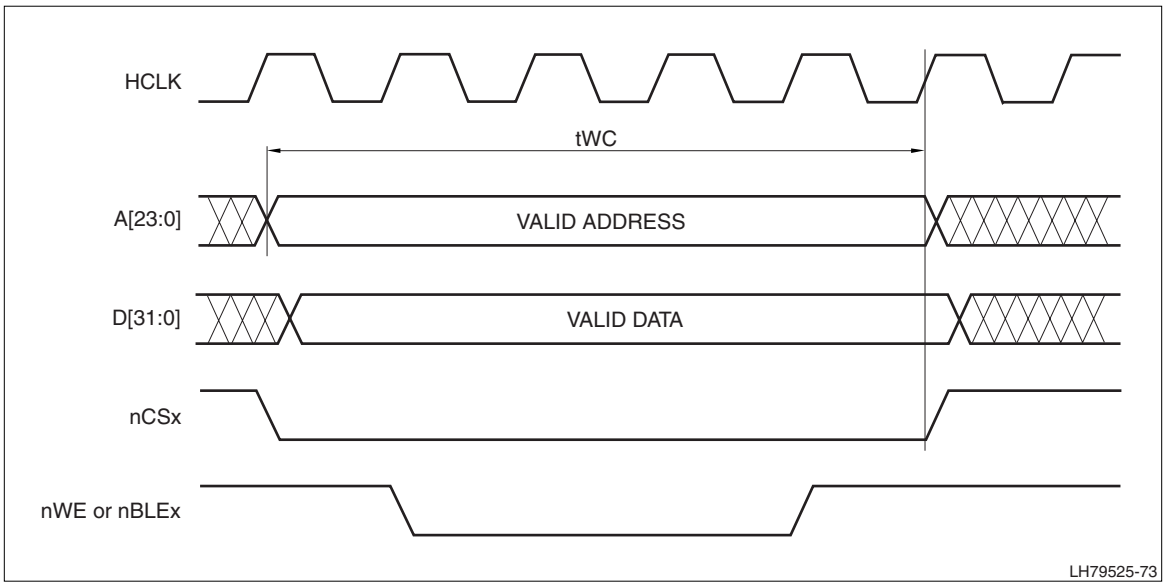
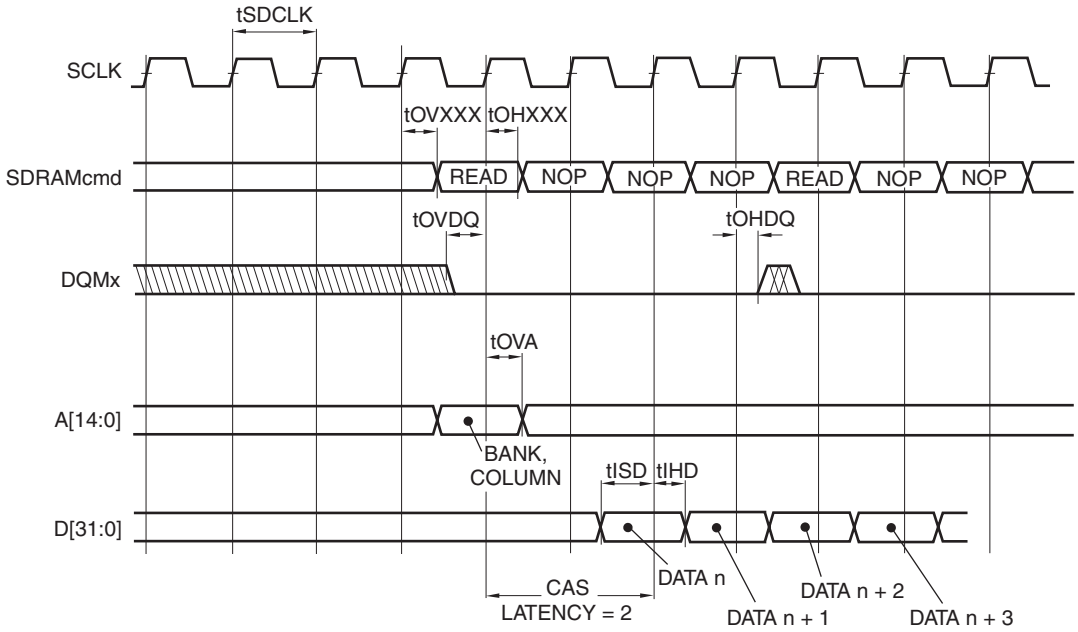


Figure 20. External Static Memory Write with Two Wait States

SDRAM MEMORY CONTROLLER WAVEFORMS

Figure 21 shows the waveform and timing for an SDRAM Burst Read (page already open). Figure 22 shows the waveform and timing for SDRAM to Activate a Bank and Write.



NOTES:
1. SDRAMcmd is the combination of nRAS, nCAS, nSDWE, and nSDCS(X).
2. tOVXXX represents tOVRA, tOVCA, tOVSDW, or tOVSC.
3. tOHXXX represents tOHRA, tOHCA, tOHSDW, or tOHSC.
4. SDCKE is HIGH.

LH79525-3

Figure 21. SDRAM Burst Read

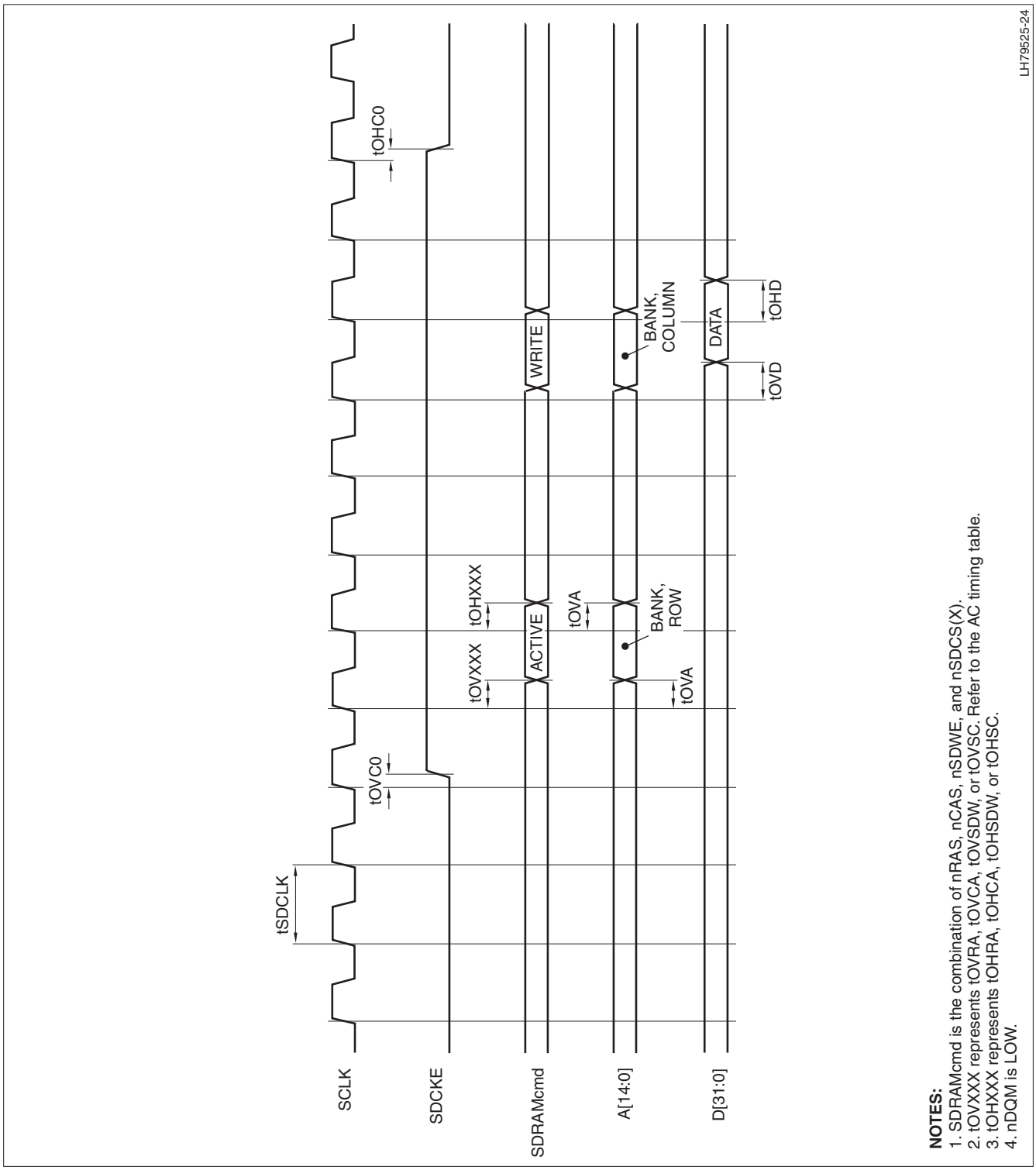


Figure 22. SDRAM Bank Activate and Write

External DMA Handshake Signal Timing

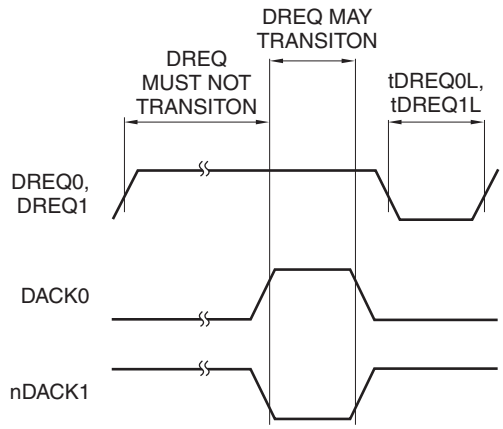
DREQ TIMING

Once asserted, DREQ must not transition from LOW to HIGH again until after nDACK has been asserted.

DACK/DEOT TIMING

These timing diagrams indicate when nDACK and DEOT occur in relation to an external bus access to/from the external peripheral that requested the DMA transfer.

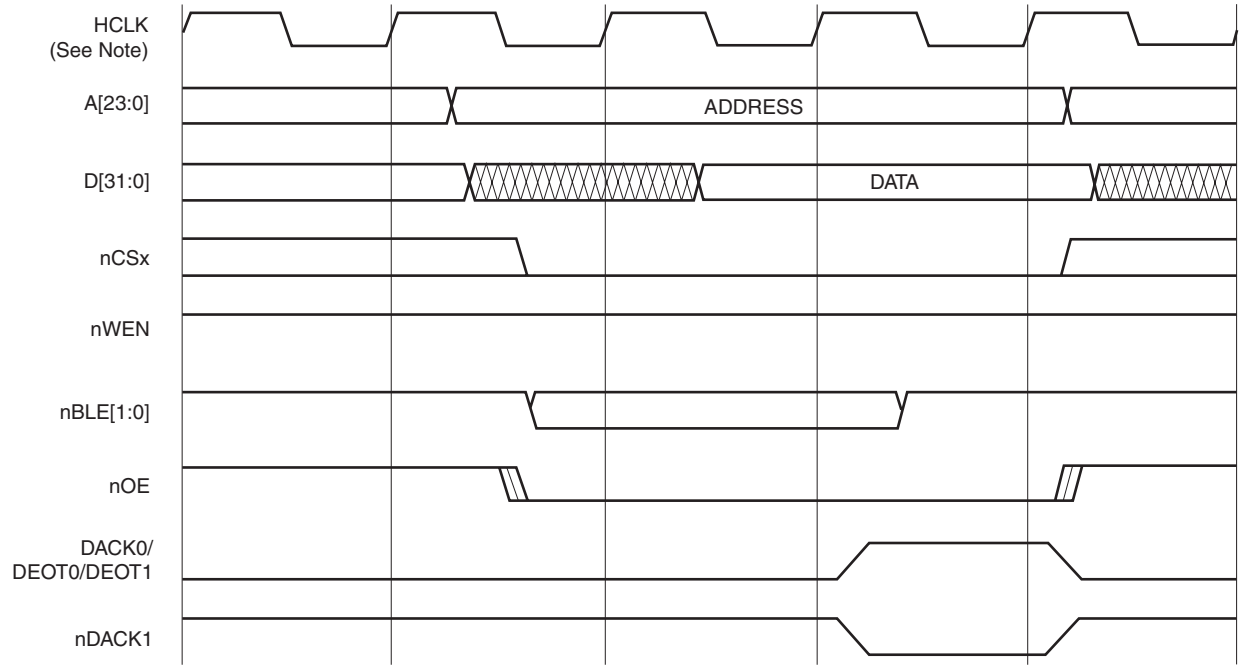
The first diagram shows the timing with relation to a single read or the last word of a burst read from the requesting peripheral. The remaining diagrams show timing for data transfers.



NOTE: tDREQ0L = DREQ0 LOW Pulse Width = 2 HCLK MIN.
tDREQ1L = DREQ1 LOW Pulse Width = 2 HCLK MIN.

LH79525-5

Figure 23. DREQ Timing Restrictions



NOTE: * HCLK is an internal signal provided for reference only.

LH79525-6

Figure 24. Read, from Peripheral to Memory, Burst Size = 1

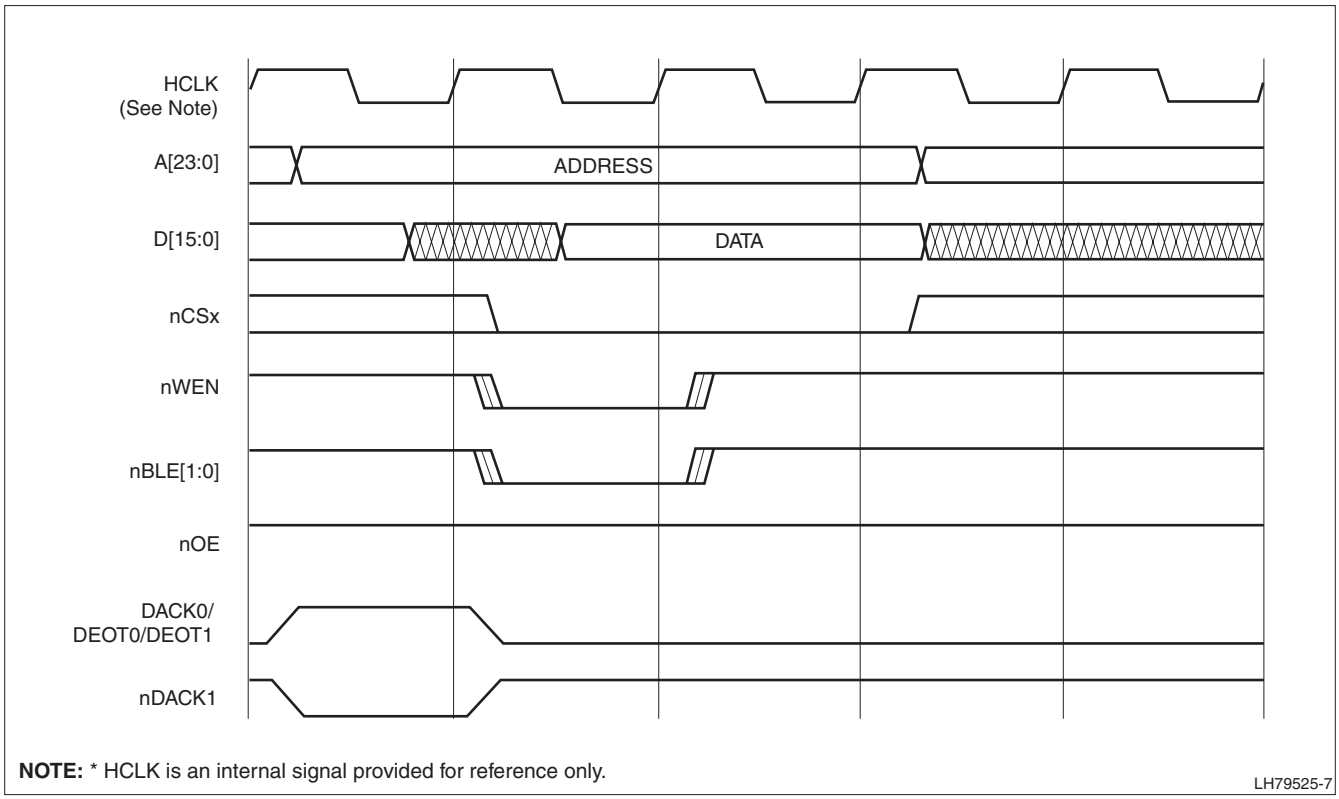


Figure 25. Write, from Memory to Peripheral, Burst Size = 1

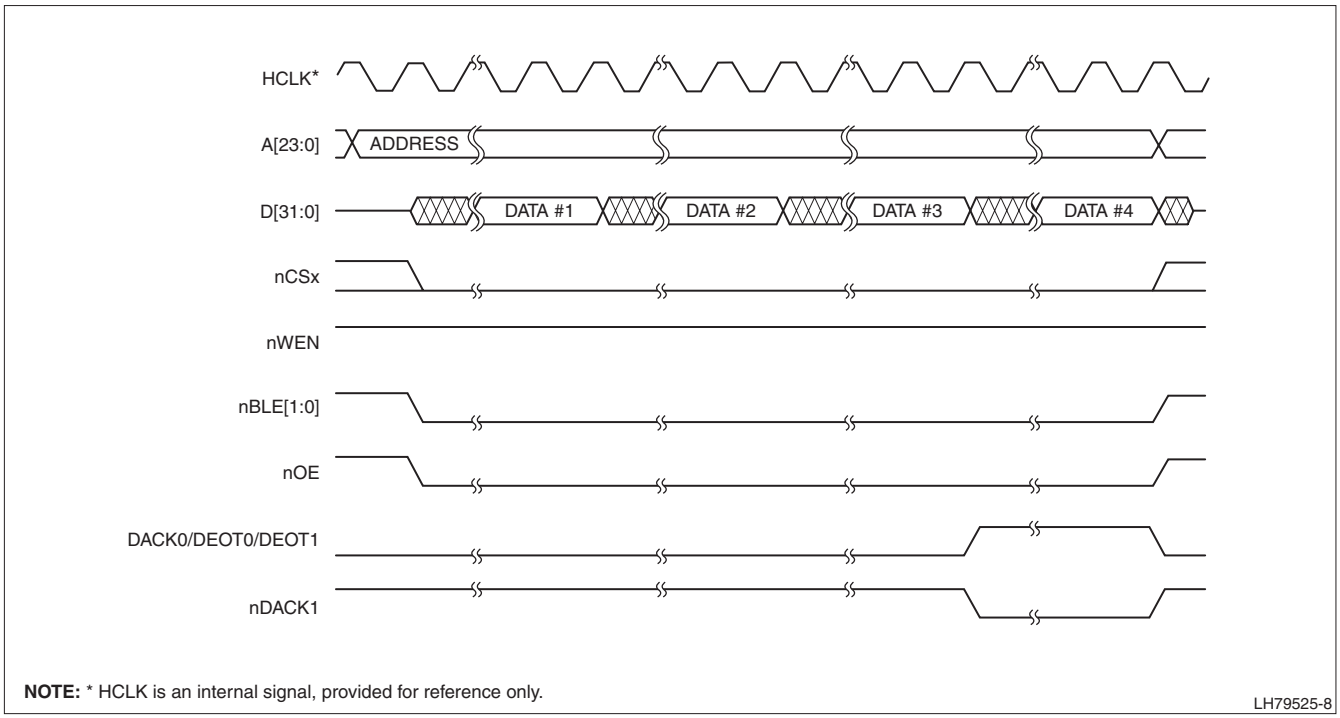


Figure 26. Read, Peripheral to Memory: Peripheral Burst Size = 4

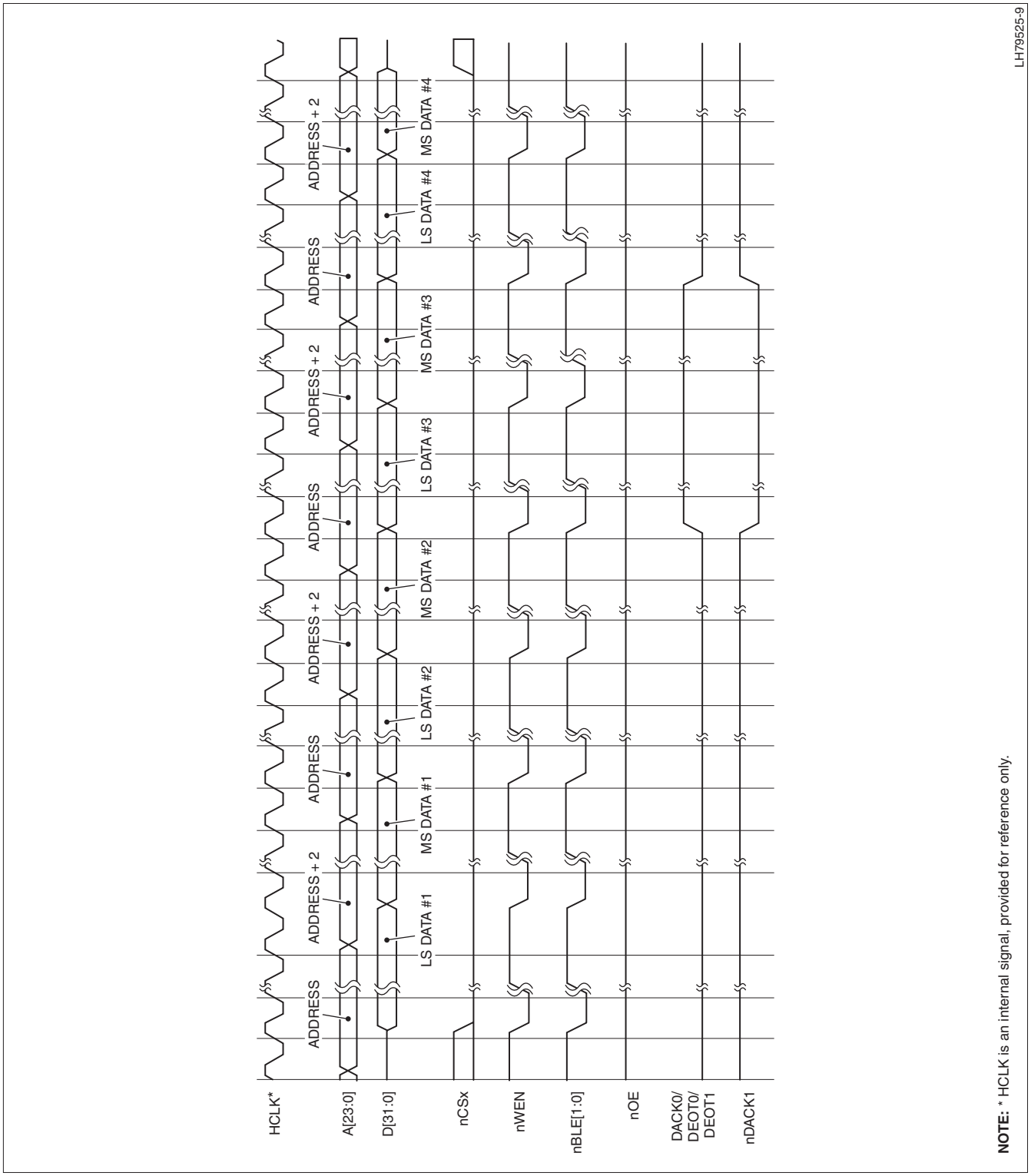


Figure 27. Write, Memory-to-Peripheral: Burst Size = 4; Destination Width > External Access Width

Color LCD Controller Timing Diagrams

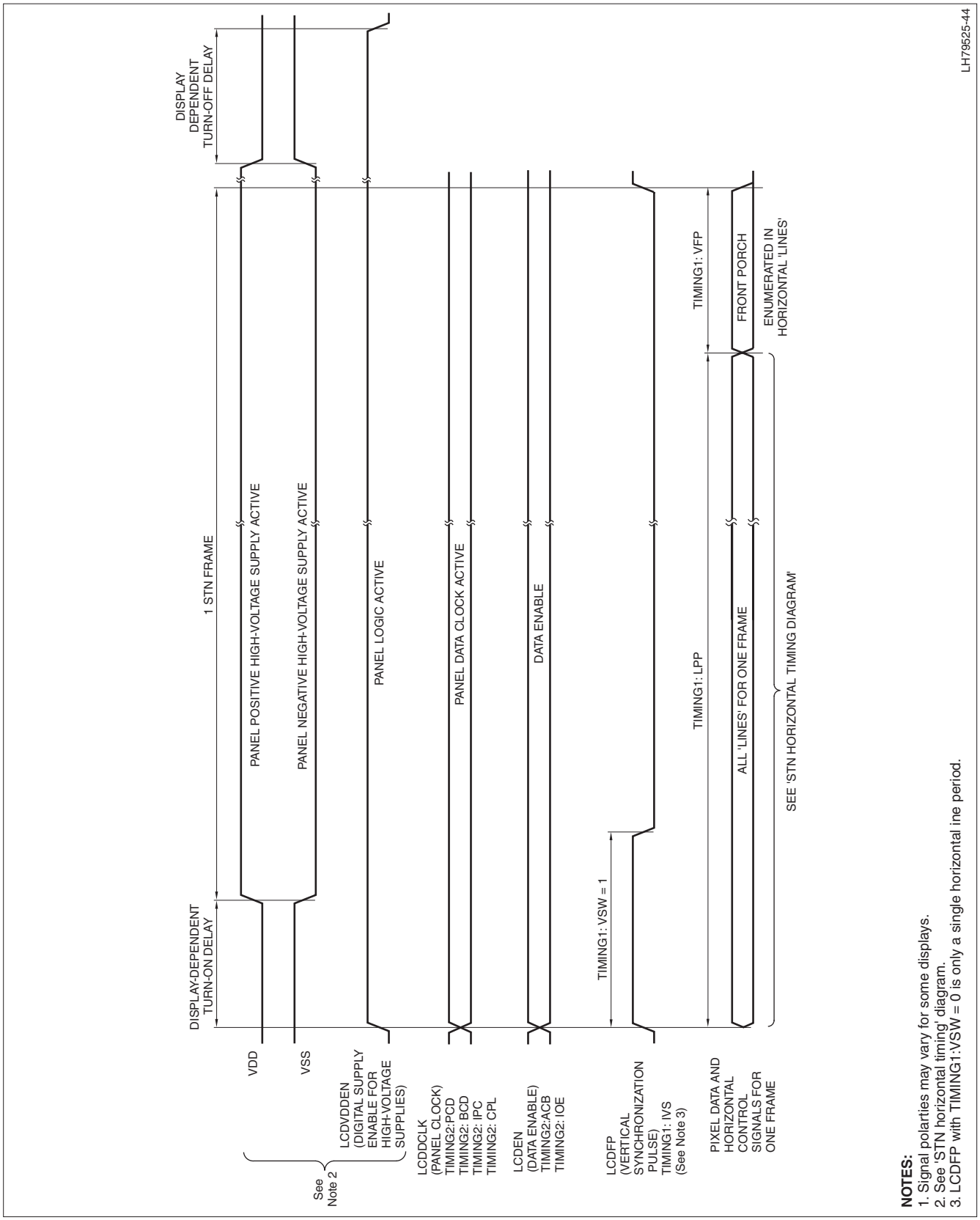


Figure 28. STN Horizontal Timing

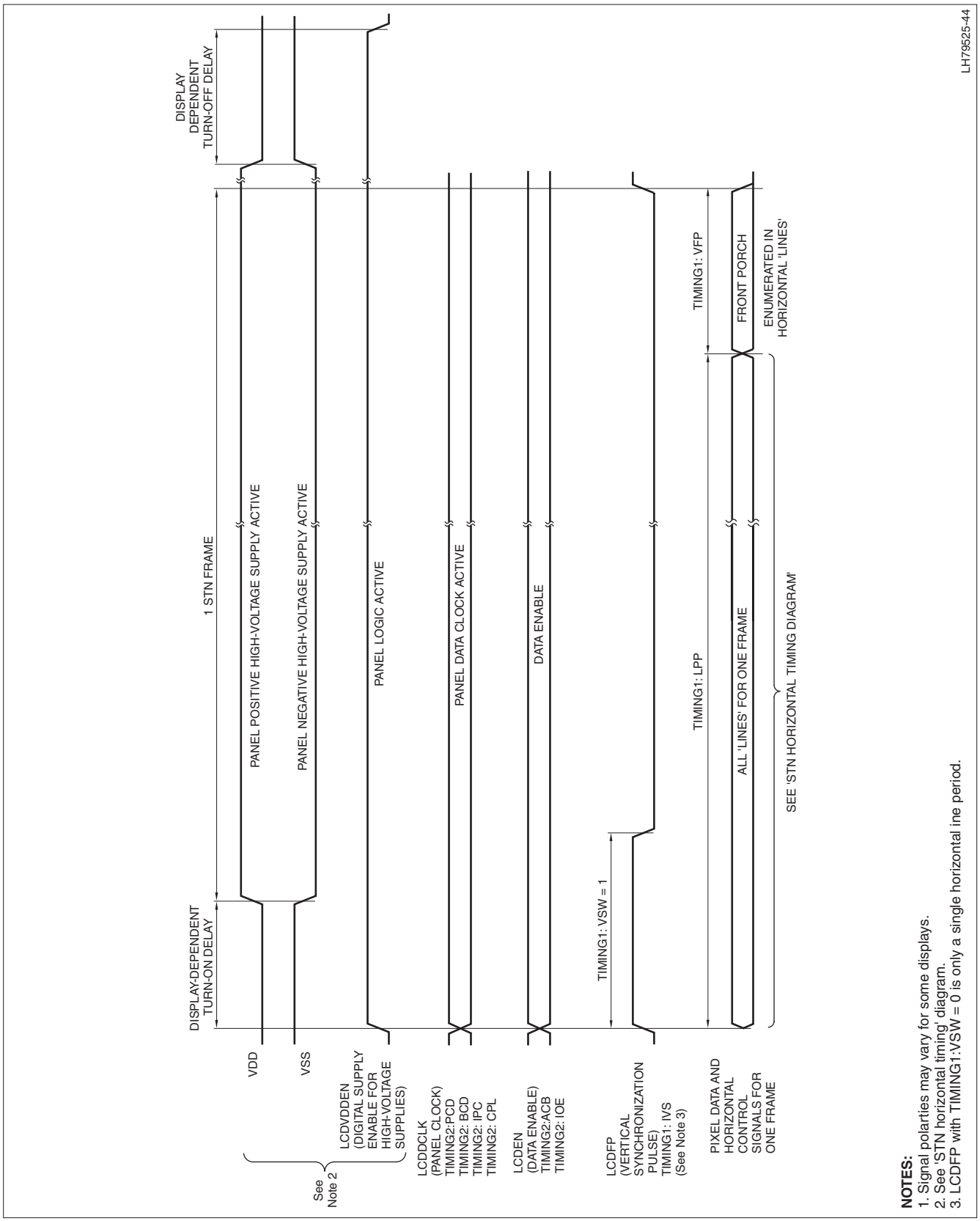


Figure 29. STN Vertical Timing

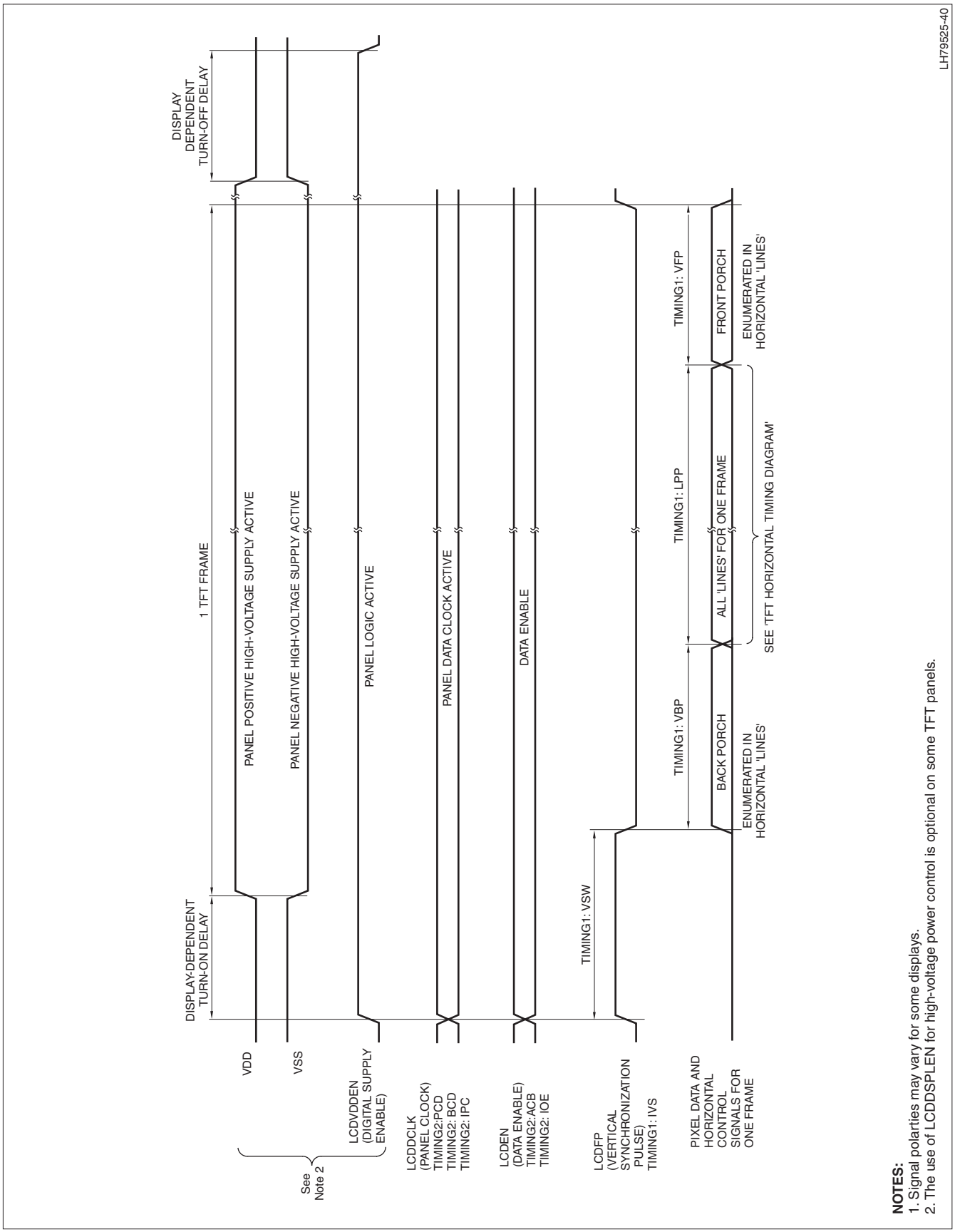


Figure 30. TFT Horizontal Timing

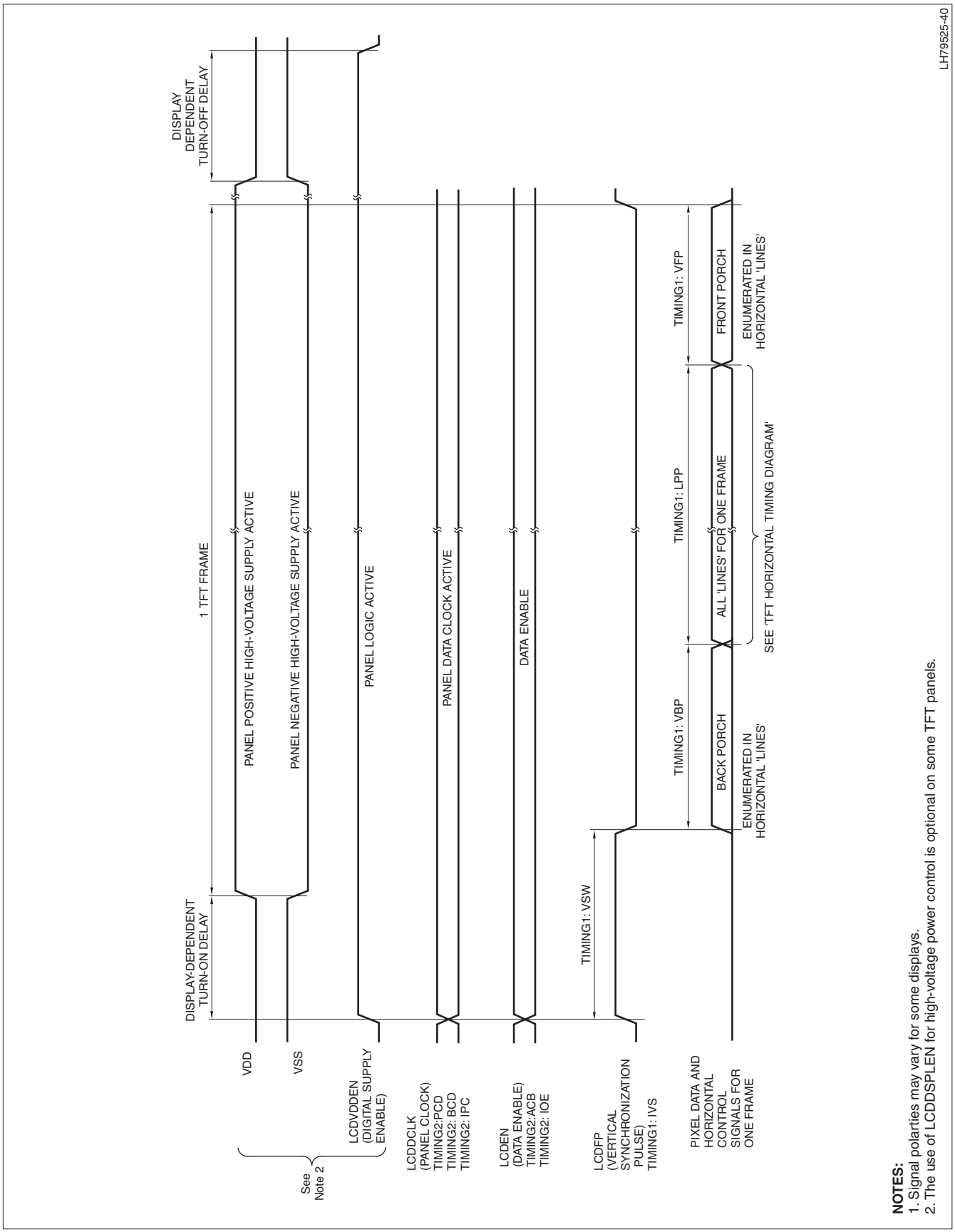


Figure 31. TFT Vertical Timing

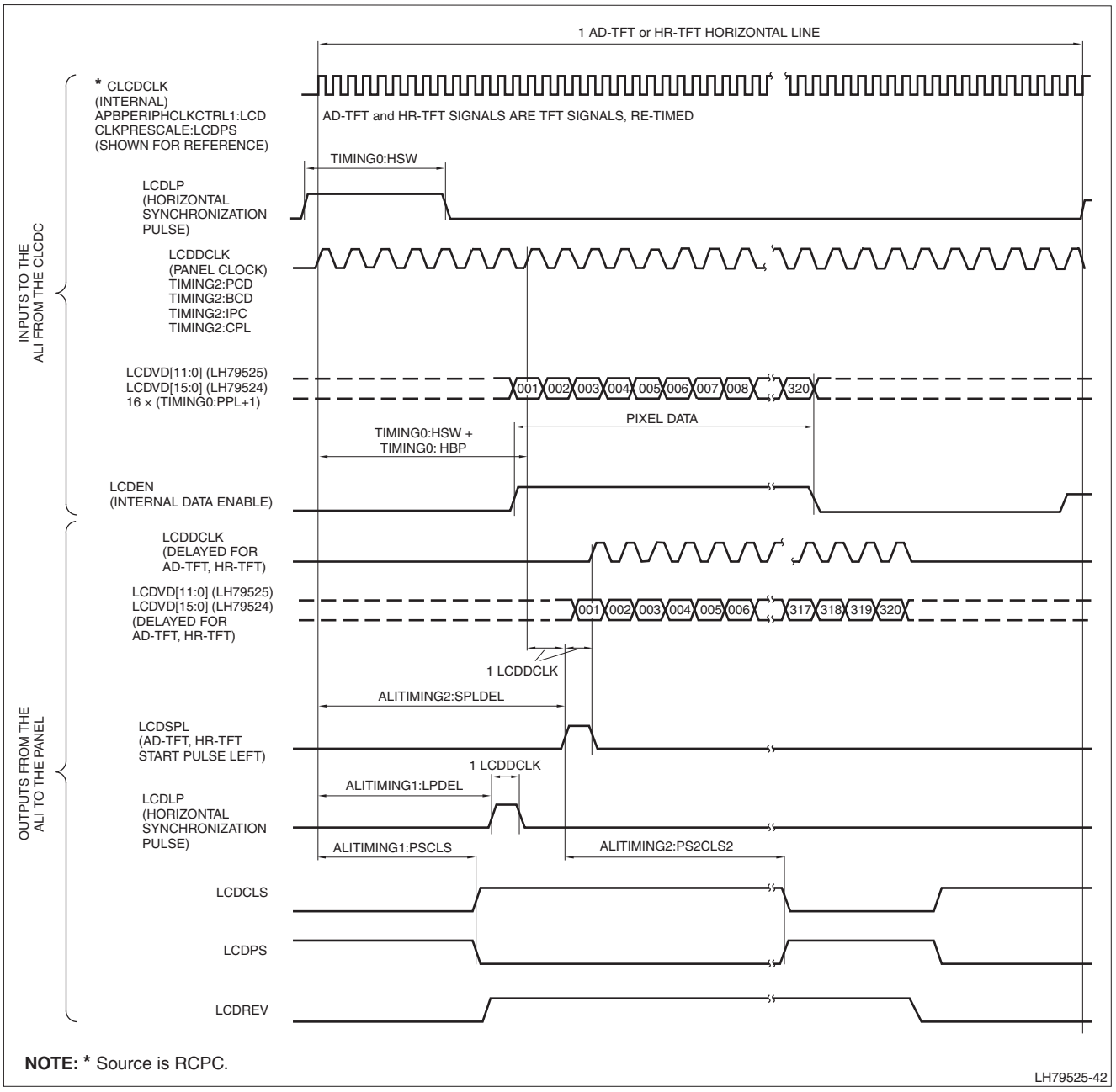


Figure 32. AD-TFT, HR-TFT Horizontal Timing

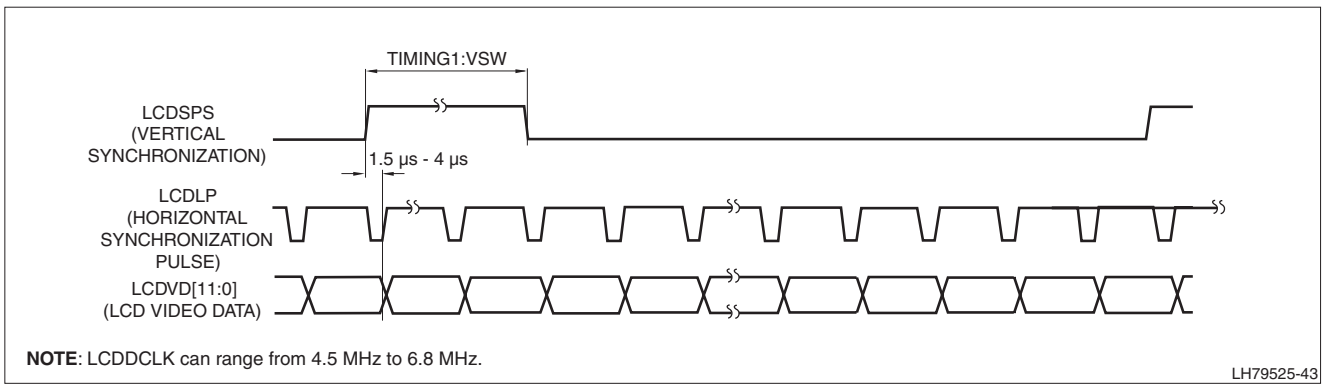


Figure 33. AD-TFT, HR-TFT Vertical Timing

Synchronous Serial Port

The SSP timing is illustrated in Figure 34.

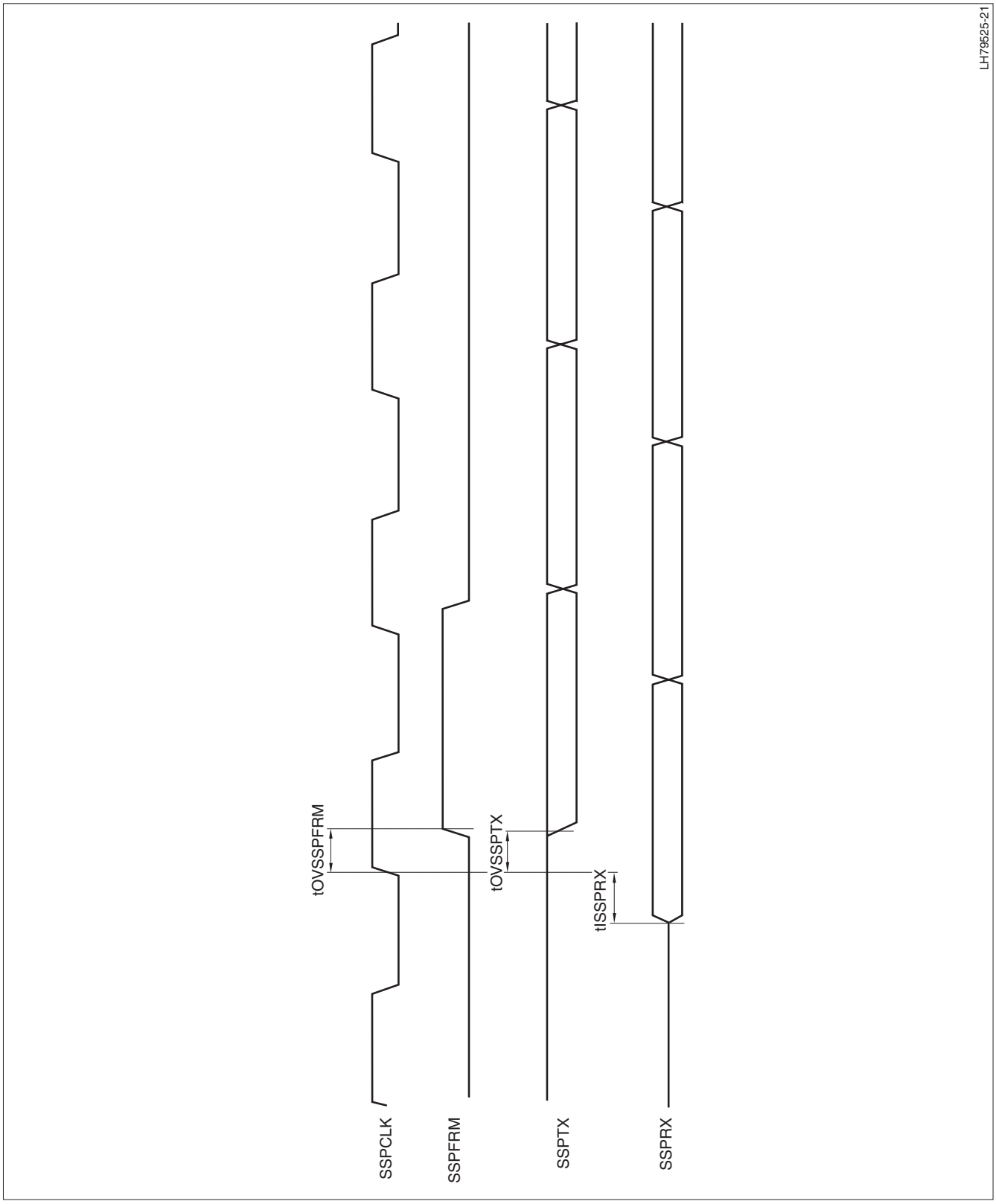


Figure 34. Synchronous Serial Port Waveform

Ethernet MAC Controller Waveforms

The timing for the EMC is presented in the following two illustrations. Figure 35 shows an Ethernet transmit and Figure 36 shows an Ethernet receive.

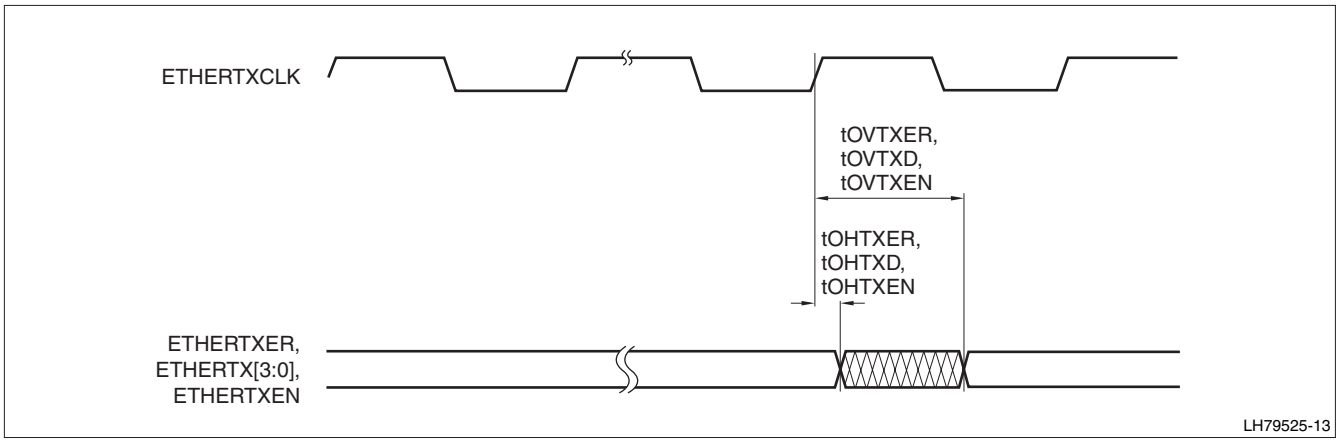


Figure 35. Ethernet Transmit Timing

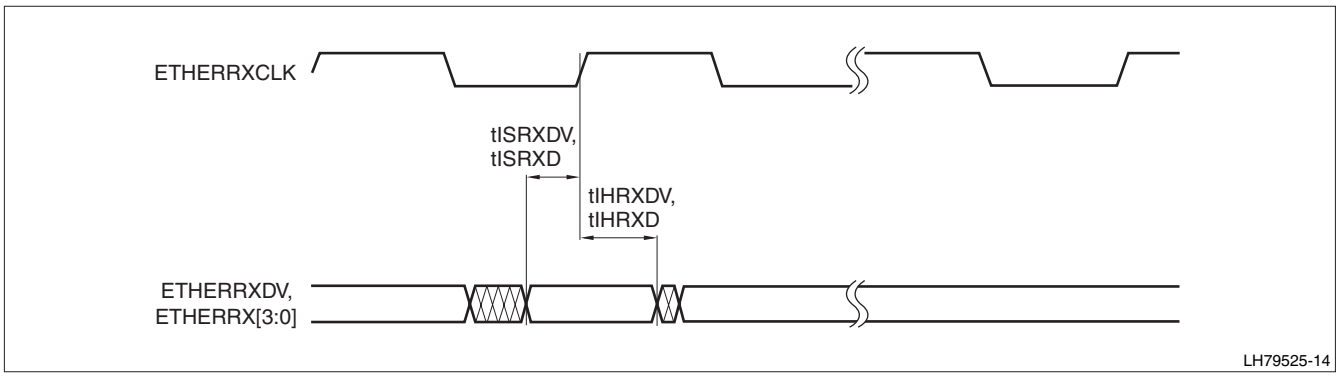


Figure 36. Ethernet Receive Timing

Reset, Clock, and Power Controller (RCPC) Waveforms

Figure 37 shows the method the LH79524/LH79525 uses when coming out of Reset or Power On.

Figure 38 shows external reset timing, and Table 18 gives the timing parameters.

Table 18. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
tOSC32	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)			550	ms
tOSC14	Oscillator stabilization time after Power Up (VDDC = VDDCMIN) or exiting STOP2			2.5	ms
tRSTIH	nRESETIN hold time after crystal stabilization	200			µS
tRSTIW	nRESETIN Pulse Width (once sampled LOW)	2			HCLK
tRSTOV	nRESETIN LOW to nRESETOUT valid (once nRESETIN sampled LOW)		3.5		HCLK
tRSTOH	nRESETOUT hold relative to nRESETIN HIGH		1		HCLK

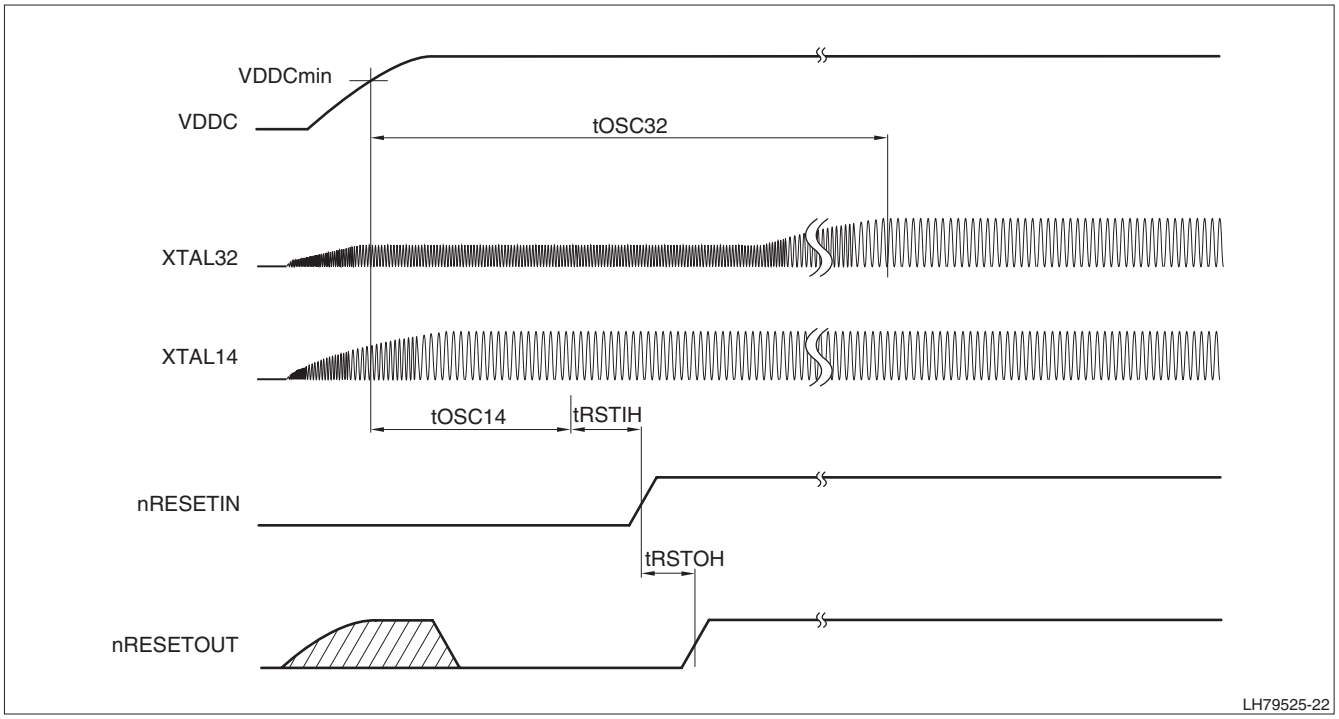


Figure 37. PLL Start-up

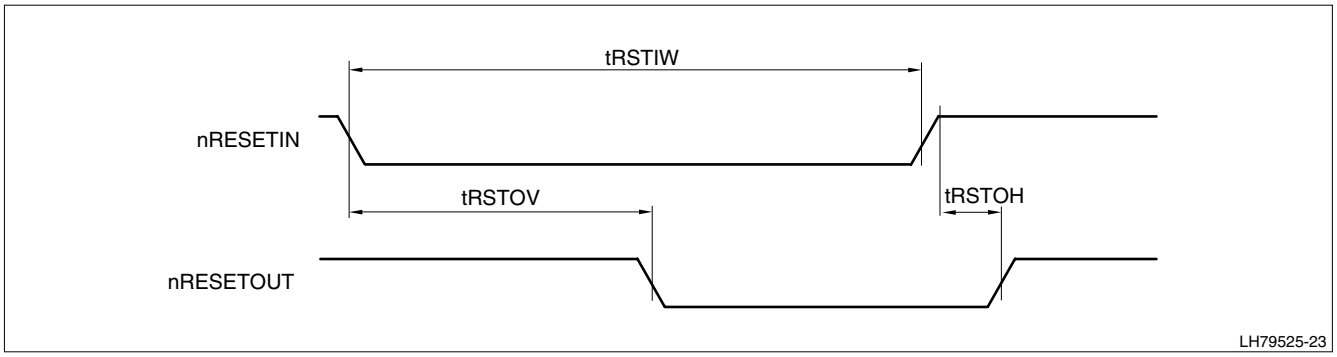


Figure 38. External Reset

UNUSED INPUT SIGNAL CONDITIONING

Floating input signals can cause excessive power consumption. Unused inputs which do not include internal pull-up or pull-down resistors should be pulled up or down externally, to tie the signal to its inactive state.

Some GPIO signals may default to inputs. If the pins which carry these signals are unused, software can program these signals as outputs, to eliminate the need for pull-ups or pull-downs. Power consumption may be higher than expected until such software executes.

Some LH79524/LH79525 inputs have internal pull-ups or pull-downs. If unused, these inputs do not require external conditioning.

OTHER CIRCUIT BOARD LAYOUT PRACTICES

All output pins on the LH79524/LH79525 have fast rise and fall times. Printed circuit trace interconnection length must therefore be reduced to minimize overshoot, undershoot and reflections caused by transmission line effects of these fast output switching times. This recommendation particularly applies to the address and data buses.

When considering capacitance, calculations must consider all device loads and capacitances due to the circuit board traces. Capacitance due to the traces will depend upon a number of factors, including the trace width, dielectric material the circuit board is made from and proximity to ground and power planes.

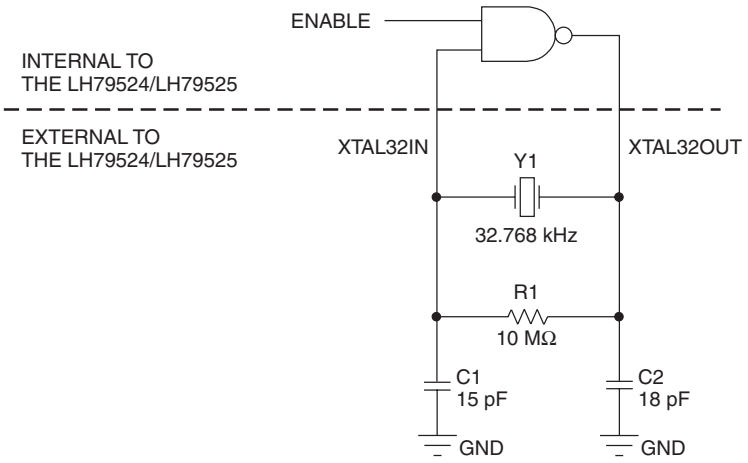
Attention to power supply decoupling and printed circuit board layout becomes more critical in systems with higher capacitive loads. As these capacitive loads increase, transient currents in the power supply and ground return paths also increase.

Add pull-ups to all unused inputs unless an internal pull-down resistor has been specified; see Table 3. Consider all signals that are Inputs at Reset.

SUGGESTED EXTERNAL COMPONENTS

Figure 39 shows the suggested external components for the 32.768 kHz crystal circuit to be used with the NXP LH79524/LH79525. The NAND gate represents the logic inside the SoC. See the table in Figure 39 for crystal specifics.

Figure 40 shows the suggested external components for the 10 - 20 MHz crystal circuit to be used with the NXP LH79524/LH79525. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.



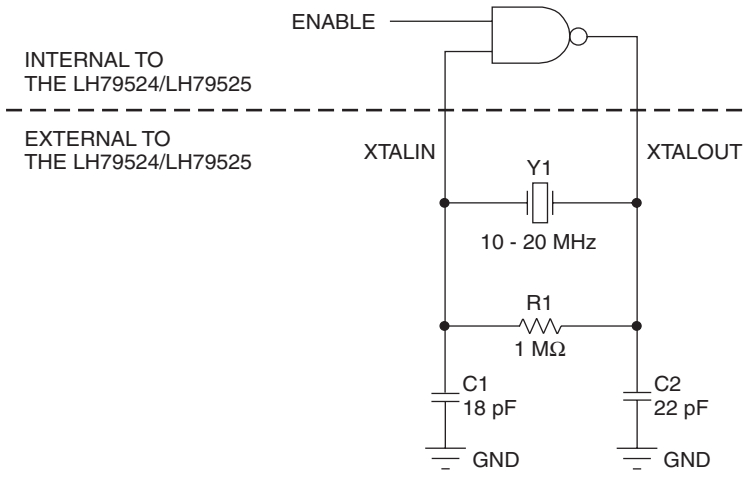
NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 µW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

LH79525-11

Figure 39. Suggested External Components, 32.768 kHz Oscillator (XTAL32IN and XTAL32OUT)



RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
11.2896 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	CITIZEN CM309S - 11.2896 MABJTR or equivalent

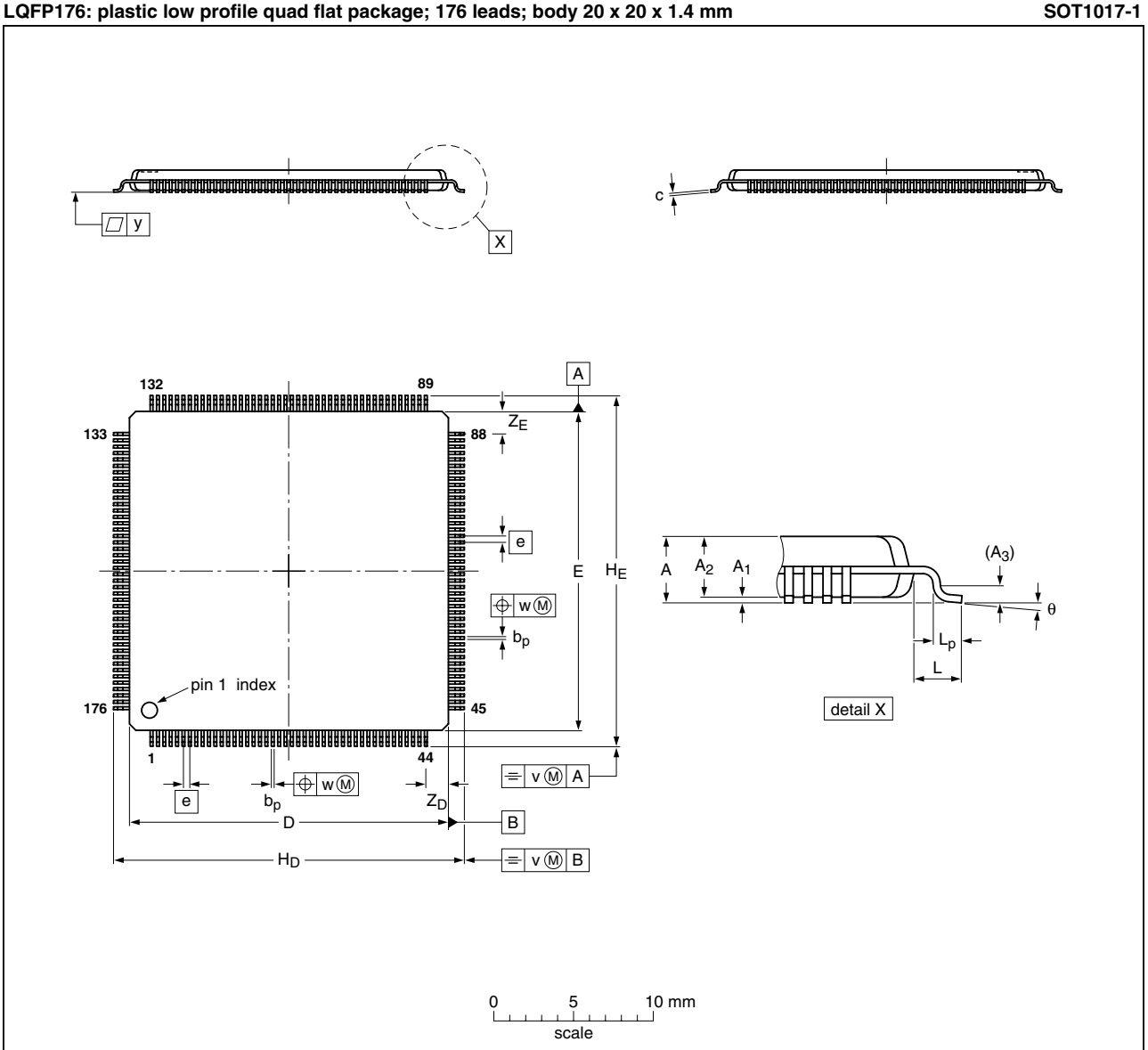
NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

LH79525-12

Figure 40. Suggested External Components, 10 MHz to 20 MHz Oscillator

PACKAGE SPECIFICATIONS

LQFP176: plastic low profile quad flat package; 176 leads; body 20 x 20 x 1.4 mm **SOT1017-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	20.2 19.8	20.2 19.8	0.4	22.2 21.8	22.2 21.8	1	0.75 0.45	0.2	0.07	0.08	1.5 1.3	1.5 1.3	7° 0°

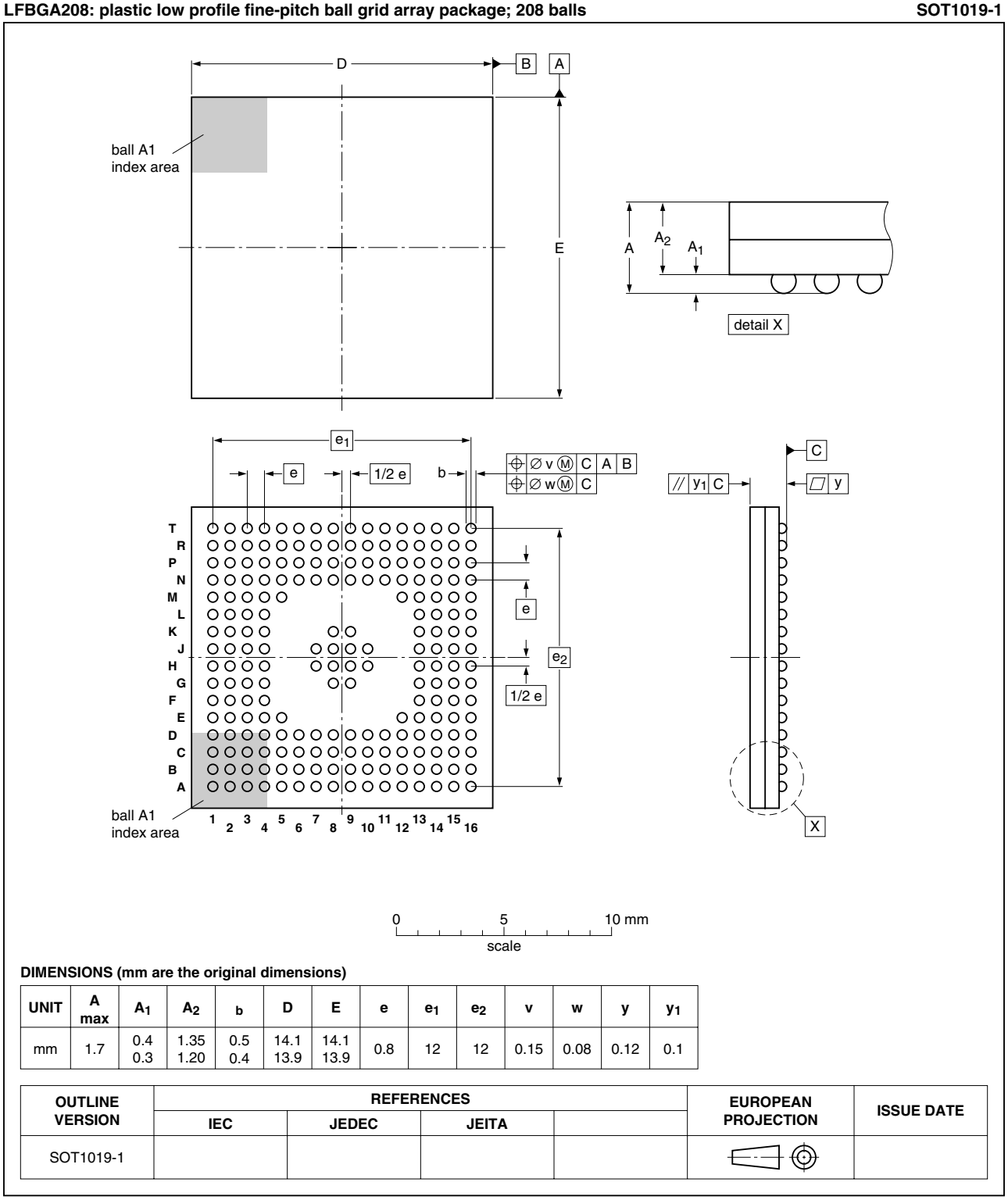
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1017-1						

Figure 41. Package outline SOT1017-1 (LQFP176)

LFBGA208: plastic low profile fine-pitch ball grid array package; 208 balls **SOT1019-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.7	0.4 0.3	1.35 1.20	0.5 0.4	14.1 13.9	14.1 13.9	0.8	12	12	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1019-1						

Figure 42. Package outline SOT1019-1 (LFBGA208)

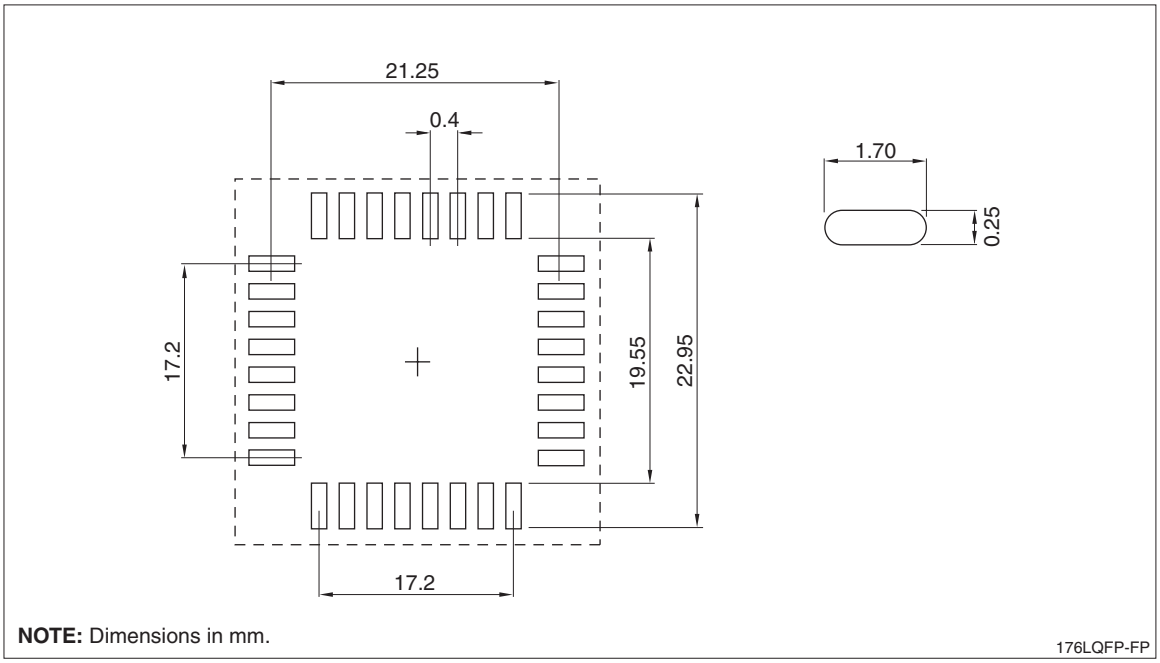


Figure 43. LH79525: LQFP176 PCB Footprint

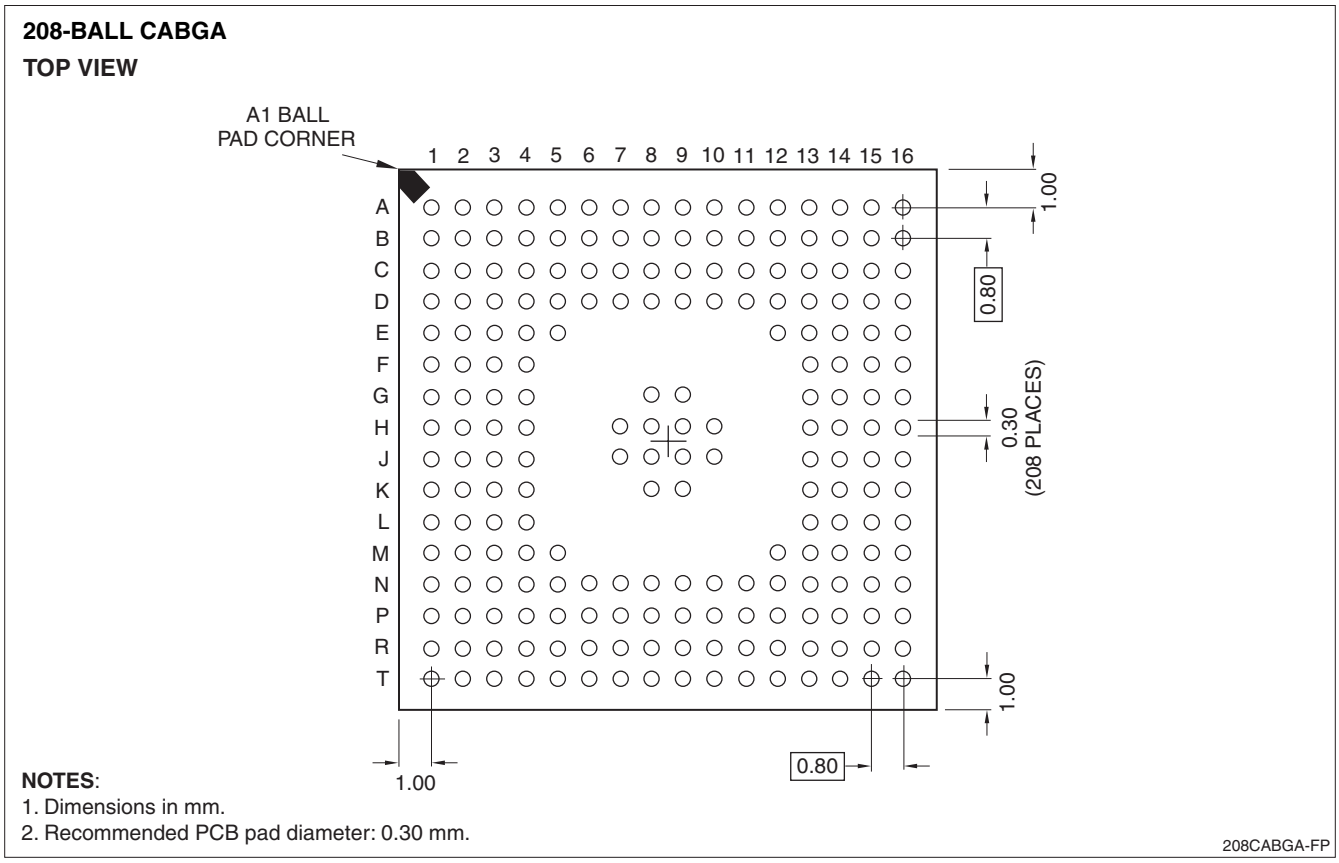


Figure 44. LH79524: LFBGA208 PCB Footprint

REVISION HISTORY

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LH79524_525_N_1	20070716	Preliminary data sheet	-	9-29-06 LH79524-525 Data Sheet REV A1
Modifications: • First NXP version based on the LH79524/LH79525 data sheet of 20060929				

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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