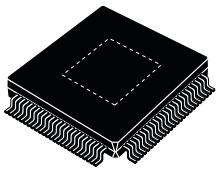
L9788

Multifunction IC for automotive engine management system

Datasheet - production data



LQFP100 14 x 14 x 1.4 mm
(exposed pad down)

GADG2411160920PS

Features

- AEC-Q100 qualified
- Engineered for ISO26262 compliant system
- 1 pre-boost regulator and 1 pre-buck regulator
- 1 linear 5 V regulator with 1 A output current
- 3 independent self-protection 5 V tracking regulator with 150 mA output.
- 1 input voltage pin for monitor external tracking.
- Coordinated soft start-up of all regulators
- 4 channels LS injector LS drivers
- 2 channels LS drivers for O2H load with current sense
- 2 channels LS camshaft or solenoid drivers
- 5 channels LS relay drivers
- 2 channels LS LED drivers
- 3 channels LS/HS drivers with low battery function for smart start
- 1 channel LS main relay driver (MRD) with internal diode for reverse battery protection
- 5 channels pre-drivers for external FET drivers. Pre-driver 1&3 configurable for O2H load with external Rshunt-on the source of Ext. N-channel MOS
- 6 channels pre-drivers for internal or external igniter drivers
- 1 K-Line ISO9141/LIN 2.1 compliant
- Integrated charge-pump
- VRS-interface
- Watchdog
- Wake-up pin
- Temperature sensor and monitoring
- Stop-counter with wakeup
- Dual bandgap reference & oscillator
- Micro-second-channel MSC for differential single ended mode
- SEO function
- CAN-FD with wakeup by CAN function
- Package LQFP100 exposed pad

Description

The L9788 is an integrated circuit designed for automotive engine management system.

L9788 is a device realized in ST BCD proprietary technology, able to provide the full set of power supplies and signal preprocessing peripherals needed to control a 4-cylinders internal combustion engine.

Table 1. Device summary

Order code	Package	Packing
L9788	LQFP100 14x14x1.4 mm (Exposed pad down 7.6x7.6 mm)	Tube
L9788TR		Tape & Reel

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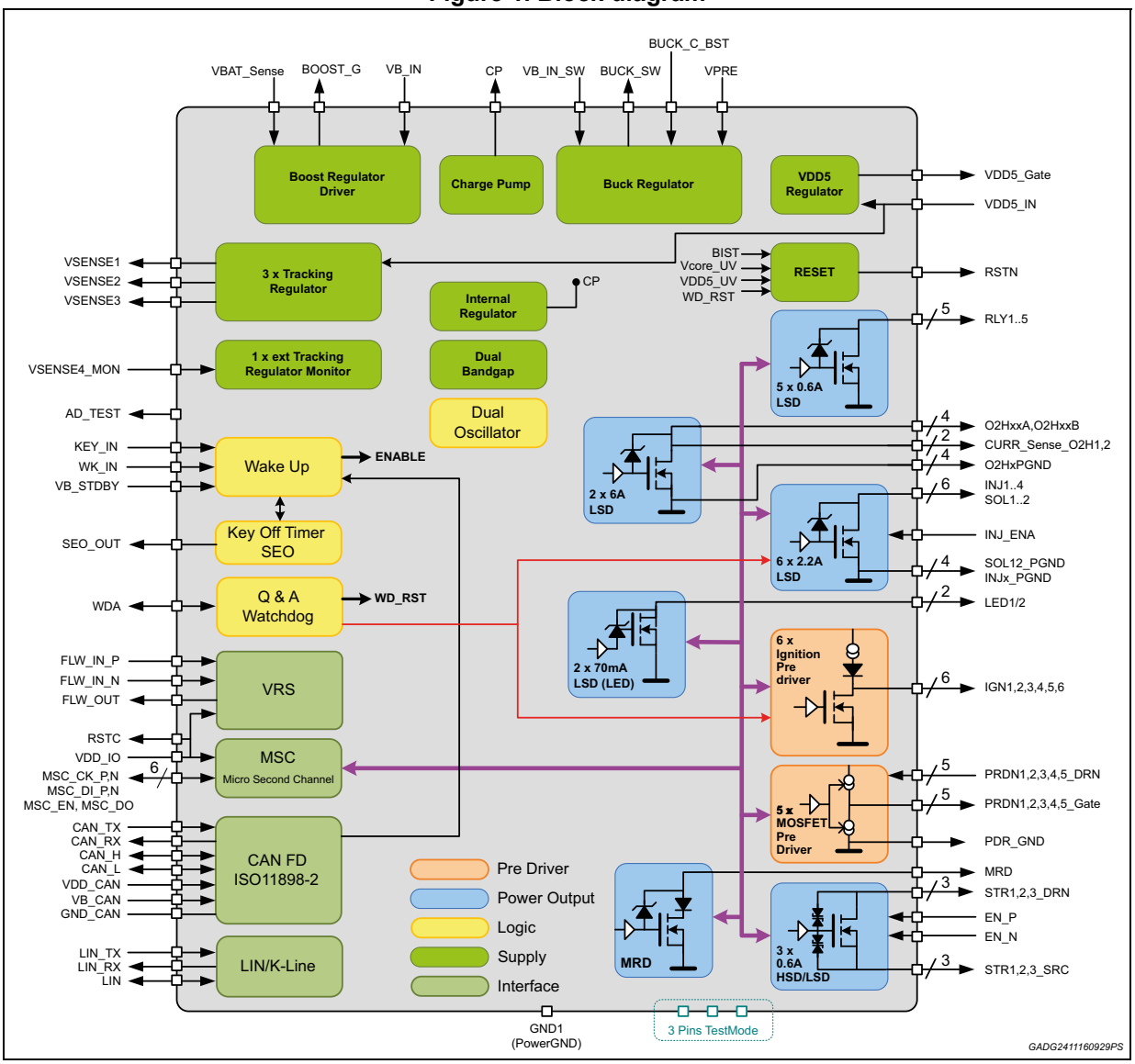
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection diagram (top view)

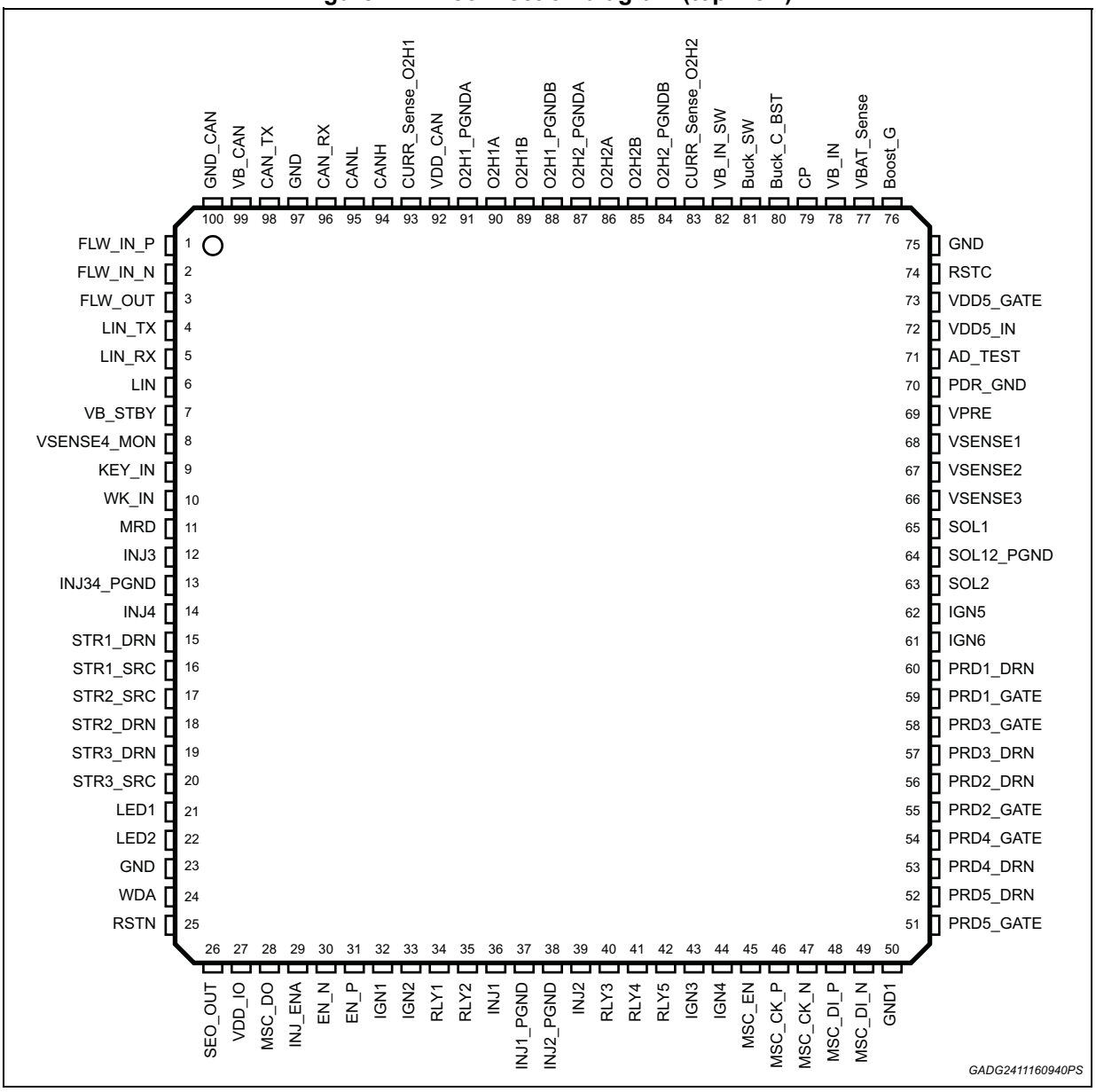


Table 2. Pin function

Pin #	Name	Function	Type	Note
1	FLW_IN_P	Flying wheel inputs voltage positive	Power In	-
2	FLW_IN_N	Flying wheel inputs voltage negative	Power In	-
3	FLW_OUT	Flying wheel output voltage	Digital Out	-
4	LIN_TX	LIN data input	Digital In	-
5	LIN_RX	LIN data output	Digital Out	-

Table 2. Pin function (continued)

Pin #	Name	Function	Type	Note
6	LIN	LIN driver output	Power In/Out	-
7	VB_STBY	Standby function supply voltage	Supply	-
8	VSENSE4_MON	tracking sensor supply Monitor	Analog In	-
9	KEY_IN	Key signal input	Power In	-
10	WK_IN	wake up signal input	Power In	-
11	MRD	Main relay drivers outpour voltage	Power Out	-
12	INJ3	Injector Driver output voltage	Power Out	-
13	INJ34_PGND	Ground	GND	-
14	INJ4	Injector Driver output voltage	Power Out	-
15	STR1_DRN	Configurable high/low-side drain voltage	Power Out	-
16	STR1_SRC	Configurable high/low-side source voltage	Power Out	-
17	STR2_SRC	Configurable high/low-side source voltage	Power Out	-
18	STR2_DRN	Configurable high/low-side drain voltage	Power Out	-
19	STR3_DRN	Configurable high/low-side drain voltage	Power Out	-
20	STR3_SRC	Configurable high/low-side source voltage	Power Out	-
21	LED1	LED Driver output voltage	Power Out	-
22	LED2	LED Driver output voltage	Power Out	-
23	GND	Ground	GND	-
24	WDA	Watchdog output	Digital In/Out	-
25	RSTN	Reset output for VDD5	Digital Out	-
26	SEO_OUT	SEO output pin	Digital Out	-
27	VDD_IO	Dedicated supply for FLW_OUT, MSC_DO,LIN_RX, CAN_RX	Supply	-
28	MSC_DO	MSC digital I/O voltage	Digital Out	-
29	INJ_ENA	Enable pin for injector driver	Digital In	-
30	EN_N	enable signals	Digital In	-
31	EN_P	enable signals	Digital In	-
32	IGN1	Ignition pre-driver output voltage	Power Out	-
33	IGN2	Ignition pre-driver output voltage	Power Out	-
34	RLY1	Relay Driver output voltage	Power Out	-
35	RLY2	Relay Driver output voltage	Power Out	-
36	INJ1	Injector Driver output voltage	Power Out	-
37	INJ1_PGND	Ground	GND	-
38	INJ2_PGND	Ground	GND	-
39	INJ2	Injector Driver output voltage	Power Out	-

Table 2. Pin function (continued)

Pin #	Name	Function	Type	Note
40	RLY3	Relay Driver output voltage	Power Out	-
41	RLY4	Relay Driver output voltage	Power Out	-
42	RLY5	Relay Driver output voltage	Power Out	-
43	IGN3	Ignition pre-driver output voltage	Power Out	-
44	IGN4	Ignition pre-driver output voltage	Power Out	-
45	MSC_EN	MSC digital I/O voltage	Digital In	-
46	MSC_CK_P	MSC digital I/O voltage	Digital In	-
47	MSC_CK_N	MSC digital I/O voltage	Digital In	-
48	MSC_DI_P	MSC digital I/O voltage	Digital In	-
49	MSC_DI_N	MSC digital I/O voltage	Digital In	-
50	GND1	Power ground	GND	Shorted to GND by package
51	PRD5_GATE	General purpose pre-drivers gate voltage	Power Out	-
52	PRD5_DRN	General purpose pre-drivers feedback voltage	Power In	-
53	PRD4_DRN	General purpose pre-drivers feedback voltage	Power In	-
54	PRD4_GATE	General purpose pre-drivers gate voltage	Power Out	-
55	PRD2_GATE	General purpose pre-drivers gate voltage	Power Out	-
56	PRD2_DRN	General purpose pre-drivers feedback voltage	Power In	-
57	PRD3_DRN	General purpose pre-drivers feedback voltage	Power In	-
58	PRD3_GATE	General purpose pre-drivers gate voltage	Power Out	-
59	PRD1_GATE	General purpose pre-drivers gate voltage	Power Out	-
60	PRD1_DRN	General purpose pre-drivers feedback voltage	Power In	-
61	IGN6	Ignition pre-driver output voltage	Power Out	-
62	IGN5	Ignition pre-driver output voltage	Power Out	-
63	SOL2	Valve driver output voltage	Power Out	-
64	SOL12_PGND	Ground	GND	-
65	SOL1	Valve driver output voltage	Power Out	-
66	VSENSE3	5V tracking sensor supply output voltage	Power Out	-
67	VSENSE2	5V tracking sensor supply output voltage	Supply Out	-
68	VSENSE1	5V tracking sensor supply output voltage	Supply Out	-
69	VPRE	Buck output voltage	Supply Out	-
70	PDR_GND	Ground pin for predriver supply feedback input	GND	-
71	AD_TEST	AD test pin	Analog Out	-
72	VDD5_IN	5V regulator feedback voltage	Power In	-
73	VDD5_GATE	5V linear regulator pre-driver output	Power Out	-

Table 2. Pin function (continued)

Pin #	Name	Function	Type	Note
74	RST_{case}	Reset output for VDDIO supply	Digital Out	-
75	GND	Ground	GND	-
76	Boost_G	Boost LS gate voltage	Power Out	-
77	VBAT_Sense	Battery supply voltage	Supply In	-
78	VB_IN	Battery supply voltage	Supply In	-
79	CP	Charge pump	Power Out	-
80	Buck_C_BST	Bootstrap capacitor pin	Power Out	-
81	Buck_SW	Buck switching pin	Power Out	-
82	VB_IN_SW	BUCK supply voltage	Power In	-
83	CURR_Sense_O2H2	O2heater drivers output current value	Analog Out	-
84	O2H2_PGNDB	Ground	GND	-
85	O2H2B	O2H2B Driver output voltage	Power Out	-
86	O2H2A	O2H2A Driver output voltage	Power Out	-
87	O2H2_PGNDA	Ground	GND	-
88	O2H1_PGNDB	Ground	GND	-
89	O2H1B	O2H1BDriver output voltage	Power Out	-
90	O2H1A	O2H1A Driver output voltage	Power Out	-
91	O2H1_PGNDA	Ground	GND	-
92	VDD_CAN	CAN Supply 5 V	Supply In	-
93	CURR_Sense_O2H1	O2heater drivers output current value	Analog Out	-
94	CANH	CANH output	Power In/Out	-
95	CANL	CANL output	Power In/Out	-
96	CAN_RX	CAN RX data output	Digital In/Out	-
97	GND	Ground	GND	-
98	CAN_TX	CAN TX data input	Digital In	-
99	VB_CAN	CAN enable signal	Supply In	-
100	GND_CAN	Ground CAN	GND	-

2 Absolute maximum ratings

The component withstands all the following stimuli without any damage or latch-up. Exceeding any of these values or sustaining it for extended periods may lead to characteristics degradation or component damage.

All voltages are related to analog ground

T_j -40 to 175 °C unless otherwise specified.

Table 3. Absolute maximum ratings

Pin name	Parameter	Referred to	Constr.	Min	Max	Unit	Pin(1) Direction
VB_IN	Chip supply voltage	GND1	-	-0.3	+40	V	S
			10 ms (ISOpulse1) VB_IN pin shorted with VB_IN_SW	-2	-	V	S
VB_IN_SW	Buck supply voltage	GND1	-	-0.3	+40	V	S
			10 ms (ISOpulse1)	-2	-	V	S
VBAT_Sense	Battery supply voltage sense	GND1	-	-0.3	+40	V	S
VBAT_Sense	Input current	GND1	Protect from Reverse battery with 1k Ω resistor	-16	-	mA	S
VBAT_Sense	Input current	GND1	Protect from ISOPULSE 1 with 1 kΩ resistor	-150	-	mA	S
VB_STBY	Standby function supply voltage for EOT	GND1	-	-16	+40	V	S
Boost_G	Boost LS gate voltage	GND1	-	-0.3	+20	V	O
VPRE	Buck output voltage	GND1	-	-0.3	+20	V	S
Buck_SW	Buck switching pin	GND1	-	-0.3(2)	+40	V	S
Buck_C_BST	Bootstrap capacitor pin	GND1	-	-0.3	+45	V	I
VDD5_GATE	5 V linear regulator pre-driver output	GND1	-	-0.3	+20	V	O
VDD5_IN	5 V regulator feedback voltage	GND1	-	-0.3	+20	V	S

Table 3. Absolute maximum ratings (continued)

Pin name	Parameter	Referred to	Constr.	Min	Max	Unit	Pin(1) Direction
VDD_IO	Dedicated 5 V voltage for FLW_OUT, MSC_DO, TxDC, RxDC	GND1	-	-0.3	+20	V	S
VSENSE1, VSENSE2, VSENSE3	5 V tracking sensor supply output voltage	GND1	-	-2	+40	V	S
VSENSE4_MON	External tracking sensor supply Monitor	GND1	-	-2	+40	V	I
CP	Charge pump	GND1	-	-0.3	VB_IN+ 5V	V	S
GND1	Power ground	-	-	-0.3	+0.3	V	O
GND_CAN	Power ground	GND1	-	-0.3	+0.3	V	O
WDA	Digital output (open drain) / Digital input	GND1	-	-0.3	+20	V	I/O
SEO_OUT	Digital output	GND1	-	-0.3	+20	V	O
RSTN, RSTC	Digital output / open drain	GND1	-	-0.3	+20	V	I/O
AD_TEST	Digital output voltage	GND1	-	-0.3	+20	V	O
INJ_ENA,	Digital input / Digital output	GND1	-	-0.3	+20	V	I/O
KEY_IN, WK_IN	Input voltage	GND1	-	-0.3	+40	V	I
KEY_IN, WK_IN	Input current	GND1	Protect from Reverse battery with 1 kΩ resistor	-16	-	mA	I
KEY_IN, WK_IN	Input current	GND1	Protect from ISOPULSE 1 with 1 kΩ resistor	-150	-	mA	I
MSC_EN, MSC_CK_P, MSC_CK_N, MSC_DI_P, MSC_DI_N, MSC_DO	MSC digital I/O voltage	GND1	-	-0.3	+20	V	I/O
FLW_IN_P, FLW_IN_N	Flying wheel inputs voltage	GND1	With 20 mA (Max) inputs current	-0.3	Vclamp	V	I
FLW_IN_P, FLW_IN_N	Flying wheel inputs current	-	-	-20	+20	mA	I

Table 3. Absolute maximum ratings (continued)

Pin name	Parameter	Referred to	Constr.	Min	Max	Unit	Pin(1) Direction
FLW_OUT	Flying wheel output voltage (open drain)	GND1	-	-0.3	+20	V	O
MRD	Main relay drivers outpour voltage	GND1	-	-16	Vclamp	V	O
INJ1 INJ2 INJ3 INJ4 O2H1A O2H1B O2H2A O2H2B SOL1 SOL2 RLY1 RLY2 RLY3 RLY4 RLY5 LED1 LED2	Low-side drivers output voltage	GND1	-	-1	Vclamp	V	O
STR1_DRN STR2_DRN STR3_DRN	Configurable high/low-side drain voltage	GND1	-	-1	Vclamp	V	O
STR1_SRC STR2_SRC STR3_SRC	Configurable high/low-side source voltage	GND1	-	Vclamp*	+40	V	O
IGN1 IGN2 IGN3 IGN4 IGN5 IGN6	Ignition pre-driver output voltage	GND1	Negative voltage with limited current at 20 mA, protected by external resistor	-1	+40	V	O
CURR_Sense_O2H1 CURR_Sense_O2H2	O2heater drivers output current value	GND1	-	-0.3	+20	V	O

Table 3. Absolute maximum ratings (continued)

Pin name	Parameter	Referred to	Constr.	Min	Max	Unit	Pin(1) Direction
INJ1_PGND INJ2_PGND INJ34_PGND O2H1_PGNDA O2H1_PGNDB O2H2_PGNDA O2H2_PGNDB SOL12_PGND PDR_GND	Low-side drivers GND	GND1	-	-0.3	+0.3	V	O
PRD1_GATE PRD2_GATE PRD3_GATE PRD4_GATE PRD5_GATE	General purpose pre-drivers gate voltage	GND1	-	-0.3	+20	V	O
PRD1_DRN PRD2_DRN PRD3_DRN PRD4_DRN PRD5_DRN	General purpose pre-drivers feedback voltage	GND1	-	-0.3	+60	V	I
EN_N EN_P	Digital input (Cranking drivers enable signals)	GND1	-	-0.3	+20	V	I
LIN_TX	LIN data input	GND1	-	-0.3	+20	V	I
LIN_RX	LIN data output	GND1	-	-0.3	+20	V	O
LIN	LIN driver output	GND1	T = -40 °C	-18	+40	V	O
LIN	LIN driver output	GND1	T = -27 °C, 175 °C	-27	+40	V	O
CAN_TX	CAN data input	GND1	-	-0.3	+20	V	I
CAN_RX	CAN data output	GND1	-	-0.3	+20	V	O
CANH	CAN driver output	GND1	-	-27	+40	V	O
CANL	CAN driver output	GND1	-	-27	+40	V	O
VDD_CAN	CAN Supply 5V	GND1	-	-0.3	+20	V	S
VB_CAN	CAN Supply Battery	GND1	-	-16	+40	V	S

Table 3. Absolute maximum ratings (continued)

Pin name	Parameter	Referred to	Constr.	Min	Max	Unit	Pin[1] Direction
VCANH-VCANL	Differential CAN-bus voltage	-	-	-5	10	V	-

1. S: supply pin;
I: input pin;
O: output pin;
I/O: input/output pin
2. -2 V allowed during transients.

2.1 Latch-up trials

Latch-up tests performed according to JEDEC 78 class 2 Level A.

2.2 ESD

Table 4. ESD

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ESD HBM Global	HBM global pins	ESD according to Human Body Model (HBM), Q100-002 for global pins; (100pF/1.5kΩ)	-4	-	4	kV	Global
ESD HBM	HBM local pins	ESD according to Human Body Model (HBM), Q100-002 for all pins; (100pF/1,5kΩ)	-2	-	2	kV	ALL
ESD HBM Global CAN	CAN_H, CAN_L pins	ESD according to Human Body Model (HBM), Q100-002 for global pins; (100pF/1.5kΩ) [1]	-8	-	8	kV	Global
ESD HBM Global CAN	CAN_H, CAN_L pins	Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04)	-6	-	6	kV	Global
ESD CDM Corner	CDM corner pins	ESD according to Charged Device Model (CDM), Q100-011 Corner pins	-750	-	750	V	Corner
ESD CDM	CDM all pins	ESD according to Charged Device Model (CDM), Q100-011 All pins	-500	-	500	V	ALL

1. HBM with all not zapped pins grounded.

Table 5. Pin classify

Pin classify	
Global pin (ECU connector)	VB_IN VBAT_Sense VB_STBY VSENSE1/2 VESNSE3/4_MON KEY_IN WK_IN MRD INJ1/2/3/4 O2H1/2 SOL1/2 RLY1/2/3/4/5 LED1/2 STR1/2/3_DRN STR1/2/3_SRC IGN1/2/3/4/5/6 LIN PRD1/2/3/4/5_DRN
Direction pin (power and I/O)	VDD_IO WDA SOE_OUT RSTN INJ_ENA MSC_EN MSC_CK_P MSC_CK_N MSC_DI_P MSC_DI_N MSC_DO FLW_OUT CURR_Sense_O2H1/2 PRD1/2/3/4/5_GATE EN_P EN_N LIN_TX LIN_RX VDD5_IN CP EN_N EN_P
Local pins	VB_IN_SW Boost_G VPRE BUCK_SW Buck_C_BST VDD5_GATE FLW_IN_P FLW_IN_N
GND pins	GND1 INJ1/2/3/4_PGND O2H1/2_PGND_A O2H1/2_PGND_B GND

2.3 Temperature ranges and thermal data

Table 6. Temperature ranges and thermal data

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
-	Ta	Operating temperature	-	-40	-	125	°C
-	Tj	Junction temperature	-	-40	-	175	°C
-	Tstr	Storage temperature	-	-50	-	175	°C
-	R_{THj-c} (1)	Thermal resistance junction to case	-	-	1	-	°C/W
-	R_{THj-a} (1)	Thermal Resistance junction to ambient	supposing a mounting on board 2s2p + heatsink vias (refer to application note for PCB parameters)	-	10	-	°C/W

1. With 2s2p PCB thermally enhanced, cold plate as per std Jedec best practice guidelines (JESD51), assuming Pdiss = 5 W dissipated statically and homogeneously, thermal vias under package exposed pad assuming filling ratio 50% and 35 µm vias diameter (157 vias estimation); refer to *Figure 3: Thermal simulation set-up on page 26*.

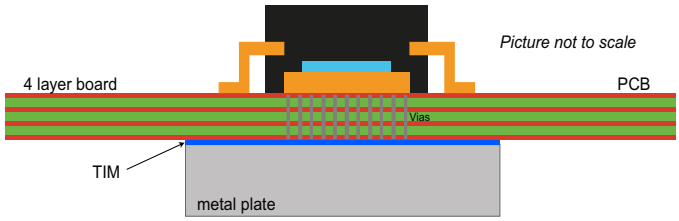
Note: All parameters are tested in the temperature range T_j -40 - 150°C; device functionality at high temperature is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).

Temperature sensor present, please refer to Section 3.5.

Figure 3. Thermal simulation set-up

Boundary conditions

- Thermal simulations carried on using typical boundaries for ECU applications:
- 4 layer board with thermal vias
- metal plate in contact with board
- Thermal interface material (TIM) between PCB and metal plate
- T_{AMB} = 135 °C / natural convection



With these boundaries and considering uniform power on overall chip surface, ST package thermal resistance is:

$Theta_{J-A}$ = 10 °C/W

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2.4 Functional range

Table 7. Functional range

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
-	Cranking condition	u-chip in cranking condition, reduced operation range, main relay and delayed off power stages keep the status if delay-off function is triggered All other driver/regulators/CAN/LIN are in off condition. See description in the Reset Matrix Table, *Section 12.10*.	3.1	-	4.8	V	VB_IN
-	Low drop condition	u-chip in low drop operation condition, all functions are guaranteed all parametersare guaranteed unless specified. Vpre and VDD5 are in low drop condition	4.8	-	7	V	VB_IN
-	Normal condition	u-chip in normal operation condition. all functions and parameters are guaranteed, considering the description range of electrical characteristic table and parameters test set up	7	-	19	V	VB_IN

Table 7. Functional range (continued)

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
-	Jump start condition	u-chip in jump start condition, all functions are guaranteed. parameters are guaranteed unless specified.	19	-	28	V	VB_IN
-	Load dump condition	u-chip in load dump condition. U-chip is no damage. All drivers/regulators/CAN/LIN are in off condition. See description in the Reset Matrix Table, *Section 3.3* and *Section 12.10*.	28		40	V	VB_IN

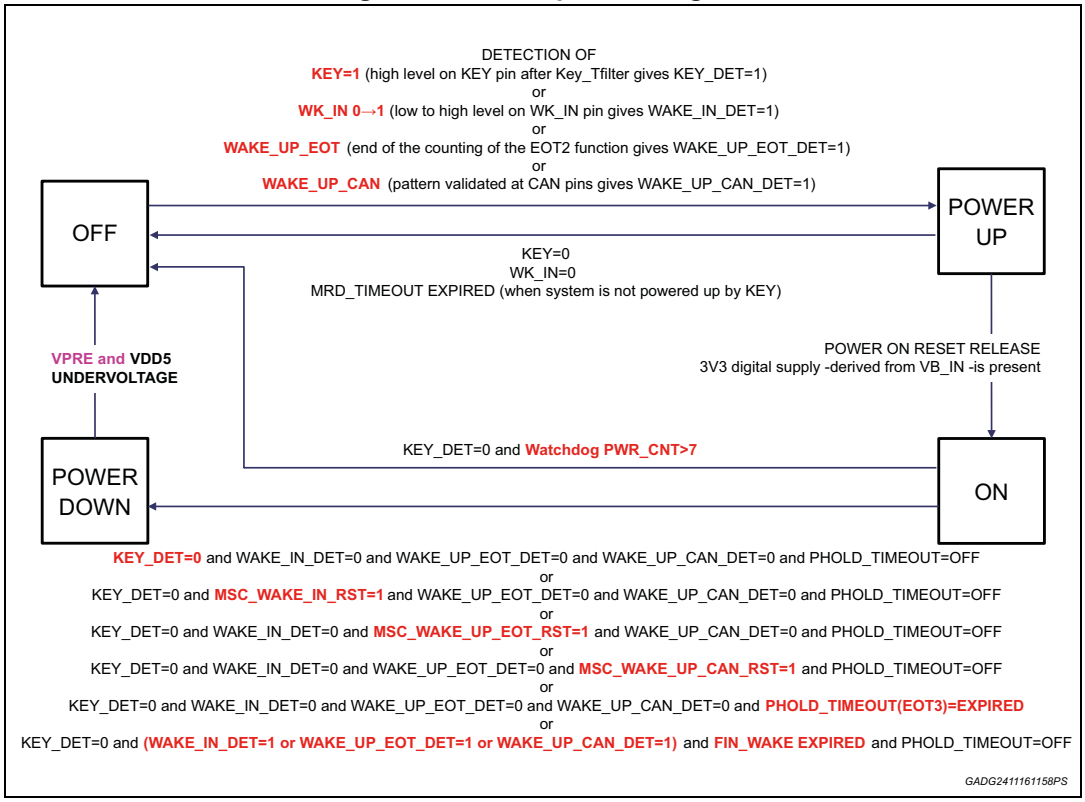
3 Operation behavior

3.1 Power up/down

3.1.1 Power up/down state diagram chart

The power up/down sequences are shown as state diagram in the following figure:

Figure 4. Power up state diagram



3.1.2 Power up sources and actions summary

Table 8. Power up sources and actions summary

KEY_IN	WK_IN	EOT	CAN_FD	VB_IN	MRD	Actions
active	-	-	-	not permanent	on	MRD on by KEY_IN pin
active	-	-	-	permanent	on	MRD on by KEY_IN pin
	active	-	-	not permanent	on	MRD on by WK_IN pin
-	active	-	-	permanent	off	MRD used as normal low-side driver (is controlled by MSC)
-	-	active	-	not permanent	on	MRD on by EOT
-	-	active	-	permanent	off	MRD used as normal low-side driver (is controlled by MSC)

Table 8. Power up sources and actions summary (continued)

KEY_IN	WK_IN	EOT	CAN_FD	VB_IN	MRD	Actions
-	-	-	active	not permanent	on	MRD on by CAN
-	-	-	active	permanent	off	MRD used as normal low-side driver (is controlled by MSC)

3.1.3 Power up from KEY_IN

The chip is powered up if KEY_IN signal stays asserted for Key_Tfilter.There is a MSC bit *(KEY_IN_PIN_FLT in read command 15 frame 2)* to indicate the status of KEY_IN pin signal after filter time.

3.1.4 Power down from KEY_IN when PHOLD = 0

The chip is powered down if KEY_IN signal stays de-asserted for Key_Tfilter if no other power up source is active.

Condition:

4.8 ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 9. Key pins electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_{IH}	Logic input high voltage threshold	-	3.6	-	4.1	V	KEY_IN
V_{IL1}	Logic input low voltage threshold Main logic in POR not released	-	3.1	-	3.6	V	KEY_IN
V_{IL2}	Logic input low voltage threshold Main logic POR released	-	1.7	-	2.3	V	KEY_IN
V_{IHYS}	Logic input hysteresis	-	0.1	-	0.8	V	KEY_IN
Key_Tfilter	Filter time for switching on/off	Guaranteed by test scan(1)	7.5	16	24	ms	KEY_IN
I_{input}	Input current of KEY_IN	KEY_IN ≤ 5 V	-	-	340	µA	KEY_IN
R_{PD}	Pull-down resistor	KEY_IN = 1 V	170	300	500	kΩ	KEY_IN

1. Filter time for switching on, is active until KEY logic is out of POR, Filter time for switching off, is active until main logic out of POR.

3.1.5 Power up from WK_IN

The chip is powered up if WK_IN signal has a rising edge and stays asserted for WK_Tfilter. In case the power up of the chip is not completed in a MRD_EN_TIMEOUT from WK_IN rising edge detection the Main Relay Driver is switched off and the chip goes in OFF state. The u-chip will not power up until further rising edge on WK_IN pin. This detection of a WK_IN condition flag is named *WK_IN_DET* (detection of a WK_IN condition) and is cleared by VDD5/VDDIO under voltage or by the MSC command *WK_IN_RST*. In these cases, if no other power-on source is active, a power down sequence is started.When U chip is already in on state (the logic is out of power on reset), the rising edge on pin WK_IN only sets a flag, with no impact on power supply.

The Main Relay Driver is not switched on by *WAKE_IN_DET* rising edge if the device is in permanent battery. To recognize the permanent battery condition the main logic has to be out of Power On Reset within Tbattery_det.

There is a MSC bit *(WAKE_IN_PIN_FLT in read command 15 frame 2)* to indicate the status of WK_IN pin signal after filter time.

A negative glitch on WK_IN can produce unwanted power up and also prevent the correct power down.

To cover the major cases the falling edge filtering is done both in the VB_STBY domain and in the VB_IN domain. Depending on which supply is present the behavior is described in the following cases:

1. If VB_STBY is present the falling edge filtering is applied also to power up so a negative glitch on WK_IN will not power up the device.

If VB_STBY is not present a negative glitch on WK_IN will power up the device.

2. If VB_IN is present (after the device is already powered up) the falling edge filtering on WK_IN avoids that a glitch (happening in PHOLD after the MSC has cleared the WK_IN detection) is recognized as valid detection and the device is kept on.

3.1.6 Power down from WK_IN when PHOLD=0

The chip is powered down if the MSC clears, by the MSC command *WK_IN_RST*, the detection of WK_IN positive edge if no other power up source is active. The power down is actuated even if WK_IN is still high. The power down is not activated by WK_IN going low or WK_IN low level. The detection reset by MSC command, *WK_IN_RST* (CONFIG_REG12[7]), is active at level, so from when MSC writes them at 1 they keep on clearing the detections. If there is further wake detection signal, the detection signal will be cleared, until the MSC writes 0 in the bits.

Condition:

4.8 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 10. WK pins electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_{IH}	Logic input high voltage threshold	-	3.6	-	4.1	V	WK_IN
V_{IL}	Logic input low voltage threshold	-	3.1	-	3.6	V	WK_IN
V_{IHYS}	Logic input hysteresis	-	0.1	-	0.8	V	WK_IN

Table 10. WK pins electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{input}	Input current of WK_IN	WK_IN ≤ 5 V	-	-	340	µA	WK_IN
WK_Tfilter	Filter time for switching on/off	Guaranteed by test scan	1	2	3	ms	WK_IN
RP_D	Pull-down resistor	WK_IN=1V	170	300	500	kΩ	WK_IN
MRD_EN_TIMEOUT	Timeout for power up execution	-	331	500	650	ms	WK_IN
Tbattery_det	Main logic POR timeout (used to recognize permanent battery condition)	-	210	-	450	µs	-

3.1.7 Power up from WAKE_UP_TIMER

The chip is powered up when an end counting is reached inside the wake_up_timer block. The end and enable counting are set by MSC before the chip is powered down. In case the power up of the chip is not completed in a MRD_EN_TIMEOUT from WAKE_UP_EOT end of counting detection the Main Relay Driver is switched off and the chip goes in OFF state.

When U chip is already in on state (the logic is out of power on reset), the wake_up_timer end counting only sets a flag, with no impact on power supply. This flag is named *WAKE_UP_EOT_DET* (detection of a wake_up end of time condition) and is clear by VDD5/VDDIO under voltage or by the MSC command *WAKE_UP_EOT_RST*. If no other power on source is active a power down sequence is started.

The Main Relay Driver is not switched on by WAKE_UP_EOT if the device is powered in permanent battery.

The MSC sets the programmable time on *Wake up timer_SET Registers (CONFIG-REG15-0 to CONFIG_REG15-2)*. The counting can be started/stopped by MSC command - *CONFIG_REG1[6:7] = WAKE_UP_TIMER_START_STOP[0:1] (CONFIG_REG1 D6;D7)* - or by switching the pin KEY_IN according to a selection set by MSC bit - *CONFIG_REG20[2] = WAKE_UP_TIMER_EN_SEL*.

The counter counts time on the *WAKE_UP_TIMER_CNT* Register. *WAKE_UP_TIMER_CNT* Register and Wake up timer_SET Register are being compared, and when they match, *WAKE_UP_EOT_DET* signal will be set to high level to trigger a power up sequence.

Condition:

4.8 V ≤ VB_IN ≤ 18 V, 3.5 V ≤ VB_STBY ≤ 18 V Tj -40 to 175 °C unless otherwise specified;
VB_STBY > 3.5 V, EOT can keep the counter value (allow to stop counting),
5 V < VB_STBY < 18 V, EOT full function, full parameter.

Table 11. VB_STBY pins electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VVB_STBY_Th	VB_STBY voltage range that EOT counter keep data or operating correctly	-	3.5	-	-	V	VB_STBY
IVB_STBY_EOT_disable	VB_STBY current with EOT 32 kHz Clock device OFF	3.5 < VB_STBY< 18 V VB_CAN < 0.7 V	-	-	30	µA	VB_STBY
IVB_STBY_ EOT_enable	VB_STBY current with EOT 32 kHz Clock device ON	3.5 < VB_STBY< 18 V VB_CAN < 0.7 V -40 °C < T_{amb} < 80 °C	-	-	50	µA	VB_STBY
IVB_STBY_EOT_enable	VB_STBY current with EOT 32 kHz Clock device ON	3.5 < VB_STBY< 18 V VB_CAN < 0.7 V 80 °C < T_{amb} < 125 °C	-	-	70	µA	VB_STBY
EOT_clock_frequency	Freq EOT 32 kHz Clock internal components	6 V < VB_STBY <18 V -40° C <T_{amb} < 80 °C	-6%	1	+6%	Hz	VB_STBY
EOT_clock_frequency	Freq EOT 32 kHz Clock internal components	6 < VB_STBY < 18 V 80 °C < T_{amb} < 125 °C	-7%	1	+7%	Hz	VB_STBY
VB_STBY_UV	VB_STBY under voltage threshold the 32 kHz clock is active but counter is stopped during crank.	VB_STBY > 3.1 V	3.5	-	5	V	VB_STBY

When VB_STBY_UV happens, it stops the counter.

The counter will resume when vb_stby_uv goes low (no undervoltage).

Figure 5. Timing for Wake Up Timer - driver by MSC start/stop commands

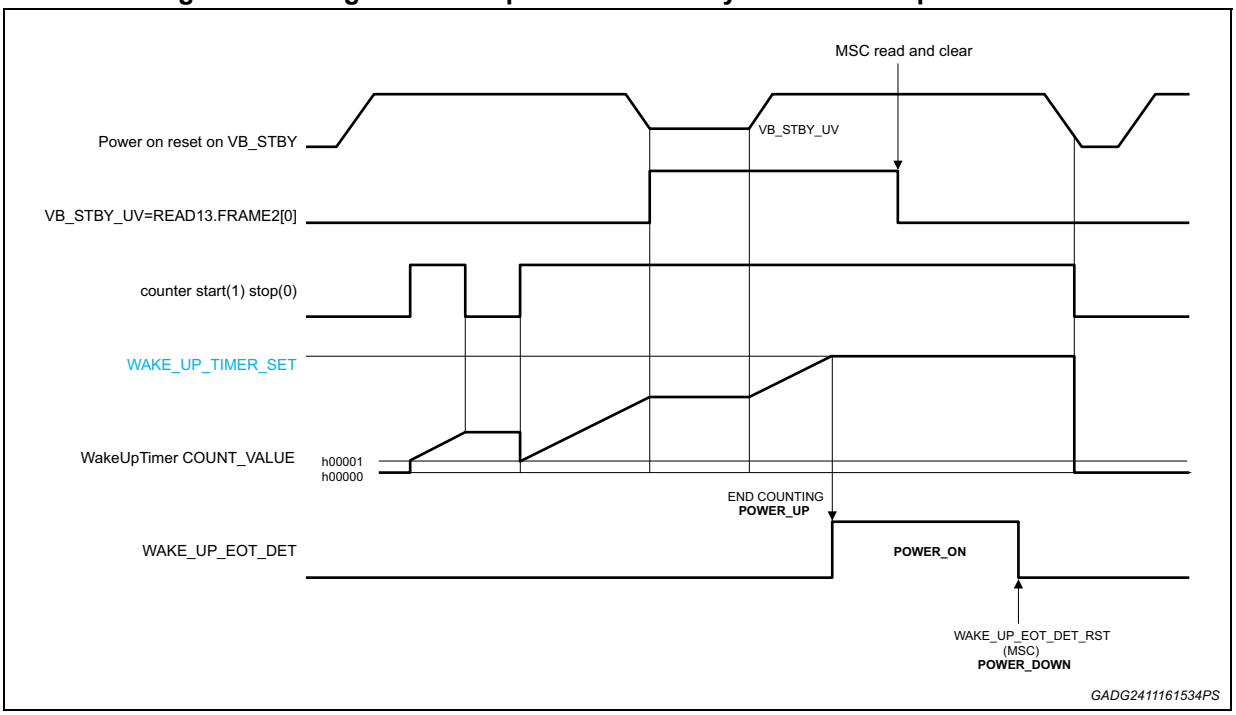
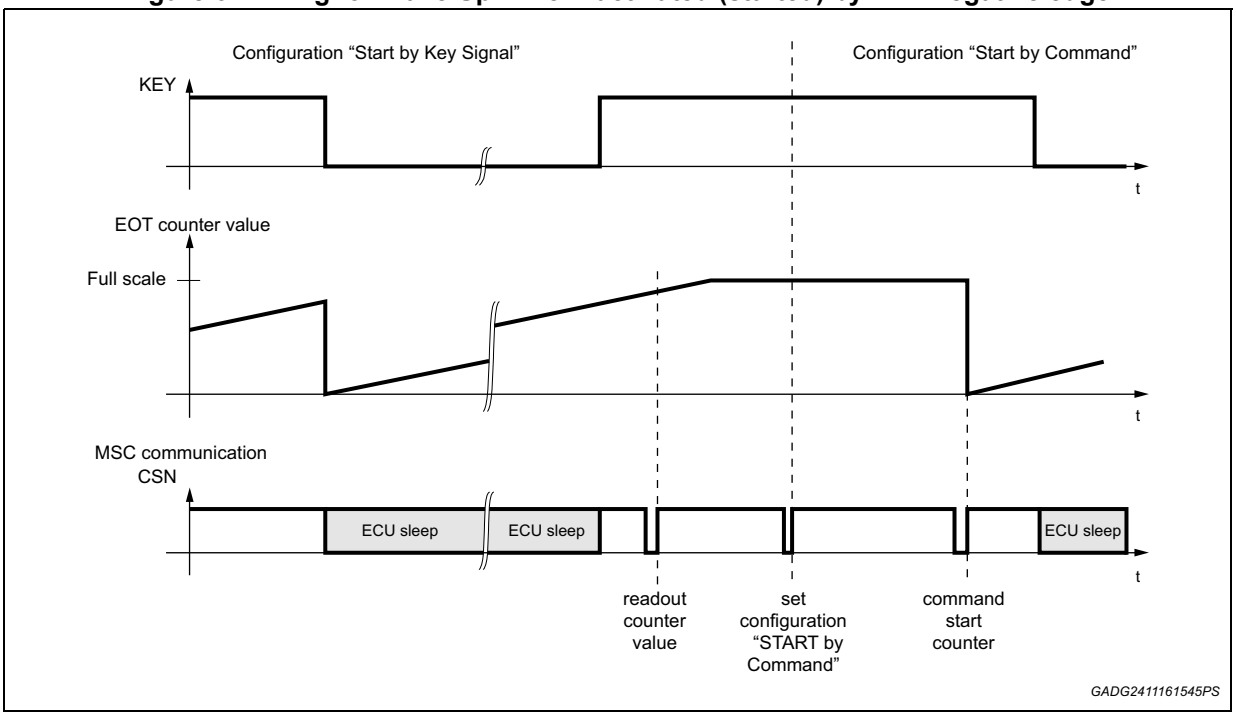


Figure 6. Timing for Wake Up Timer - activated (started) by KEY negative edge



Reset condition

VB_STBY under voltage stops (not reset) EOT counter during cranking. The counter is reset in case of power on reset generated on VB_STBY supply.

Count up

Wake up Timer shall count up the timer from 1 while the MSC *Wake Up Timer Start* command is given. When *Wake Up Timer Stop* command is given, the Wake Up Timer shall stop counting and hold the value until *Wake Up Timer Start* command is given again. While the counter is counting the *EOT_STATUS* will be 1. If it's not counting *EOT_STATUS* will be 0.

Wake Up Timer start/stop commands

Wake Up Timer counts up when msc start command in the MSC *WAKE_UP_TIMER_START_STOP* register is given. When the msc stop command in the MSC *WAKE_UP_TIMER_START_STOP* register is given the timer shall stop counting up but hold the *WAKE_UP_TIMER_CNT* Register. The bit can be set or reset via MSC.

WAKE_UP_TIMER_CNT Register

WAKE_UP_TIMER_CNT Register consists of 24 bits it's Read Only. The range of *WAKE_UP_TIMER_CNT* is from 0 (h'000000) to 16777215 (h'FFFFFF). *WAKE_UP_TIMER_CNT* Register is set to 0 (h'00000) when power on reset of VB_STBY occurs. *WAKE_UP_TIMER_CNT* Register is set to all "0" via MSC when power on reset period or VB_STBY is open.

Wake up timer_SET time register

The *Wake up timer_SET register* consists of 24 bits. And the register is Read and Write register. The range of *Wake up timer_SET* is from 0 (h'000000) to 16777215 (h'FFFFFF). *Wake Up Timer_SET* Register is set to 0(h '000000) when power on reset of VB_STBY occurs.

EOT function 1

EOT Function 1 - count “stand” time: After the start of the counter, the counter starts to count up till the value that has to be set before starting it using *Wake_up_timer_SET*. If ECU switches on before the counter reaches the wake up timer_set value, the µC can read the “stand” time via MSC. If the counter reaches the wake up timer_set value before ECU switches on, the count keeps the wake up timer_set value.

This function is selected with *MSC CONFIG_REG6[6]=EOT_MODE=0*. The EOT function 1 does not set *WAKE_UP_EOT_DET* at 1. EOT_MODE bit can be correctly read only when wake up timer logic is working, else it is read 0.

VB_STBY must be provided to correctly read the *EOT_MODE* bit. If VB_STBY is removed the register content will be lost.

EOT function 2

EOT Function 2 - wake-up via *WAKE_UP_TIMER_SET*. Set *WAKE_UP_TIMER_SET (CONFIG-REG15-0 / CONFIG-REG15-1/ CONFIG-REG15-2)* to a certain value, then start the counter before shutting down the ECU. The counter counts up until the WAKE_UP_TIMER_SET is reached. The reaching of *WAKE_UP_TIMER_SET* activates the wake signal and will start a wake-up sequence. This function is selected with MSC *CONFIG_REG6[6]=EOT_MODE=1*. *EOT_MODE* bit can be correctly read only when wake-up timer logic is working, else it is read 0.

VB_STBY supply must be provided to correctly read the *EOT_MODE* bit.

Figure 7. Wake up timer block diagram

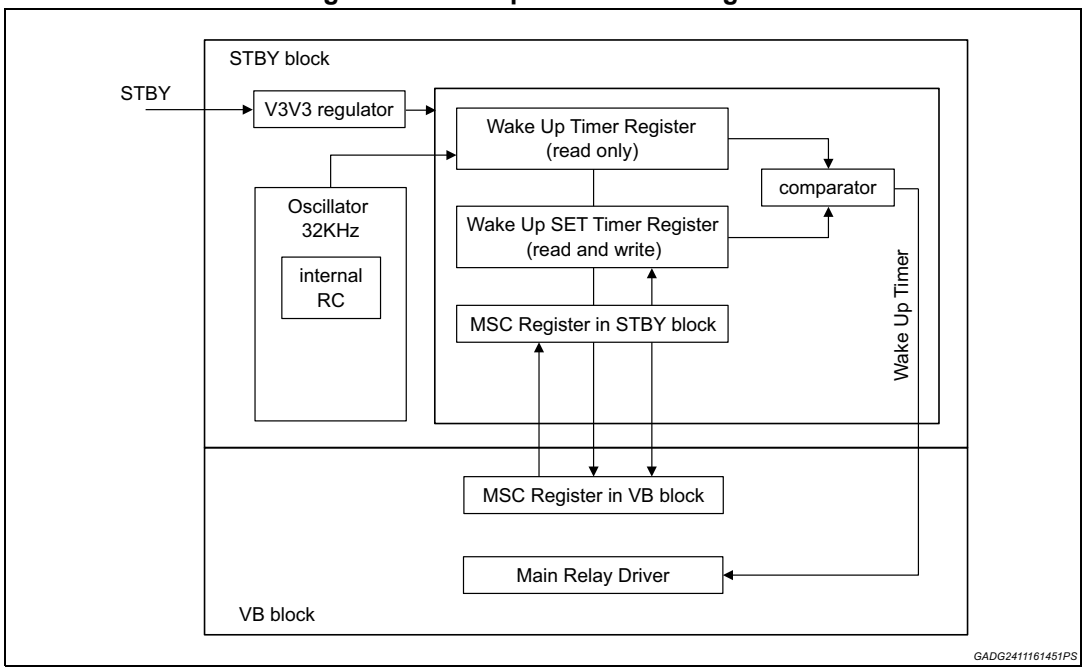


Table 12. Wake up timer resolution

range	resolution
0 - 16777215	1 second

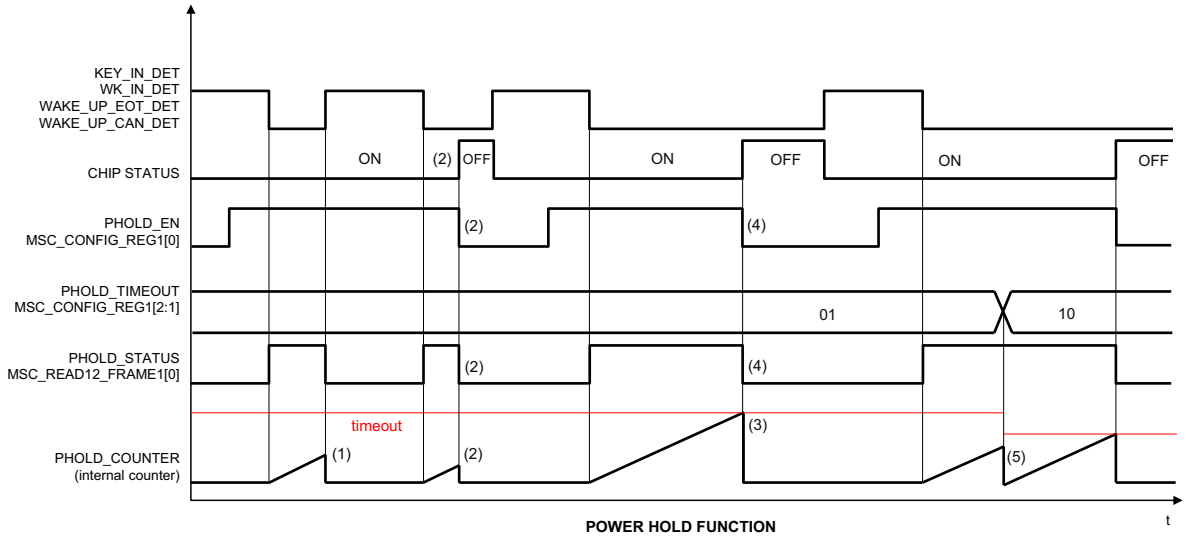
WAKE_UP_TIMER_CNT Register can be read via MSC. *Wake up timer_SET* Register can be read and write via MSC.

3.1.8 Power on with PHOLD_EN (EOT function 3)

The chip is kept switched on by an MSC command (*PHOLD_EN CONFIG_REG1[0]*) even though one of the power down sources has been asserted (KEY_IN, WK_IN, WAKE_UP_TIMER, WAKE_UP_CAN). The chip is kept on in power hold mode for a time programmed (default is infinity) by MSC (*PHOLD_TIME[0:1] CONFIG_REG1 (D1;D2)*). This is also EOT function 3. The power hold mode is enabled by MSC and is cleared by the conditions reported in the reset matrix.

After setting the *PHOLD_EN=CONFIG_REG1[0]*=1 the PHOLD and the PHOLD timer are enabled when the *KEY_DET, WK_IN_DET, WAKE_UP_EOT_DET, WAKE_UP_CAN_DET* detections are not active. The *PHOLD_TIMER[14:0]=READ12.FRAME[2:1]* starts counting when the *KEY_DET, WK_IN_DET, WAKE_UP_EOT_DET, WAKE_UP_CAN_DET* detections are cleared. When the *PHOLD_TIME=CONFIG_REG1[2:1]* is configured as 00 (default) the timeout is disabled and the *PHOLD_TIMER[14:0]=READ12.FRAME[2:1]* is read always at 0.

Figure 8. Power hold diagram



(1) The timeout counter is cleared on the detection of at least one of the power up sources.
(2) The timeout counter is cleared if MSC disables the PHOLD function, MRD is switched off, a power down sequence is started.
(3) The counter has reached the timeout, MRD is switched off, a power down sequence is started.
(4) The PHOLD_EN and the PHOLD_STATUS bits are clear along with the power down sequence.
(5) A new MSC setting for the timeout makes the timeout counter clear and restart.

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3.1.9 Power down from WAKE_UP_TIMER when PHOLD_EN=0

The chip is powered down if the MSC clears, by the MSC command *WAKE_UP_EOT_RST*, *WAKE_UP_EOT_DET* (The counter counts up until the *WAKE_UP_TIMER_SET* is reached) if no other power up source is active and *PHOLD_EN* = 0. The detection reset by MSC command, *WAKE_UP_EOT_RST=CONFIG_REG12[6]*, is active at level not at change, so from when MSC writes them at 1 they keep on clearing the detections. If there is further wake detection signal, the detection signal will be cleared, until the MSC writes 0 in the bits.

3.1.10 Power down from PHOLD

The chip is powered down after the power hold timer programmed by MSC has expired or if the PHOLD function is disabled by MSC. The PHOLD timer can be programmed as timeout disabled so that the chip stays powered up.

3.1.11 Power up from CAN

The chip can be powered up from CAN according to what reported in the Wake Up (From CAN) chapter. To allow the power up from CAN the pins VB_CAN, VB_STBY must be supplied. In case the power up of the chip is not completed in a MRD_EN_TIMEOUT from CAN valid pattern detection the Main Relay Driver is switched off and the chip goes in OFF state

When U chip is already in on state (the logic is out of power on reset), the validation of a valid CAN pattern only sets a flag, with no impact on power supply. This flag is named *WAKE_UP_CAN_DET* (detection of a valid can pattern) and is cleared by VDD5/VDDIO under voltage or by the MSC command *WAKE_UP_CAN_RST*. In this case if no other power on source is active a power down sequence is started.

The Main Relay Driver is not switched on by WAKE_UP_CAN if the device is powered in permanent battery.

3.1.12 Power down from WAKE_UP_CAN when PHOLD_EN=0

The chip is powered down if the MSC clears, by the MSC command *WAKE_UP_CAN_RST*, *WAKE_UP_CAN_DET* (the detection of WAKE_UP_CAN high) if no other power up source is active and PHOLD_EN = 0. The detection reset by MSC command, *WAKE_UP_CAN_RST=CONFIG_REG12[5]*, is active at level, so from when MSC writes them at 1 they keep on clearing the detections. If there is further wake detection signal, the detection signal will be cleared, until the MSC writes 0 in the bits.

3.1.13 Finish wake function

There is a Finish wake function (auto clear mechanism) of *WK_IN_DET, WAKE_UP_EOT_DET and WAKE_UP_CAN_DET*. The purpose is to ensure the system could power down from wake up state after the impulse timer timeout (typ. 1s).

If the software does not stop the impulse timer before time out, the *WK_IN_DET, WAKE_UP_EOT_DET and WAKE_UP_CAN_DET* will be cleared as long as time out. If the software stops the impulse timer (*FIN_WAKE = 1*) before time out, the *WK_IN_DET, WAKE_UP_EOT_DET and WAKE_UP_CAN_DET* will not be cleared.

The impulse timer is not affected by watchdog(*ERR_CNT*>4) and EOT. The Finish wake function is not disabled by RSTN pulled low externally and *MSC_SW_RESET* active. The

Finish wake function can be disabled by power supply undervoltage. The reset sources of FIN_WAKE bit are the same as fin_wake function.

Software can decide to clear the *WK_IN_DET, WAKE_UP_EOT_DET or WAKE_UP_CAN_DET* before or after the impulse timer timeout, through set *WK_IN_RST, WAKE_UP_EOT_RST or WAKE_UP_CAN_RST* to 1

FIN_WAK function is stopped by

1. FIN_WAKE time out,
2. *FIN_WAKE* BIT =1,
3. *WK_IN_RST / WK_EOT_RST /WK_CAN_RST* of relevant detect signal.

When *WK_IN_DET & WK_EOT_ DET &WK_CAN_ DET =0*, FIN_WAK can be re-triggered by any detection of *WK_IN_DET / WK_EOT_ DET /WK_CAN_ DET*. The counter is restarted from 0.

Figure 9. Impulse timer clear WAKE_IN_DET after time out

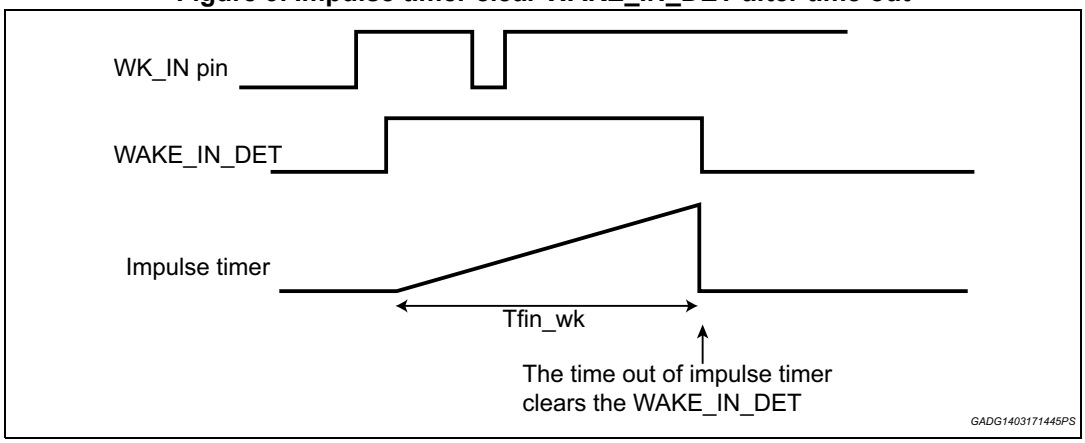


Figure 10. Impulse timer disabled before time out

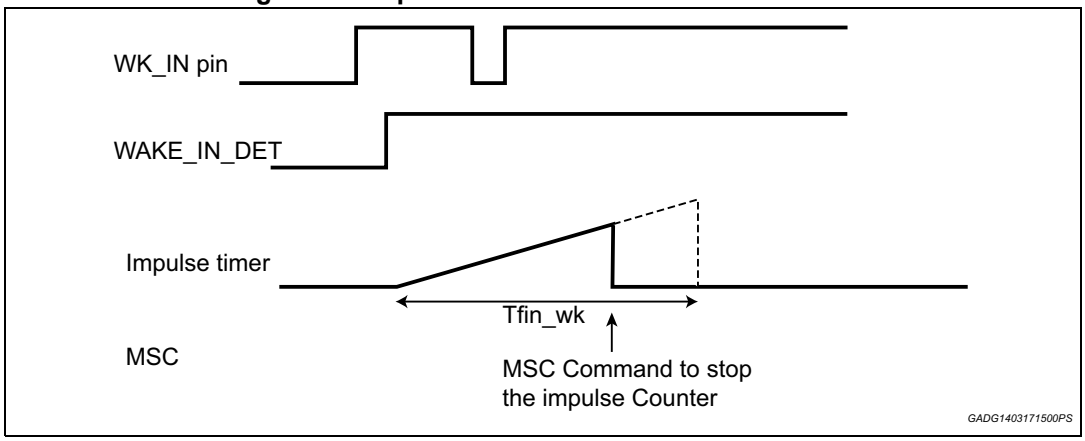
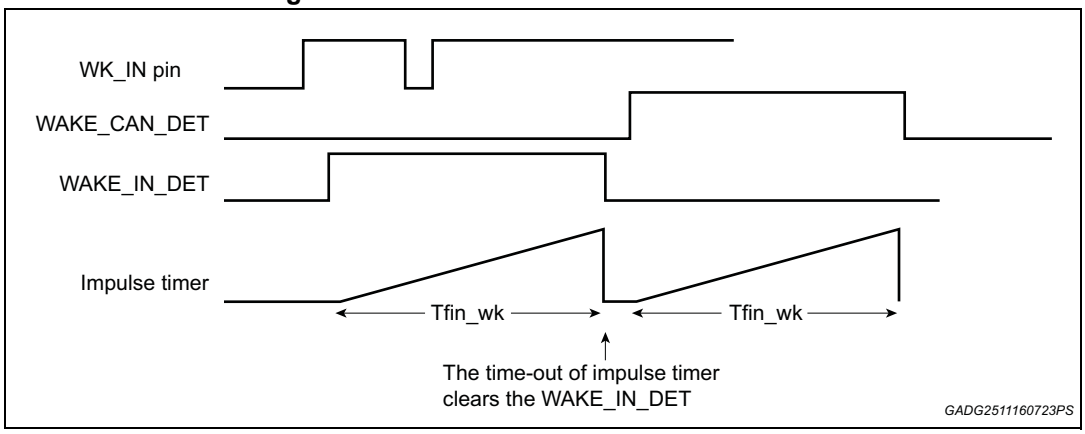


Figure 11. Timer enabled for a new detection



Note: Same mechanism applied to WAKE_IN_DET, WAKE_UP_EOT_DET and WAKE_UP_CAN_DET.

Table 13. Finish wake timer electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Tfin_wk	Finish wake timer	0.94	1	1.06	s

3.2 Secure Engine Off (SEO) function

Secure Engine Off functional switches off, with a certain delay from KEY_OFF, the engine by a hardware path and without any dependence on external micro and no matter what are the other conditions (e.g. the power hold mode).

After the falling edge of the filtered KEY_IN a programmable counter is started. The clock of the timer does not depend on any micro clock or function.

SEO_OUT pin is the output of KEY_IN after a *T_SEO_DELAY (CONFIG_REG3 [6:7]*)delay.

Input pin INJ_ENA enables the internal drivers as listed above (INJ[1:4], is configured), so the configuration of enable/disable of SEO function is realized by hardware in the following way:

For PFI application, SEO_OUT is connected to INJ_ENA, when key goes off internal drivers can be switched off.

For GDI application, SEO_OUT is connected to GDI injector driver enable if present, INJ_ENA is always enabled. When key off, only the external GDI injector driver is switched off.

During SEO time the external micro can switch on/off the drivers

SEO output is implemented with a push pull output stage, the *T_SEO_DELAY* can be programmed according to *Table 14*.

Table 14. SEO timing

Symbol	Parameter	MSC_CONF	Min	Typ	Max	Unit	Pin
T_SEO_DELAY	default	00	100	-	140	ms	SEO_OUT
T_SEO_DELAY	-	01	200	-	250	ms	SEO_OUT
T_SEO_DELAY	-	10	400	-	480	ms	SEO_OUT
T_SEO_DELAY	-	11	800	-	920	ms	SEO_OUT

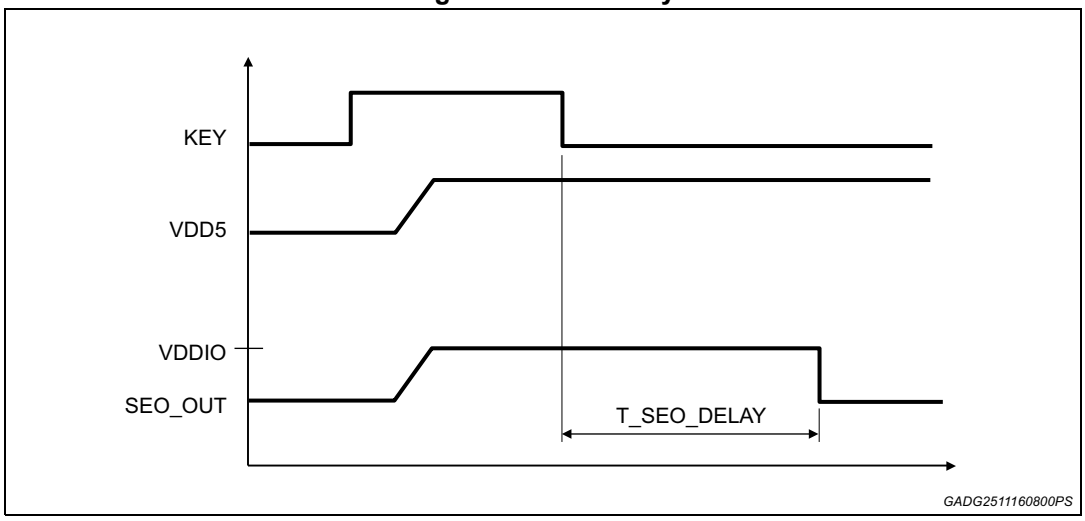
Condition:

5.5 V ≤ VB_IN ≤ 18 V, 4.75 V ≤ VDD_IO ≤ 5.25V, T_j -40 to 175 °C unless otherwise specified.

Table 15. SEO Circuit electrical characteristic

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
SEO_OUT_L	SEO_OUT output low level	VDDIO = 5 V or 3.3 V I_{sink} current = 2 mA	-	-	0.5	V	SEO_OUT
SEO_OUT_H	SEO_OUT high level	VDDIO = 5 V or 3.3 V I_{sink} current = 2 mA	VDDIO -0.5	-	-	V	SEO_OUT

Figure 12. SEO delay



3.3 Reset strategies

Figure 13. Reset table

		SUPPLY DOMAIN	VB_STBY WAKE_UP_EOT WAKE_UP_CAN				V3V3		BUCK 6V		REG 5V					V3V3D															TRACK 5V
		EVENT	VB_STBY	VB_IN/VB_IN_SW			V3V3A V3V3D		VPRE		VDD5		VDDIO	OSC	GND	WDA_QA				MSC_ACT	SW_RESET	afterrun reset active	WATCHDOG internal reset			RSTN (IN)	EN_P EN_N	FAULT WARNING		
			UV	OV t>tTBOV2	OV tTBOV1<t<tTBOV2	UV	OV	UV	OV	UV	OV	UV	UV	FAULT	LOSS	WDA(IN)	ERR_CNT>4	ERR_CNT>7	PWR_CNT>7 and KEY_IN=0				RST_PRL	WDA_CNT_RST	WD A_REG_RST	IN	IN		OV/UV
				MSC en/dis (for BUCK, VDD5, TRK) VB_IN_OV_RST_EN							MSC en/dis					BID PIN		MSC wda_init=1	MSC en/dis			MSC en/dis				BID PIN				
		FLAG READ BY MSC	VB_STBY_UV	VB_IN_ OV	VB_IN_ OV	VB_IN_UV (POWER LOSS)	V3V3A_OV V3V3D_OV	V3V3A_UV V3V3D_UV	VPRE_OV	VPRE_UV	VDD5_OV	VDD5_RST					WDA_INT	WDA_RST	power_down	TRANS_F										TRK[1-4]_OV/UV
VB_STBY		VB_STBY	x	○	○	○	○	○	○	○	○	○	○	○		○	○	○	○	○	○	○	○			○	○	○	○	○
VB		wake_up_timer(EOT)	▲ no rese t	○	○	○	○	○	○	○	○	○	○	○		○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
		KEY_IN_DET	○	○	○	○	○	○	○	○	○	○	○	○		○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
		POWER HOLD	○	○	○	○	▲	▲	○	○	▲	○	▲	○		○	○	▲	▲	○	▲	▲	○	○	○	▲	○	○	○	○
		WAKE_IN_DET/WAKE_UP_EOT_DET/WAKE_UP_CAN_DET	○	○	○	○	○	○	○	○	○	▲	▲	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
	V3V3	V3V3A V3V3D	○	○	○	○	x	x	○	○	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
		BOOST	○	-	-	▲	▲	▲	▲	○	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
		BUCK	○	▲	○	▲	▲	▲	x	x	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
		VCP	○	▲	○	○	▲	▲	○	○	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
	VDD5	VDD5(5V)	○	▲	○	▲ *1 5	▲	▲	○	▲	x	x	x	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
	TRACK 5V	TRACK(5V)	○	▲	○	▲	▲	▲	○	○	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	x
	WDA	WDA (OUT)	-	-	-	-	Δ	Δ	-	-	Δ	Δ	Δ	-		x	Δ	Δ	Δ	-	Δ	Δ	Δ	○	○	Δ	-	-	-	-
		WDA sequence	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	○	○	○	▲	○	○	○	○	○	○
		WDA error counter	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	▲	▲	○	▲	▲	▲	○	○	▲	○	○	○	○
		WDA power down counter	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	INC+1	○	○	▲	○	○	○	○	○	○
		WDA reset counter	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	○	○	○	▲	○	○	○	○	○	○
		WDA question register	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	○	○	○	▲	○	○	○	○	○	○
		WDA config register	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	▲	▲	○	▲	▲	▲	○	▲	▲	○	○	○	○
		WDA diagnostic register	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	○	○	▲	○	○	▲	○	○	○	○
		RST_PRL	-	-	-	-	Δ	Δ	-	-	Δ	Δ	Δ	○		-	-	Δ	Δ	-	Δ	Δ	x	-	-	Δ	-	-	-	-
		WDA_CNT_RST	-	-	-	-	Δ	Δ	-	-	Δ	Δ	Δ	-		-	-	-	Δ	-	-	-	x	-	x	-	-	-	-	-
		WDA_REG_RST	-	-	-	-	Δ	Δ	-	-	Δ	Δ	Δ	-		-	-	Δ	Δ	-	Δ	Δ	Δ	-	x	Δ	-	-	-	-
		afterrun reset enable bit (TNL) (default enabled)	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
	MSC	MSC communication*5	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	▲	▲	○	○	▲	○	○	○	▲	○	○	○	○
		MSC_ACT	○	○	○	○	▲	▲	○	○	▲	▲	▲	○		○	○	○	▲	x	○	○	○	○	○	▲	○	○	○	○
		MSC REGISTERS*14	○	○	○	○	▲	▲	○	○	○	▲	▲	○		○	○	○	▲	○	▲	▲	○	○	○	▲	○	○	○	○
		FIN_WAKE	○	○	○	○	▲	▲	○	○	○	▲	▲	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
		RSTN (OUT)	-	Δ	-	Δ	Δ	Δ	-	-	Δ	Δ	Δ	-		-	-	Δ	Δ	-	-	Δ	-	-	-	x	-	-	-	-
		RSTN (OUT) pull down time		Td_UV_RST		Td_UV_RST	Td_UV_RST	Td_UV_RST			Td_UV_RST	Td_UV_RST	Td_UV_RST					TWDA_RST				TNL_RST								
		RSTC (OUT)	-	-	-	Δ	-	-	-	-	-	Δ	-	-		-	-	Δ	-	-	-	Δ	-	-	-	-	-	-	-	-
		FAULT WARNING	-	-	-	-	Δ	Δ	-	-	-	-	-	Δ	Δ	-	-	-	-	-	-	-	-	○	○	-	x	x	-	-
		MRD	○	○	○	○	▲	▲	○	○	○	○	○	○		○	○	○	▲	○	○	○	○	○	○	○	○	○	○	○
		INJ[1:4]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		O2H[1:2]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		SOL[1:2]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		RLY[1:5]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		LED[1:2]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		HSD/LSD[1:2:3]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		RLY4 STR[2:3] *7	○	▲	▲	○	▲	▲	○	○	○	○	○	▲		○	▲*11	▲*11	▲	○	▲	▲	▲	○	○	○	▲*16	▲	○	○
		DELAY OFF FUNCTION	-	-	-	-	-	-	-	-	Δ	Δ	-	-		Δ	-	-	-	Δ	-	-	-	○	○	Δ	-	-	-	-
		PRD[1:5]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		IGN[1:6]	○	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲		▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	○	○	○	○
		K/LIN	○	● *9	○	▲	▲	▲	○	○	● *9	● *9	● *9	● *9		○	● *8	● *8	▲	○	○	● *9	● *8	○	○	● *9	○	○	● *9	○
		VRS	○	▲	○	▲	▲	▲	○	○	▲	▲	▲	▲		○	○	○	▲	○	○	▲	○	○	○	▲	○	○	○	○
		CAN	● *13	● *13	○	● *13	● *13	● *13	○	○	● *12	● *13	● *13	● *12		○	● *10	● *10	▲	○	○	● *12	● *10	○	○	● *12	○	○	○	○

x	detection
○	normal operation
-	not active
●	partial functionality
▲	stop/reset
Δ	active

*5 At the rising edge of reset, the MSC communication is reset. un-sent up stream frame should be discard.
*6 SEO_OUT is triggered by KEY_IN=0
*7 RLY4 and STR[2:3] are MSC configured as starters (CONFIG3[0]=CONFIG3[4:5]=1)
*8 LIN works as receiving mode only (if the disable of the transmitting mode is enabled by MSC)
*9 LIN works as receiving mode only due to watchdog BOSCH IP the WDA_ERR_CNT can be reset if also RST_PRL is activated
*10 CAN works as receiving-only mode only if bit CAN_TDI =1
*11 If the related delay off function is active the driver stays ON
*12 CAN works as receiving-only mode
*13 CAN works as Low-power mode
*14 excluded WAKE_UP_TIMER_START_STOP, EOT_MODE, CAN parameters, WAKE_UP_TIMER_EN_SEL, KEY_OC_RERTY_MAX_EN
*15 When VDD5_OFF_SEL=1, VDD5 does not depend on VB_IN UV. If VDD5_OFF_SEL=0, VDD5 depends on VB_IN UV
*16 RLY4 and STR[2:3] are stop by EN_N/EN_P if they are configured or not as starter

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Note: When VB_STBY_UV happens, it stops the EOT counter.The EOT counter will resume when vb_stby_uv goes low (no undervoltage).

3.4 Smart reset circuit

There are two Reset pins:

1. RSTN: reset pin linked to VDD5 supply;
2. RSTC: reset pin linked to VDDIO supply.

3.4.1 Smart reset RSTN pin

The RSTN pin is an input/output active low. As output pin the Smart Reset circuit takes into account several events in the device in order to generate the proper reset signal at RSTN pin for the microcontroller and for portion of the internal logic as well.

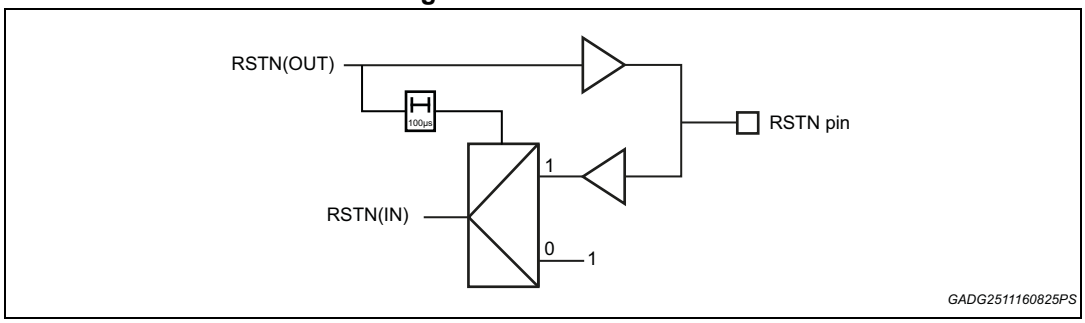
The RSTN in output (RSTN(OUT) is activated by the contributions described by the reset matrix and is intended as reset for the external microcontroller.

The RSTN in input (RSTN(IN)) is filtered Trst_flt_RST and stops the internal logic as described in the reset matrix.

The internal RSTN(OUT) has higher priority respect to the external RSTN(IN). The RSTN(IN) is masked until Tmsk_RSTN after RSTN(OUT) has been released.

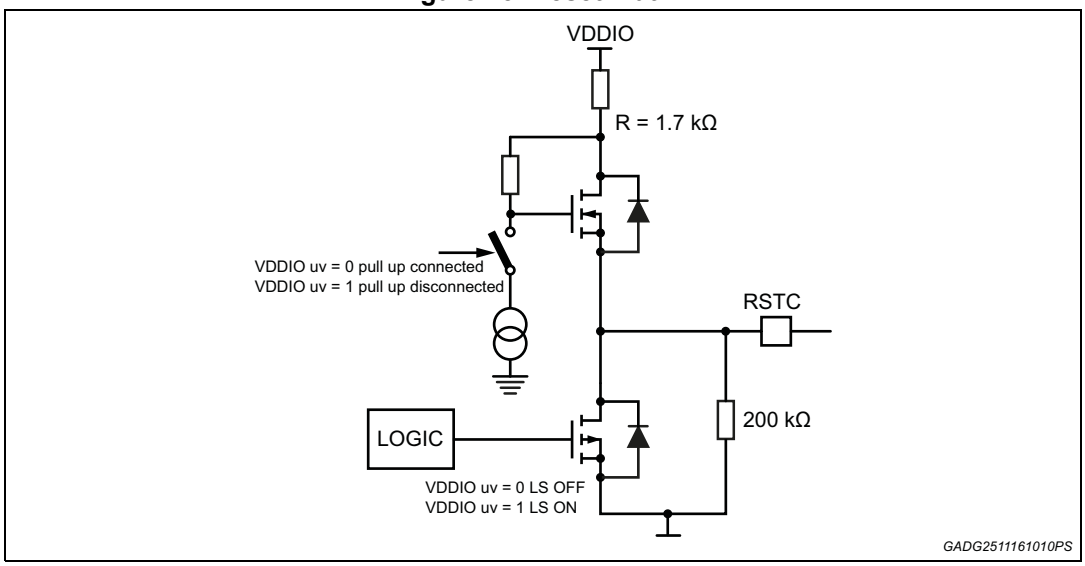
RSTN(OUT) and RSTN(IN) are recombined on the pad according to the scheme.

Figure 14. Reset circuit



The RSTN activates on the contributions specified by the reset matrix:

Figure 15. Reset matrix



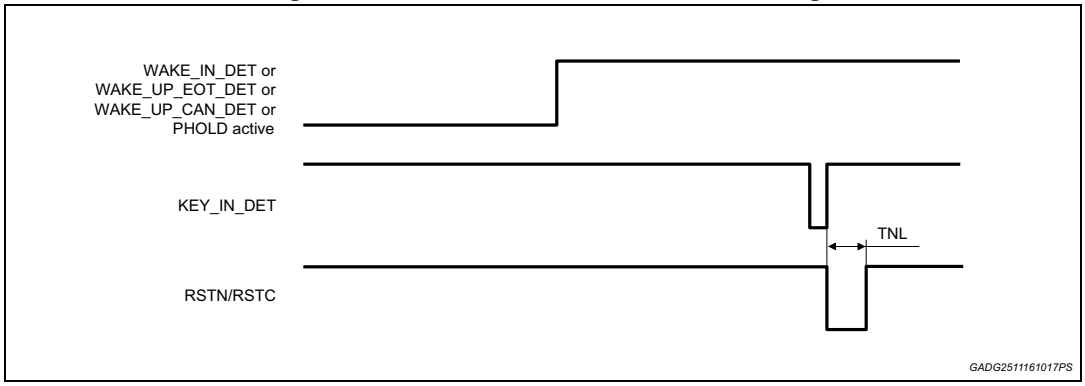
3.4.2 Smart Reset RSTC pin

The RSTC pin is an output active low. As output pin the Smart Reset circuit takes into account several events in the device in order to generate the proper reset signal at RST pin for the microcontroller and for portion of the internal logic as well.

The RSTC activates on the contributions specified by the reset matrix:

3.4.3 After run reset

Figure 16. RSTN/RSTC after run reset timing



As output:

4.8 ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 16. Smart reset circuit electrical characteristic table 1

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VUV_LO RSTN	Output low voltage	1 < VDD5 < VDD_UV	-	-	0.6	V	RSTN
VUV_LO RSTC	Output low voltage	1 < VDDIO< VDDIO_UV	-	-	0.6	V	RSTC
IUVres_max_RSTN	Input current	VDD5 = VDD_UV V_{UV_reset} = 0,6V	1	-	-	mA	RSTN
IUVres_max_RSTC	Input current	VDDIO= VDDIO_UV V_{UV_reset} = 0,6V	1	-	-	mA	RSTC

As input:

4.8 ≤ VB_IN ≤ 18V, 4.5 ≤ VDD_IO ≤ 5.5 V, T_j -40 to 175°C unless otherwise specified;

Table 17. Smart reset circuit electrical characteristic table 2

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RST_L	RST input low voltage	-	-0.3		1.1	V	RSTN
RST_H	RST Input high voltage	-	2.3		VDD_IO +0.3	V	RSTN
Trst_flt_RST	Reset RST filter time	Tested by scan	7.5	10	11.5	µs	RSTN

Table 17. Smart reset circuit electrical characteristic table 2 (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RRST_PU	RST pull up resistor + HS Ron	RSTN / RSTC pins to 0V	0.95	-	2.5	kΩ	RSTN RSTC
RRST_PD	RST pull down resistor	RSTN / RSTC pin to VDDIO	100	-	320	kΩ	RSTN RSTC
TNL RST	After run reset time	-	1.4	2	2.6	ms	RSTN RSTC
TWDA_RST	watchdog RST reset time	-	1.4	2	2.6	ms	RSTN RSTC
Td_UV_RST	Power on RST reset delay	-	17	-	30	ms	RSTN/RSTC
Tmsk_RST	Masking time on RST(IN) after RTN(OUT) is released.	-	95	100	105	µs	RSTN

3.5 Thermal shutdown

Table 18. Thermal shutdown

Block	Overtemperature flags																
	OVT[1]	*OVT[2]*	*OVT[3]*	*OVT[4]*	*OVT[5]*	*OVT[6]*	*OVT[7]*	*OVT[8] or OVT[9]*	*OVT[18] or OVT[19]*	*OVT[10]*	*OVT[11]*	*OVT[12]*	*OVT[13]*	*OVT[14]***	*OVT[15]*	*OVT[16]*	*OVT[17]*
REGULATOR BUCK	▲																▲
REGULATOR VDD5,																	▲
REGULATOR TRACK			▲														▲
DRIVER INJ1				▲													▲
DRIVER INJ2					▲												▲
DRIVER INJ3						▲											▲
DRIVER INJ4							▲										▲
DRIVER O2H1								▲									▲
DRIVER O2H2									▲								▲
DRIVER SOL1										▲							▲
DRIVER SOL2											▲						▲
DRIVER RLY[1:2]												▲					▲
DRIVER RLY[3:5]													▲				▲
DRIVER MRD														▲			▲
DRIVER STR[1:3]															▲		▲
DRIVER LED[1:2]																	▲
LIN																▲	▲
VRS																	▲

Legenda:

▲	Shutdown
<blank>	Not shutdown
OVT[1-16]	Dedicated temperature sensor for the power
OVT[3]	OVT[3] is used as a common thermal sensor for the three Tracking Regulators
OVT[17]	Central Temperature sensor
OVT[14]**	Over temperature protection MRD is available only when VB_IN is present.

4 Watchdog

4.1 Basic feature

L9788 has an internal query and answer (Q&A) watchdog with the aim of monitoring the correctness of microcontroller activity. Via MSC bus a WDA “question” shall be read from a MSC-WDA register. A correct response shall then be written back via MSC in a well defined timing. If response or timing is not correct, then the WDA error counter EC (or ERR_CNT) is increased. If the error counter is increased to values greater than 4, some output functions are shut off. If the error counter reaches values greater than 7 (overflow), then a RST reset may be generated if this is previously configured via MSC.

The first sequence of questions and responses starts from VDD5 higher than the UV threshold.

Other way round, with a RST event also the WDA output pin goes to low.

Note that after startup, reset or an RST_CNT overflow the initial value of the error counter is 6.

If WDA resets are enabled via MSC (*WDA_INIT CONFIG-REG 9_1 D3*): the number of RST events generated by an error counter overflow is limited by the reset counter *RST_CNT*. If *RST_CNT* reaches the value of 7, then RST resets via WDA are no longer generated.

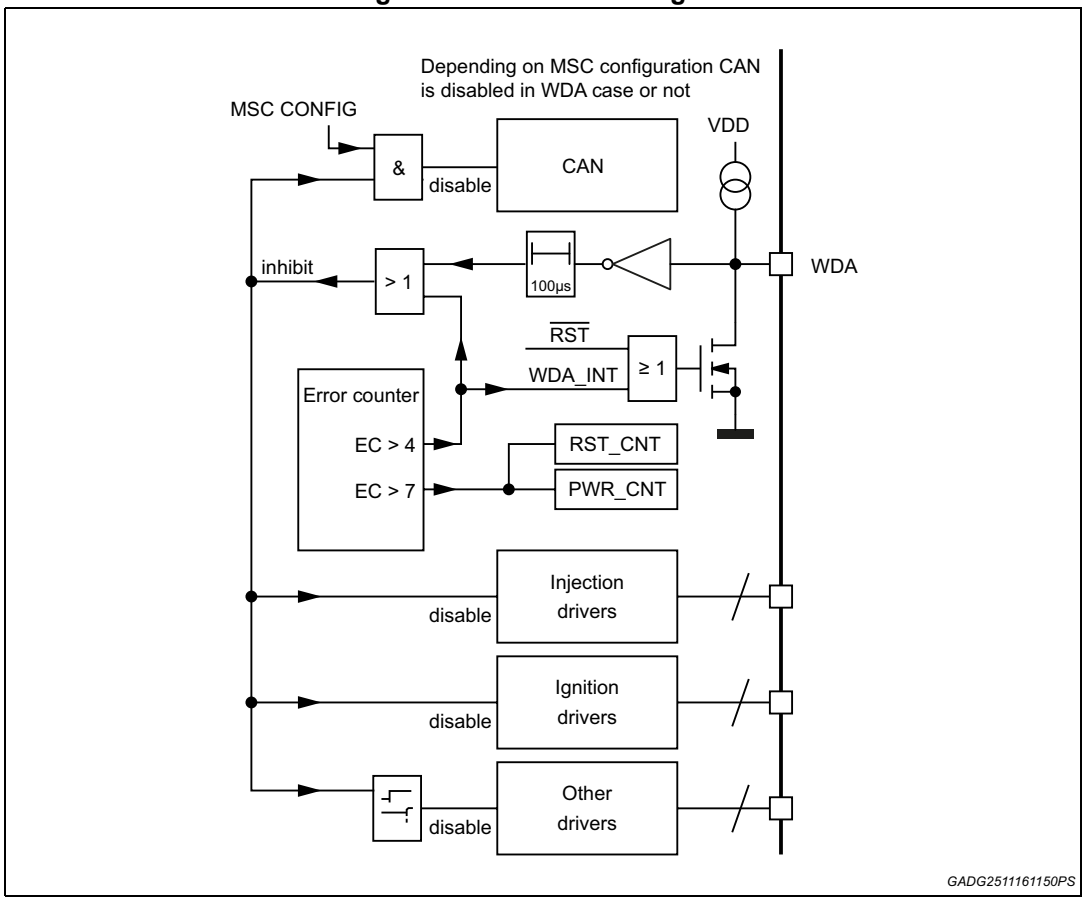
With each error counter overflow, the *PWR_CNT* counter is increased. If it reaches a value greater than 7, then the power latch mode is terminated.

Watchdog legenda:

ERR_CNT, EC	error 3-bit counter;
RST_CNT	reset 3-bit counter;
WDA_RST	internal reset generated by Watchdog;
PWR_CNT	power off 3-bit counter;
PWR_INT	internal signal indicating *PWR_CNT* overflow;
WDA	WDA open drain pin (low active);
WDA_INT	WDA internal signal, when high it drives WDA = low, when low it sets WDA= Hi-z;
Sequencer-run	current state of WDA when it is active.

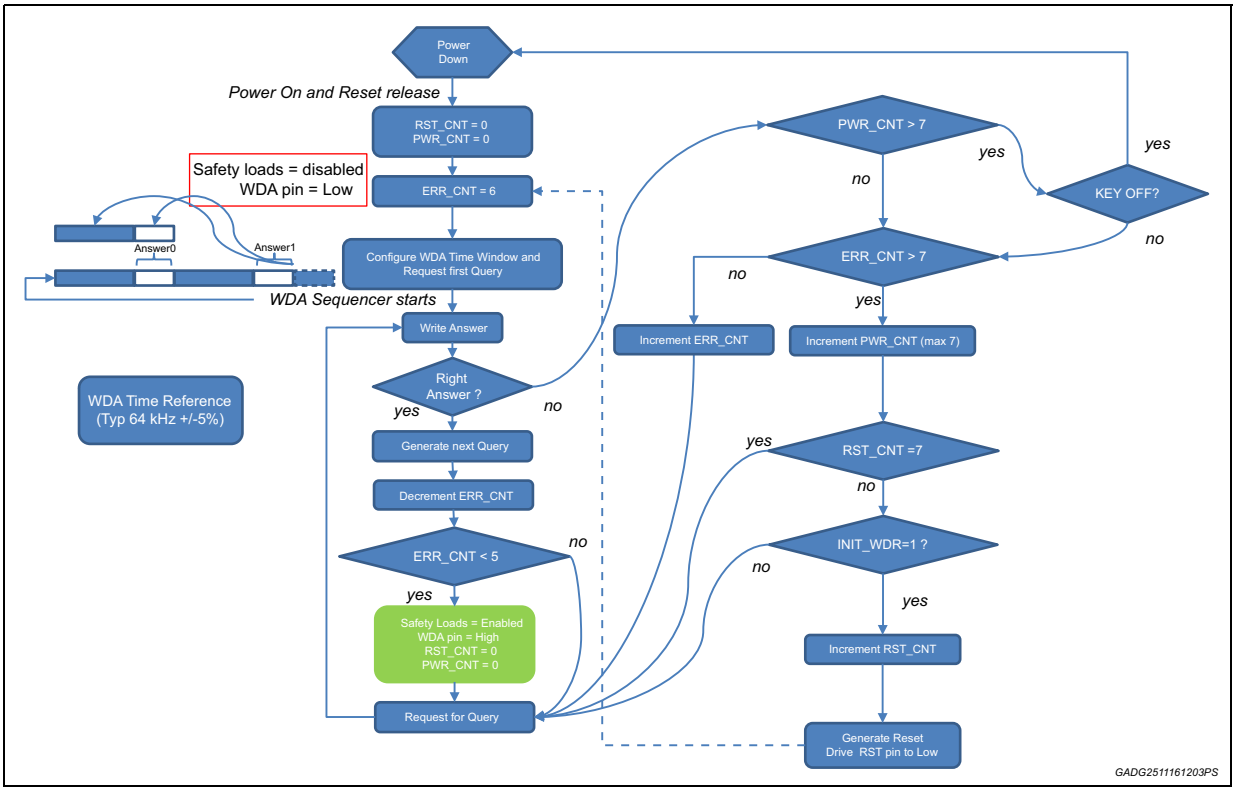
4.1.1 Monitoring module - WDA Functionality

Figure 17. WDA block diagram



Note: Delay-off function is not considered in this Block Diagram.

Figure 18. WDA state flow



Each time the watchdog error counter is EC > 7 counter *PWR_CNT* counter increases. When this counter is *PWR_CNT*=7 and a further error occurs, the power-latch will be terminated if KEY_IN is low. The *PWR_CNT*-counter is not cleared when EC <7. *PWR_CNT*-counter is cleared when EC < 5 or by RST_UV.

The monitoring module works independently of the controller functionality. The monitoring module generates various questions, which the controller must fetch and correctly respond to within a defined time window. The monitoring module checks whether the response is returned in a time window and if the response is fully correct.

The question is a 4-bit word. This 4-bit word can be fetched by the controller using a read access to register *WDA REQULO*. The monitoring module also calculates the expected correct response, which is compared to the actual response from the controller.

The response is a 32-bit word consisting of the 4 bytes *RESP_BYTE3, RESP_BYTE2, RESP_BYTE1* and *RESP_BYTE0*. The 4 bytes are sent to the monitoring module via MSC in the order *RESP_BYTE3 - RESP_BYTE2 - RESP_BYTE1 - RESP_BYTE0* using four times the command *WDA_RESP* - once for each answer byte.

The monitoring cycle phase is initialized by (the end of) writing of *RESP_BYTE0* (least significant response byte) or by a write access to the *RESPTIME* register. The cycle starts with a variable wait time (response time, set by register *RESPTIME*), followed by a fixed time window. When a monitoring cycle ends (the end of the fixed time window has been reached) a new monitoring cycle is started automatically.

A correct response within the time window (at a response time > 0 ms) decreases an ERROR COUNTER by one. An incorrect response, a response outside the time window or response time = 0 ms leads to the incrementing of the ERROR COUNTER by one.

"… within the time window" means that the end of writing the last answer byte - i.e. *RESP_BYTE0* - falls into the fixed time window mentioned above (see picture below).

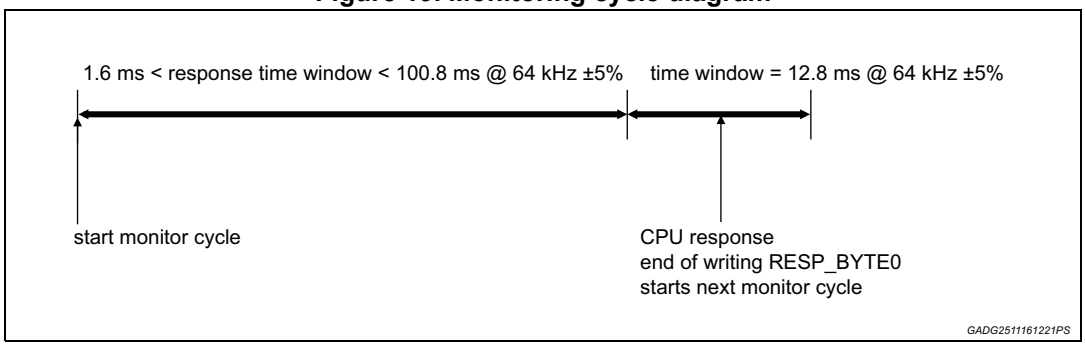
Except the last answer byte, the previous answer bytes may also be written earlier than the beginning of the fixed time window.

The question sequence is deterministic. A question will be repeated until it is answered correctly both in value and in time. Then the next question is placed in the sequence.

The ERROR COUNTER (EC) is a 3-bit counter. Various actions are activated depending on the value of the counter.

The result of the comparison of the controller response and the calculated correct response, as well as the next question, are available in registers *REQULO* after receiving the µC response (LSB of *RESP_BYTE0*) and can be read by the controller.

Figure 19. Monitoring cycle diagram



4.1.2 ERR CNT (EC) and reactions, PWR COUNTER (PWR_CNT) and generation of the monitoring module reset

Various actions are initiated for specific counter states of the *ERROR COUNTER* EC. The counter reset state is 6.

For *ERROR COUNTER* (EC) > 4, the open drain output WDA is pulled low (active).

Table 19. Error counter

ERR_CNT	0 … 4	5	6 … 7	Overflow *ERR_CNT > 7*
WDA	Hi-Z	Low	Low	Low
PWR_CNT	0	unchanged	unchanged	Incremented by 1
Internal *PWR_CNT* signal	Low (not active)	If *PWR_CNT* = 7 and *ERR_CNT* increase => High (active) Else unchanged	If *PWR_CNT* = 7 and ERR_CNT increase => High (active) Else unchanged	*PWR_CNT* < 7 Low (inactive) *PWR_CNT* 6->7 Low (inactive) *PWR_CNT* 7 -> 7 High (active)

If the ERROR COUNTER reaches the value “7” and a further error occurs the *PWR_CNT* is incremented by one during a sequencer-run.

The state "EC = 7 and a further error occurs" is also called ERROR COUNTER overflow ("EC" > 7).

The counter *PWR_CNT* is a 3 bit counter.

Behaviour of *PWR_CNT*:

- asynchronous reset to "000" with RST_UV
- synchronous reset to "000" IF (EC < 5)
- IF (PWR_CNT < 7) AND (sequencer-run AND "EC" > 7) THEN PWR_CNT = PWR_CNT + 1 ELSE unchanged.

The counter cannot be decremented and can be only reset to "000" by an active RST_UV signal (asynchronous) or <*WDA_INT*> = '0' (synchronous).The signal PWR_INT becomes active '1' when PWR_CNT = "111" and a further error is detected. When KEY_IN =0, the active PWR_INT signal causes a shut-down of the main relay and the voltage regulators. This function ensures a secure shutdown of the system in an error state of the µC in "power-latch". Signal PWR_INT is set to '0' again only when <*WDA_INT*> = '0'.

4.1.3 Generation of a monitoring module reset

The monitoring module may cause a reset at the pin [RSTN] named "monitoring module reset" in conjunction with the internal signal WDA_RST. The generation of a monitoring module reset depends on the state of the bit <*WDA_INT*>.

< *WDA_INT*> = '0' (reset state):

If < *WDA_INT*> = '0', the signal <*WDA_RST*> remains always inactive '0' and the monitoring module can never generate a reset. The error counter can only be decremented via correct responses. If < *WDA_INT*> = '0' the state of the reset counter <RST_CNT> remains unchanged when an ERROR COUNTER overflow occurs (description of the reset counter <RST_CNT> see below).

< *WDA_INT*> = '1':

If < *WDA_INT*> = '1', an ERROR COUNTER overflow activates a reset [RST] (signal <WDA_RST> becomes active). The signal <*WDA_RST*> becomes active (i.e. '1') due to an ERROR COUNTER overflow when the value of the 3 bit reset counter <*RST_CNT*(2-0)> is 0..6. If the value of <*RST_CNT*> = "111" and an ERROR COUNTER overflow occurs <*WDA_RST*> remains inactive (i.e. '0') and no reset is generated. The "reset counter" <*RST_CNT*> is incremented by one during a sequencer-run due to an ERROR COUNTER overflow when < *WDA_INT*> = '1' and <*RST_CNT*> is between 0 and 6. If <*RST_CNT*> = 7 and an ERROR COUNTER overflow occurs, the counter state remains 7. The counter can not be decremented and can only reset to zero by an active RST_UV signal. The occurrence of a monitoring module reset is indicated via the flag <*WDA_RST*> = '1'. Reading the flag via MSC clears it automatically. In effect maximum 7 monitoring module resets can be generated between 2 active RST_UV signal. (see also state table for < *WDA_INT*> = '1' below).The state of the "reset counter" <*RST_CNT*> can be read via MSC but cannot be changed.

Table 20. Internal states for WDA_INIT=1

RST_CNT old value	EC>7 and sequencer-run	RST_CNT new value	WDA_RST
000 … 111	False	= RST_CNT old	0, no monitoring module reset
000 … 110	True	= RST_CNT old + 1	1, monitoring module reset generated
111	True	= 111	0, no monitoring module reset

4.1.4 Question generation

The generation of the 4-bit question (*REQU[3-0]*) is realized as in the table below. The 4-bit counter only changes to the next state during the sequencer-run when the previous question has been answered correctly in value and in time. The state is changed by a sequencer-run because of a write-access to the RESPTIME register or the expiration of the time window.

When RST_UV is active the state is set to 0000b

4.1.5 Response comparison

The 2-bit counter <*RESP_CNT (1-0)*> counts the received bytes of the 32-bit response and controls the generation of the expected response. Its default value is "11" (corresponds to "waiting for *RESP_BYTE3*").

The <RESP_ERR> flag is set '1' when a response byte is incorrect. The flag remains '0' if the 32-bit response is correct. The ERROR COUNTER is updated with the flag. The default state of the flag is '0'.

The 2-bit counter <*RESP_CNT (1-0)*> and the <*RESP_ERR*> flag are reset to their corresponding default values at a sequencer-run. The reset condition of the counter <*RESP_CNT (1-0)*> and the <*RESP_ERR*> flag are the corresponding default states.

Procedure of the sequential response comparison:

<*RESP_CNT (1-0)*> = "11": switch the expected response for *RESP_BYTE3* to the comparator

Write access: *RESP_BYTE3*

Set <*RESP_CNT*> to "10", update <*RESP_ERR*> flag

<*RESP_CNT (1-0)*> = "10": switch the expected response for *RESP_BYTE2* to the comparator

Write access: *RESP_BYTE2*

set <*RESP_CNT*> to "01", update <*RESP_ERR*> flag

<*RESP_CNT (1-0)*> = "01": switch the expected response for *RESP_BYTE1* to the comparator

Write access: *RESP_BYTE1*

set <*RESP_CNT*> to "00", update <*RESP_ERR*> flag

<*RESP_CNT (1-0)*> = "00": switch the expected response for *RESP_BYTE0* to the comparator

"update <*RESP_ERR*> flag" previously described means that it sets <*RESP_ERR*> flag to 1 if a response byte is incorrect. Once <*RESP_ERR*> flag is set to 1 it maintains its value until next sequencer run.

Write access: *RESP_BYTE0*

Start sequencer (SEQU_START signal), set <*RESP_CNT*> to "11", update <*RESP_ERR*> flag, update ERROR COUNTER

Sequencer clears <*RESP_ERR*> flag to '0

SEQU_START = (RESP_CNT1=0) AND RESP_CNT0=0) AND "response byte write"

Table 21. Question and answer

question REQU (3-0)	RESP_BYTE3	RESP_BYTE2	RESP_BYTE1	RESP_BYTE0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

4.1.6 Reset behaviour

All monitoring module registers are reset by RST_UV. The following monitoring module components are also reset by RST_PRL (internal partial reset).

Table 22. Watchdog reset behaviour

Component	Reset Condition
ERROR COUNTER	110b
Register for “EC>7”	‘0’
Register RESPTIME	Maximum value:0011 1111b

RST_PRL is active when at least one of the following signals is active: RSTN or SW_RST.

4.1.7 Access during a sequencer-run

A sequencer-run (which means the same as a monitoring cycle) is initiated by the writing of a response (i.e. all answer bytes <*RESP_BYTE3..0*>) or a write to <*RESPTIME*> or by reaching "end of time window". It's not interrupted by a new access, i.e. the monitoring module completes the action already started:

- A sequencer-run was initiated by a "response write": The sequencer completes its task with the data of the previous access and the new data are ignored.
- A sequencer-run was initiated by a "response-time write": The sequencer uses the response-time of the previous access, the error counter is correspondingly incremented by one and the <*CHRT*> bit (REQUHI register) is set and the new data are ignored. <*CHRT*> will be reset by reading and by the next start of a sequencer run (not reset by the sequencer run that is started by a "response-time write")
- A sequencer-run was initiated by "end of time window": The sequencer finishes the started run, the error counter is incremented by one and the new data are ignored.

The writing of a response-time during a sequencer-run will not set the <*CHRT*> bit (REQUHI register). The new response-time value is also not accepted.

At the end of the sequencer run *W_RESP* bit is set to 0 if the response is correct, it is set to 1 if the response is incorrect.

4.1.8 Clock and time references

The monitoring module works independently by the micro-controller clock so that it can monitor the timing of the micro-controller.

This oscillator is integrated in the U-chip and it provides a clock CLK1 for the monitoring module.

Clocked with CLK1, a divider generates the base time of 1.6 ms @ 64 kHz for the response-time and 8*1.6 ms = 12.8 ms @ 64 kHz for the fixed time window. Accuracy of CLK1 is ± 5%.

The response-time is adjustable by the controller in the range 0ms to about 100ms (register *RESPTIME*).

The response-time can be calculated with the equation

Response_Time = *RESPTIME [5:0]*) *1.6 ms

If 39 kHz clock is selected by wda_win_sel configuration bit, the base time changes becoming 2.6ms @ 39 kHz. This implies the change of all related timing values: 8*2.6 ms = 20.8 ms @ 39 kHz for the fixed time window and response time becomes RESPTIME [5:0] *2.6 ms.

The *WDA_RESPTIME (CONFIG_REG9_0)* register is set to '0011 1111'b after a reset. The ERROR COUNTER is incremented by one if the controller changes the response-time. If the response-time is set to 0 ms, then the ERROR COUNTER is incremented by one even if a correct response is received within the time window. The maximum error reaction time is given by: maximum response-time, response at the end of a time-window and ERROR COUNTER 0 Is 5 *(100.8 ms + 12.8 ms) = 568 ms.

In order to assure correct response write, there must be a minimum distance between 2 consecutive writes equal to 5us, this time does not depend on *WDA_WIN_SEL (CONFIG_REG9_1 D2)*.

Note: These clock-tolerances have to be taken into account additionally.

As output (open drain):

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 23. WDA circuit electrical characteristic

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
WDA_UV_LO	Output low voltage	1 < VDD5 < VDD_UV R_{reset} = 4.7 kΩ	-	-	0.6	V	WDA
WDA_IUVres_max	Input current	VDD5 = VDD_UV V_{UV_reset} = 0.6 V	5	-	-	mA	WDA
$WDA\_Ilk_{UV\_reset}$	Input leakage current	V_{UV_reset}> VDD_UV	-	-	1	µA	WDA

As input:

5.5 V ≤ VB_IN ≤ 18V, 4.75 V ≤ VDD_IO ≤ 5.25 V T_j -40 to 175 °C unless otherwise specified;

Table 24. WDA reset circuit electrical characteristic

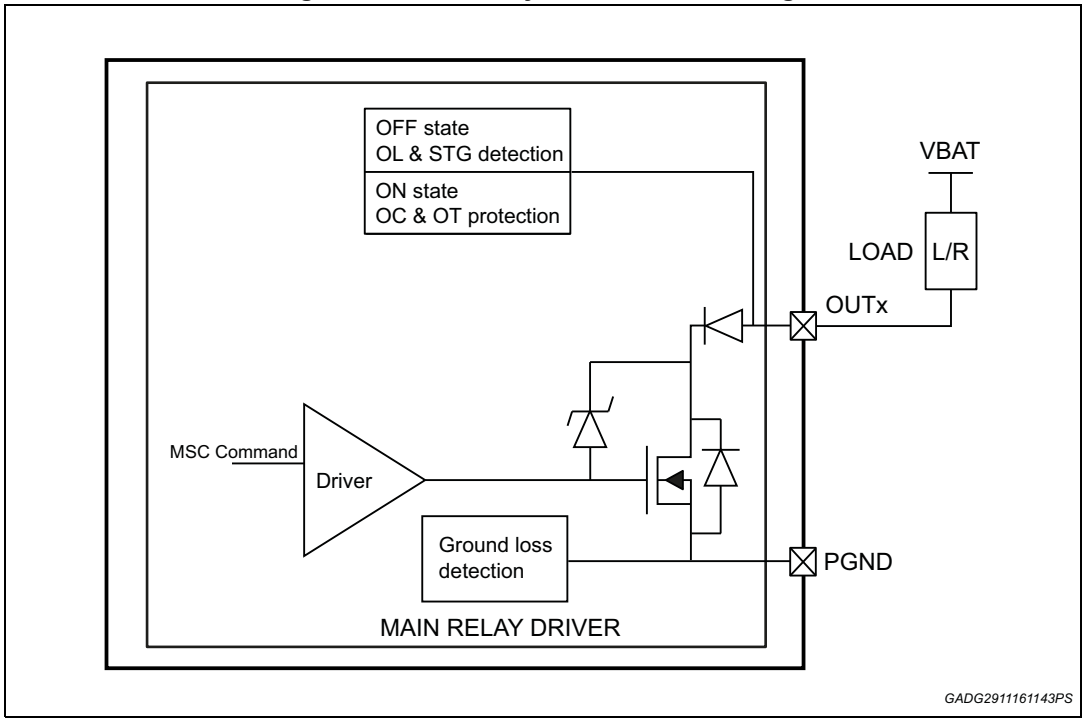
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
WDA_RST_L	WDA input low voltage	-	-0.3	-	1.1	V	WDA
WDA_RST_H	WDA input high voltage	-	2.3	-	VDD_IO +0.3	V	WDA
WDA_Trst_flt	WDA Reset filter time	Tested by scan	-	10	-	µs	WDA
-	WDA pull up external resistor	Application note, parameter not tested	50	-	250	kΩ	WDA

5 Main relay driver (low-side driver)

This driver is used to drive the main relay only.

The on/off status of the driver depends on the following sources of power on: KEY_IN WK_IN WAKE_UP_TIMER POWER_HOLD (MSC), CAN see *Table 20*. The Main Relay Driver can be also switched on/off by a MSC command protected by lock. This is intended to use in the permanent battery supply scheme only if power up was done by wk_in/EOT/ CAN according to *Table 25*. MSC micro commands protected by lock are available for fast on and off diagnosis.

Figure 20. Main relay low-side driver stage



The low-side (main relay) can work down to VB_IN= VOFF_VB_IN, during cold crank conditions. The driver has integrated diagnosis, with over-current and overtemperature protection circuit during the driver on. The driver turn on/off slew-rate is internally controlled.

The Main Relay Driver on/off status is controlled by the power up/down modes or by the msc commands according to *Table 25*.

These notes are linked to *Table 25*

1. The battery status can be determined at power up only.
2. The key detection switches on always MRD and does not determine the battery status.
3. Once the key detection has switched on MRD, MRD is switched off by one of these events:
   – Clearing of all detections and phold not active (power down),
   – Watchdog power counter timeout,
   – *MSC MRD OFF* command when phold is active (all detections cleared).
4. The msc_enable_driver command or trans_f error or clock monitor error does not affect the MRD even if it is controlled by MSC commands.

5.1 ON state diagnostic

Table 25. ON state diagnostic

-	-		MRD	MSC command		OVC	OVT
				ON	OFF		
KEY_DET=1	Permanent Supply		ON	Y	N	restart by MSC scenario 19 (see *Figure 109*)	Auto restart without limit of number scenario 21 (see *Figure 111*)
	Non Permanent Supply	Before Power up	ON	N/A	N/A	Auto restart without limit of number scenario 12/13 (see *Figure 102*)	N/A
		After Power up	ON	N	N	Auto restart without limit of number scenario 14/27/15 (see *Figure 102*, *104* and *105*)	Auto restart without limit of number scenario 26/27 (see *Figure 100* and *Figure 104*)
WAKE_IN_DET / WAKE_EOT_DET / WAKE_CAN_DET =1 *KEY_DET=0*	Permanent Supply		OFF	Y	Y	restart by MSC scenario 19 (see *Figure 109*)	Auto restart without limit of number scenario 21 (see *Figure 111*)
	Non Permanent Supply	Before Power up	ON	N/A	N/A	Auto restart for MRD_EN_TIMEOUT min 331 ms typ 500 ms max 650 ms Scenario 17/18 (see *Figure 102* and *107*)	N/A
		After Power up	ON	N	N	No restart scenario 31 (see *Figure 108*)	No restart scenario 28 (see *Figure 115*)

Table 25. ON state diagnostic (continued)

-	-		MRD	MSC command		OVC	OVT
				ON	OFF		
PHOLD_EN =1 KEY_DET/WAKE_IN_DET/ WAKE_EOT_DET/ WAKE_CAN_DET = 0	Permanent Supply		Keep the status	Y	Y	restart by MSC scenario 20 (see *Figure 110*)	Auto restart without limit of number scenario 29 (see *Figure 112*)
	Non Permanent Supply	Before Power up	N/A	N/A	N/A	N/A	N/A
		After Power up	Keep the status	N	Y	No restart scenario 16 (see *Figure 105*)	No restart scenario 30 (see *Figure 116*)

5.1.1 Overcurrent protection

When overcurrent fault is detected the Main Relay Driver MRD is switched off.

The MRD is automatically restarted every T_res if KEY_IN is still active in not permanent battery supply scheme. No restart is done in permanent battery supply schemes.

In non permanent supply system waked up by WK_IN or WAKE_UP_EOT or WAKE_UP_CAN, MRD OVC retry is just done before VB_IN present. No restart of MRD after VB_IN power loss due to OVC, unless a next rising edge at WK_IN or WAKE_UP_EOT or WAKE_UP_CAN.

The retry is done for MRD_EN_TIMEOUT from the detection of WK_IN or WAKE_UP_EOT or WAKE_UP_CAN.

In permanent battery supply scheme in case of power up from WK_IN or WAKE_UP_TIMER or WAKE_UP_CAN the MRD is not switched on at power up. In case of permanent battery supply scheme and OVC protection is activated the driver is restarted by a positive transition on the MSC *MRD_ON* command. It is not restarted by MSC reading.

5.1.2 Thermal protection

The overtemperature fault is detected only when VB_IN is present and the logic is out of power on reset, so when the device is in ON state.

When overtemperature fault is detected the Main Relay Driver is switched off. In not permanent battery supply schemes the switching off of the Main Relay Driver produces a power down. If KEY is still active, a new power up sequence is started. If wake up from WK_IN or EOT or CAN, or *PHOLD_EN* =1, no power up sequence is started. In permanent battery supply schemes the switching off of the Main Relay Driver does not produce a power down. The MRD is switched on again when temperature decreases to T_SD_LOW.

5.2 OFF state diagnostic

The OFF diagnosis is performed only in the supply scheme with battery permanently connected.

The off diagnosis is the same as other low-side drivers.

There is a bit *Ipupd_EN* which is controlled by a MSC bit (CONFIG_REG2 D6), it is used by external µController if it is needed to switch on/off both pull up and pull down diagnosis current.

There is a bit *Ipupd_MODE* which is controlled by a MSC bit(CONFIG_REG2 D7), it is used by external uController if it is needed to switch on/off the bigger diagnosis current (I_LS_PU1) in fast mode. It is possible to define the maximum number of retry in case of OVC after wake up by KEY. It can be done setting *KEY_OC_RETRY_MAX_EN* bit in CONFIG-REG 20.

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 26. Main relay low-side driver electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Main relay							
MRD_out_voltage_low	Low-side out voltage	VB_IN = 3.9 V I_{load} = 0.1 A	-	-	0.9	V	MRD
MRD_out_voltage_nom	Low-side out voltage	5.5 V < VB_IN < 18 V I_{load} = 0.3 A	-	-	1.35	V	MRD
MRD_lkg	Output leakage current	Output disabled, diagnostic off	-10	-	+10	µA	MRD
rev_MRD	-	Reverse battery	-	-	-16	V	MRD
I_load	Output current	Application Info	-	-	0.5	A	MRD
SR_ON_20	Voltage slew ON State	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 20 Ω C_{load} = 10 nF	2	-	6	V/µs	MRD
SR_OFF_20	Voltage slew OFF State	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 20 Ω C_{load} = 10 nF	2	-	6	V/µs	MRD
Ton_MRD_20	Propagation Delay from Chip_EN rising edge to 80% output MRD voltage	VB_IN = 14 V, R_{load} = 20 Ω C_{load} = 10 nF	-	-	10	µs	MRD

Table 26. Main relay low-side driver electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Toff_MRD_20	Propagation Delay from Chip_EN falling edge to 20% output MRD voltage	VB_IN=14V, R_{load} = 20 Ω C_{load} = 10 nF	-	-	10	µs	MRD
Vclamp_MRD	MRD clamping Voltage	I_{load} = 0.3 A	48		55	V	MRD
Vclamp_MRD_high_curr	MRD clamping Voltage	I_{load} = 1 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	48	-	55	V	MRD
IOVC_MRD	Over current driver threshold	-	1	-	2	A	MRD
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	MRD
TfT_Res	Self retry time after OVC with KEY_IN on or WK_IN active or WKE_UP_EOT active	Guaranteed by scan	15.2	16	16.8	ms	MRD
NRes_NN	Maximum number of retry when KEY_OC_RETRY _MAX_EN=1	Guaranteed by scan	-	32	-	-	MRD
T_SD_HIGH	Temperature shut down	-	185		200	°C	MRD
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	MRD
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	MRD
tmsd_pre_an	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	MRD
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	30	-	-	µs	MRD
OFF state diagnostic							
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9	-	VOUTOPEN -190mV	V	MRD

Table 26. Main relay low-side driver electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUTOPEN +160 mV	-	3.0	V	MRD
VOUTOPEN	Open load output voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	MRD
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”1”	2.5	3.6	4.7	mA	MRD
I_LS_PU2	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”0”	40	70	100	µA	MRD
I_LS_PD1	Diagnostic pull down current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB	60	85	110	µA	MRD
Tflt_diagoff1	DIAG Filter time	Filter Mode=0	75	100	125	µs	MRD
Tflt_diagoff2	DIAG Filter time	Filter Mode=1	450	600	750	µs	MRD
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10 nF) Filter Mode = 0	175	-	-	µs	MRD
-	Fast OFF diagnostic ON→OFF→ON	Filter Mode = 0	175	200	240	µs	MRD
-	Fast ON diagnostic OFF→ON→OFF	-	65	-	90	µs	MRD
Driver Reliability Data							
EnergyRep MRD	Energy Repetitive Pulses	I_OT_n = 0.3 A Freq = 1 Hz ; 4 Miopulses T_j =150 °C	-	-	6.5	mJ	MRD

5.3 Error handling

The Main Relay Driver follows the same error handling table as other low-side drivers.

6 Multi-voltage regulator supplies

The chip has one pre-boost regulator and one pre-buck regulator, which will supply a 5 V regulator with external MOS. Three 5 V tracking regulators are included. One charge pump is used for HS channel and by the 5 V linear regulator to drive the external MOS. See the diagram in *Figure 21*. The chip becomes to be supplied and the regulators are enabled in the sequence: VB_in grows till is higher than VB_IN_uv threshold, then internal 3V3 supply, charge pump and buck, pre-boost regulator, 5 V linear regulator, 5 V tracking regulator 1, 2 and 3 are switched on. Then the power on reset is released and the chip is working.

Figure 21. Power supply block diagram with pre-boost regulator and MRD

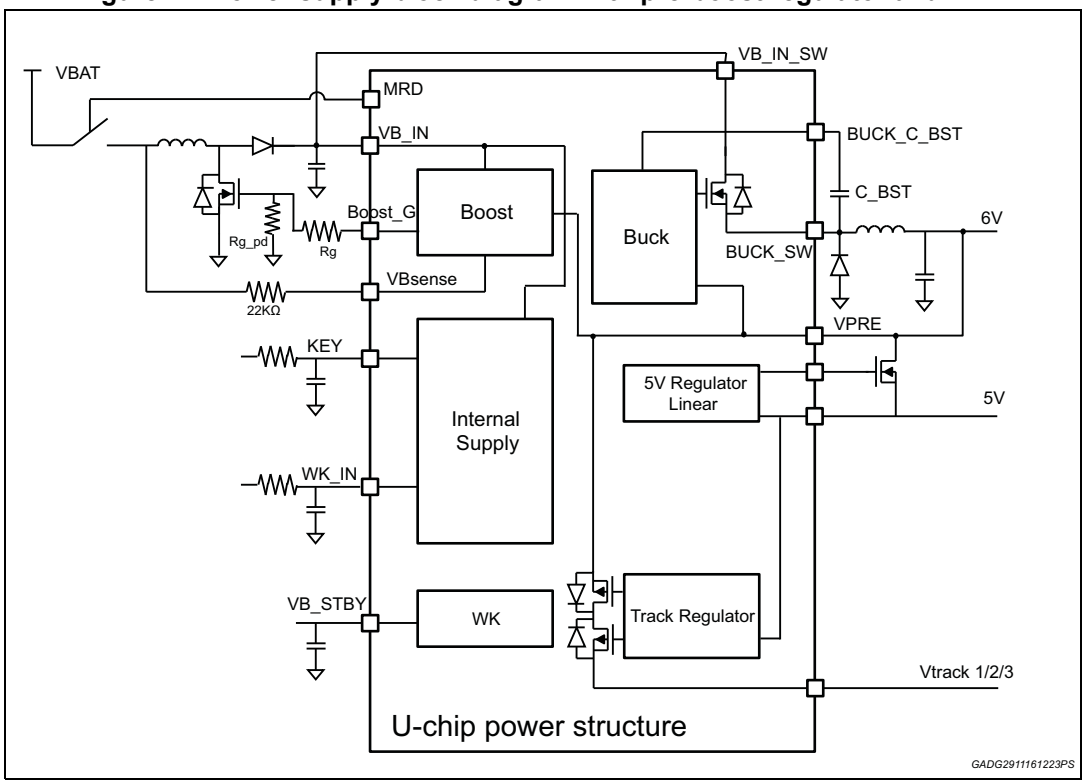
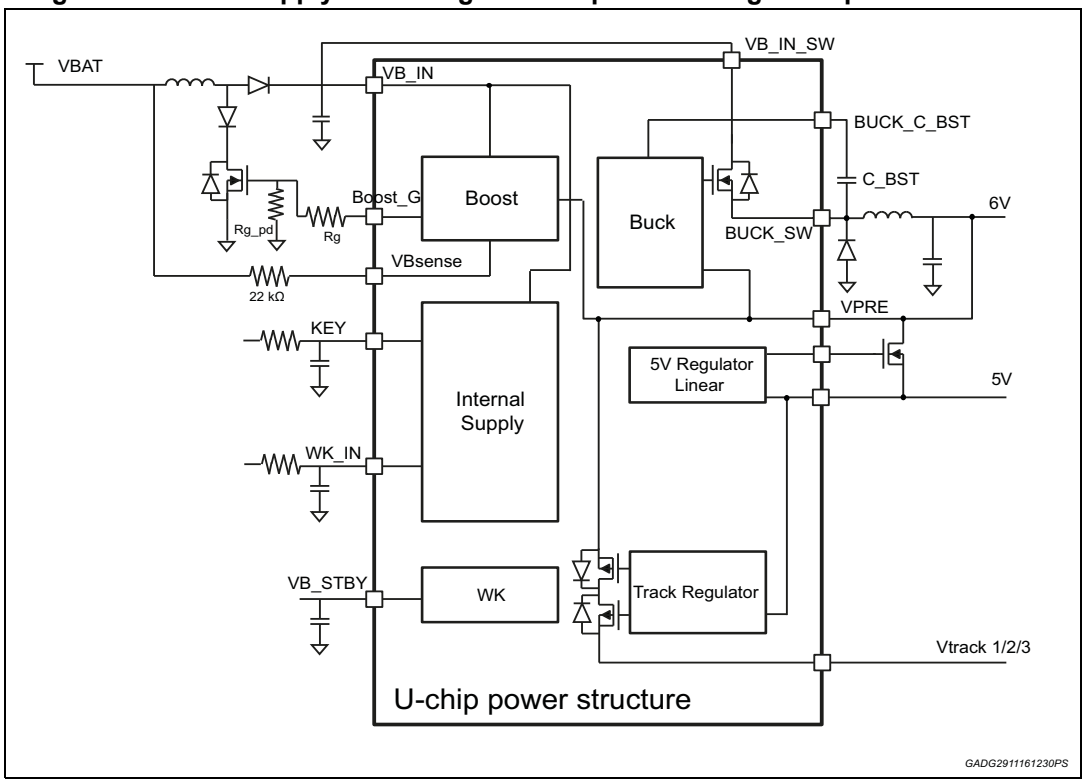


Figure 22. Power supply block diagram with pre-boost regulator permanent VBAT



The pre-boost regulator is an optional choice. It can be disabled (BOOST_EN (CONFIG-REG 1 D5) in case battery voltage is high enough in cranking phase to supply the pre-buck regulator. See the diagram in *Figure 23*

Figure 23. Power supply block diagram with charge pump without pre-boost

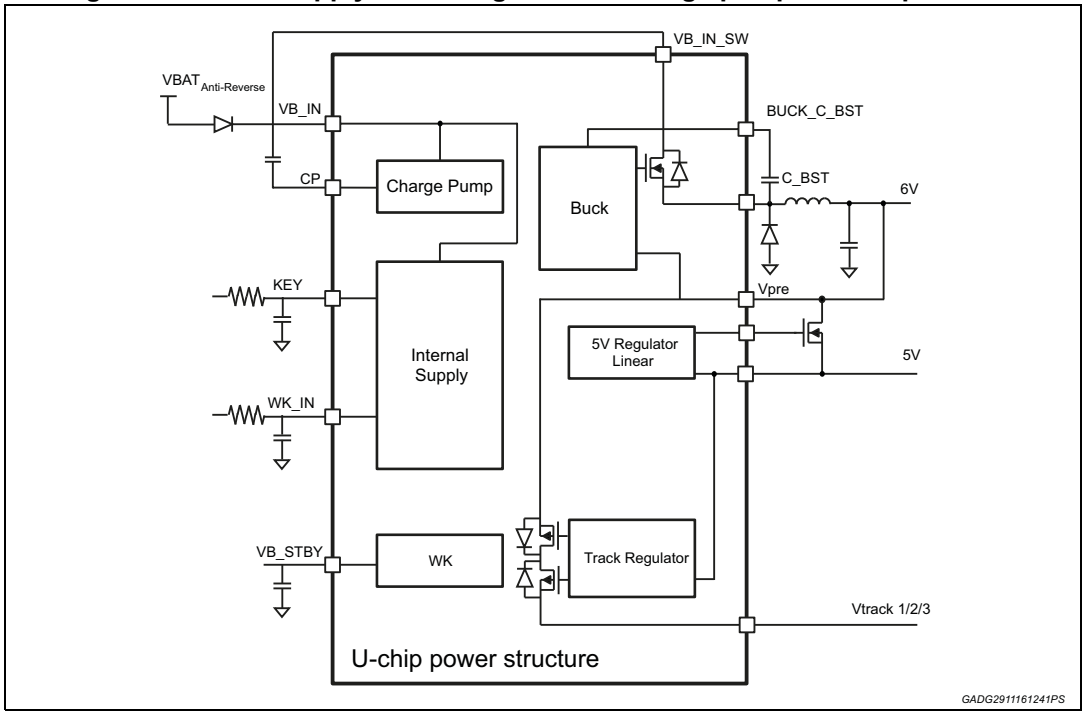
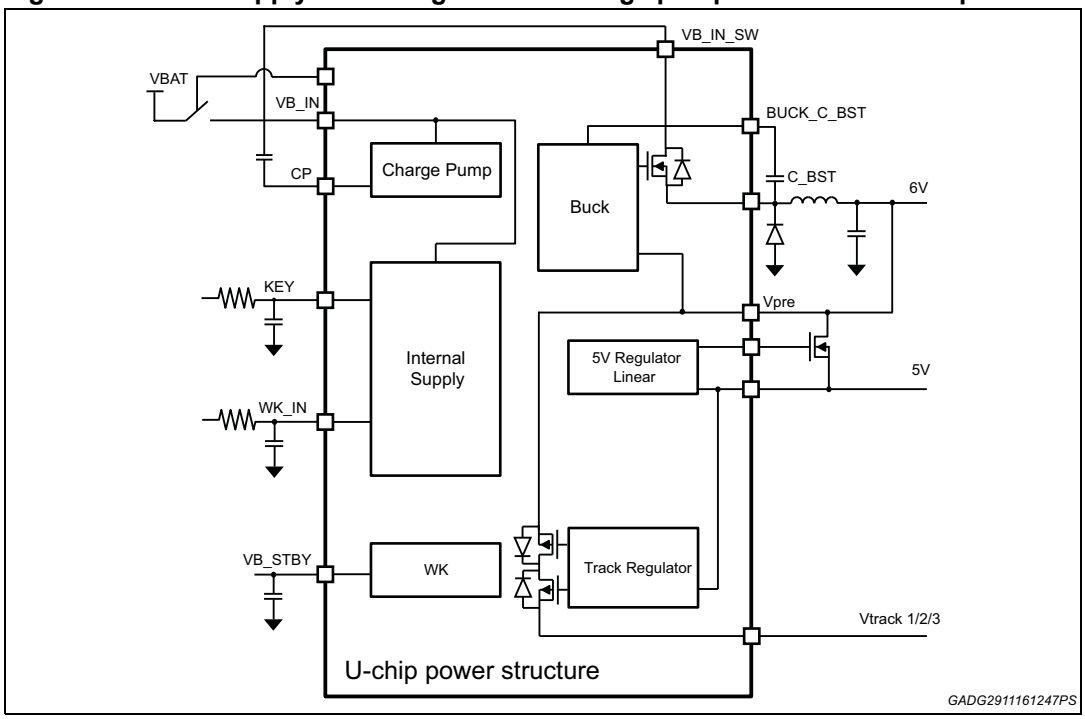


Figure 24. Power supply block diagram with charge pump and MRD without pre-boost



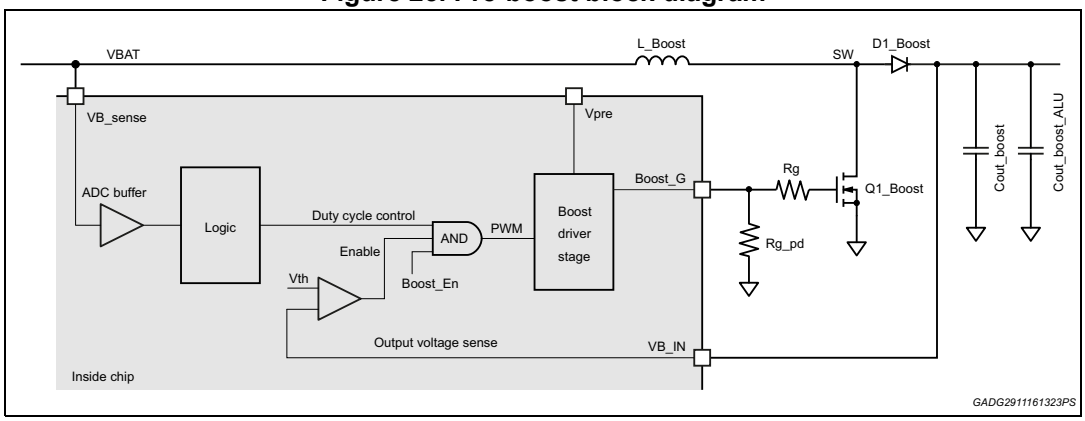
6.1 Pre-boost regulator

The boost regulator will provide a higher voltage than battery to the buck regulator when battery voltage is too low to maintain 5 V regulator out of reset conditions. Once the output of the pre-boost is higher than VB_IN_th (typ 8.5 V), the pre-boost will stop working.

The boost is disabled at the beginning of the power down sequence. When *Boost_EN* (CONFIG_REG 1 D5) = 0 the internal driver keeps OFF the external MOS.

The parameters of Pre-boost regulator can be guaranteed when Vbat goes down to 3.0 V during cranking phase. The block diagram of the pre-boost is *Figure 25*.

Figure 25. Pre-boost block diagram



3.0 V ≤ VBAT(*) < 18 V, T_j -40 to 175 °C unless otherwise specified.

Note: (*)VBAT is the battery line of Figure 25 in front of the limiting 22 kΩ resistor (not shown in the figure).

Table 27. Pre-boost regulator output electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VB_IN_th	BOOST enable/disable threshold	When VB_IN < VB_IN_TH, the boost starts for time (t_{ON}). When VB_IN ≥ VB_IN_TH, Boost is disabled after t_{ON} is completed. t_{ON} depends on different duty cycle	8.07	8.5	8.93	V	VB_IN
tdBOOST_EN	BOOST Enable/disable comparator delay time	-	0.19	-	2	µs	VB_IN
Fsw_BOOST	Switching frequency	43 cycles of 15 MHz main clk, Guaranteed by SCAN	334	352	370	kHz	VB_IN
Boost_DC1	Boost Duty cycle 1	0V < VBAT_SENSE < Vcomp_th1 33 out of 43 cycles of 15MHz main clk (100% DC is 43 clk cycles) Guaranteed by SCAN	-	76.74	-	%	VB_IN
Vcomp_th1	VBAT_SENSE comparator threshold 1	-	3.95	4.15	4.35	V	VBAT_SENSE
Boost_DC2	Boost Duty cycle 2	Vcomp_th1 < VBAT_SENSE < Vcomp_th2 25 out of 43 clk cycles Guaranteed by SCAN	-	58	-	%	VB_IN
Vcomp_th2	VBAT_SENSE comparator threshold 2	-	5	5.36	5.7	V	VBAT_SENSE
Boost_DC3	Boost Duty cycle 3	Vcomp_th2 < VBAT_SENSE < Vcomp_th3 18 out of 43 clk cycles Guaranteed by SCAN	-	41.86	-	%	VB_IN
Vcomp_th3	VBAT_SENSE comparator threshold 3	-	6.25	6.6	6.95	V	VBAT_SENSE

Table 27. Pre-boost regulator output electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Boost_DC4	Boost Duty cycle 4	Vcomp_th3 < VBAT_SENSE < Vcomp_th4 10 out of 43 clk cycles Guaranteed by SCAN	-	23.85	-	%	VB_IN
Vcomp_th4	VBAT_SENSE comparator threshold 4	-	7.4	7.8	8.2	V	VBAT_SENSE
Boost_DC5	Boost Duty cycle 5	Vcomp_th4 < VBAT_SENSE 4 out of 43 clk cycles Guaranteed by SCAN	-	9.3	-	%	VB_IN
tdBAT_SENS	VBAT_SENSE comparators delay time	Vcomp_th1/2/3/4 comparators	0.19	-	2	µs	VBAT_SENSE
IBOOST_LS_sink	LS driver sink current	BOOST_G = 6 V	30	50	70	mA	BOOST_G
IBOOST_HS_source	HS driver source current	BOOST_G = 0 V	30	50	70	mA	BOOST_G
IBOOST_LS_sink	LS driver sink current	BOOST_G = 0.5 V	15	-	43	mA	BOOST_G
IBOOST_HS_source	HS driver source current	BOOST_G = 5.5 V	10	-	43	mA	BOOST_G
BOOST_G_Ileak	Leakage current	From 0 V to max pin voltage	-	-	1.2	µA	BOOST_G
I_VBAT_Sense_stby	Current leakage on VBAT_sense pin in st-by	-	-	-	1	µA	VBAT_SENSE
I_VBAT_Sense	Pull down current on VBAT_sense operative mode	-	-	-	100	µA	VBAT_SENSE
R_VBAT_sense	Pull-down resistor from VBAT_sense to GND	-	438	880	1320	kΩ	VBAT_SENSE
R1_VBAT_sense	Resistor divider string element	Design info, not tested	311	622	933	kΩ	-
R2_VBAT_sense	Resistor divider string element	Design info, not tested	28.75	57.5	86.25	kΩ	-

Table 27. Pre-boost regulator output electrical characteristics (continued)

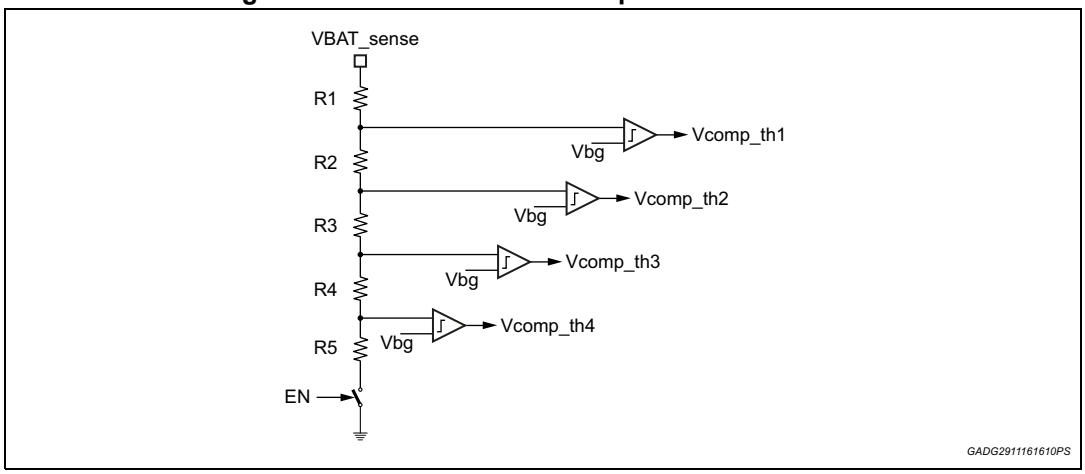
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
R3_VBAT_sense	Resistor divider string element	Design info, not tested	18.15	36.3	54.45	kΩ	-
R4_VBAT_sense	Resistor divider string element	Design info, not tested	12.5	25	37.5	kΩ	-
R5_VBAT_sense	Resistor divider string element	Design info, not tested	67.5	135	202.5	kΩ	-

Boost application information table:

Table 28. Pre-boost regulator external components electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note	Pin
C_{OUT_BOOST}	Capacitance at VB_IN	36	40	150	µF	Min 4*10 µF, 10%,25 V, X7R, 1206, CER CAP;	VB_IN
$C_{OUT\_BOOST\_ALU}$	Option ALU Capacitance at VB_IN	0	330	470	µF	ALU 35 V ESR 10 mΩ--3 Ω¸ 330 µF, 20%, 25 V, SMD,AL,ELEC CAP	VB_IN
VBoost_ripple	-	-	-	1.2 1.1 1.0 0.8	Vpp	triangular ripple @ 10 kHz and 25 kHz @ 50 kHz @ 100 kHz @ 350 kHz. All characteristics of all blocks supplied by VB_IN guaranteed	VB_IN
IBOOST	Load current at VB_IN	0.05	-	1.8	A	-	VB_IN
Q1_Boost	-	-	-	-	-	Choice: STD20NF06L	VB_IN
D1_Boost	-	-	-	-	-	Choice: STPS10H100C	VB_IN
L_boost	BOOST inductance	0.8	1	1.2	µH	ESR = 10 mΩ	VB_IN
L_boost1	BOOST inductance	-	2.5	-	µH	ESR = 25 mΩ, I_{sat} = 23 A	VB_IN
L_boost1	BOOST inductance	-	3.3	-	µH	-	VB_IN
Rsense	Resistor for VB_sense pin protection	10	22	30	kΩ	-	VBAT_Sense
Rg	-	-	2.2	-	Ω	-	BOOST_G
Rg_pd	-	-	150	-	kΩ	-	BOOST_G

Figure 26. Boost threshold comparator's schematic



6.2 Pre-buck regulator with internal MOS

Vpre features:

- 6 V regulated output voltage (VPRE);
- 1.6 A maximum output current;
- PWM block (ramp generator, comparator and main latch) with one fixed PWM frequency (Fsw_vpre);
- Internal error amplifier;
- Internal Power FET including Bootstrap;
- dV/dt Control on gate drivers to fulfill EMC requirements;
- Maximum Duty cycle 100%, to allow to charge Bootstrap capacitor;
- Protection by over temperature;
- Soft Start.

The Vpre regulator is a buck regulator which supplies Pre-boost driver/VDD5/Vtrack1.2.3. When the OV of VB_IN is detected, the Vpre(Buck) will be switched off. This function is selectable by a dedicated MSC bit (*VB_IN_OV_RST_EN* in CONFIG_REG12). A bit is also available (*BUCK_SLOW_SR* in CONFIG_REG 21) in order to select slew rate for output voltage; the default value corresponds to fast slew rate, slow slew rate helps to improve emission performance

The Vpre regulator includes a soft start. Range of dV/dt at VPRE is specified in electrical parameters.

Pulse skipping mode: the Vpre regulator can go to pulse skipping mode when the load is too low to avoid that output voltage (VPRE) rises too much. The principle of the pulse skipping mode is to skip some pulses during the switching phase, when the loop can't keep itself the output voltage regulated with a very low load because it is limited by the minimum duty cycle.

VB_IN_OV fault can trigger the turn OFF of Buck regulator, as specified into reset matrix. This effect can be masked with bit *VB_IN_OV_RST_EN* in CONFIG_REG 12.

Conditions:

5.5 V< VB_IN_SW < 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 29. Pre-buck regulator output electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VPREdc	VPRE regulated voltage (including aging and static line/load regulation)	VB_IN_SW = 7 V to 18 V, Ivpre = 50 mA ~1.6 A, C = 20 µF, L = 22 µH	5.82 (-3%)	6	6.18 (+3%)	V	VPRE
V_{drift_VPRE}	Total VPRE voltage aging drift	-	-0.8	-	0.8	%	VPRE
V_{line_VPRE}	Line regulation voltage	7 V < VB_IN_SW < 18V Ivpre = 50 mA, 1600 mA C=20 µF, L = 22 µH, T = 27 °C, 175 °C	-25	-	25	mV	VPRE
V_{line_VPRE}	Line regulation voltage	7 V < VB_IN_SW < 18V Ivpre = 50 mA, 1600 mA C=20 µF, L = 22 µH,T = -40 °C	-25	-	25	mV	VPRE
V_{line_VPRE}	Line regulation voltage	7 V < VB_IN_SW < 18V Ivpre = 50 mA, 1600 mA C=20 µF, L = 22 µH,T = -40 °C	-60	-	60	mV	VPRE
V_{load_VPRE}	Load regulation voltage	VB_IN_SW = 7 V, 18V, 50 mA<Ivpre<1600 mA, C = 20 µF, L = 22 µH, T = 27 °C, 175 °C	-25	-	25	mV	VPRE
V_{load_VPRE}	Load regulation voltage	VB_IN_SW = 7 V, 18 V, 50mA<Ivpre<1600 mA, C = 20 µF, L = 22 µH, T= -40 °C	-25	-	25	mV	VPRE
V_{load_VPRE}	Load regulation voltage	VB_IN_SW = 7 V, 18 V, 50 mA<Ivpre<1600 mA, C = 20 µF, L = 22 µH, T=-40°	-60	-	60	mV	VPRE
$V_{line\_VPRE\_tr}$	Transient line regulation accuracy	VB_IN_SW step 12 V to 18 V; 18 V to 12 V, dVB_IN_SW/dt = 3 V/µs, Ivpre = 50 mA,1.3 A, C = 20 µF, L = 22 µH, Guaranteed by design(1)	-8	VPRE	8	%	VPRE
$V_{load\_VPRE\_tr}$	Transient Load regulation accuracy	VB_IN_SW = 13 V, Ivpre = 50 mA to 1.3 A dI/dt = 500 mA/µs, C = 20 µF, L = 22 µH, Guaranteed by design(1)	-8	VPRE	8	%	VPRE

Table 29. Pre-buck regulator output electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ILIMVPRE	Current limit	-	2.4	-	3.5	A	VPRE
VPRE_coupling	VPRE capacitive coupling during battery transients	VB_IN_SW from 0 to 13 V in 100 µs, C = 40 µF, L = 22 µH, device off Design info, not tested	-	-	3	V	VPRE
Vuv_vpre_h	VPRE under voltage hysteresis threshold high; VPRE voltage at Power up to allow Boost activation threshold	Test condition: VB_IN_SW = 5.4 V	4.38	-	4.65	V	VPRE
Vuv_vpre_l	VPRE under voltage hysteresis threshold low	Test condition: VB_IN_SW = 5.4 V	4.25	-	4.51	V	VPRE
Tuv_filter_vpre	VPRE under voltage filter time (2)		10.1	12	13.3	us	VPRE
VPRE_slope	Slope control	VB_IN_SW = 13 V	5	-	30	V/ms	VPRE
Tmsd_VPRE_H	Thermal shutdown_High	Comparator threshold and functionality are tested in production	185	-	200	°C	VPRE
Tmsd_VPRE_L	Thermal shutdown_Low	Comparator threshold and functionality are tested in production	175	-	190	°C	VPRE
Tmsd_hyst	Thermal hysteresis for shutdown	-	5	-	10	°C	VPRE
tmsd_pre_an	Thermal shutdown analog filter time	-	1.5	-	4	us	VPRE
tmsd_pre_dig	Thermal shutdown digital filter time	-	10	20	30	us	VPRE
VPRE_rpd	VPRE pulldown resistor	To keep VPRE below 10 V with Buck switch leakage in OFF state	0.2	-	1.05	MΩ	VPRE
Fsw_VPRE	Switching frequency	Fosc from main 15 MHz oscillator, typical 462.5 kHz	450	Fosc/32	500	kHz	BUCK_SW
DCVPRE(BUCK)	Duty cycle range	-	3%	-	100%	-	BUCK_SW

Table 29. Pre-buck regulator output electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RVPRE	VPRE (Buck_POWER MOS) transistor RDSON	-	-	-	200	mOhm	BUCK_SW
TRVPRE	Rise Time (10-90%)	BUCK_SLOW_SR=0	5	-	25	ns	BUCK_SW
TRVPRE_slow	Rise Time (10-90%)	BUCK_SLOW_SR=1	10	-	30	ns	BUCK_SW
TFVPRE	Fall Time (10-90%)	Iload = 1 A	5	-	27	ns	BUCK_SW
VPRE_SW_Ileak	Leakage current	From 0 V to max pin voltage	-	-	1	µA	BUCK_SW

1. Fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase.
2. No VDD5 UV/OV violation is expected during specified transient.

Note: When 18 < VB_IN_SW< VOV_VB_IN_L, the function of Vpre is guaranteed and no reset happens.

Table 30. Pre-buck regulator external components electrical characteristics (Vpre application information)

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
C_{VPRE}	External capacitor on Vbuck supply	Min 2*10 µF Ceramic X7R 16 V in parallel CER,X7R,10 µF, 10%,16 V,1206, Sn	15	40	150	µF	VPRE
L_{VPRE}	Switching regulator external inductor	-	15	22	29	µH	VPRE
C_{BST}	Bootstrap capacitor	Ceramic X7R 16V 47nF, 10%, 16 V, X7R, 0603, TINNED, CER CAP/	-	47	-	nF	BUCK_C_BST
D_{VBUCK_CTRL}	Switching regulator external diode (Schottky or ultrafast)	Schottky Diode STPS5L60-Y	-	-	-	-	-

6.3 Tracking regulator for sensors supply

There are three 5V tracking regulators with self protection from over-current, over-voltage and short to battery. STB/OVC/OV don't disable tracking, but set a flag readable by MSC. Those three tracking regulators track VDD5_in voltage with 150mA output. There is one thermal sensor, shared between the three tracking regulators, to provide the thermal shut down protection for those three tracking sensor supplies. The switching off of one internal tracking occurs if that tracking is also in OVC.

Once the thermal shut down has happened, the tracking sensor in over-current condition will be off until temperature decreases to thermal shut down threshold low. Those three tracking regulators can be singularly disabled by dedicated MSC bit (*TRK_EN CONFIG_REG7 [3:5]* in CONFIG_REG 7). VB_IN_OV fault can trigger the turn OFF of Tracking regulators, as specified into reset matrix. This effect can be masked with bit *VB_IN_OV_RST_EN* in CONFIG_REG 12.

Conditions:

5.5 V < VB_IN_SW ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 31. Tracking sensor supplies electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ΔVTRK	Output voltage tracking error (including voltage aging and static load/line transient regulation)(1)	Vpre = 5.6 – 18 V 1 mA<IVSENS<150 mA	VDD5 -15m		VDD5 +15m	V	VSENSE1/2/3
I_{MAX_VS}	Output current limitation	VSENS = -1 V	150		250	mA	VSENSE1/2/3
I_{TH_VS}	Output over-current threshold	Vpre = 5.6 – 18 V	150		Imax _vs	mA	VSENSE1/2/3
V_{line_VS}	Line regulation voltage	Vpre = 5.6 – 18 V IVSENS=50mA Ctrk=470nF (2)			15	mV	VSENSE1/2/3
V_{load_VS}	Load regulation voltage	Vpre = 6 V 1 mA<IVSENS<150 mA Ctrk = 470 nF Note(2)			15	mV	VSENSE1/2/3
Vload_tran	Transient load regulation	Vpre = 6 V IVSENS =1 mA to 150 mA and viceversa dI/dt = 150 mA/µs Ctrk = 470 nF Guaranteed by design(3)	-15		+15	%	VSENSE1/2/3
Vline_tran	Transient line regulation	VPRE step 5.6V to 7V and viceversa dVPRE/dt=3V/µs IVSENS =1mA, 150mA Ctrk=470nF Guaranteed by design(4), (3)	-15		+15	%	VSENSE1/2/3
I_{sink_VS}	Short circuit reverse current	Output shorted to VB_IN+2V	-	-	-4	mA	VSENSE1/2/3

Table 31. Tracking sensor supplies electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{SCB\_TH\_VS}$	Short to battery threshold	-	Vpre		Vpre +0.2	V	VSENSE1/2/3
$V_{UV\_VS\_l}$	VSENSE1/2/3 undervoltage hysteresis threshold low	-	4.5	4.65	4.75	V	VSENSE1/2/3
$V_{UV\_VS\_h}$	VSENSE1/2/3 undervoltage hysteresis threshold high	-	4.7	4.8	4.9	V	VSENSE1/2/3
V_{OV_VS}	VSENSE1/2/3 overvoltage threshold	-	5.3	5.4	5.5	V	VSENSE1/2/3
$PSRR_{VS}$	Supply voltage tracking rejection	f =10 kHz			-35	dB	VSENSE1/2/3
V_{OS_VS}	Over shoot during power up	-			5.5	V	VSENSE1/2/3
$T_{UV\_filter\_VS\_running}$	Undervoltage filter time(2)	cover by SCAN TEST	16	24	32	µs	VSENSE1/2/3
$T_{OV\_filter\_VS\_running}$	Overvoltage filter time(2)	cover by SCAN TEST	16	24	32	µs	VSENSE1/2/3
$T_{OC\_filter\_VS\_running}$	Overcurrent filter time	cover by SCAN TEST	16	24	32	µs	VSENSE1/2/3
$T_{msd\_VPRE\_H}$	Thermal shutdown_High	Comparator threshold and functionality are tested in production	185		200	°C	VSENSE1,2,3
$T_{msd\_VPRE\_L}$	Thermal shutdown_Low	Comparator threshold and functionality are tested in production	175		190	°C	VSENSE1,2,3
T_{msd_hyst}	Thermal hysteresis for shutdown	-	5		10	°C	VSENSE1,2,3
$t_{msd\_pre\_an}$	Thermal shutdown analog filter time	Guaranteed by design	1.5		4	µs	VSENSE1,2,3
$t_{msd\_pre\_dig}$	Thermal shutdown digital filter time	Implemented in VHDL	10	20	30	µs	VSENSE1,2,3

1. No oscillation expected with 0mA load current.
2. line and load regulation are guaranteed until the loop is able to regulate after they are defined by low drop parameters; ITH_VS < IMAX_VS which is guaranteed by design; Over shoot during power up should not be triggered over voltage warning. When Vtrk output is higher than VSCB_TH_VS, The Vtrk output structure will be switched off automatically in order to block the big inrush current into chip through Vtrk circuit. When Vtrk output is higher than VOV_VS, an over voltage flag will be set. UV/OV fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase.
3. No UV/OV violation is expected during specified transient.
4. Specification valid until Tracking regulator is in regulation range, or, in other words, until Vsense X output voltage is determined by the effect of voltage regulation loop and not by secondary effects on other regulators.

Table 32. VTrack external components characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
$C_{VS1/2/3}$	VSENSE external capacitor	ESR_max<20 mΩ Suggest part numbers: GCM188R71C105KA49D	470nF -20%	0.47	20	µF	VSENSE1/2/3

6.4 External tracking regulator monitor

Vsense4_mon is an input pin for monitoring an external tracking regulator output voltage.

Conditions:

5.5 V < VB_IN_SW ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 33. External VTrack monitor

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{UV\_VS\_l}$	VSENSE4 undervoltage threshold low	-	4.55	4.65	4.75	V	VSENSE4_MON
$V_{UV\_VS\_h}$	VSENSE4 undervoltage threshold high	-	4.7	4.8	4.95	V	VSENSE4_MON
V_{OV_VS}	VSENSE4 overvoltage threshold	-	5.3	5.4	5.55	V	VSENSE4_MON
$T_{UV\_filter\_VS\_running}$(1)	Undervoltage filter time	Covered by SCAN TEST	16	24	32	µs	VSENSE4_MON
$T_{OV\_filter\_VS\_running}$(1)	Overvoltage filter time	Covered by SCAN TEST	16	24	32	µs	VSENSE4_MON

1. Fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase.

6.5 VDD5 linear regulator with external MOSFET

VDD5 voltage is generated by a linear controller with internal pre-driver and external MOS FET.

Electrical characteristics are available in *Table 34* and *Table 35*. VB_IN_OV fault can trigger the turn OFF of VDD5 regulator, as specified into reset matrix. This effect can be masked with bit *VB_IN_OV_RST_EN* in CONFIG_REG 12.

VB_IN_UV fault triggers the turn OFF of VDD5 regulator, as specified into reset matrix. This effect can be masked with bit *VDD5_OFF_SEL* in CONFIG_REG 11.

VDD5_OV fault has effects into the device specified into reset matrix. These effects can be masked with bit *VDD5_OV_RST_EN* in CONFIG_REG 12.

Conditions:

5.5 V< VB_IN_SW ≤ 18 V, 5.5 V < VB_IN ≤ 18 V, T_j -40 to 175°C unless otherwise specified.

Table 34. VDD5 linear controller pre-driver electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_{VDD5}	5 V regulated voltage including static load / line regulation	I_{load} = 10 mA, 1 A	4.9	5	5.1	V	VDD5_IN
$SR_{p\text{-}up\_VDD5}$	Output voltage slew rate at power-up	Cvdd5 = 10 µF; from VDD5*10% to VDD5*90%	2	-	25	V/ms	VDD5_IN
I_{VDD5}	Controller stability over VDD5 output current range	-	1	-	-	A	VDD5_IN
V_{line_VDD5}	Line regulation voltage	5.6 V < VPre < 18 V Iload 10mA, 1A Cvdd5 = 10 µF (1)	-25	-	25	mV	VDD5_IN
V_{load_VDD5}	Load regulation voltage	VPre 5.6 V, 18 V 10 mA < Iload < 1 A Cvdd5 = 10 µF (1)	-25	-	25	mV	VDD5_IN
$V_{line\_VDD5\_tran}$	Line transient regulation voltage	Vpre from 5.6 V to 7 V by 1 µs Iload = 10 mA, 800 mA Cvdd5 =10µF Ext MOS STD20NF06L Guaranteed by design (1)	-	-	300	mV	VDD5_IN
$V_{load\_VDD5\_tran}$	Load transient regulation voltage	VPre = 6 V Iload from 10 mA to 800 mA by 1.5us Cvdd5=10µF Ext MOS STD20NF06L Guaranteed by design (1)	-	-	280	mV	VDD5_IN
V_{drift_Vdd5}	Total VDD5 voltage aging drift	-	-0.8	-	0.8	%	VDD5_IN

Table 34. VDD5 linear controller pre-driver electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$PSRR_{VDD5}$	Supply voltage rejection ratio	Cout = 10 µF, ESR = 0.1Ω Iload = 600 mA f = 10 kHz	-	-	-35	dB	VDD5_IN
V_{OS_VDD5}	VDD5 voltage with overshoot admitted at switch on	-	0	0.1	0.2	V	VDD5_IN
$T_{UV\_filter\_VDD5}$	Undervoltage filter time(1)	-	16	24	32	µs	VDD5_IN
$T_{OV\_filter\_VDD5}$	Overvoltage filter time(1)	-	16	24	32	µs	VDD5_IN
$V_{UV\_VDD5\_L}$	VDD5 undervoltage hysteresis threshold low	-	4.5	4.65	4.75	V	VDD5_IN
$V_{UV\_VDD5\_H}$	VDD5 undervoltage hysteresis threshold high	-	4.7	4.8	4.9	V	VDD5_IN
V_{OV_VDD5}	VDD5 overvoltage threshold	-	5.3	5.4	5.5	V	VDD5_IN
$V_{VDD5\_GATE\_Min}$	Pre-driver gate voltage	VPre = 4.8 V to force regulator in low drop condition	8	-	-	V	VDD5_GATE
$V_{VDD5\_GATE\_MAX}$	Pre-driver gate voltage	Force 5 mA into VDD5_GATE	-	-	15	V	VDD5_GATE
V_{GS} OFF condition	VDD5_GATE-VDD5_IN	Device off	-	-	0.5	V	VDD5_GATE

1. line and load regulation are guaranteed until the loop is able to regulate after they are defined by low drop parameters; Over shoot during power up should not be triggered over voltage warning. UV/OV fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase. With external MOS different from STD20NF06L regulated voltage could violate UV threshold but for a time shorter than digital deglitch, so it would not be able to trigger UV/OV fault. With STD20NF06L MOS no UV/OV violation is expected on this and other regulators.

Table 35. Linear controller pre-driver. External components characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
C_{VDD5}	External VDD5 capacitor	10 µF to guarantee ESR = 50 mΩ for load transient response	5	20	60	µF	VDD5_IN
-	External n-MOS	STD20NF06L	-	-	-	-	VDD5_IN, VDD5_GATE

Table 35. Linear controller pre-driver. External components characteristics (continued)

Symbol	Parameter	Note	Min	Typ	Max	Unit	Pin
-	Rgate_source	-	-	1	-	MΩ	-
-	Rgate_source	-	-	1	-	MΩ	--
gfs	Forward Transconductance	VDS = 25 V, ID = 10 A	4.5	-	-	S	-
VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250 µA	2.0	-	4.0	V	-
C_{iss}	input capacitance of external FET	-	-	370	1020	pF	VDD5_GATE

6.6 VDD_IO

VDD_IO pin is the external supply pin for internal I/O circuit.

Table 36. VDD_IO electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{VDD_IO}	Input current of VDD_IO	VB=14V, all VDD_IO related pin without load	2	4.8	8	mA	VDD_IO
VVDD_IO	Operation range	-	3.1	-	5.5	V	VDD_IO
VDDIO_UV_LOW	Under voltage threshold on pin VDDIO	-	2.9	3.0	3.1	V	VDD_IO
Tf_VDD_IO_UV	Under voltage filter time(1)	Tested by scan	3	-	10	µs	VDD_IO

1. Fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase.

6.7 VB_IN and VB_IN_SW SUPPLY

VB_IN pin is the power supply pin for internal circuit.

During cranking phase even the VB_IN is = 3.1 V the chip can keep the status, the internal POR is not triggered and also the internal supply under voltage is not triggered (internal 3V3 regulator undervoltage), the PHOLD timer value is also kept.

Table 37. VB_IN electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{VB_IN}	VB_IN current in functional mode	-	-	-	60	mA	VB_IN
$I_{VB\_IN\_STBY}$	VB_IN current in OFF state.	-	-	-	10	µA	VB_IN
$I_{VB\_IN\_SW}$	VB_IN_SW current in functional mode	VB_IN=VB_IN_SW=13.5V, Vpre load = 500mA	200	-	350	mA	VB_IN_SW
$V_{OFF\_VB\_IN}$	Min VB_IN voltage to keep the MRD, start relay status	-	-	-	3.1	V	VB_IN
$V_{UV\_VB\_IN\_L}$	VB_IN undervoltage hysteresis threshold low	-	4.7	4.8	4.9	V	VB_IN
$V_{UV\_VB\_H}$	VB_IN undervoltage hysteresis threshold high	-	4.8	4.9	5.05	V	VB_IN
$V_{UV\_VB\_IN\_HYST}$	-	-	-	0.1	-	V	VB_IN
$V_{OV\_VB\_IN\_L}$	VB_IN over voltage threshold low	-	28	-	-	V	VB_IN
$V_{OV\_VB\_IN\_H}$	VB_IN over voltage threshold high	-	-	-	32	V	VB_IN
$V_{OV\_VB\_IN\_HYST}$	-	-	-	2	-	V	VB_IN
t_{VBOV1}	Filter time1 for VB_IN overvoltage(1)	Tested by scan	70	85	100	µs	VB_IN
t_{VBOV2}	Filter time2 for VB_IN overvoltage(1)	Tested by scan	11	15	19	ms	VB_IN
t_{VBUV1}	Filter time 1 for VB_IN undervoltage $V_{UV\_VB\_IN\_L}$(1)	Tested by scan	5	-	15	µs	VB_IN
t_{VBUV2}	Filter time 2 for VB_IN undervoltage $V_{UV\_VB\_IN\_H}$(1)	Tested by scan	5	-	15	µs	VB_IN
$V_{UV\_VB\_CP\_ON}$	VB_IN threshold for main logic reset	Charge Pump ON	2.4	2.7	3	V	VB_IN
$V_{UV\_VB\_CP\_OFF}$	VB_IN threshold for main logic reset	Charge Pump OFF	3.9	4.4	4.8	V	VB_IN

1. Fault detection during power up sequence is masked until RSTN release to avoid false triggering at ramp-up phase.

When VB_IN is higher than 3.1 V (Voff_vb_in), the starter relay and MRD can hold the state. VB_IN_SW pin is the dedicated supply pin for pre-buck regulator.

Note: VB_IN_SW must be shorted to VB_IN in PCB layout.

Conditions:

4.8 V ≤ VB_IN ≤ 18 V; T_j -40 to 175° C unless otherwise specified;

Table 38. VB_IN_SW electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Pin
$I_{VB\_IN\_sw\_STBY}$	VB_IN_SW current in OFF state.	-	-	-	10	µA	VB_IN_SW

6.8 Charge pump

Charge pump provides a permanent voltage of at least 4.8 V above VB_IN when VB_IN is higher than 5.5 V, the VDD5 linear regulator, H-side switch and so on.

Once VB_IN overvoltage is detected (VB_IN > VOV_VB_IN_H for t>tVBOV2), the charge pump will be switched off automatically.

Charge pump can provide voltage of 4V above VB_IN when VB_IN in low power condition (3.1V<VB_IN<5.5V)

This charge pump is for internal use only.

Note: It is forbidden to use this charge pump pin for external load.

Figure 27. Power up charge pump behavior

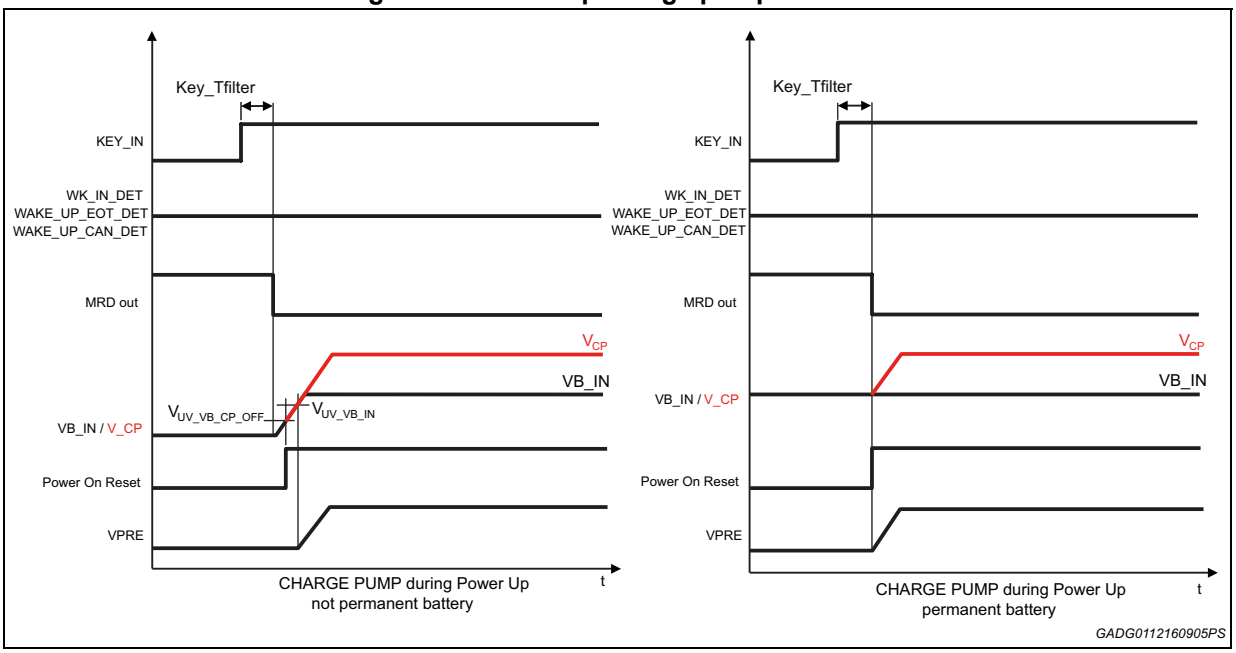
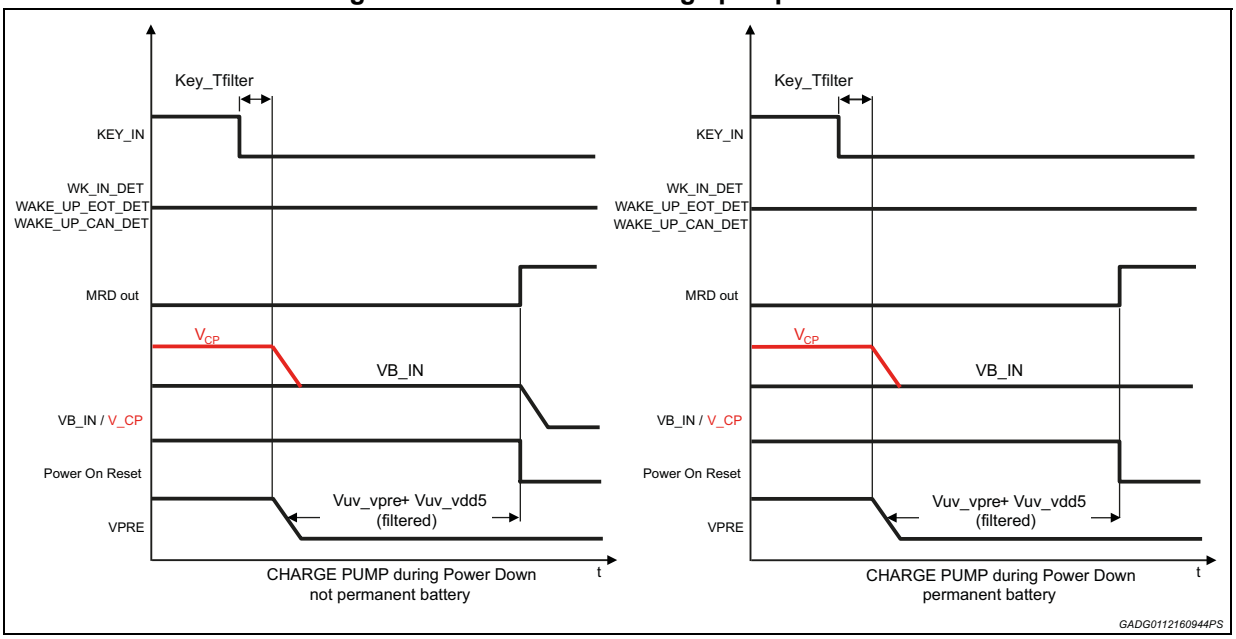


Figure 28. Power down charge pump behavior



Conditions:

4.8 V≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

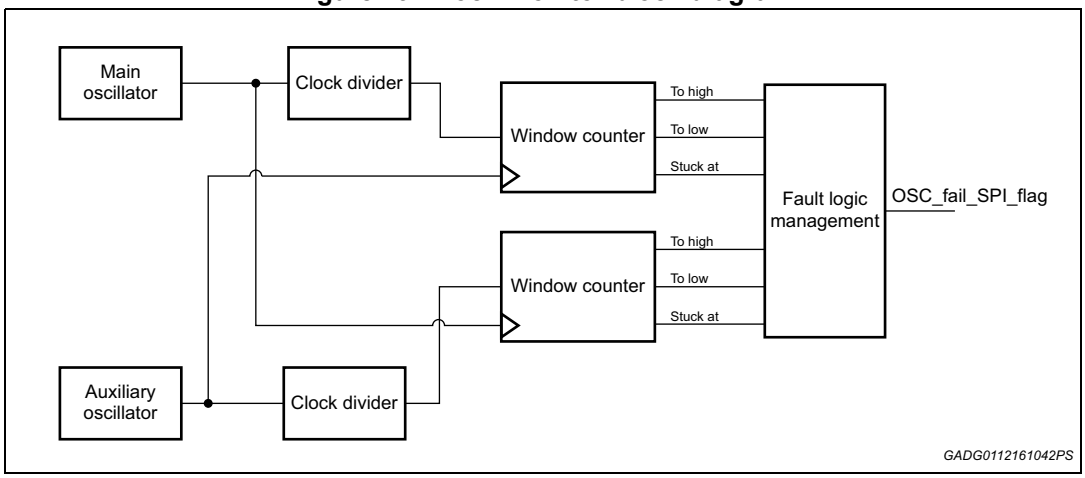
Table 39. Charge pump characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
CP	External charge pump capacitor	-	-20%	100	+20%	nF	CP
Vcp	Output voltage	VB_IN = 5.5 V-18 V Driver Starter 1 & 2 & 3 configured as HS and switching	VB_IN+4.8V	-	VB_IN+8V	V	CP
		VB_IN_OFF(3.1V)<VB_IN<5. 5 V with 2 Driver Starter configured as HS and fully ON	VB_IN+4V	-	VB_IN+8V	V	CP
Icp_leakage	Leakage current in off state	CP = VB_IN; chip off	-3	-	3	µA	CP

6.9 Main oscillator

The device uses an internal oscillator, called MAIN Oscillator, to synchronize internal logic and internal charge pump. A second oscillator is used to check internally if the Main oscillator is working correctly. The Main Oscillator output is continuously verified by the Auxiliary Oscillator output. The two clocks frequency are measured and compared so that out of range frequency values can be detected. In case of frequency error greater than 20% a flag "*freq_err*" (Upstream Read11) is set and read and cleared by MSC. In case of frequency error greater than 30% another flag "*clk_mon_fault*" (Upstream Read11) is set and read and cleared by MSC, drivers are disabled when this error occurs. The monitor circuit is able also to detect a stuck condition in the reference clock, moreover the check is done on both the main and the auxiliary oscillator so that a failure in any of the two oscillators is able to set the fault flag.

Figure 29. Clock monitor block diagram



The Main and Auxiliary oscillators are kept independent using redundant circuits, biased by independent current sources, and layouted in different floor plan regions kept isolated thanks to deep trench usage. The only common point between the oscillators is the digital supply that is however monitored by the independent mechanisms.

Aux oscillator is used just for safety purpose and connected to a small digital portion (no impact on EMC performance). The main oscillator has spread spectrum solution applied by default to reduce emissions; it means that oscillator frequency has and average value equal to MainOSCIL with a triangular modulation applied, so final frequency is MainOSCIL ± 3.5% and a triangular variation of about 111 kHz frequency

Conditions:

4.8 ≤ VB_IN ≤ 18V, T_j -40 to 175 °C unless otherwise specified;

Table 40. Clock monitor characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
MainOSCIL	Internal MAIN oscillator frequency	VB_IN = 4.8 V-18 V	14.25	15	15.75	MHz	-
MainOSCIL	Internal redundant oscillator frequency	VB_IN = 4.8 V-18 V	-	15	-	MHz	-

Table 40. Clock monitor characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
-	Delta 1 Oscillator CHECK	VB_IN = 4.8 V-18 V “freq_err= 1”	20	-	-	%	-
-	Delta 2 Oscillator CHECK	VB_IN=4.8V-18V “FREQ_ERR=1”& “clk_mon_fault=1”(drivers OFF)	30	-	-	%	-

7 Low-side drivers

Low-side drivers are used for power stages driving and they include:

- 4-channel Low-side Injectors INJ[1:4];
- 2-channel Low-side O2 Heaters O2H[1:2];
- 2-channel Low-side Solenoids SOL[1:2];
- 5-channel Low-side Relays RLY[1:5];
- 2-channel Low-side LED[1:2].

All drivers support the same failure diagnosis.

7.1 Diagnosis

The driver has the following fault diagnosis:

Overcurrent (Short To Vbat) protection in On Phase (OVC);

Open Load in Off phase (DIAGOL);

Short to Ground in Off Phase (DIAGLV);

Over Temperature Protection in On phase (OT).

When an overcurrent fault is detected the driver switches off with higher slew rate (FAST SR) to reduce the power dissipation.

7.1.1 ON state - overcurrent protection

An overcurrent protection is present for LS transistors of each driver channel. Once the overcurrent fault is detected the faulted power MOS is switched off and a fault bit is set. This bit can be reset by every Read Diag Communication to re-activate the power stage in this two condition:

- The MSC command still High, when the Fault OVC Bit is read by MSC communication.
- The MSC command becomes Low and then again High.

To increase EMC robustness and avoid unwanted fault triggering a small deglitch filter is applied.

In order to avoid false OVC detection during the turn on slew rate phase, an analog blanking time filtering strategy is implemented. This means that the OVC comparator output is masked until the driver gate voltage has reached a threshold value which guarantees that the slew rate phase is ended.

7.1.2 ON state - thermal protection

To protect power stages from temperature overheat (high battery range of operation, soft short conditions, etc.) a dedicated thermal sensor placed close to power MOS is present in the layout sensing FET temperature; One threshold is implemented (T_SD_H) with Hysteresis (T_SD_hys). When the T_SD_H threshold is detected the Driver switches OFF. Once the power stage has been switched-off for over-temperature detection, it will be able to switch on again when temperature is decreased below thermal shut down threshold plus hysteresis value to avoid high frequency on-off cycling.

7.1.3 ON/OFF state - Error in on status diagnosis

To avoid unwanted driving of power stages the consistency of gate driving signal with digital command is always monitored inside the device. Each time a turn-on/turn-off signal is output by the logic core its effectiveness is verified comparing it with the status of the output voltage.

The main logic can check the consistence between inner logic and actual signal at output pin reading the OpenLoad comparator or Short-To-Ground Comparator according to *Table 42*.

The driver status diagnosis (STA) is activated by the *MSC on command*, the relative comparator is filtered for Tsta filter time to validate the diagnosis. In case of MOS pre-driver the selected blanking time Tblank is applied before filtering.

Table 41. Driver status diagnosis

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Tsta	Driver status diagnosis filter time	Tested by scan	30	32.5	35	µs	-

Table 42. STA diagnosis for drivers

STA diagnosis for drivers				
-	INJ,SOL,O2H, RLY, STR in Low-side configuration	STR in high-side configuration.	MOS pre-driver	IGN
ON state	Detected by STG comparator, if the output pin voltage is higher than VLVT, STA fault is detected	Detected by Open load comparator, if the output pin voltage is lower than V_OL, STA fault is detected.	Detected by STG comparator, if the MOS_DRN pin voltage is higher than VLVT, STA fault is detected.	Same information as STG bit.
OFF state (for LS/HS/PDRV) LS_ON state (for IGN)	Detected by Open load comparator or Short To Ground comparator. If the output pin voltage is lower than V_OL or lower than VLVT STA fault is detected.	Detected by STG comparator, if the output pin voltage is higher than VLVT, STA fault is detected.	Detected by Open load comparator, if the MOS_DRN pin voltage is lower than V_OL, STA fault is detected.	Not able to detect.
STA processing	filtering	filtering	blanking+filtering	filtering

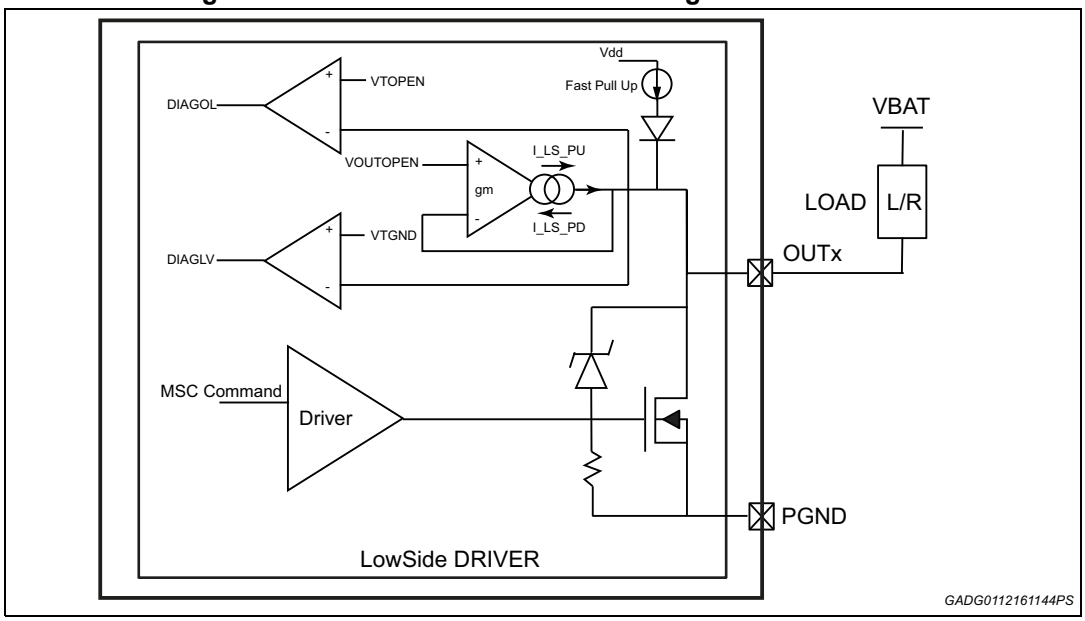
Note: In case of activation of OVT[17] the STA diagnosis is not available.

In case of activation of relative driver OVC the STA diagnosis is available.

7.1.4 OFF state - short load and open load

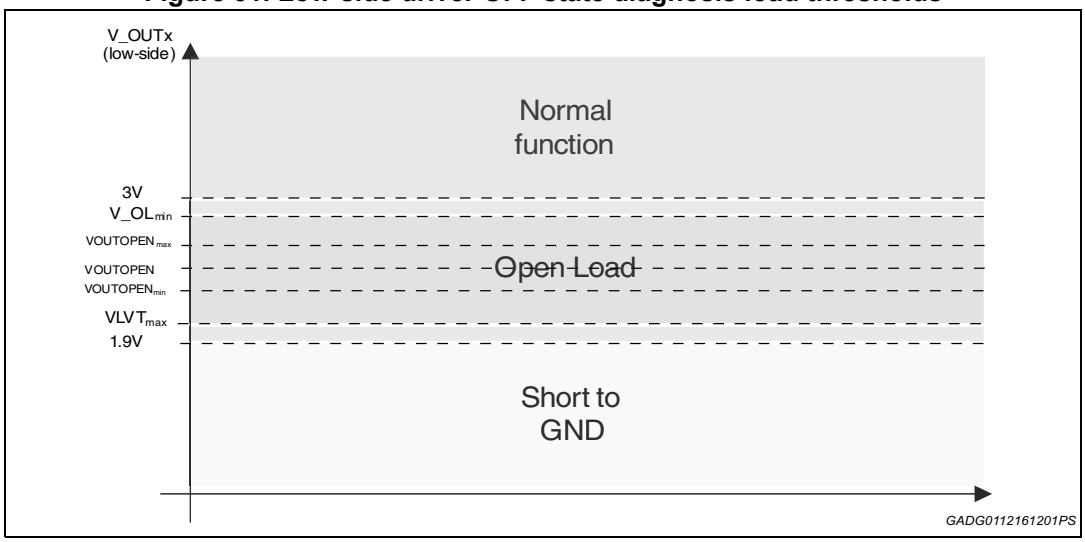
The device provides off-state diagnosis for each driver channel. Simplified schematic of implemented diagnosis is shown in *Figure 30*.

Figure 30. Low-side driver OFF state diagnosis schematic



In the Low-Side Driver we can have three different load conditions as shown in *Figure 31*:

Figure 31. Low-side driver OFF state diagnosis load thresholds



_Normal Load: it means output driver connected to the load, No Fault Present, VOUT ≥ V_OL Threshold

_Open Load: It means output driver disconnected from the load, Open Load Fault Present, VLVT ≤ VOUT ≤ V_OL Threshold

_Short To Ground: it means output driver shorted to GND voltage, Short To Gnd Fault Present, VOUT ≤ VLVT Threshold

There is a bit *IPUPD_EN* in CONFIG_REG2 which is controlled by a MSC bit, that it is used by external µController if it is needed to switch on/off both pull up and pull down diagnosis current.

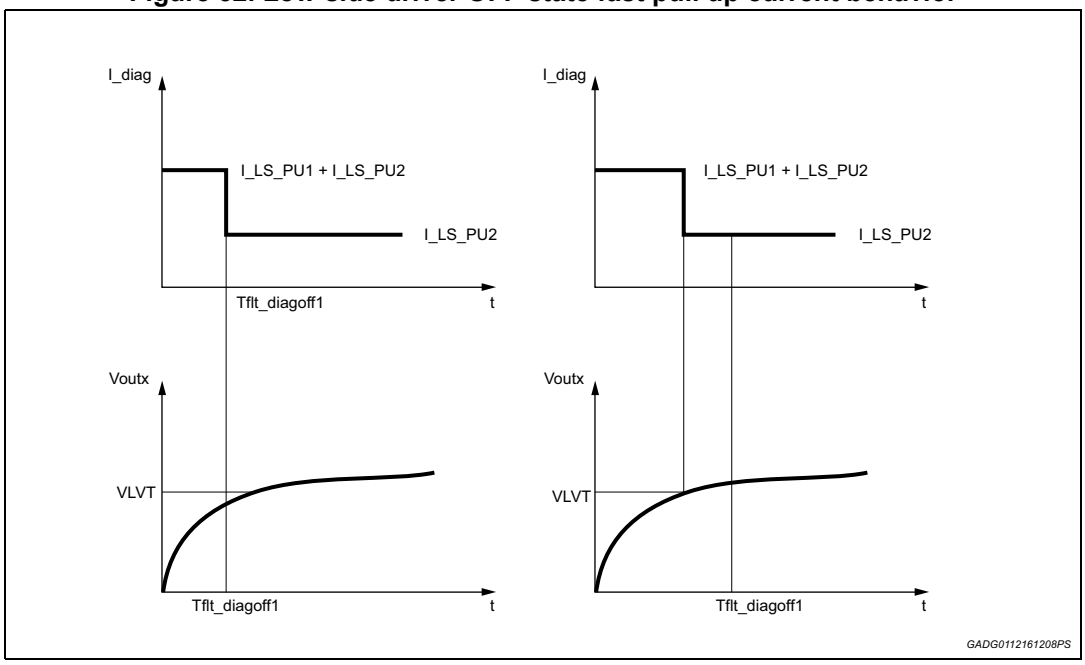
The Diagnostic in Off state is done by the following blocks:

- An internal Buffer using the pull up/down currents is able to force the VOUTOPEN voltage on the Low-Side Driver Output when the driver is in Open Load Condition.
- A comparator to detect the Open load Condition. The Open Load fault is detected when the Low-Side output pin is VLVT ≤ VOUT ≤ V_OL Threshold for a time longer than Diag Filter Time.
- A comparator to detect the Short to GND Condition. The Short to GND fault is detected when the Low-Side output pin is VOUT <= VLVT Threshold for a time longer than Diag Filter Time.

There is a bit *IPUPD_MODE* in CONFIG_REG2 which is controlled by a MSC bit, it is used by external µController if it is needed to switch on/off the bigger diagnosis current(I_LS_PU1) in fast mode.

The Fast pull up current is used to avoid the false short to t_{GND} diagnosis when the driver switches off in Open load condition. This current switches on after the falling edge of MSC command (driver in off state) and remains on until the Diag Filter Time is expired or until the VOUT is > VLVT Threshold.(note: if fast pull up current is selected, the filter time Tflt_diagoff1 is suggested. Otherwise, the filter time Tflt_diagoff2 is suggested)

Figure 32. Low-side driver OFF state fast pull up current behavior

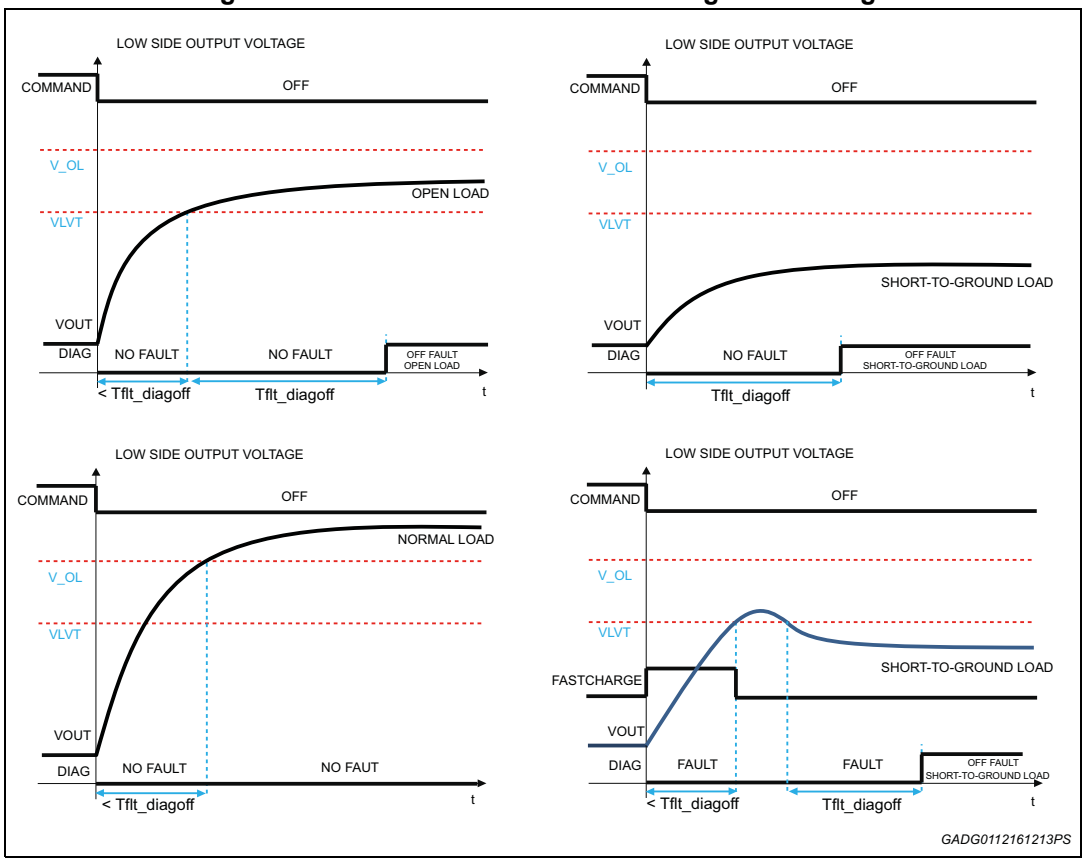


Despite the fast mode of all drivers in off diagnostic condition (*Ipupd_MODE* bit), for Injector and Solenoid drivers there is a dedicated MSC bit (*IDIAG_HIGH_SOL/IDIAG_HIGH_INJ* in CONFIG_REG13) for each kind of driver to select off diagnostic high or low pull up/down current

By default diagnostic pull up/down currents are disabled and comparator outputs are masked by internal logic, to enable OFF state diagnostic the channel must be put first in tristate condition and then (if not already done with previous MSC frames) diagnostic must be enabled.

A Filter Time (Diag Filter Time) is implemented in order to avoid detecting false diagnosis as shown in *Figure 33*.

Figure 33. Low-side driver OFF state diagnosis timings



If DiagOL or DiagLV signals remain high for a time higher than Diag Filter Time the fault bit is set and can be read by Read Diag Communication.

This bit is reset by every Read Diag Communication.

7.1.5 Error handling

Table 43. Low-side driver error handling

Type of error	Detection condition	Action	Clear MSC flag	Restart condition
Driver Diagnostic				
Overcurrent (OVC)	Driver on	Driver is put in off state. The fault is latched in MSC diagnosis register.	On read	At MSC read of diagnosis register if MSC command is still high. If MSC command is low and high again.
Short to ground (STG)	Driver off	The fault is latched in MSC diagnosis register.	On read	-
Open load (OPL)	Driver off	The fault is latched in MSC diagnosis register.	On read	-

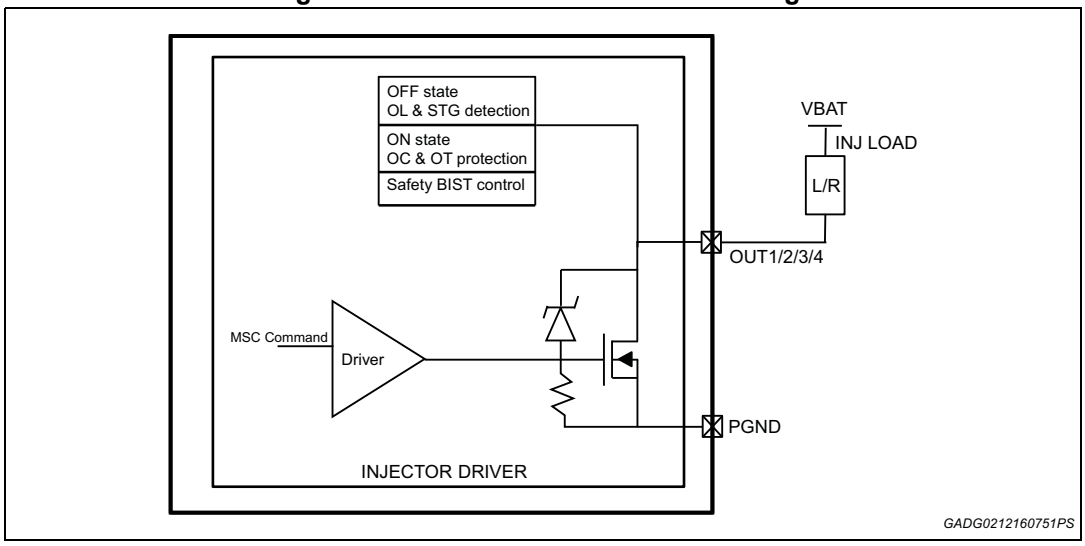
Table 43. Low-side driver error handling (continued)

Type of error	Detection condition	Action	Clear MSC flag	Restart condition
Driver Status Error (STA)	Driver on/off When the driver output level is not aligned with the command on/off	The fault is latched in MSC diagnosis register.	On read	-
Overtemperature (OVT) Shutdown	Driver on	Driver is put in off state. The fault is latched in MSC diagnosis register.	On read	The driver restarts when the temperature decreases. The fault is cleared at MSC read.

7.2 Low-side driver - INJECTOR INJ[1:4]

These 4 low-side drivers are designed to driver Injector Load. They are driven by *MSC command*. The output voltage is clamped to voltage limit by internal clamp circuit.

Figure 34. INJECTOR LowSide driver stage



Conditions:

5.5 V ≤ VB_IN ≤ 18 V; T_j -40 to 175 °C unless otherwise specified;

Table 44. Low-side driver - INJECTOR electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
INJECTOR							
LS_RdsON	Low-side RdsON	T_j = 150 °C, I_{LOAD} = 3 A	0.35	0.44	0,6	Ω	INJ1/2/3/4
LS_RdsON	-	T_j = 25°C,I_{LOAD} = 3 A	0.22	0.3	0.31	Ω	INJ1/2/3/4
LS_RdsON	-	T_j = -40 °C, I_{LOAD} = 3 A	0.15	0.2	0.25	Ω	INJ1/2/3/4

Table 44. Low-side driver - INJECTOR electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
OUTx_lkg	Output leakage current	Output disabled, diagnostic off	-10	-	10	µA	INJ1/2/3/4
Irev_OUTx	Body Diode reverse current voltage drop	I_{LOAD} = -2 A	-	-	2	V	INJ1/2/3/4
SR_ON	Voltage slew ON State	From 80% to 30% of V_{OUT}, VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	0.6	-	1.84	V/µs	INJ1/2/3/4
SR_OFF	Voltage slew OFF State	From 80% to 30% of V_{OUT}, VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	0.6	-	1.84	V/µs	INJ1/2/3/4
S/RGkill_LSH	FAST VS/R off when and OVC fault happens	From 30% to 80% of V_{OUT}, VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	5	-	20	V/µs	INJ1/2/3/4
Ton_OUTx	Propagation Delay from MSC_EN rising edge to 80% output OUTx voltage	VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	-	-	8	µs	INJ1/2/3/4
Toff_OUTx	Propagation Delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	-	-	8	µs	INJ1/2/3/4
clamp_OUTx	OUTx clamping Voltage	I_{LOAD} = 1.3 A	50	55	60	V	INJ1/2/3/4
Vclamp_OUTx_ high_curr	OUTx clamping Voltage	I_{LOAD} = 3 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	50	55	60	V	INJ1/2/3/4
IOVC_OUTx	Over Current Driver Threshold	-	3	-	6	A	INJ1/2/3/4
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	INJ1/2/3/4
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	INJ1/2/3/4
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	INJ1/2/3/4
T_SD_hys	Temperature shut down hysteresis	-	5		10	°C	INJ1/2/3/4

Table 44. Low-side driver - INJECTOR electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
tmsd_pre_an	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	INJ1/2/3/4
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	INJ1/2/3/4
Driver Reliability Data							
EnergyRep INJ	Energy repetitive pulse	T_{case} = 30 °C; I_OUT_n = 1.8 A, 18 Miopulses	-	-	7.5	mJ	INJ1/2/3/4
EnergyRep INJ	Energy repetitive pulse	T_{case}= 115 °C; I_OUT_n = 1.4 A 648 Miopulses	-	-	4	mJ	INJ1/2/3/4
EnergyRep INJ	Energy repetitive pulse	T_{case}= 130 °C; I_OUT_n = 1 A 96 Miopulses	-	-	3	mJ	INJ1/2/3/4
EnergyRep INJ	Energy repetitive pulse	T_{case}= 140 °C; I_OUT_n = 1 A 4 Miopulses	-	-	3	mJ	INJ1/2/3/4
Driver Reliability Data Generator Defect							
EnergyRep INJ	Energy repetitive pulse	T_{case}= 25 °C ; I_OUT_n = 2 A 0.5 Miopulses	-	-	9	mJ	INJ1/2/3/4
EnergyRep INJ	Energy repetitive pulse	T_{case}= 135 °C; I_OUT_n = 1.5 A 0.5 Miopulses	-	-	8	mJ	INJ1/2/3/4
Driver Reliability Data jump start							
EnergyRep INJ	Energy repetitive pulse	T_{case}= 25 °C; I_OT_n = 3.0 A MAX.0.021Mio cycles 10 jumps starts over liftime, each start < 2min	-	-	17.5	mJ	INJ1/2/3/4
EnergyRep INJ	Energy repetitive pulse	Tc=75°C ; I_OT_n=2.3A MAX.0.021Mio cycles 10jumps starts over liftime,each start<2min	-	-	10	mJ	INJ1/2/3/4
OFF state diagnostic							
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9	-	$V_{OUTOPEN}$ -180 mV	V	INJ1/2/3/4
V_OL	Open load threshold voltage	Driver tristate, diag enabled	$V_{OUTOPEN}$ +160 mV	-	3	V	INJ1/2/3/4
VOUTOPEN	Open load threshold voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	INJ1/2/3/4

Table 44. Low-side driver - INJECTOR electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN =ENB, Ipupd_MODE = "1"	2.5	3.6	4.7	mA	INJ1/2/3/4
I_LS_PU2	Diagnostic pull up low current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = "0" and IDIAG_HIGH_INJ = "0"	40	70	100	µA	INJ1/2/3/4
I_LS_PU3	Diagnostic pull up high current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = "0" and IDIAG_HIGH_INJ = "1"	100	-	200	µA	INJ1/2/3/4
I_LS_PD1	Diagnostic pull down low current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB IDIAG_HIGH_INJ = "0"	60	85	110	µA	INJ1/2/3/4
I_LS_PD2	Diagnostic pull down high current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB IDIAG_HIGH_INJ = "1"	325	-	550	µA	INJ1/2/3/4
Tflt_diagoff1	DIAG Filter time	Filter Mode = 0	75	100	125	µs	INJ1/2/3/4
Tflt_diagoff2	DIAG Filter time	Filter Mode = 1	450	600	750	µs	INJ1/2/3/4
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10nF) Filter Mode=0	175	-	-	µs	ESVx

7.2.1 Enable pin INJ_ENA

The Pin INJ_ENA is a digital input pin that is used as enable of Injector driver. If this pin is at low digital level the internal logic drives all injector drivers in OFF state. If this pin is at high digital, all injector drivers can be switched on by *dedicated MSC bit*. This pin can be used also as a SEO function for injector driver. If the application doesn't use this enable function, the INJ_ENA pin have to be pulled up externally to VDD5 by a resistor of 10 kΩ.

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 45. INJ_ENA electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VIH_T_X	HIGH_level input voltage	-	1.75	-	-	V	INJ_ENA
VIL_T_X	LOW_level input voltage	-	-	-	0.75	V	INJ_ENA
VHYS_T_X	Input voltage hysteresis	-	0.1	0.5	-	V	INJ_ENA
PDOWN_T_X	Pull-down resistance	-	50	100	200	kΩ	INJ_ENA

7.3 Low-side driver - O2 HEATER O2H[1:2]

These 2 LowSide drivers are designed to driver O2 heater Load. They are driven by *MSC command*. The Output voltage is clamped to voltage limit by internal clamp circuit. O2 channel can be configured as valve driver with faster slew rate and lower over current threshold by MSC commands. Current sense generates on Curr_sense_O2H pin a reduced copy of the current flowing through O2H Power. Current sense current generator is done with a P-channel current mirror connected to VDD5_IN, for this reason voltage on Curr_sense_O2H1 and Curr_sense_O2H2 pins can never exceed VDD5_IN.

Figure 35. O2 heater LowSide driver stage

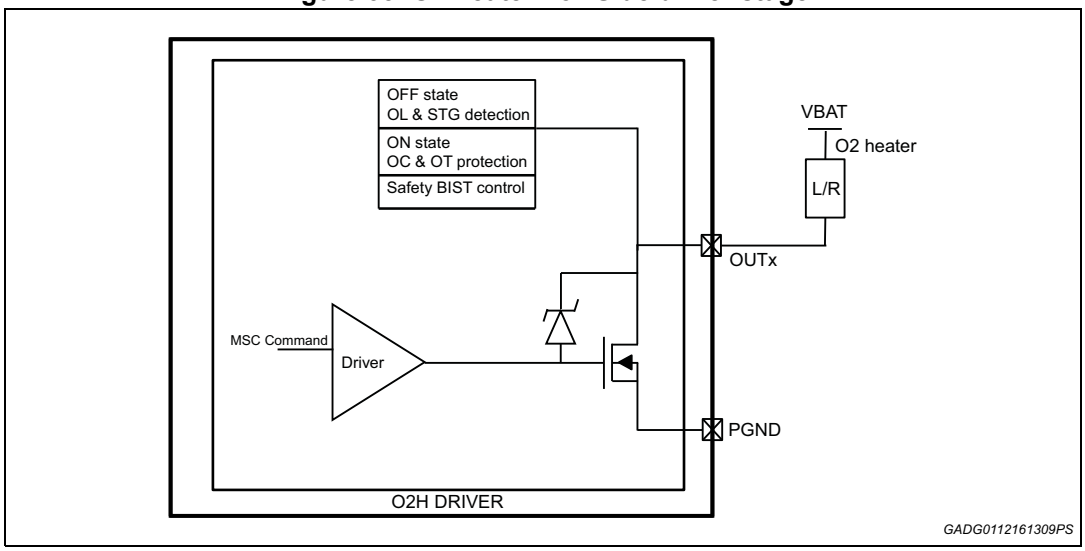
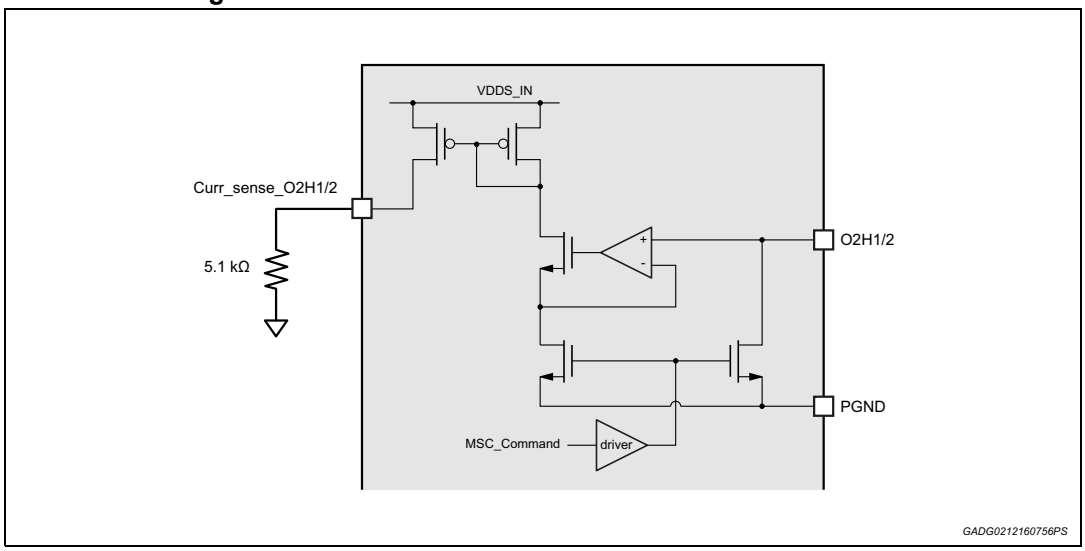


Figure 36. O2 Heater LowSide driver current sense block



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 46. Low-side driver - O2 HEATER electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
O2H							
LS_RdsON	Low-side RdsON	T_j = 150 °C, I_{LOAD} = 3 A	0.047	0.16	0.216	Ω	O2H1/2
		T_j = 25 °C, I_{LOAD} = 3 A	0.04	0.12	0.155	Ω	O2H1/2
		T_j = -40 °C, I_{LOAD} = 3 A	0.03	0.9	0.12	Ω	O2H1/2
OUTx_lkg	Output leakage current	Output disabled, diagnostic off Vpin = 13.5 V	-10	-	+10	µA	O2H1/2
Irev_OUTx	Body diode reverse current voltage drop	I_{LOAD} = -2 A	-	-	2	V	O2H1/2
SR_ON	Voltage slew ON State	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF; configure as O2	0.2	-	0.8	V/µs	O2H1/2
SR_ON_fast	Fast voltage slew ON State	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF; configure as sol, fast slew rate	2	-	6	V/µs	O2H1/2
SR_OFF	Voltage slew OFF state	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF; configure as O2	0.2	-	0.8	V/µs	O2H1/2
SR_OFF_fast	Fast Voltage slew OFF State	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF; configure as sol, fast slew rate	2	-	6	V/µs	O2H1/2

Table 46. Low-side driver - O2 HEATER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
S/RGkill_LSH	FAST VS/R off when an OVC fault happens	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF	5	-	20	V/µs	O2H1/2
Ton_OUTx	Propagation Delay from MSC_EN rising edge to 80% output OUTx voltage	VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF	-	-	12	µs	O2H1/2
Toff_OUTx	Propagation Delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load} = 3 Ω, C_{load} = 10 nF	-	-	10	µs	O2H1/2
Vclamp_OUTx	OUTx clamping Voltage	I_{LOAD} = 1.3 A	45	50	55	V	O2H1/2
Vclamp_OUTx_ high_curr	OUTx clamping Voltage	I_{LOAD} = 1.3 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	45	50	55	V	O2H1/2
I_ovc1_o2h	Over current driver threshold 1	configure as sol	3	4.5	6	A	O2H1/2
I_ovc2_o2h	Over current driver threshold 2	T_j = -40 °C configured as O2	8.6	-	12.4	A	O2H1/2
I_ovc2_o2h	Over current driver threshold 2	T_j = +25 °C configured as O2	8.0	-	11.2	A	O2H1/2
I_ovc2_o2h	Over current driver threshold 2	T_j = +150 °C configured as O2	7.8	-	10.5	A	O2H1/2
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	O2H1/2
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	O2H1/2
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	O2H1/2
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	O2H1/2
tmsd_pre_an	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	O2H1/2
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	O2H1/2
Driver reliability data							
EnergyRep O2H	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n =1.5A 18 Miopulses	-	-	15	mJ	O2H1/2
EnergyRep O2H	Energy repetitive pulses	T_{case}= 115 °C ; I_OT_n = 1.2A 648 Miopulses	-	-	10	mJ	O2H1/2

Table 46. Low-side driver - O2 HEATER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
EnergyRep O2H	Energy repetitive pulses	T_{case}= 130 °C ; I_OT_n = 1.0A 96 Miopulses	-	-	9	mJ	O2H1/2
EnergyRep O2H	Energy repetitive pulses	T_{case}= 140 °C ; I_OT_n = 1.0A 4 Miopulses	-	-	9	mJ	O2H1/2
Driver Reliability Data jump start							
EnergyRep O2H	Energy repetitive pulses	T_{case}= 25 °C ; I_OT_n = 2.2A 0.021 Miopulses 10 jumps starts over lifetime, each start<2	-	-	30	mJ	O2H1/2
EnergyRep O2H	Energy repetitive pulses	T_{case} = 75 °C ; I_OT_n = 1.8A 0.021 Miopulses 10 jumps starts over lifetime, each start < 2	-	-	18	mJ	O2H1/2
Driver reliability data generator defect							
EnergyRep O2H	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n = 1.6A 0.5 Miopulses	-	-	17.5	mJ	O2H1/2
EnergyRep O2H	Energy repetitive pulses	T_{case} = 135 °C ; I_OT_n = 1.1 A 0.5 Miopulses	-	-	10	mJ	O2H1/2
OFF state diagnostic							
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9	2.1	VOUT OPEN -180 mV	V	O2H1/2
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUT OPEN +160 mV	2.9	3.0	V	O2H1/2
VOL	Open load voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	O2H1/2
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”1”	2.5	3.6	4.7	mA	O2H1/2
I_LS_PU2	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”0”	40	70	100	µA	O2H1/2
I_LS_PD1	Diagnostic pull down current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB	60	85	105	µA	O2H1/2
Tflt_diagoff1	DIAG Filter time	Filter Mode = 0	75	100	125	µs	O2H1/2
Tflt_diagoff2	DIAG Filter time	Filter Mode = 1	450	600	750	µs	O2H1/2

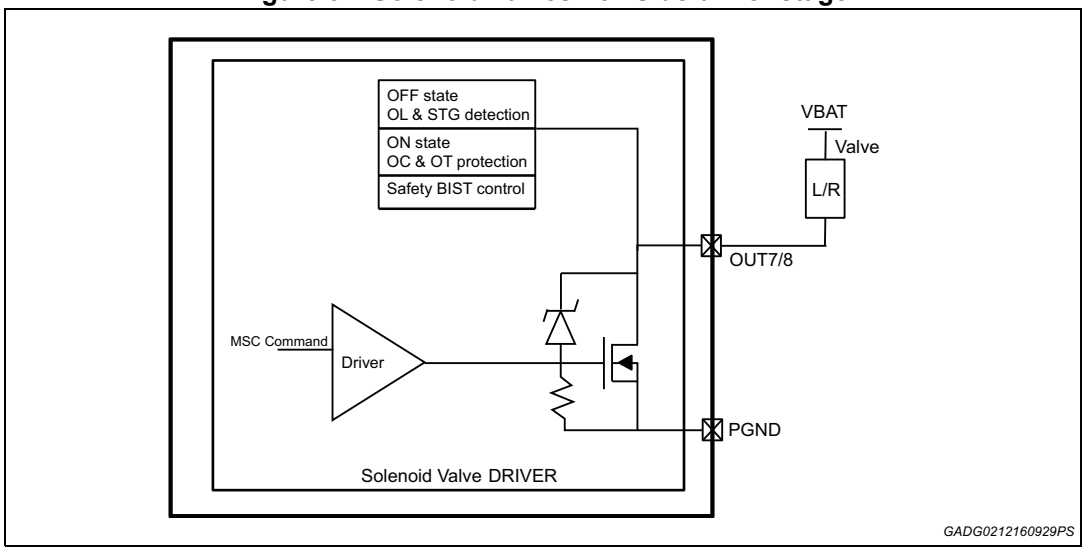
Table 46. Low-side driver - O2 HEATER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10 nF,) Filter Mode = 0	175	-	-	µs	O2H1/2
Current sensing characteristics							
Gain_sense	Transresistance sense gain	-		0.8		V/A	Curr_Sense _O2H1/2
V_OUT_0p5A	Output voltage AD for Ipower = 0.5 A	Rext = 5.1 kΩ	0.32	0.4	0.55	V	Curr_Sense _O2H1/2
V_OUT_1A	Output voltage AD for Ipower = 1 A	Rext = 5.1 kΩ	0.64	0.8	0.96	V	Curr_Sense _O2H1/2
V_OUT_2A	Output voltage AD for Ipower = 2 A	Rext = 5.1 kΩ	1.44	1.6	1.76	V	Curr_Sense _O2H1/2
V_OUT_3A	Output voltage AD for Ipower = 3 A	Rext = 5.1 kΩ	2.16	2.4	2.64	V	Curr_Sense _O2H1/2
V_OUT_4A	Output voltage AD for Ipower = 4 A	Rext = 5.1 kΩ	2.88	3.2	3.52	V	Curr_Sense _O2H1/2

7.4 Low-side driver - SOLENOID SOL [1:2]

These 2 LowSide drivers are designed to driver Solenoid Valves Load. They are driven by *MSC command.*The Output voltage is clamped to voltage limit by internal clamp circuit.

Figure 37. Solenoid valves LowSide driver stage



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified.

Table 47. Low-side driver - SOLENOID VALVE electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Solenoid valves							
LS_RdsON	Low-side RdsON	T_j = 150 °C, I_{LOAD} = 3 A	0.24	0.35	0.47	Ω	SOL1/2
LS_RdsON	Low-side RdsON	T_j = 25 °C, I_{LOAD} = 3 A	0.17	0.22	0.29	Ω	SOL1/2
LS_RdsON	Low-side RdsON	T_j = -40 °C, I_{LOAD} = 3 A	0.12	0.17	0.2	Ω	SOL1/2
OUTx_lkg	Output leakage current	Output disabled, diagnostic off Vpin = 13.5 V	-10	-	+10	µA	SOL1/2
Irev_OUTx	Body diode reverse current voltage drop	I_{LOAD} = -2 A	-	-	2	V	SOL1/2
SR_ON	Voltage slew ON state	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	0.6	-	1.75	V/µs	SOL1/2
SR_OFF	Voltage slew OFF state	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	0.6	-	1.75	V/µs	SOL1/2
S/RGkill_LSH	FAST VS/R off when an OVC fault happens	From 30% to 80%of VOUT VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	5	-	20	V/µs	SOL1/2

Table 47. Low-side driver - SOLENOID VALVE electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ton_OUTx	Propagation delay from MSC_EN rising edge to 80% output OUTx voltage	VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	-	-	8	µs	SOL1/2
Toff_OUTx	Propagation delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load} = 15 Ω, C_{load} = 10 nF	-	-	8	µs	SOL1/2
Vclamp_OUTx	OUTx clamping voltage	I_{LOAD} = 1.3 A	50	55	60	V	SOL1/2
Vclamp_OUTx _high_curr	OUTx clamping voltage	I_{LOAD} = 3 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	50	55	60	V	SOL1/2
I_ovc_sol	Over current driver threshold	-	3	4.5	6	A	SOL1/2
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	SOL1/2
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	SOL1/2
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	SOL1/2
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	SOL1/2
-	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	SOL1/2
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	SOL1/2
OFF state diagnostic							
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9	2.1	VOUT OPEN -180mV	V	SOL1/2
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUT OPEN +160mV	2.9	3.0	V	SOL1/2
VOL	Open load voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	SOL1/2
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”1”	2.5	3.6	4.7	mA	SOL1/2
I_LS_PU2	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”0” and IDIAG_HIGH_SOL =”0”	40	70	100	µA	SOL1/2

Table 47. Low-side driver - SOLENOID VALVE electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_LS_PU3	Diagnostic pull up high current	In OFF condition, OUTx < VLVT, Ipupd_EN=ENB,Ipupd_MODE=”0” and IDIAG_HIGH_SOL =”1”	100		200	µA	SOL1/2
I_LS_PD1	Diagnostic pull down current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB and IDIAG_HIGH_SOL =”0”	60	85	105	µA	SOL1/2
II_LS_PD2	Diagnostic pull down high current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB IDIAG_HIGH_SOL =”1”	325	-	550	µA	SOL1/2
Tflt_diagoff1	DIAG filter time	Filter mode = 0	75	100	125	µs	SOL1/2
Tflt_diagoff2	DIAG filter time	Filter mode = 1	450	600	750	µs	SOL1/2
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10nF,) Filter Mode=0	175	-	-	µs	SOL1/2
Driver reliability data							
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n =1.5A 18 Miopulses	-	-	15	mJ	SOL1/2
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 115 °C ; I_OT_n = 1.2 A 648 Miopulses	-	-	10	mJ	SOL1/2
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 130 °C ; I_OT_n = 1.0 A 96 Miopulses	-	-	9	mJ	SOL1/2
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 140 °C ; I_OT_n = 1.0 A 4 Miopulses	-	-	9	mJ	SOL1/2
Driver reliability data generator defect							
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n = 1.6 A 0.5 Miopulses	-	-	17.5	mJ	SOL1/2
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 135 °C ; I_OT_n = 1.1 A 0.5 Miopulses	-	-	10	mJ	SOL1/2
Driver reliability data JUMP START							
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n = 2.2 A 0.021 Miopulses 10 jumps starts over lifetime, each start < 2 min	-	-	30	mJ	SOL1/2
Energy_Rep_SOL	Energy repetitive pulses	T_{case} = 75 °C ; I_OT_n = 1.8 A 0.021 Miopulses 10jumps starts over lifetime, each start < 2 min	-	-	18	mJ	SOL1/2

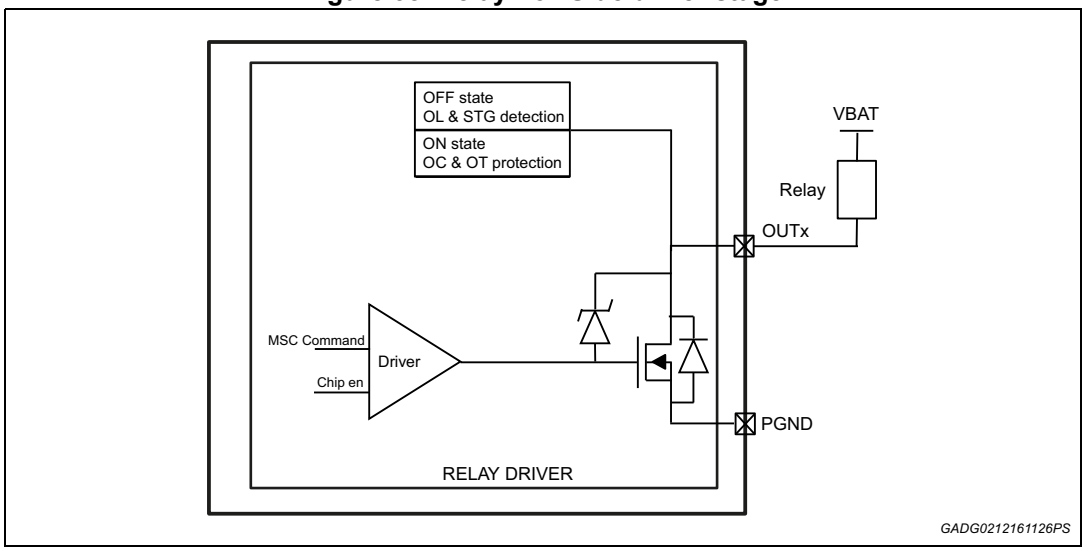
7.5 Low-side driver - RELAY RLY [1:5]

These 5 LowSide drivers are optimized for relay or generic low current loads driving. They are driven by MSC command. The Output voltage is clamped to voltage limit by internal clamp circuit.

Each relay driver is separately put in on or off state by the *MSC CONFIG-REG 14 [0:4]* just for the time required to perform on or off diagnosis (Fast Diagnosis). At the end of the diagnosis it is automatically put in the state determined by the current value of MSC data frame.

The micro command is activated by writing 1 from 0 in the MSC registers (both for ON and OFF).

Figure 38. Relay LowSide driver stage



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified; the RLY4 can be associated to DELAY_OFF function if the MSC *CONFIG_REG_3 [0] = RLY4_DLY_OFF_EN* is set. In this case the RLY4 is configured as starter and can work down to VB_IN = 3.1 V for THOLD.

Table 48. Low-side driver - RELAY electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Relay							
LS_RdsON	Low-side RdsON	T_j = 150 °C, I_{LOAD} = 1 A	-	-	1.5	Ω	RLY/1/2/3/4/5
LS_RdsON	Low-side RdsON	T_j = 25 °C, I_{LOAD} = 1 A	-	-	0.82	Ω	RLY/1/2/3/4/5
LS_RdsON	Low-side RdsON	T_j = 40 °C, I_{LOAD} = 1 A	-	-	0.63	Ω	RLY/1/2/3/4/5

Table 48. Low-side driver - RELAY electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
LS_RdsON_ RL4	Low-side RdsON	VB_IN = 3.1 V, I_{LOAD} = 0.6 A	-	-	3	Ω	RLY4
OUTx_lkg	Output leakage current	Output disabled, diagnostic off	-10	-	+10	µA	RLY/1/2/3/4/5
Irev_OUTx	Body diode reverse current voltage drop	I_{LOAD} = -0.6 A	-	-	2	V	RLY/1/2/3/4/5
SR_ON	Voltage slew ON State	From 80% to 30% of VOUT, VB_IN = 14 V, R_{load} = 68 Ω C_{load} = 10 nF	0.4	-	2.1	V/µs	RLY/1/2/3/4/5
SR_OFF	Voltage slew OFF State	From 30% to 80% of VOUT, VB_IN = 14 V, R_{load} = 68 Ω C_{load} = 10 nF	0.4	-	2.1	V/µs	RLY/1/2/3/4/5
S/RGkill	FAST VS/R off when an OVC fault happens	From 30% to 80% of VOUT, VB_IN = 14 V, R_{load} = 68 Ω C_{load} = 10 nF	5	-	20	V/µs	RLY/1/2/3/4/5
Ton_OUTx	Propagation Delay from MSC_EN rising edge to 80% output OUTx voltage	VOUT, VB_IN = 14 V, R_{load} = 68 Ω C_{load} = 10 nF	-	-	10	µs	RLY/1/2/3/4/5
Toff_OUTx	Propagation Delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load} = 68 Ω C_{load} = 10 nF	-	-	10	µs	RLY/1/2/3/4/5
Vclamp_OUTx	OUTx clamping Voltage	I_{LOAD} = 0.6 A	45	-	55	V	RLY/1/2/3/4/5
Vclamp_OUTx _high_curr	OUTx clamping Voltage	I_{LOAD} = 1 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	45	-	55	V	RLY/1/2/3/4/5
-	Over current driver threshold	-	1	1.5	2	A	RLY/1/2/3/4/5
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	RLY/1/2/3/4/5
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	RLY/1/2/3/4/5

Table 48. Low-side driver - RELAY electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	RLY/1/2/3/4/5
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	RLY/1/2/3/4/5
-	Thermal shutdown analog filter time	Guaranteed by design	1.5		4	µs	RLY/1/2/3/4/5
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	RLY/1/2/3/4/5
Driver reliability data							
EnergyRep RLY	Energy repetitive pulses	T_{case} = 25 °C; I_OT_n = 0.45 A 1.1 Miopulses	-	-	9	mJ	RLY/1/2/3/4/5
EnergyRep RLY	Energy repetitive pulses	T_{case} = 115 °C; I_OT_n = 0.3 A 40 Miopulses	-	-	6.5	mJ	RLY/1/2/3/4/5
EnergyRep RLY	Energy repetitive pulses	T_{case} = 130 °C; I_OT_n = 0.3 A 9 Miopulses	-	-	6.5	mJ	RLY/1/2/3/4/5
EnergyRep RLY	Energy repetitive pulses	T_{case} = 140 °C; I_OT_n = 0.3 A 1 Miopulses	-	-	6.5	mJ	RLY/1/2/3/4/5
Driver reliability data generator defect							
EnergyRep RLY	Energy repetitive pulses	T_{case} = 25 °C; I_OT_n = 0.5 A 0.02 Miopulses	-	-	11	mJ	RLY/1/2/3/4/5
EnergyRep RLY	Energy repetitive pulses	Tc=135°C; I_OT_n = 0.35 A 0.02 Miopulses	-	-	8	mJ	RLY/1/2/3/4/5
Driver reliability data JUMP START							
EnergyRep RLY	Energy repetitive pulses	T_{case} = 25 °C; I_OT_n = 0.75 A 0.001 Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	25	mJ	RLY/1/2/3/4/5
EnergyRep RLY	Energy repetitive pulses	Tc=75°C ; I_OT_n=0.5A 0.001Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	17	mJ	RLY/1/2/3/4/5

Table 48. Low-side driver - RELAY electrical characteristics (continued)

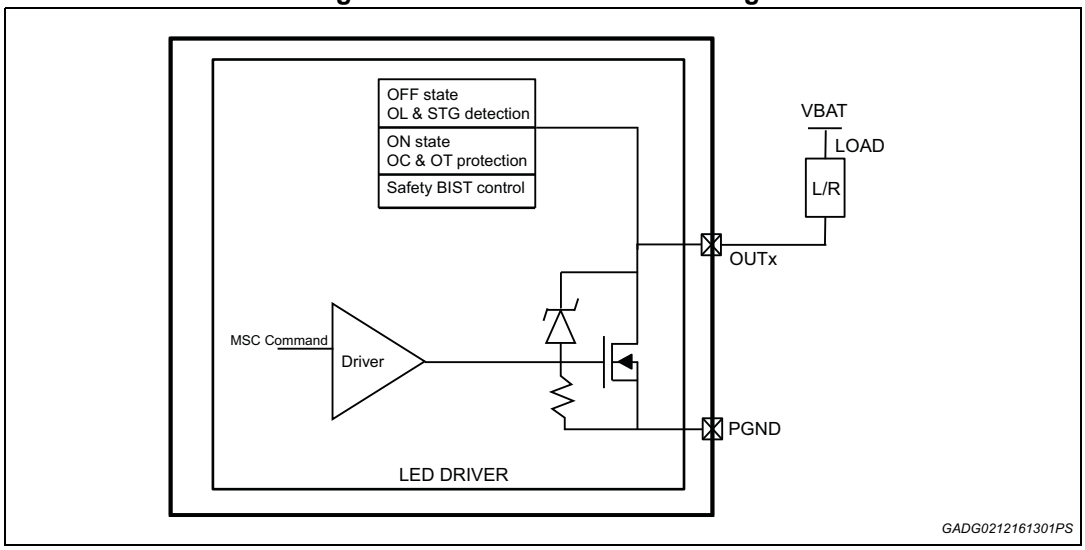
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
OFF state diagnostic							
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9		VOUTOPEN -180mV	V	RLY/1/2/3/4/5
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUTOPEN +160mV		3.0	V	RLY/1/2/3/4/5
VOUTOPEN	Open load output voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	RLY/1/2/3/4/5
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”1”	2.3	3.6	4.7	mA	RLY/1/2/3/4/5
I_LS_PU2	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”0”	40	70	100	µA	RLY/1/2/3/4/5
I_LS_PD1	Diagnostic pull down current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB	60	85	105	µA	RLY/1/2/3/4/5
Tflt_diagoff1	DIAG Filter time	Filter Mode=0	75	100	125	µs	RLY/1/2/3/4/5
Tflt_diagoff2	DIAG Filter time	Filter Mode=1	450	600	750	µs	RLY/1/2/3/4/5
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10 nF,) Filter Mode = 0	175	-	-	µs	RLY/1/2/3/4/5
-	Fast OFF diagnostic ON→OFF→ON	Filter Mode = 0	175	200	225	µs	RLY/1/2/3/4/5
-	Fast ON diagnostic OFF→ON→OFF	-	72		90	µs	RLY/1/2/3/4/5

7.6 Low-side driver - LED[1:2]

These 2 LowSide drivers are designed to drive LED Load. They are driven by *MSC command*. The Output voltage is clamped to voltage limit by internal clamp circuit.

The pull down diagnostic current of LED driver is configurable by MSC (*LEDx_PD_EN CONFIG_REG1 D3;D4*). Overcurrent and Short to Ground diagnostic function are available, open load diagnostic function is not available when pull down diagnostic current is disabled.

Figure 39. LED LowSide driver stage



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 49. Low-side driver - LED electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
LED							
LS_RdsON	Low-side RdsON	T_j = 150 °C, I_{LOAD} = 70 mA	10	14	20	Ω	LED1/2
		T_j = 25 °C, I_{LOAD} = 70 mA	6	8	12	Ω	LED1/2
		T_j = -40 °C, I_{LOAD} = 70 mA	4.9	6	9	Ω	LED1/2
OUTx_Ikg	Output leakage current	Output disabled, diagnostic off	-10	-	+10	µA	LED1/2
Irev_OUTx	Body diode reverse current voltage drop	I_{LOAD} = -50 mA	-	-	2	V	LED1/2
SR_ON	Voltage slew ON state	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 270 Ω,	10	-	25	V/µs	LED1/2
SR_OFF	Voltage slew OFF state	From 30% to 80%of VOUT VB_IN = 14 V, R_{load} = 270 Ω	14	-	21	V/µs	LED1/2

Table 49. Low-side driver - LED electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ton_OUTx	Propagation Delay from MSC_EN rising edge to 80% output OUTx voltage	VB_IN = 14 V, R_{load}=270 Ω,	-	-	5	µs	LED1/2
Toff_OUTx	Propagation Delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load}=270 Ω,	-	-	5	µs	LED1/2
Vclamp_OUTx	OUTx clamping Voltage	I_{LOAD} = 50 mA	40	45	50	V	LED1/2
Vclamp_OUTx_ high_curr	OUTx clamping Voltage	I_{LOAD} = 70 mA Guaranteed by design, provided single pulse energy limits are not violated by clamping action	40	45	50	V	LED1/2
IOVC_OUTx	Over current driver threshold	-	70	-	110	mA	LED1/2
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	LED1/2
VLVT	Short to GND threshold voltage	Driver tristate, diag enabled	1.9	-	VOUTOPEN -180mV	V	LED1/2
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUTOPEN +160mV	-	3	V	LED1/2
VOUTOPEN	Open load voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	LED1/2
I_LS_PU1	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE = ”1”	2.5	3.6	4.7	mA	LED1/2
I_LS_PU2	Diagnostic pull up current	In OFF condition, OUTx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”0”	40	70	100	µA	LED1/2
I_LS_PD1	Diagnostic pull down current	In OFF condition, OUTx > VOUTOPEN, Ipupd_EN = ENB LEDx_PD_EN = 1	60	85	105	µA	LED1/2
Tflt_diagoff1	DIAG filter time	Filter Mode = 0	75	100	125	µs	LED1/2

Table 49. Low-side driver - LED electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Tflt_diagoff2	DIAG Filter time	Filter Mode = 1	450	600	750	µs	LED1/2
-	Minimum OFF time for correct diagnostic	Application note (esd cap < 10nF,) Filter Mode=0	175	-	-	µs	LED1/2

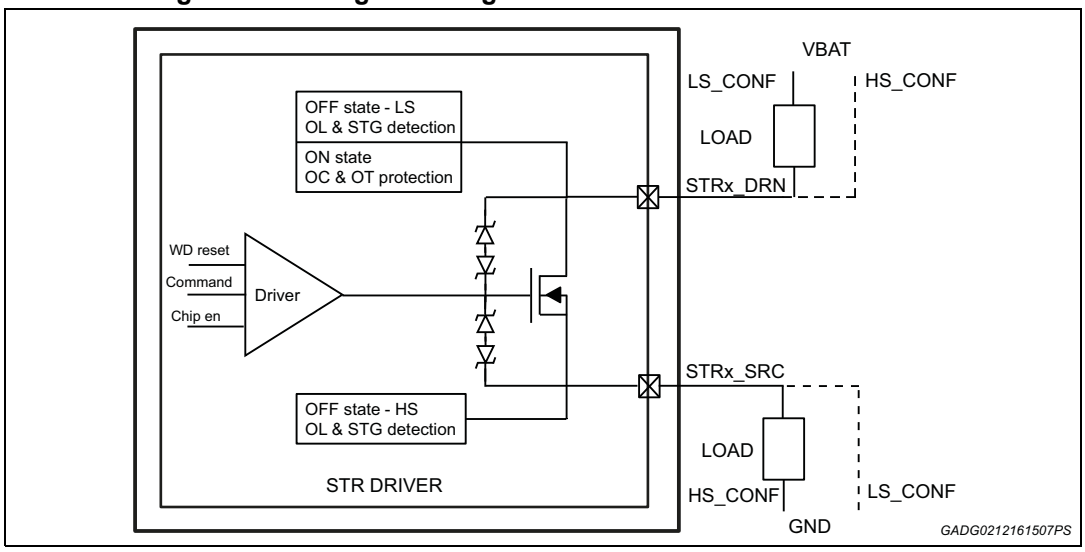
8 High/low-side drivers - STARTER STR[1:3]

These 3 high/low-side drivers with diagnosis and overcurrent protection have a floating architecture and can be used in high-side or low-side mode.

The configuration is defined by MSC bit (*LSD/HSD_DRVx-CFG CONFIG_REG3 D1~D3*). The driver is optimized for relay and low-current loads, and it can be associated to smart starter functional block.

They are driven by MSC command. The Output voltage is clamped to voltage limit by internal clamp circuit. In order to guarantee a negligible output current in case of LED application an internal dedicated comparator is present. This comparator, in case of high-side configuration, Diagoff disabled and channel OFF, determines the disabling of internal driver in case of output voltage (STR_SRC) pin in the range of -0.4V typ < STR_SRC< 1.8V typ. This implementation guarantees a negligible output current down to 0V on STR_SRC pin (where internal compensation is no more effective) and at the same time the correct re-enabling of the driver when the output voltage goes negative, in order to guarantee the correct clamping functionality during recirculation. In any other condition (Low-side configuration, or Diagoff enabled, or channel ON) the effect of this comparator is masked and an output current will be observed.

Figure 40. Configurable high/low -side Driver block schematic



The driver has the following detection diagnosis in low-side mode:

- Overcurrent (Short to Vbat) protection in On Phase (OVC);
- Open Load in Off phase (DIAGOL);
- Short to Ground in Off Phase (DIAGLV);
- Over Temperature Protection in On phase (OT);
- The driver has the following detection diagnosis in high-side mode:
  Overcurrent (Short To GND) protection in On Phase (OVC);
- Open Load in Off phase (DIAGOL);
- Short to battery in Off Phase (DIAGHV);
- Over Temperature Protection in On phase (OT);

In low-side configuration, if they are configured as starter *CONFIG_REG3[4]=STR2_EN=1* and *CONFIG_REG3[5]=STR3_EN=1*, the driver STR2 and STR3 can work down to VB_IN = 3.1 V. for THOLD.

In high-side configuration, if they are configured as starter *CONFIG_REG3[4]=STR2_EN=1* and *CONFIG_REG3[5]=STR3_EN=1*, the driver STR2 and STR3 can work down to VB_IN = 3.1 V for THOLD.

Furthermore, the driver can latch its ON state for THOLD even if the main microcontroller is temporarily not working due to low-battery conditions.

HS/LS are intended to be used as starter relay driver. One for high-side, one for low-side. STR2/3 should keep the status till VOFF_VB_IN.(3.1 V).

Each starter driver is separately put in on or off state by the *MSC CONFIG-REG 14[5:7]* just for the time required to perform on or off diagnosis (Fast Diagnosis). At the end of the diagnosis it is automatically put in the state determined by the current value of *MSC data frame*.

The micro command is activated by writing 1 from 0 in the MSC registers (both for ON and OFF).

8.1 ON state diagnosis

The ON state diagnosis has the same features as the low-side driver ON state diagnosis described in chapter *Section 7.1.1* and *Section 7.1.2*.

8.2 ON/OFF state - Error in on status diagnosis

Refer to paragraph *Section 7.1.3*.

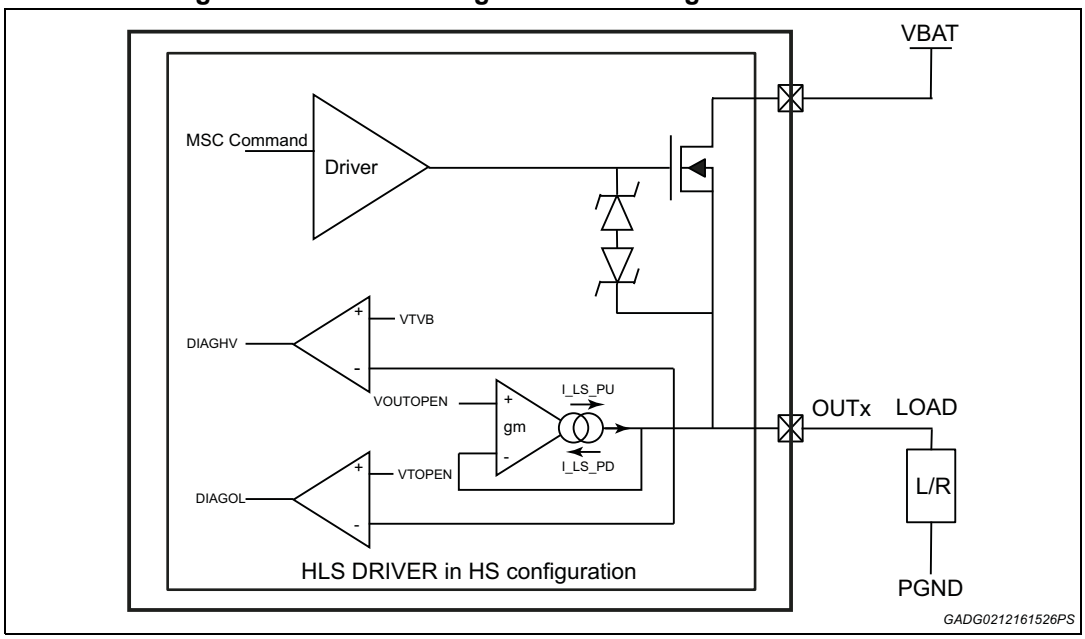
8.3 OFF state diagnosis LS mode

The OFF state diagnosis in LS mode has the same features as the low-side driver OFF state diagnosis described in paragraph *Section 7.1.4*.

8.4 OFF state diagnosis HS mode

The device provides off-state diagnostic for HS mode, simplified schematic of implemented diagnostic is shown in *Figure 41*.

Figure 41. OFF state diagnostic HS config block schematic



In the HS mode we can have three different load conditions:

- Normal Load, it means output driver connected to the load, No Fault Present, VOUT≤ V_OL Threshold;
- Open Load, It means output driver disconnected to the load, Open Load Fault Present, VHVT ≥ VOUT ≥ V_OL Threshold;
- Short To VB, it means output driver shorted to VB voltage, Short To VB Fault Present, VOUT > VHVT.

There is a bit *IPUPD_EN_STRx* in CONFIG_REG13 which is controlled by a MSC bit, it is used by external µController if it is needed to switch on/off both pull up and pull down diagnosis current.

There is a bit *IPUPD_MODE* in CONFIG_REG2 which is controlled by a MSC bit, it is used by external uController if it is needed to switch on/off the bigger diagnosis current(I_HS_PD1) in fast mode.

The Diagnostic in Off state is done by the following block:

- An internal Buffer using the pull up/down currents is able to force the VOUTOPEN voltage on the High-Side Driver Output when the driver is in Open Load Condition.
- A comparator to detect the Open load Condition. The Open Load fault is detected when the OUTx pin is VHVT >= VOUT>= V_OL Threshold for a time longer than Diag Filter Time.
- A comparator to detect the Short to VB Condition. The Short To VB fault is detected when the OUTx pin is VOUT >= VHVT Threshold for a time longer than Diag Filter Time.
- Fast pull down current, this current is used to avoid the false short to VB diagnosis when the driver switches off in Open load condition. This current switches on after the falling edge of *MSC command* (driver in off state) and remains on until the Diag Filter Time is expired or until the VOUT is < VHVT Threshold. (Note: if fast pull down current is selected, the filter time Tflt_diagoff1 is suggested. Otherwise, the filter time Tflt_diagoff2 is suggested).

Figure 42. OFF state diagnostic HS config

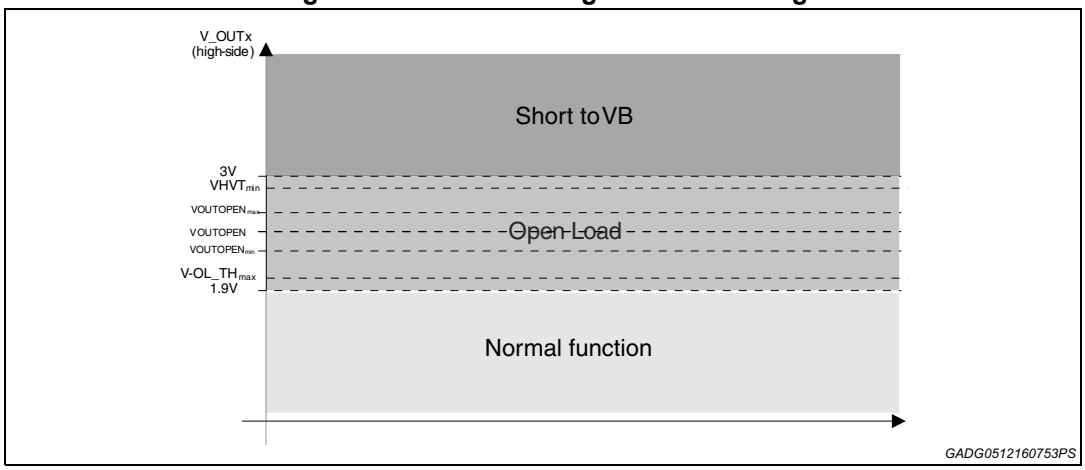
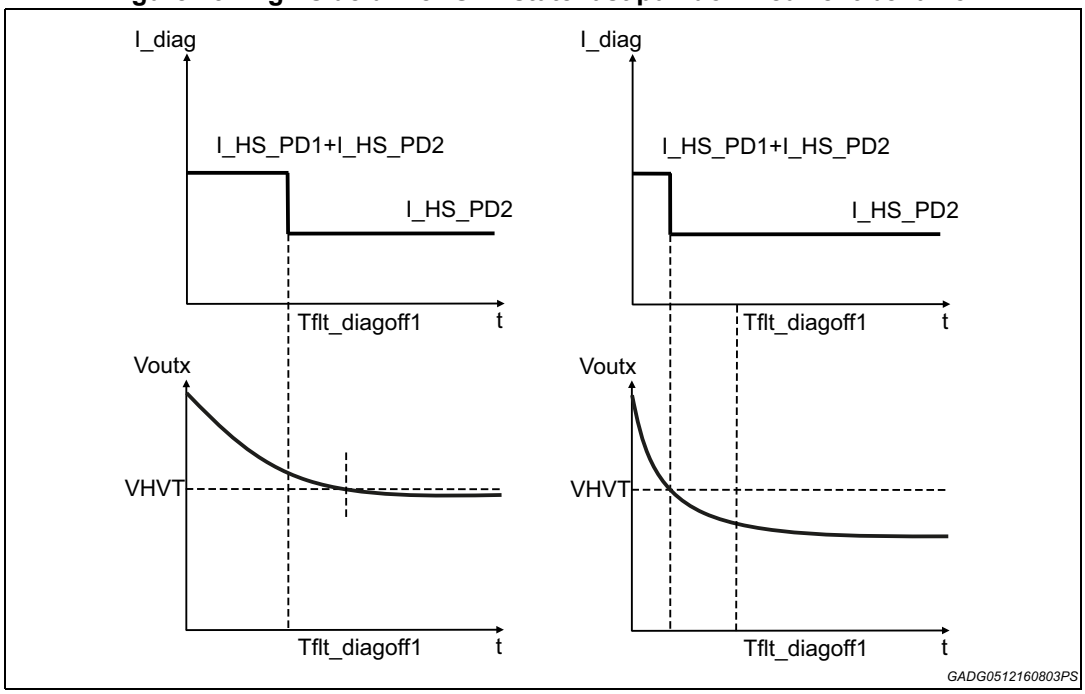


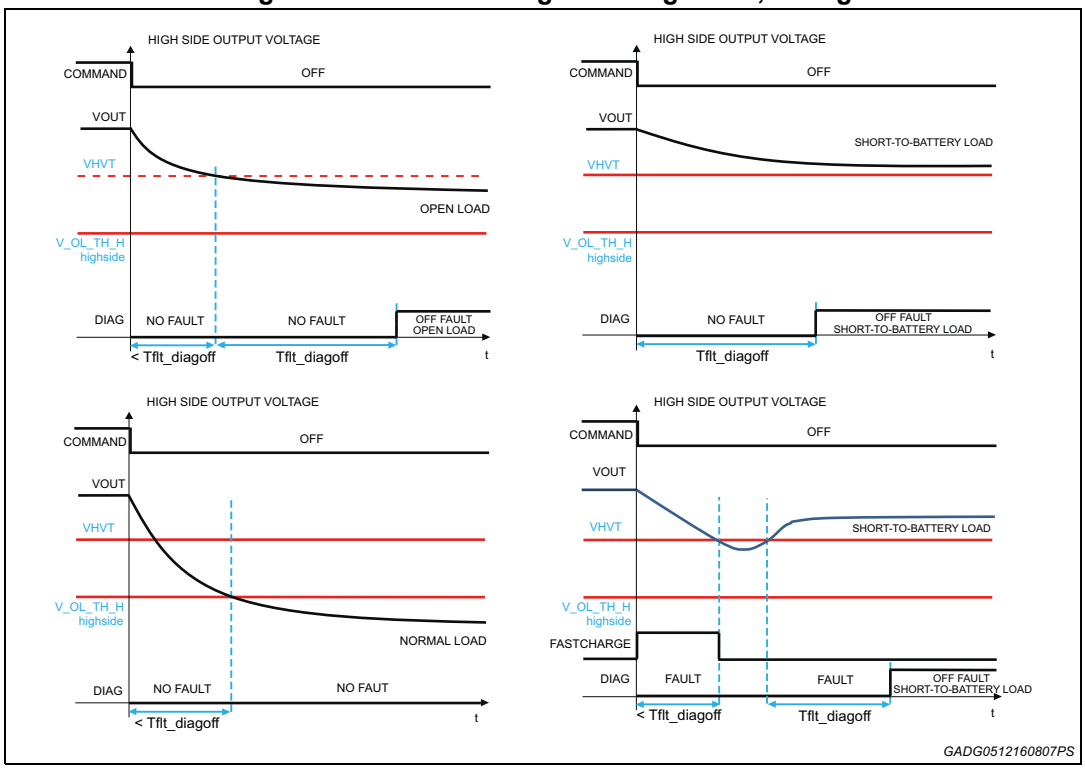
Figure 43. High-side driver OFF state fast pull down current behavior



By default diagnostic pull up/down currents are disabled and comparator outputs are masked by internal logic, to enable OFF state diagnostic the channel must be put first in tristate condition and then (if not already done with previous MSC frames) diagnostic must be enabled. Once the desired channel is put in tristate a false diagnostic can be sensed due to the time needed to discharge output voltage through the load.

A Filter Time (Diag Filter Time) is implemented in order to avoid detecting false diagnosis as shown in *Figure 44*.

Figure 44. OFF state diagnostic high-side, timing



If DiagOL or DiagHV signal remains high for a time higher than Diag Filter Time the fault bit is set and can be read by Read Diag Communication.

This bit can be reset by every Read Diag Communication.

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 50. High/low-side driver - STARTER electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Irev_OUTx	Body diode reverse current voltage drop	I_{LOAD} = -0.6 A	-	-	1	V	STR1/2/3
Relay HS configuration							
RdsON	Drain-source resistance	HS configuration VB_IN = 13.5 V; T_j =150 °C, I_load = 1A	-	-	1.5	Ω	STR1/2/3
RdsON	Drain-source resistance	HS configuration VB_IN = 13.5 V; T_j = 25 °C, I_load = 1 A	-	-	0.81	Ω	STR1/2/3
RdsON	Drain-source resistance	HS configuration VB_IN = 13.5 V; T_j =40 °C, I_load = 1 A	-	-	0.63	Ω	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RdsON	Drain-source resistance	HS configuration VB_IN = 3.1 V I_load = 1 A	-	-	3	Ω	STR1/2/3
STR_SRC_lkg	Output leakage current	Driver disabled, diagnostic off; HSide configuration	-10	-	+10	µA	STR1/2/3
SR_ON	HS configuration Voltage slew ON State	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 68 Ω	0.7	-	2.1	V/µs	STR1/2/3
SR_OFF	HS configuration Voltage slew OFF State	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 68 Ω	0.7	-	2.1	V/µs	STR1/2/3
S/RGkill_HS	FAST VS/R off when an OVC fault happens high-side configuration	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 68 Ω	5	-	20	V/µs	STR1/2/3
Ton_OUTx_Hside	Propagation Delay from MSC_EN rising edge to 20% output OUTx voltage	VB_IN = 14 V, R_{load} = 68 Ω	-	-	10	µs	STR1/2/3
Toff_OUTx_Hside	Propagation Delay from MSC_EN falling edge to 80% output OUTx voltage	VB_IN = 14 V, R_{load} = 68 Ω	-	-	10	µs	STR1/2/3
Vclamp_OUTx_HS	OUTx clamping voltage HS configuration	I_{LOAD} = 0.6 A	-4.1	-	-2.5	V	STR1/2/3
-	Over current driver threshold HS configuration	-	1	1.5	2	A	STR1/2/3
I_HS_ocv_flt	HS overcurrent filter time	Guaranteed by scan	4	-	7	µs	STR1/2/3
Relay LS configuration							
RdsON	Drain-source resistance	LS configuration VB_IN = 13.5 V Tj = 150 °C I_load = 1A	-	-	1.5	Ω	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RdsON	Drain-source resistance	LS configuration VB_IN = 13.5 V, T_j = 25 °C, I_load = 1 A	-	-	0.81	Ω	STR1/2/3
RdsON	Drain-source resistance	LS configuration VB_IN = 13.5 V T_j = -40 I_load = 1 A	-	-	0.63	Ω	STR1/2/3
RdsON	Drain-source resistance	LS configuration VB_IN = 3.1 V I_load = 1 A	-	-	3	Ω	STR1/2/3
STR_DRN_lkg	Output leakage current	Output disabled, diagnostic off ; Low-Side configuration, DRN1=DRN2=DRN3=18 V, total current from 3 pins, T=-40 °C, 27 °C	-10	-	+18	µA	STR1/2/3
STR_DRN_lkg	Output leakage current	Output disabled, diagnostic off ; Low-Side configuration, DRN1=DRN2=DRN3=18 V, total current from 3 pins, T = 175 °C	-10	-	+48	µA	STR1/2/3
SR_ON	LS configuration voltage slew ON State	From 80% to 30% of VOUT VB_IN = 14 V, R_{load} = 68 Ω	0.8	-	2.5	V/µs	STR1/2/3
SR_OFF	LS configuration voltage slew OFF State	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 68 Ω,	0.8	-	2.5	V/µs	STR1/2/3
S/RGkill_LS	FAST VS/R off when an OVC fault happens in low-side configuration	From 30% to 80% of VOUT VB_IN = 14 V, R_{load} = 68 Ω,	5	-	20	V/µs	STR1/2/3
Ton_OUTx_Lside	Propagation Delay from MSC_EN rising edge to 80% output OUTx voltage	VB_IN =14 V, R_{load} = 68 Ω,	-	-	10	µs	STR1/2/3
Toff_OUTx_Lside	Propagation Delay from MSC_EN falling edge to 20% output OUTx voltage	VB_IN=14V, R_{load} = 68 Ω,	-	-	10	µs	STR1/2/3
Vclamp_OUTx_LS	OUTx clamping voltage LS configuration	I_{LOAD} = 0.6 A	40	-	50	V	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Vclamp_OUTx_LS_high_curr	OUTx clamping voltage LS configuration	I_{LOAD} = 1 A Guaranteed by design, provided single pulse energy limits are not violated by clamping action	40	-	50	V	STR1/2/3
	Over current driver threshold LS configuration	-	1	1.5	2	A	STR1/2/3
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	4	-	7	µs	STR1/2/3
Driver reliability data as Low-Side							
EnergyRep	Energy repetitive pulses	T_{case} = 25 °C ; I_OT_n = 0.45 A 1.1 Miopulses	-	-	9	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	T_c = 115 °C ; I_OT_n = 0.3 A 40 Miopulses	-	-	6.5	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	T_c =130 °C ; I_OT_n = 0.3 A 9 Miopulses	-	-	6.5	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	T_c = 140 °C ; I_OT_n = 0.3 A 1 Miopulses	-	-	6.5	mJ	STR1/2/3
Driver reliability data as High-Side							
EnergyRep	Energy repetitive pulses	T_{case} = 25 °C ; I_OUT_n = 0.45 A 1.1 Miopulses	-	-	12.5	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	Tc = 115 °C ; I_OT_n = 0.3 A 40 Miopulses	-	-	9	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	Tc = 130 °C ; I_OT_n = 0.3 A 9 Miopulses	-	-	9	mJ	STR1/2/3
EnergyRep	Energy repetitive pulses	Tc = 140 °C ; I_OT_n = 0.3 A 1 Miopulses	-	-	9	mJ	STR1/2/3
Driver reliability data generator defect as Low-Side							
EnergyRep STR	Energy repetitive pulses	Tc = 25 °C ; I_OT_n = 0.5 A 0.02 Miopulses	-	-	11	mJ	STR1/2/3
EnergyRep STR	Energy repetitive pulses	Tc = 135 °C ; I_OT_n = 0.35 A 0.02 Miopulses	-	-	8	mJ	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Driver reliability data generator defect as High-Side							
EnergyRep STR	Energy repetitive pulses	Tc = 25 °C ; I_OT_n = 0.5 A 0.02 Miopulses	-	-	15	mJ	STR1/2/3
EnergyRep STR	Energy repetitive pulses	Tc = 135 °C ; I_OT_n = 0.35 A 0.02 Miopulses	-	-	11	mJ	STR1/2/3
Driver reliability data JUMP START as Low-Side							
EnergyRep STR	Energy repetitive pulses	Tc = 25 °C ; I_OT_n = 0.75A 0.001 Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	25	mJ	STR1/2/3
EnergyRep STR	Energy repetitive pulses	Tc = 75 °C ; I_OT_n = 0.5 A 0.001 Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	17	mJ	STR1/2/3
Driver reliability data JUMP START as High-Side							
EnergyRep STR	Energy repetitive pulses	Tc = 25 °C ; I_OT_n = 0.75 A 0.001 Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	31	mJ	STR1/2/3
EnergyRep STR	Energy repetitive pulses	Tc = 75 °C; I_OT_n = 0.5 A 0.001 Miopulses, 10 jumps starts over lifetime, each start < 2 min	-	-	21	mJ	STR1/2/3
OFF state diagnostic – HS configuration							
VHVT	Short to VB threshold voltage	HS configuration	VOUT OPEN +160mV	-	3.0	V	STR1/2/3
V_OL_TH_Highside	Open load threshold voltage	HS configuration	1.9	-	VOUT OPEN -180mV	V	STR1/2/3
VOUTOPEN_Highside	Open load threshold voltage	HS configuration	2.3	2.5	2.7	V	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_HS_PD1	Diagnostic pull down current in high-side configuration	In OFF condition, OUTx STRx_SRC >VHVT, Ipupd_EN IPUPD_EN_STRx =ENB, Ipupd_MODE =”1”	2.5	3.6	4.7	mA	STR1/2/3
I_HS_PD2		In OFF condition, OUTx STRx_SRC >VHVT, Ipupd_EN IPUPD_EN_STRx =ENB, Ipupd_MODE =”0”	40	70	100	µA	STR1/2/3
I_HS_PU1	Diagnostic pull up current in high-side configuration	In OFF condition, OUTx STRx_SRC <VOUTOPEN, Ipupd_EN IPUPD_EN_STRx =ENB STR_SRCx = 1.9 V	35	-	75	µA	STR1/2/3
I_HS_PU2		In OFF condition, OUTx STRx_SRC <VOUTOPEN, Ipupd_EN IPUPD_EN_STRx =ENB STR_SRCx = 0 V	100	-	180	µA	STR1/2/3
I_HS_OUT_Dis1	Output current in high-side configuration (measured on STR_SRC)	OFF condition, Diagoff disabled, STR_SRC > or = 0 V	-15	-	+15	µA	STR1/2/3
I_HS_OUT_Dis2		OFF condition, Diagoff disabled, STR_SRC < 0 V	-190	-	+10	µA	STR1/2/3
V_negative_threshold	Output voltage of STR_SRC below which the output current is measured again	OFF condition, Diagoff disabled Guaranteed by design	-	-	-0.2	V	STR1/2/3
V_positive_threshold	Positive threshold of internal comparator responsible of remove output current on STR_SRC pin (over this voltage negligible current is guaranteed by compensation circuit)	OFF condition, Diagoff disabled Guaranteed by design	-	1.8	-	V	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Tflt_diagoff2	-	Guaranteed by scan Cload = 15 nF	1000	1200	1500	us	STR1/2/3
Tflt_diagoff1	-	Guaranteed by scan Cload = 15 nF	130	160	200	us	STR1/2/3
OFF state diagnostic – LS configuration							
VLVT	Short to GND threshold voltage	LS configuration	1.9	-	VOUT OPEN -180mV	V	STR1/2/3
V_OL_TH_Lowside	Open load threshold voltage	LS configuration	VOUT OPEN +160mV	-	3.0	V	STR1/2/3
VOUTOPEN_Lowside	Open load voltage	LS configuration	2.3	2.5	2.7	V	STR1/2/3
I_LS_PU1	Diagnostic pull up current in Ls configuration	In OFF condition, STRx_DRN < VLVT, IPUPD_EN_STRx =ENB, Ipupd_MODE =”1”	2.5	3.6	4.7	mA	STR1/2/3
I_LS_PU2		In OFF condition, STRx_DRN < VLVT, IPUPD_EN_STRx =ENB, Ipupd_MODE =”0”	40	70	100	µA	STR1/2/3
I_LS_PD1	Diagnostic pull down current in Ls configuration	In OFF condition, STRx_DRN > VOUTOPEN, IPUPD_EN_STRx =ENB	55	85	100	µA	STR1/2/3
Tflt_diagoff2	DIAG Filter time in Ls configuration Filter Mode = 1	Guaranteed by scan Cload = 15 nF	450	600	750	µs	STR1/2/3
Tflt_diagoff1	DIAG Filter time in Ls configuration fast discharge enable Filter Mode = 0 (fast diag off)	Guaranteed by scan Cload = 15 nF	75	100	125	µs	STR1/2/3
Common diagnostic – LS/HS configuration							
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	STR1/2/3
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	STR1/2/3
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	STR1/2/3

Table 50. High/low-side driver - STARTER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
-	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	STR1/2/3
t_SD_deglitch	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	STR1/2/3
-	Fast OFF diagnostic ON->OFF->ON	Filter Mode=0	220	245	270	µs	STR1/2/3
-	Fast ON diagnostic OFF->ON->OFF	-	65	-	90	µs	STR1/2/3

8.5 Delay-off function

The Delay-off function involves the RLY4 and STR[2:3] drivers when they are configured as starters by the bit *MSC_CONFIG_REG3[0]=RLY4_DELAY_OFF_EN=1, CONFIG_REG3[4]=STR2_EN=1, CONFIG_REG3[5]=STR3_EN=1*. These drivers follow the reset matrix as other drivers when they are not configured as starters.

If the drivers are configured as starter and it is in on state its delay-off timer starts when one of the following events occurs:

- under-voltage of the main supply VDD5 is detected,
- over-voltage of the main supply VDD5 is detected,
- the MSC time out occurs,
- an active signal ("0") at pin WDA(IN),
- an active signal ("0") at pin RSTN(IN)

During the delay off time THOLD

- The driver is ON regardless of whether the ON/OFF command is reset.
- The starter configuration is held.
- The HSD/LSD configuration bit is held.
- The driver is ON even in case of Watchdog *ERR_CNT>4 and ERR_CNT>7*
- The driver is ON even in case of VDDIO_UV.
- Once it has started, the delay_off is not restarted by a new triggering event before THOLD has expired.

The delay-off timer can be terminated by one of the following events:

- THOLD time expires.
- Driver is switched off by *MSC command off*.

After DELAY_OFF time the RLY4, STR[2:3] take the status of the on/off data command. If before the delay off time expires, the above triggering sources are recovered, the delay-off function remains valid.

Figure 45. DELAY_OFF timing

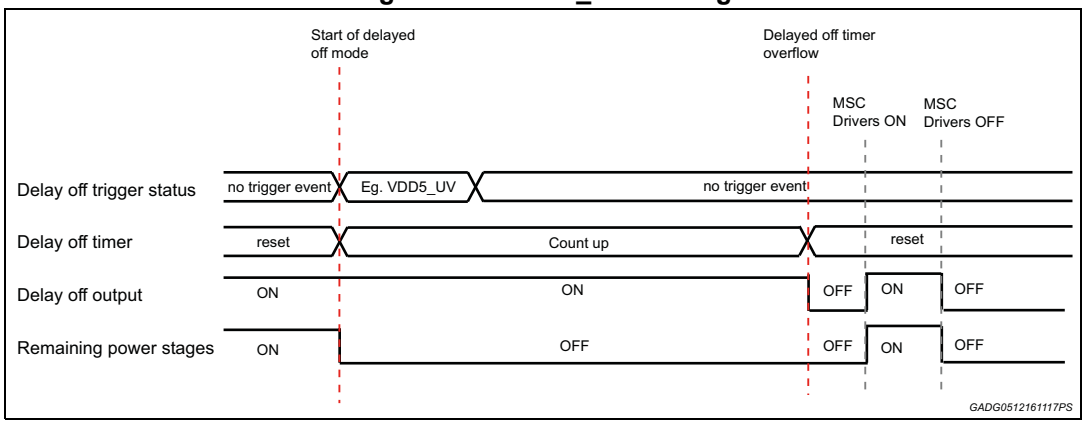
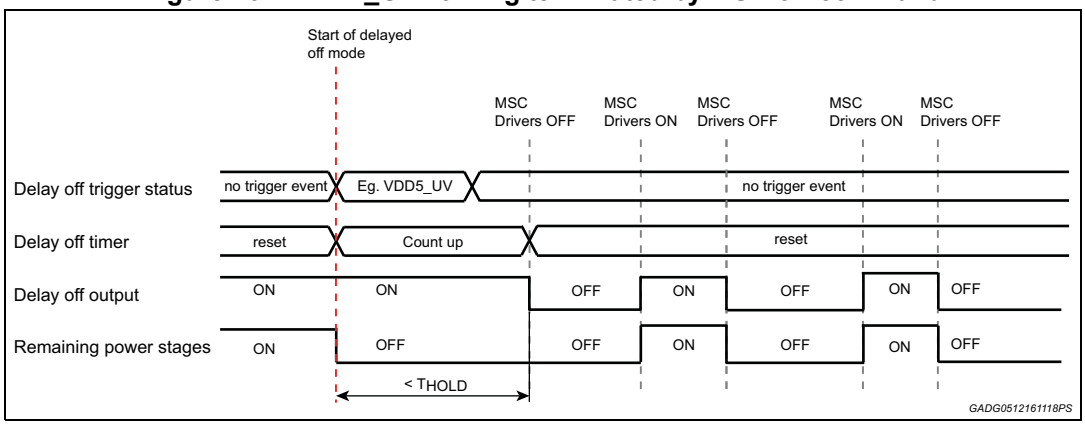


Figure 46. DELAY_OFF timing terminated by MSC off command



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 51. High/low-side driver delay-off function electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
THOLD	Delay off time	-	400	-	800	ms	RLY4 STR2/3

8.6 Starter control

To prevent unintended activation of starter relays at the same time a dual control mechanism is implemented inside the logic by means of independent MSC commands for on/off for each starter (*RLY4_ON RLY4_OFF STR2_ON STR2_OFF STR3_ON STR3_OFF*). If the RLY4, STR2, STR3 are not configured as starter they are controlled by data frame on/off as the other drivers

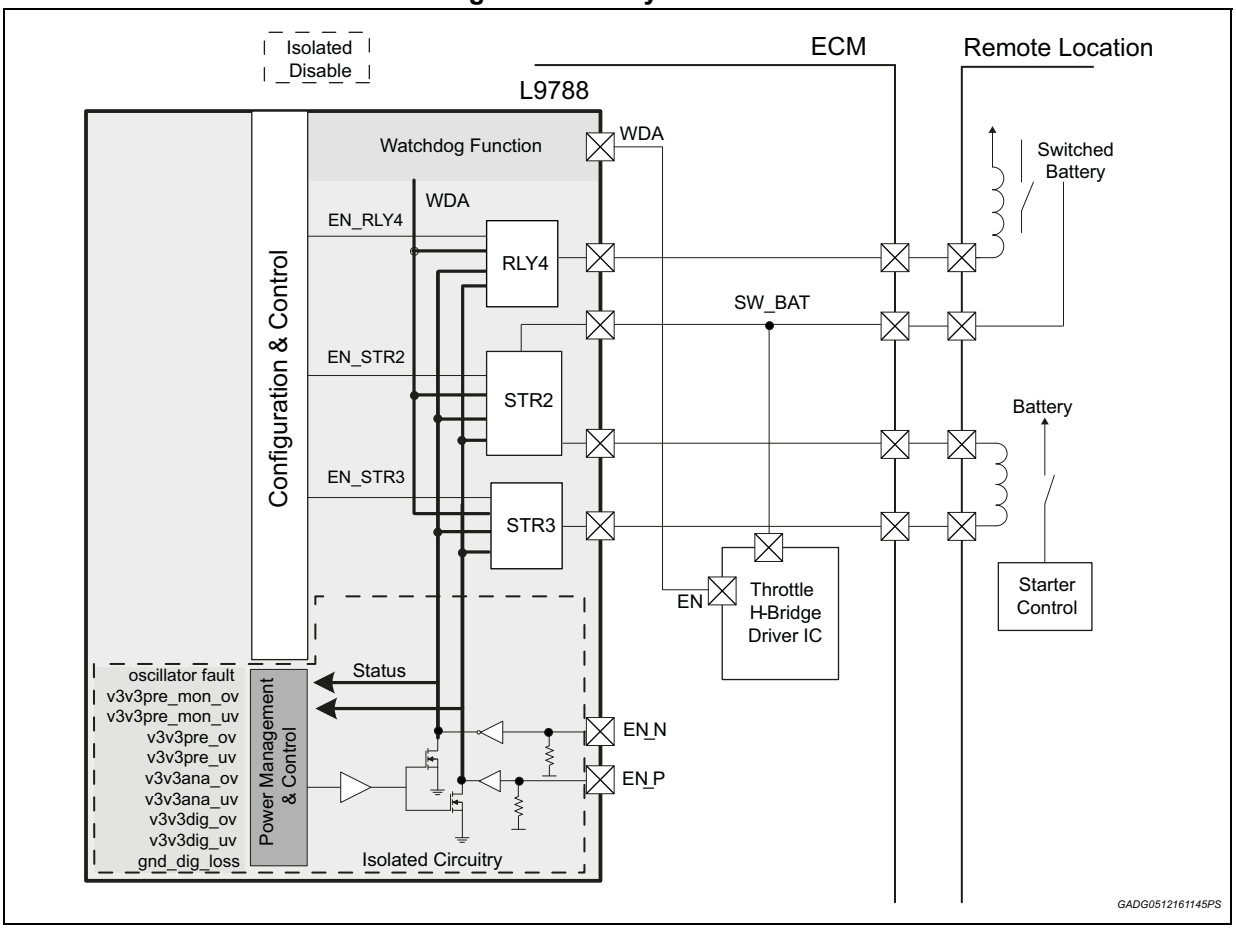
The starter control function comes with a dedicated failsafe management circuit to always provide a safety switch off path able to disconnect the main supply in case of fault conditions. Starter switch off path is implemented with dual polarity command acting on drivers STR[2:3] and RLY4: if the EN_P pin is high or the EN_N pin is high or if the FAULT_WARN is activated. RLY4, STR2, STR3 are switched off by the safety switched off path independently if they are configured as starter.

Safety switch off path can be triggered both by the micro-controller through EN pins or by the L9788 detection of an internal fault as described in the *Figure 47*.

The functionality of the switch off path is guaranteed through physical isolation from the rest of the device: the circuit is kept layouted in a dedicated area surrounded by trench isolations, avoiding top routing over this cell and keeping a safe distance respect to the nearby functional top routing to ensure complete independency.

The switch off path generates locally its supply voltage to drive the safety turn-off switch in order to avoid interactions with the rest of the L9788; the supply voltage is created starting directly from battery line. All the circuits used inside the switch-off path are able to sustain high voltage to prevent unwanted functionality in case of local failure, moreover no external reference is routed to this area and the EN_N and EN_P control logic is located inside this area as well to complete isolation and remove any dependency from the rest of the L9788.

Figure 47. Safety switch off



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

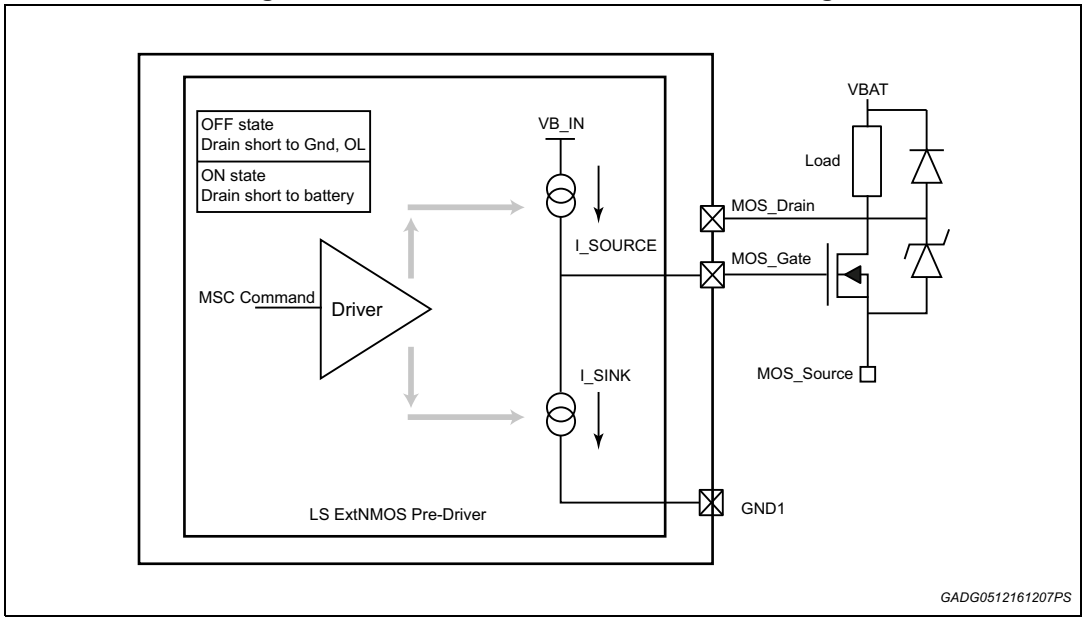
Table 52. EN_P and EN_N electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VIH_TX	HIGH_level input voltage	-	1.75	-	-	V	EN_P
VIL_T_X	LOW_level input voltage	-	-	-	0.75	V	EN_P
VHYS_T_X	Input voltage hysteresis	-	0.06	0.5	-	V	EN_P
PULL_T_X	Pull-up resistance	-	50	100	200	kΩ	EN_P
VIH_T_X	HIGH_level input voltage	-	1.75	-	-	V	EN_N
VIL_T_X	LOW_level input voltage	-	-	-	0.75	V	EN_N
VHYS_T_X	Input voltage hysteresis	-	0.06	0.5	-	V	EN_N
PULL_T_X	Pull-up resistance	-	50	100	200	kΩ	EN_N

Note: For this application the function is implemented, but kept disabled using external resistor to pull EN_N and EN_P to low.

9 Pre-drivers - ExtFET (MOS_Gate1/2/3/4/5) - PRD[1:5]

Figure 48. LS External MOSFET Pre-Driver Stage



9.1 LS external MOSFET pre-driver

These 5 pre-drivers are designed to drive LS external MOSFET Load. They are driven by *MSC command*.

The push-pull stage is made up of limited source current and sink current. The voltage of MOS_Drain is monitored for diagnosis.

The driver has the following detection diagnosis:

- _Drain short to battery @ pre-driver = On state
- _Drain short to ground @ pre-driver = Off state
- _Drain open load @ pre-driver = Off state

Predriver1 & Predriver3 can be used to drive ExtMos for O2H Load.

For these two predrivers there is the possibility to select a lower gate current and sink current (typ = 250 µA).

A dedicated MSC bit is used to select the predriver O2H function (Bit *O2H_PDRV = CONFIG_REG_16_1[7:6]*). Considering that this sink/source current is very low the logic will switch to the selected higher sink/source current after the cmd delay time (typ 150 µs for *CONFIG_REG20[7]=PDRV_O2H_DLY=0* or 300 µs *CONFIG_REG20[7]=PDRV_O2H_DLY=1*). After the CMD delay time the current used is the one selected by *CONFIG_REG4=PRDx_IDRV[1:0]*.

When the Predriver is used for O2H load the overcurrent detection can't be done using a VDS comparator due to slow voltage slew-rate, for this reason an external Rshunt has to be used.

When the Predriver is used for O2H load no blanking time is applied to OVC detection.The OVC dectection is done reading the voltage drop on this external Rshunt by the VDS comparator of another predriver (not used).

This means that when the Predriver 1 and Predriver 3 are used for O2H load the Predriver 2 and Predriver 4 can't be used.

Bit *O2H_PDRV = CONFIG_REG_16_1[7:6]= 00*: all 5 predriver channels can be used

Bit *O2H_PDRV = CONFIG_REG_16_1[7:6]= 11:*

- predriver 2 & Predriver 4 can't be used;
- predriver 1 & predriver3 work with low gate current and sink current (typ = 250 µA);
- it is possible to read the Overcurrent on external Rshunt of Predriver1&3 using the Vds comparator of Drain2 and Drain4;
- Predriver 5 works as in *O2H_PDRV = CONFIG_REG_16_1[7:6]= 00*.

There is a dedicated ground pin PDR_GND used for source pin of External Mos or ground connection of External shunt resistor. The internal voltage reference for VDS comparator threshold (Vth_VDS_xxx parameter) is connected to this ground pin PDR_GND. Application has to connect this PDR_GND pin to the source of external MOS or ground of external shunt resistor in order to obtain a good accuracy of overcurrent threshold.

Pre-driver after power up is OFF, output LOW.

Figure 49. PreDriver3 configured for O2H load bit O2H_PDRV_3 = CONFIG_REG_16_1[7] = 1:

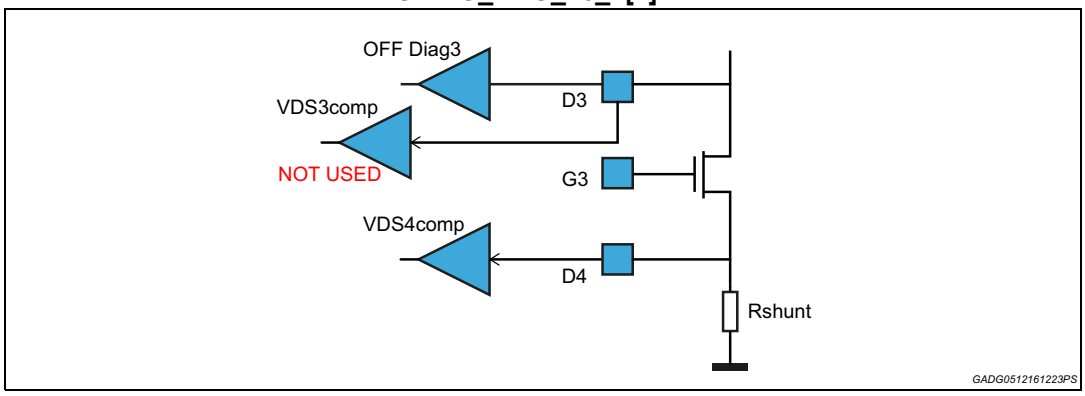
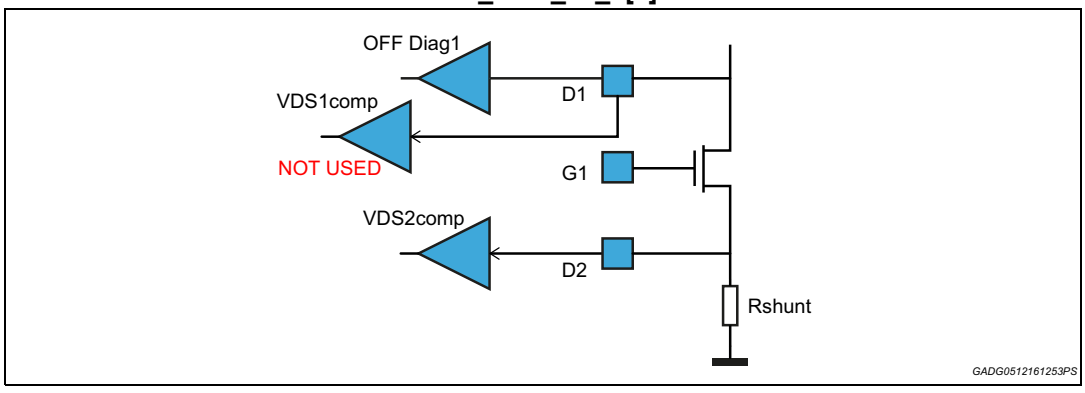


Figure 50. PreDriver1 configured for O2H load bit O2H_PDRV_1 = CONFIG_REG_16_1[6] = 1:



9.2 ON state diagnostic

In the On state of pre-driver, the diagnosis will compare the Drain-source voltage with the threshold generated internal. If MOS_DRAIN_X>Vth_DS_XXX (PRDx_VDS[0:2] *CONFIG_REG5*/ *CONFIG_REG6* / *CONFIG_REG7*)for a filter time, the Drain short to battery fault will be confirmed. The internal comparator reads the voltage on drain pin versus a dedicated GND sense pin (PIN X) that at application should be connected on the source of external mos. Starting from the condition ON state a programmable blanking time (MSC *CONFIG_REG16=PRDx_BLK[1:0])* is applied to prevent the detection of the short-to-battery fault. The blanking time is not applied when the driver is already ON.The pre-driver will switch OFF and the fault will be latched until the Read_Diag_CMD action. This bit can be reset by every Read Diag Communication. To re-activate ON the power stage in this two following conditions:

- The MSC command still High, when the Fault OVC Bit is read by MSC communication.
- The MSC command becomes Low and then again High.

When Bit MSC_O2HPredr_1 = 1 the VDS comparator of predriver 1 is ignored.

When Bit MSC_O2HPredr_3 = 1 the VDS comparator of predriver 3 is ignored.

When Bit MSC_O2HPredr = 1 the VDS comparator of predriver 2 (or 4) is enabled immediately with the turn ON command of Predriver (and checked by logic after the blanking time), while when Bi*t MSC_O2HPredr = 0* the VDS comparator of corresponding channel is enabled after selected blanking time.

The over current protection can be done reading the voltage on external Rshunt using the VDS comparator of predriver 2&4.

9.3 ON/OFF state - Error in status diagnosis

Refer to *Section 7.1.3*.

9.4 Error handling

Table 53. Pre-driver - ExtFET error handling

Type of error	Detection condition	Action	Clear MSC flag	Restart condition
Driver diagnostic				
Overcurrent (OVC)	Driver on	Driver is put in off state. The fault is latched in MSC diagnosis register.	On read	At MSC read of diagnosis register if MSC command is still high. If MSC command is low and high again.
Short to ground (STG)	Driver off	The fault is latched in MSC diagnosis register.	On read	

Table 53. Pre-driver - ExtFET error handling (continued)

Type of error	Detection condition	Action	Clear MSC flag	Restart condition
Open load (OPL)	Driver off	The fault is latched in MSC diagnosis register.	On read	
Driver Status Error (STA)	Driver on/off When the driver output level is not aligned with the cmd on/off	The fault is latched in MSC diagnosis register.	On read	

9.5 OFF state diagnostic

The Predriver follows the same off diagnosis as low-side driver. But despite the fast mode of all drivers in off diagnostic condition (*Ipupd_MODE* bit), for all pre_Driver, there is a dedicated MSC bit (*IDIAG_HIGH_PDRV*) to select off diagnostic high or low pull up/down current

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 54. Pre-driver - ExtFET electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Pre-driver							
Vgate_on	On state MOS_ Gate voltage	I_source_00	5	-	6	V	MOS_Gate 1/2/3/4/5
Vgate_off	Off state MOS_Gate voltage	I_sink_00	0	-	0.1	V	MOS_Gate 1/2/3/4/5
Ileak_off	Leakage current of MOS_Gate @ driver in tri-state	-	-1	-	1	µA	MOS_Gate 1/2/3/4/5
I_source_00	Pre-driver source current 1	MOS_Gate1/2/3/4/5 short to gnd	14	20	26	mA	MOS_Gate 1/2/3/4/5
I_source_01	Pre-driver source current 2	MOS_Gate1/2/3/4/5 short to gnd	7	10	13	mA	MOS_Gate 1/2/3/4/5
I_source_10	Pre-driver source current 3	MOS_Gate1/2/3/4/5 short to gnd	2.8	4	5.2	mA	MOS_Gate 1/2/3/4/5
I_source_11	Pre-driver source current 4	MOS_Gate1/2/3/4/5 short to gnd	1.3	2	2.6	mA	MOS_Gate 1/2/3/4/5
I_source_O2H	Pre-driver source current 5	MOS_Gate1/3/ short to gnd	0.175	0.25	0.325	mA	MOS_Gate 1/3
I_sink_00	Pre-driver sink current 1	MOS_Gate1/2/3/4/5 short to 5V	-26	-20	-14	mA	MOS_Gate 1/2/3/4/5
I_sink_01	Pre-driver sink current 2	MOS_Gate1/2/3/4/5 short to 5V	-13	-10	-7	mA	MOS_Gate 1/2/3/4/5

Table 54. Pre-driver - ExtFET electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_sink_10	Pre-driver sink current 3	MOS_Gate1/2/3/4/5 short to 5V	-5.2	-4	-2.8	mA	MOS_Gate 1/2/3/4/5
I_sink_11	Pre-driver sink current 4	MOS_Gate1/2/3/4/5 short to 5V	-2.6	-2	-1.4	mA	MOS_Gate 1/2/3/4/5
I_sink_O2H	Pre-driver sink current 5	MOS_Gate1/3 short to 5V	-0.175	-0.25	-0.325	mA	MOS_Gate 1/3
ON/OFF state diagnostic							
Vth_DS_000	Diagnosis Vds threshold 1	-	120	150	180	mV	MOS_Drai n1/2/3/4/5
Vth_DS_001	Diagnosis Vds threshold 2	-	220	245	270	mV	MOS_Drai n1/2/3/4/5
Vth_DS_010	Diagnosis Vds threshold 3	-	300	325	350	mV	MOS_Drai n1/2/3/4/5
Vth_DS_011	Diagnosis Vds threshold 4	-	380	405	430	mV	MOS_Drai n1/2/3/4/5
Vth_DS_100	Diagnosis Vds threshold 5	-	500	525	550	mV	MOS_Drai n1/2/3/4/5
Vth_DS_101	Diagnosis Vds threshold 6	-	620	660	700	mV	MOS_Drai n1/2/3/4/5
Vth_DS_110	Diagnosis Vds threshold 7	-	900	950	1000	mV	MOS_Drai n1/2/3/4/5
T_filter_ovc	Over current filtering time	Tested by scan	5	-	7	µs	MOS_Drai n1/2/3/4/5
V_OL	Open load threshold voltage	Driver tristate, diag enabled	VOUTO PEN+16 0mV	-	3	V	MOS_Drai n1/2/3/4/5
VOUTOPEN	Open load output voltage	Driver tristate, diag enabled	2.3	2.5	2.7	V	MOS_Drai n1/2/3/4/5
VLVT	Output short-circuit to GND Voltage threshold	Driver tristate, diag enabled	1.9	-	VOUTO PEN-180mV	V	MOS_Drai n1/2/3/4/5
I_LS_PU1	Diagnostic pull up current	In OFF condition, MOS_DRAINx <VLVT, Ipupd_EN = ENB, Ipupd_MODE =”1”	2.5	3.6	4.7	mA	MOS_Drai n1/2/3/4/5
I_LS_PU2	Diagnostic pull up current	In OFF condition, MOS_DRAINx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”0”and IDIAG_HIGH_PDRV =”0”	40	70	100	µA	MOS_Drai n1/2/3/4/5

Table 54. Pre-driver - ExtFET electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_LS_PU3	Diagnostic pull up high current	In OFF condition, MOS_Drainx < VLVT, Ipupd_EN = ENB, Ipupd_MODE =”0” and IDIAG_HIGH_PDRV =”1”	100	-	200	µA	MOS_Drain1/2/3/4/5
I_LS_PD1	Diagnostic pull down current	In OFF condition, MOS_DRAINx > VOUTOPEN, Ipupd_EN = ENB and IDIAG_HIGH_PDRV =”0”	60	85	105	µA	MOS_Drain1/2/3/4/5
I_LS_PD2	Diagnostic pull down high current	In OFF condition, OUT MOS_Drainx > VOUTOPEN, Ipupd_EN = ENB IDIAG_HIGH_PDRV = ”1”	350	-	550	µA	MOS_Drain1/2/3/4/5
I_leakage	MOS_DRAIN leakage current	Output disable diagnostic OFF condition,	-10		10	µA	MOS_Drain1/2/3/4/5
Tflt_diagoff1	DIAG Filter time	Filter Mode=0	75	100	125	µs	MOS_Drain1/2/3/4/5
Tflt_diagoff2	DIAG Filter time	Filter Mode=1	450	600	750	µs	MOS_Drain1/2/3/4/5
Tblank_00	Blanking time on ON diag	PRD1_BLK[0:1]=00	5.1	6	6.7	µs	MOS_Drain1/2/3/4/5
Tblank_01	Blanking time on ON diag	PRD1_BLK[0:1]=01	11.1	12	13.5	µs	MOS_Drain1/2/3/4/5
Tblank_10	Blanking time on ON diag	PRD1_BLK[0:1]=10	17.1	18	20	µs	MOS_Drain1/2/3/4/5
Tblank_11	Blanking time on ON diag	PRD1_BLK[0:1]=11	23.1	24	26.7	µs	MOS_Drain1/2/3/4/5
cmd_dly_0	Command delay for *MSC_CONFIG_REG20[7]=PDRV_O2H_DLY=1*	Tested by scan	140	150	160	µs	MOS_Drain1/2/3/4/5
cmd_dly_1	Command delay for *MSC_CONFIG_REG20[7]=PDRV_O2H_DLY=1*	Tested by scan	280	300	320	µs	MOS_Drain1/2/3/4/5

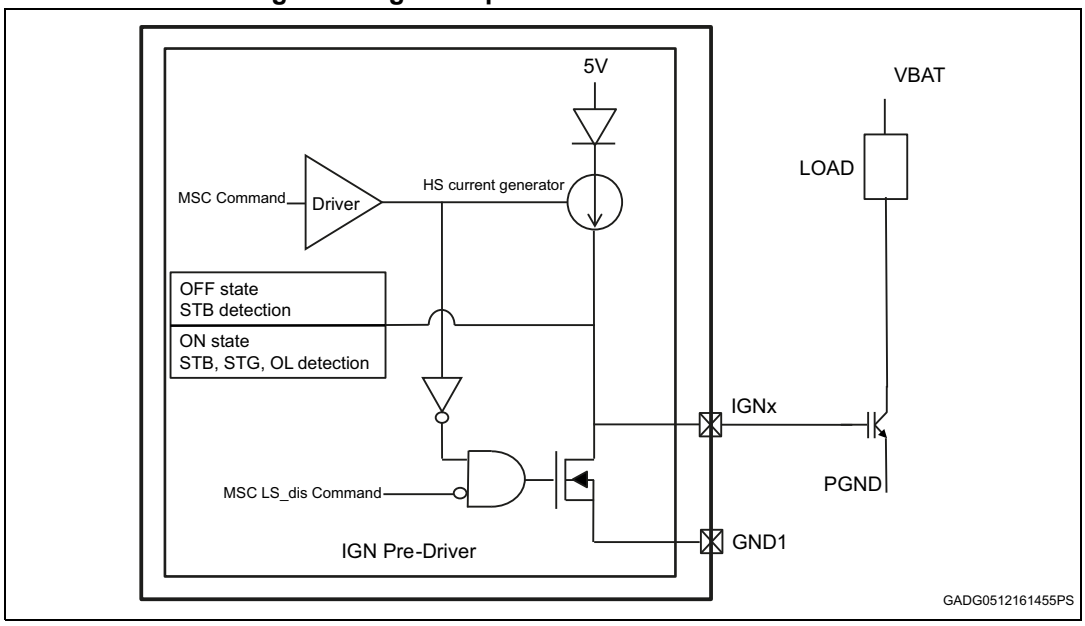
10 Pre-drivers - IGNITER IGN[1:6]

These 6 Ignition pre-drivers are designed to drive ignition load. They are driven by *MSC command*. The push-pull stage is made up of a high-side current generator and a low-side driver.

When an overcurrent fault is detected the driver switches off with higher slew rate (FAST SR) to reduce the power dissipation.

There is a bit selection for disabling the LSD in case of external IGBT. It is suggested to configure the MSC bit (*IGN_LSD_DIS CONFIG_REG6 D7*) disabling the LSD of igniter before the *msc_driver_enable* command.

Figure 51. Ignition pre-drivers block schematic



10.1 Ignition pre_drivers diagnosis

The driver has the following detection diagnosis:

- Short To Vbat protection by checking the IGNx pin voltage higher than Vth_STB_IGN, when the driver is enabled high (high-side on) or low (low-side on);
- Open Load when the driver is enabled high (high-side on) (DIAGOL);
- Short to Ground when the driver is enabled high (high-side on) (DIAGLV).

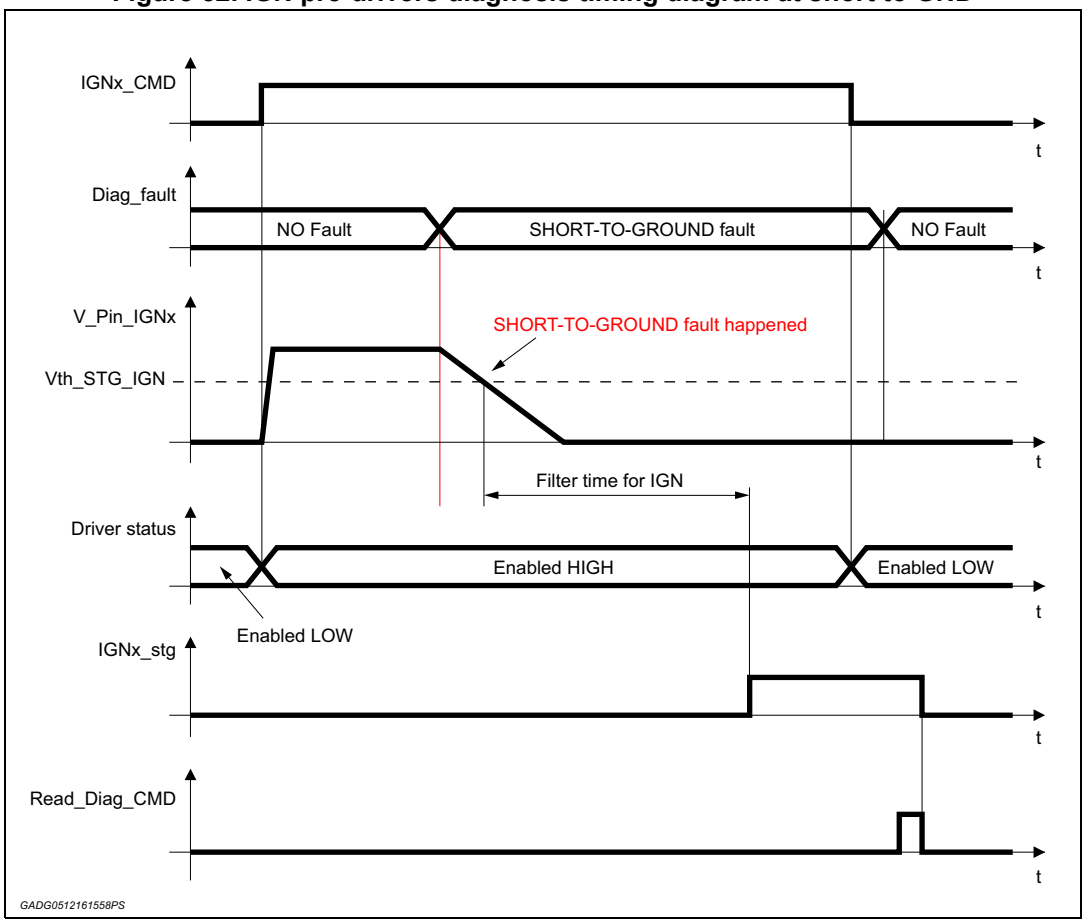
Table 55. Pre-driver - IGNITER diagnosis

Controlled load	Diagnosis & protection type	Detected faults @ pre-driver enabled HIGH	Detected faults @ pre-driver enabled LOW
Internal IGBT/smart IGBT *(IGN_DIAG (CONFIG_REG2 D5)* = '0')	The controlled device is module internal. No diagnosis and protection required	-	-
External IGBT Load (*IGN_DIAG = '1'*)	IGNx voltage and current monitoring	_ IGNx short to GND _ IGNx open load _ IGNx short to VBAT	_ IGNx short to VBAT

10.2 Short to GND

When IGNx pin voltage is lower than Vth_STG_IGN for a filter time at pre-driver is enabled high, short to ground fault is detected. So the fault is latched until Read_Diag_CMD action.

Figure 52. IGN pre-drivers diagnosis timing diagram at short to GND



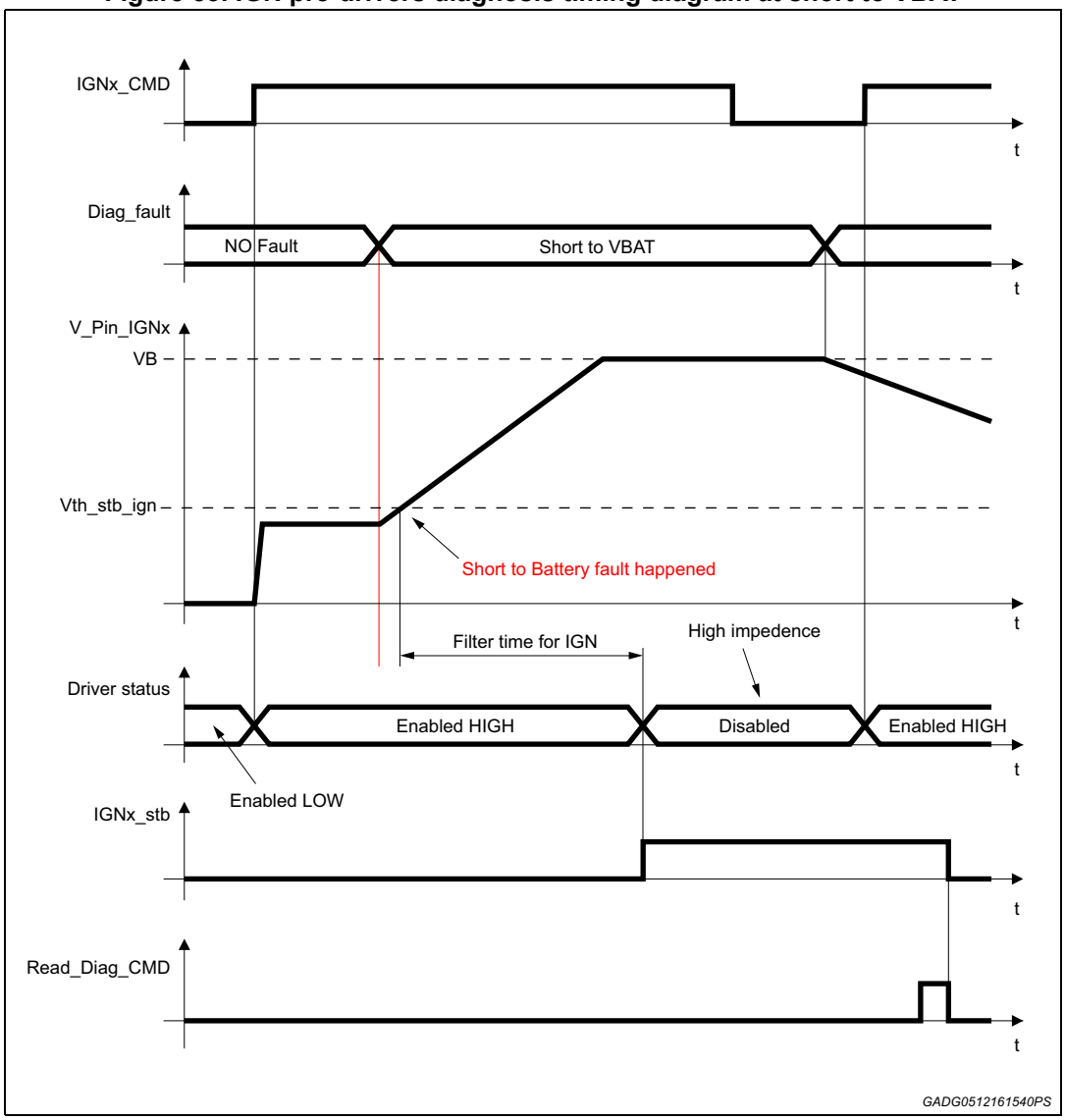
10.3 Short to BAT

When IGNx pin voltage is higher than Vth_STB_IGN for a filter time at pre-driver is enabled high or enabled low, short to battery fault is detected and the driver is disabled. So the fault is latched.

During Short-to-Bat fault present the driver is auto-restart with these modalities:

- The high-side restart during OVC is on read diagnostic or *IGNx_CMD* goes to low and high again.
- The low-side restart during OVC is on read diagnostic.

Figure 53. IGN pre-drivers diagnosis timing diagram at short to VBAT



10.4 Open load

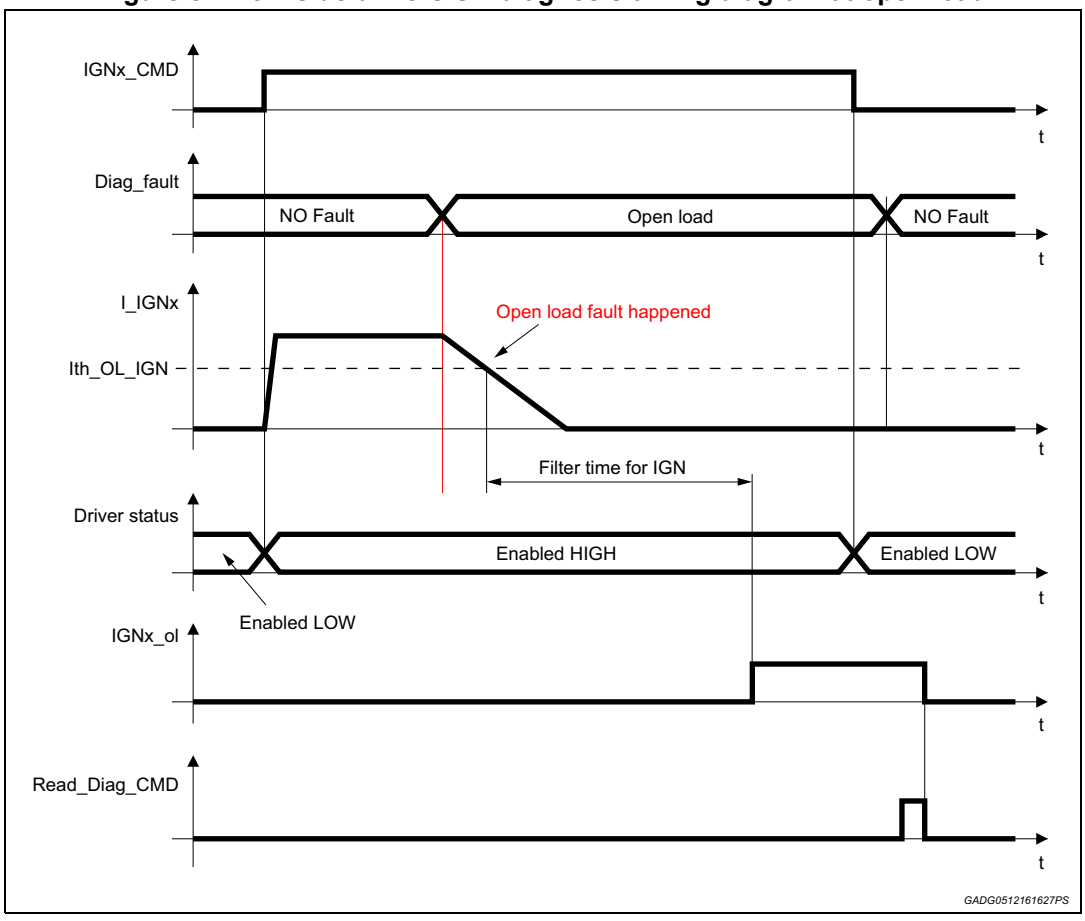
When IGNx pre-driver is enabled HIGH, if IGNx current is lower than OL current detection Ith_OL_IGN for a filter time, open load fault is detected and the driver is not disabled. Open load function can be disabled by a MSC bit. Open Load fault is latched until Read_Diag_cmd action. OPL threshold is selectable between 2 values, the default (between 0.4 and 0.8mA) and a lower one.

OPL threshold reduction is available just in low current limitation condition, so when *OL_RED and IGN_CURRENT_CFG (CONFIG_REG2 D4)* bits are both high.

10.5 Error in driver status

Refer to *Section 7.1.3*.

Figure 54. Low-side drivers ON diagnosis timing diagram at open load



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 56. Pre-driver - IGNITER electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
High-side current generator parameters							
IOH1_HS_IGN	High-side output current 1	VIGNX = 4 V VDD5 = 5 V MSC Bit IGN_CURRENT CFG = 1, OL_RED = 0	4.7	-	15.3	mA	IGN1/2/3/4/5/6
IOH1_HS_IGN_OL_RED	High-side output current 1	VIGNX = 4 V VDD5 = 5 V MSC Bit IGN_CURRENT CFG = 1, OL_RED = 1	2	-	15	mA	IGN1/2/3/4/5/6
IOH2_HS_IGN	High-side output current 2	VIGNX = 4 V VDD5 = 5 V MSC Bit IGN_CURRENT CFG = 0 (Default Value)	14.7	-	30.3	mA	IGN1/2/3/4/5/6
VOH1_HS_IGN	Output voltage 1 @ high-side on	Isource = 5 mA MSC Bit IGN_CURRENT CONFIG = 1, OL_RED = 0	VDD5 -0.4	-	VDD5	V	IGN1/2/3/4/5/6
VOH1_HS_IGN_OL_RED	Output voltage 1 @ high-side on	Isource = 2 mA MSC Bit IGN_CURRENT CONFIG = 1, OL_RED = 1	VDD5 -0.4	-	VDD5	V	IGN1/2/3/4/5/6
VOH2_HS_IGN	Output voltage 2 @ high-side on	Isource = 15mA MSC Bit IGN_CURRENT CONFIG = 0 (Default Value)	VDD5 -0.6	-	VDD5	V	IGN1/2/3/4/5/6
IOFF_LK_IGN	High-side leakage current @ off condition	IGNx = 2.5 V in off	-	-	10	µA	IGN1/2/3/4/5/6
Low-side MOSFET parameters							
RDS-on_LS_IGN	Drain–source resistance	I_load = 0.1A @ T = -40 °C	1.8	2.2	3.1	Ω	IGN1/2/3/4/5/6
RDS-on_LS_IGN	Drain–source resistance	I_load = 0.1 A @ T = 27 °C	2.4	3.0	3.91	Ω	IGN1/2/3/4/5/6

Table 56. Pre-driver - IGNITER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RDS-on_LS_IGN	Drain–source resistance	I_load = 0.1 A @ T = 150 °C	3.8	5.0	7.0	Ω	IGN1/2/3/4/5/6
VOL_LS_IGN	Output voltage @ LS low-side on	IOL = 20 µA sinked	-	-	0.1	V	IGN1/2/3/4/5/6
VOL_LS_IGN	Output voltage @ LS low-side on	IOL= 100 mA sinked	-	-	0.7	V	IGN1/2/3/4/5/6
Irev_LS_IGN	Body diode reverse current voltage drop	I_load = 0.3 mA sourced	-	-	1	V	IGN1/2/3/4/5/6
General IGN block parameters							
TDON_IGN	Turn-on delay time	CLOAD =10 nF Isource = 10 mA	-	-	10	µs	IGN1/2/3/4/5/6
TDOFF_IGN	Turn-off delay time	CLOAD = 10 nF	-	-	10	µs	IGN1/2/3/4/5/6
TR_IGN	Output rise time	CLOAD = 10 nF Isource = 10 mA	-	-	9	µs	IGN1/2/3/4/5/6
TF_IGN	Output fall time	CLOAD = 10 nF	0.05	-	2	µs	IGN1/2/3/4/5/6
IOUT_LK_IGN	Output leakage current	Vpin = 13.5 V	-	-	10	µA	IGN1/2/3/4/5/6
Vth_STB_IGN	Short circuit to VBAT voltage threshold	IGNx = VBAT	5.3	-	6.5	V	IGN1/2/3/4/5/6
Vth_STG_IGN	Short circuit to GND threshold	-	2.1	-	2.7	V	IGN1/2/3/4/5/6
Ileak_STG_IGN	Leakage current @ short circuit to GND, IGN in tri-state	IGNx = GND	-	-	10	µA	IGN1/2/3/4/5/6
Ileak_STB_IGN	Leakage current @ short circuit to VBAT,IGN in tri-state	IGNx = VBAT	-	-	1	mA	IGN1/2/3/4/5/6
Ileak_STB_IGN	Leakage current @ short circuit to VBAT	GND = VB_IN = 0V IGNx = 18 V	-	-	10	µA	IGN1/2/3/4/5/6
TFLT_SCGOL IGN	Open load and short circuit to GND filter time	-	72	-	90	µs	IGN1/2/3/4/5/6

Table 56. Pre-driver - IGNITER electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
TFLT_SCB IGN	Short circuit to VBAT switch-off delay	-	5.9	-	7.2	µs	IGN1/2/3/4/5/6
Ith_OL_IGN	Open load current threshold	-	0.18	-	1.22	mA	IGN1/2/3/4/5/6
Ith_OL_IGN_OL_RED	Open load current threshold	OL_RED = 1	0.03	-	0.2	mA	IGN1/2/3/4/5/6

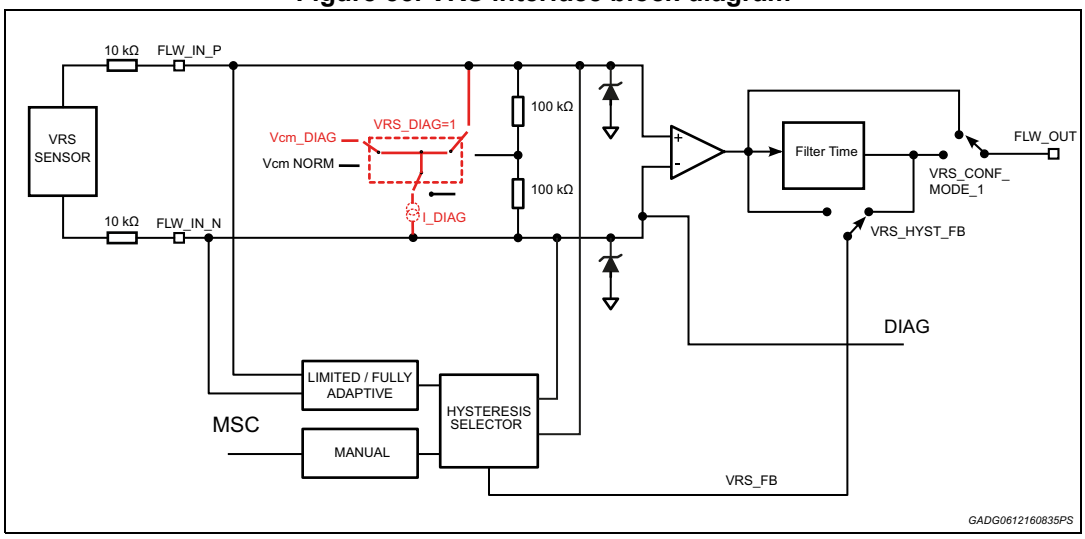
11 Inductive sensor interface

The interface handles signals coming from magnetic pick-up sensors or Hall Effect sensors. The interface feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

11.1 VRS interface

VRS interface runs either in normal mode to convert the input differential voltage or in diagnostic mode to detect eventual short to ground, short to battery or open condition at sensor pins. *Figure 55* shows the main parts inside VRS block and, in red, the internal connection in case of diagnostic mode active.

Figure 55. VRS interface block diagram



Operating mode is defined in VRS register through *VRS_DIAG* in CONFIG_REG8 bit: when *VRS_DIAG=0*, VRS block is set in normal mode; when *VRS_DIAG=1* the VRS diagnosis mode is activated.

If L9788 is supplied and VRS is running, in case FLW_IN_P or FLW_IN_N voltage rises their values are clamped at VclpH.

In case of activation of clamp both on FLW_IN_P and FLW_IN_N, it is guaranteed by design that FLW_IN_P voltage is higher than FLW_IN_P.

11.2 VRS - Normal mode

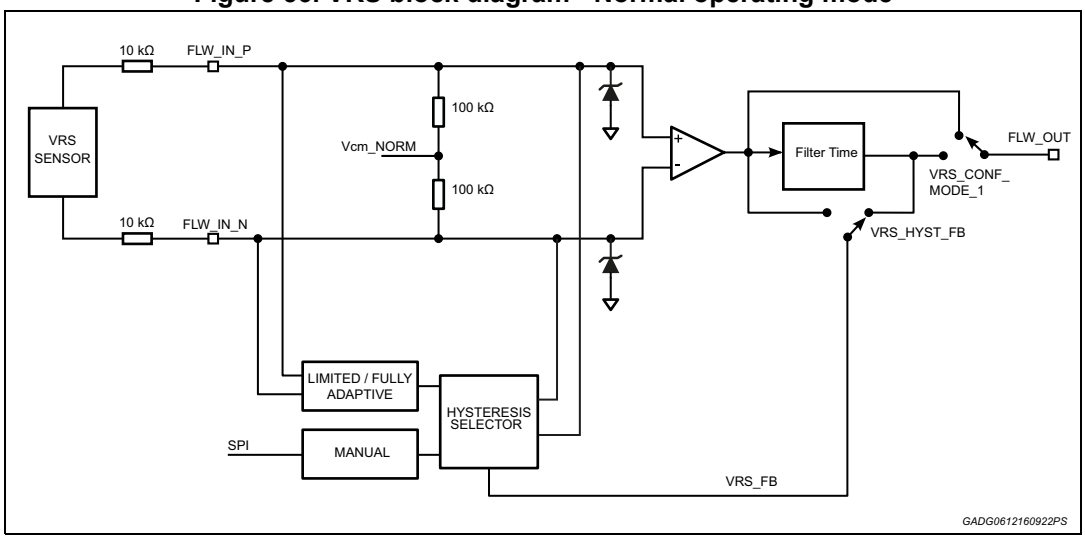
The VRS normal mode is set with *VR_DIAG=0*

In Normal mode, the circuit is configured as the one reported in *Figure 56*. It allows decoding the VRS signal while flying wheel is in rotation.

Due to high variability of the input signal (±200 V) The input is clamped in the range [VclpH:VclpL] in order to allow the analog circuitry processing the signal itself. Moreover, the sensor input pins have an input common mode, VCM.

The preconditioned input signal is then processed by a zero-crossing comparator, which toggles at each transition of the input signal.

Figure 56. VRS block diagram - Normal operating mode



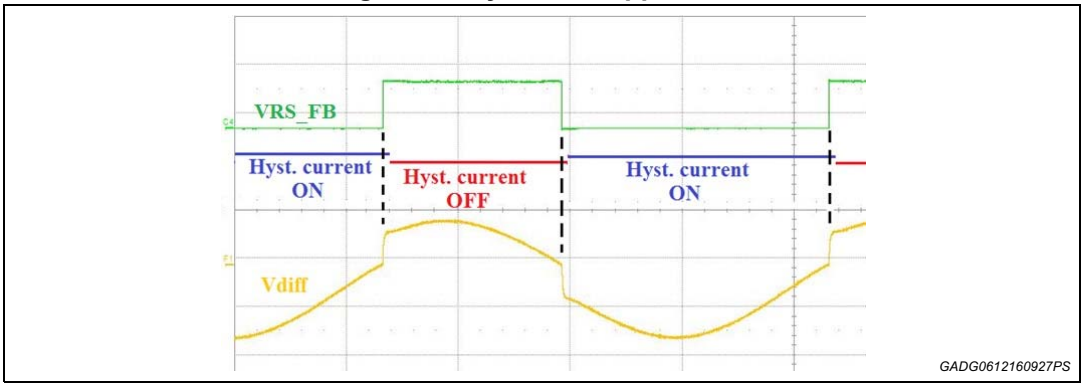
To avoid spurious commutations of the zero crossing comparator, a hysteresis mechanism is implemented. L9788 is able to sink a hysteresis current which generates a voltage drop across the external resistors. The voltage levels related to the hysteresis function shown hereafter are calculated considering an external series resistance of 10 kΩ on FLW_IN_P and 10 kΩ on FLW_IN_N pins.

As reported in *Figure 57*, the Vdiff (FLW_IN_P - FLW_IN_N) input differential signal exhibits some steps at each zero crossing:

- when the output of the zero crossing comparator is high, the hysteresis current is kept OFF;
- when the output of the zero crossing comparator is low, the hysteresis current is switched ON.

This approach applies the hysteresis current only on the transition L-H of the VRS_FB signal.

Figure 57. Hysteresis application



The output of the zero crossing comparator can be further processed by a filtering circuit or directly routed to FLW_OUT.

11.2.1 VRS normal mode configurations

L9788 integrates two main configurable architectures: VRS_A and VRS_B. These architectures are selected in VRS register, *VRS_MODE_SEL* bit in CONFIG_REG 2.

Once VRS_A (*VRS_MODE_SEL* =1) or VRS_B (*VRS_MODE_SEL* =0) has been configured, hysteresis and filtering strategy are defined through *VRS_MODE[1:0]* bit in the same CONFIG_REG 8 register:

VRS_MODE[1] defines filtering function (OFF/ON and if ON, its time value)

VRS_MODE[0] defines the hysteresis (manual or adaptive)

Table 57 summarizes the parameters of VRS_A and VRS_B architecture; the next paragraphs detail the two configurations.

Table 57. VRS_A, VRS_B hysteresis and filter time definition

VRS_MODE_SEL	*VRS_MODE[1:0]*	Filter		Hyst.	
VRS_A configuration					
1	00	OFF	0 µs	Manual	Ref to VRS_A - Manual Hysteresis
1	01	OFF	0 µs	Full adaptive	Ref. to VRS_A - Fully Adaptive Hysteresis
1	10	ON	T(n-1)/32	Manual	Ref to VRS_A - Manual Hysteresis
1	11	ON	T(n-1)/32	Full adaptive	Ref. to VRS_A - Fully Adaptive Hysteresis
VRS_B configuration					
0	00	OFF	0 µs	Manual	Ref. to VRS_B - Manual Hysteresis
0	01	OFF	0 µs	Limited adaptive	Ref. to VRS_B -Limited Adaptive Hysteresis
0	10	ON	4 µs	Manual	Ref. to VRS_B - Manual Hysteresis
0	11	ON	4 µs	Limited adaptive	Ref. to VRS_B -Limited Adaptive Hysteresis

In case a change of *VRS_MODE_SEL* bit within the normal operating mode occurs (1->0 or 0->1) with hysteresis current active, this leads to the change of the hysteresis (to HI1 or HI3,

according to the new selection programmed) not synchronized with any VRS_FB zero crossing.

11.2.2 VRS_A - Manual Hysteresis

To set the manual hysteresis on VRS_A configuration, bit *VRS_MODE[0]* has to be configured at '0'. Hysteresis value is manually set through *VRS_HYST[2:0]* of CONFIG-REG 8 according to *Table 58*. Such hysteresis is fixed until a new SPI programming occurs.

Default hysteresis current after exiting reset is HI3.

New MSC current value is updated during HYST CURRENT OFF phase that means the output comparator is high.

Table 58. VRS_A hysteresis value

Hysteresis current [H]	Min	Typ	Max	Unit	Correspondent value on 20 kΩ ext. resistor	Unit
HI1	3	5	7	µA	100	mV
HI2	7.5	10	13.5	µA	200	mV
HI3	13	17	23	µA	347	mV
HI4	23	32	40	µA	644	mV
HI5	35	51	60	µA	1020	mV
No Hyst	-	-	-	-	-	-

11.2.3 VRS_A - Fully Adaptive Hysteresis

To set the adaptive hysteresis on VRS_A configuration, bit *VRS_MODE[0]* has to be set to '1'. In this configuration, VRS input differential signal is fed into a peak detector circuit and then quantized on 5 different voltage levels, based on 4 PVi thresholds (see *Table 59*). Default hysteresis current after exiting reset is HI3.

Table 59. Peak voltage value ranges

Peak voltage [PVi]	Min	Typ	Max	Unit
PV1	600	930	1300	mV
PV2	1200	1600	1950	mV
PV3	2000	2300	2650	mV
PV4	2600	3000	3300	mV

The quantized output is sent to a logic block (Hysteresis Selection Table) that chooses the proper hysteresis value (HIi) depending on the input peak voltage (PVi), see *Table 60*.

Table 60. Insert title here

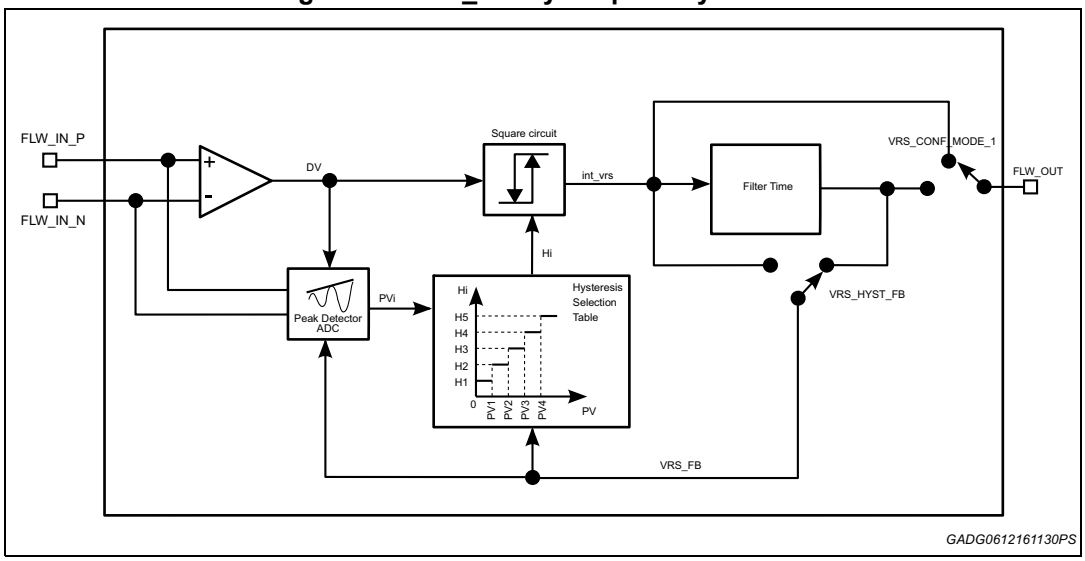
Input peak voltage range	Selected hysteresis (HIi)
0 - PV1	HI1
PV1 – PV2	HI2
PV2 – PV3	HI3
PV3 – PV4	HI4
> PV4	HI5

Peak detector and Hysteresis Selection Table circuits are enabled by VRS_FB signal according to *HYS_FB_SEL* in CONFIG-REG 8 bit value that establishes if the feedback signal is before or after the filter time.

VRS input differential voltage is continuously acquired: its max value, reached during time-frame VRS_FB signal is asserted (hysteresis current is off), is latched through a peak detector; such a peak defines a specific value of hysteresis current, turned on as soon as the VRS_FB falls to zero and switches OFF when next rising edge occurs.

Based on the hysteresis current, the signal is processed by a squaring circuit which processes the output signal of the comparator, see *Figure 58*.

Figure 58. VRS_A fully adaptive hysteresis



11.2.4 VRS_A - Adaptive filter time

In VRS_A mode, it is possible to enable the filter time on the output of the zero crossing comparator through the bit *VRS_MODE[1]* of CONFIG-REG 8.

Once enabled, the most suitable internal filter based on the input signal frequency is determined.

According to VRS previous output period, filter time value is updated as follows:

$$Tfilter_{(n)} = \frac{Tperiod_{(n-1)}}{32}$$

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If the value of the previous period is lower than 128 µs, the filter time would be saturated at 4 µs fixed value. After reset Tfilter = 200 µs (TYP)

Through *EN_FALLING_FILT* CONFIG-REG8 bit in VRS register, it is possible to configure two different strategies for the filtering algorithm.

VRS_OUT rising edge: the transition depends on the hysteresis crossing of differential signal Vdiff; VRS output is set if Vdiff remains asserted and stable for a period longer than Tfilter.

VRS OUT falling edge: the transition depends on the zero crossing of differential signal Vdiff:

- *EN_FALLING_FILT = 1*: VRS_OUT is deasserted when the signal is low and remains stable for at least Tfilter; see *Figure 59*
- *EN_FALLING_FILT = 0*: VRS_OUT is de-asserted at first zero crossing transition of differential signal and next eventual commutations are ignored for Tfilter time. see *Figure 60*.

Figure 59. EN_FALLING_FILT = 1

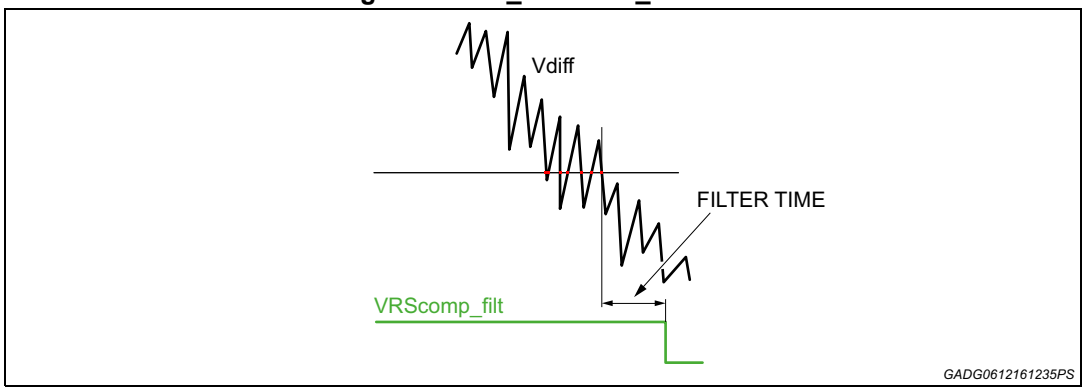
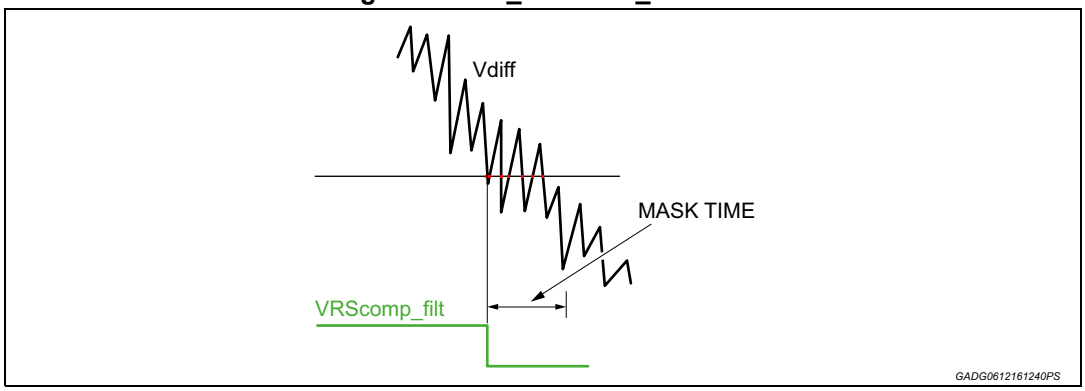


Figure 60. EN_FALLING_FILT = 0



11.2.5 VRS_B - Manual Hysteresis

To set the manual hysteresis on VRS_B configuration, bit *VRS_MODE [0]* has to be set to '0'. Hysteresis value is manually set through *VRS_HYST [2:0]* of CONFIG-REG 8 according to *Table 58* Such hysteresis is fixed until a new SPI programming occurs.

Once a new value is defined, new hysteresis threshold is applied after the second VRS_FB H-L transition and until the next rising edge of the VRS input differential voltage occurs.

11.2.6 VRS_B -Limited Adaptive Hysteresis

To set the limited adaptive hysteresis on VRS_B configuration, bit *VRS_MODE [0]* has to be set to '1'. In this mode, user programs a hysteresis threshold through *VRS_HYST [2:0]* bit in VRS register and the internal logic selects a hysteresis based on input signal peak value: the maximum of these two values is actually applied.

Once a new value is defined, new hysteresis threshold is applied after the second VRS_FB H-L transition and until the next rising edge of the VRS input differential voltage occurs.

11.2.7 VRS_B - Fixed Filter Time

In VRS_B configuration, it is possible to enable the filter time on the output of the zero crossing comparator through the bit *VRS_MODE[1]* of VRS register. This configuration allows defining the internal filter time at a fixed value of 4 µs, active on both rising and falling edges of VRS output.

As per VRS_A architecture, *EN_FALLING_FILT* allows configuring the same two different strategies for the filtering algorithm.

11.3 VRS diagnostic mode

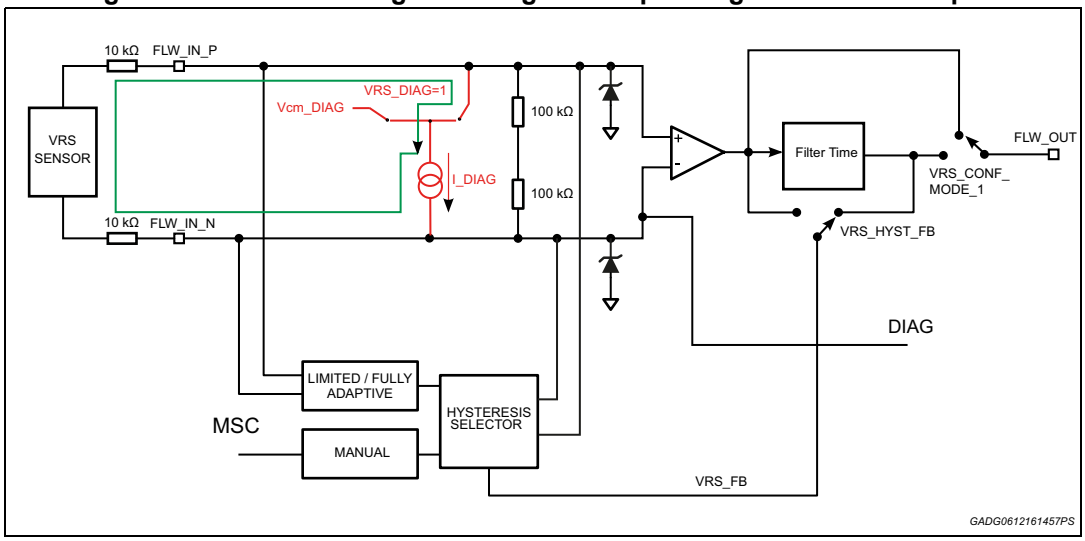
The diagnostic mode is selected through *VRS_DIAG = '1'* in CONFIG-REG8. This mode provides feedback to detect faulty conditions either on FLW_IN_P or FLW_IN_N.

To be noted that diagnostic results are not reliable while the flying wheel is rotating.

If a fault is detected in DIAG mode, VRS correct functionality is not guaranteed. Fault bit *VRS_DIAG* of VRS register is consequently set.

Figure 61 shows the circuit used ikn Diagnostic mode. When VRS diagnostic mode is activated, FLW_IN_P is fixed at Vcm_DIAG and IDIAG current generator is enabled, the current path is that one in green in *Figure 61*.

Figure 61. VRS block diagram - Diagnostic operating mode - Current path



11.4 Application circuit

Sensor sketch and parameters are reported in *Figure 62* and *Table 61*.

Figure 62. Sensor sketch

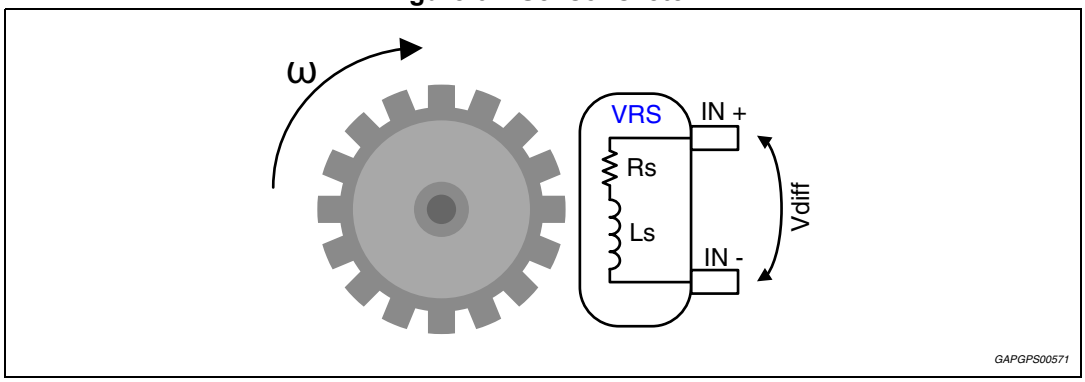


Table 61. VRS sensor parameters

Symbol	Parameter	Min	Typ	Max	Unit
Rs	Sensor resistance	300	600	1000	Ω
Ls	Sensor inductor	-	250	-	mH
Vdiff	Sensor output voltage	-200	-	+200	V
Tout	Output period	100	-	5000	µs

The interface handles signals coming from magnetic pick-up sensors, see *Figure 63*, or Hall Effect sensors with two possible configurations, as per *Figure 64* and *Figure 65*.

The interface feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

Figure 63. Variable reluctance sensor (VRS)

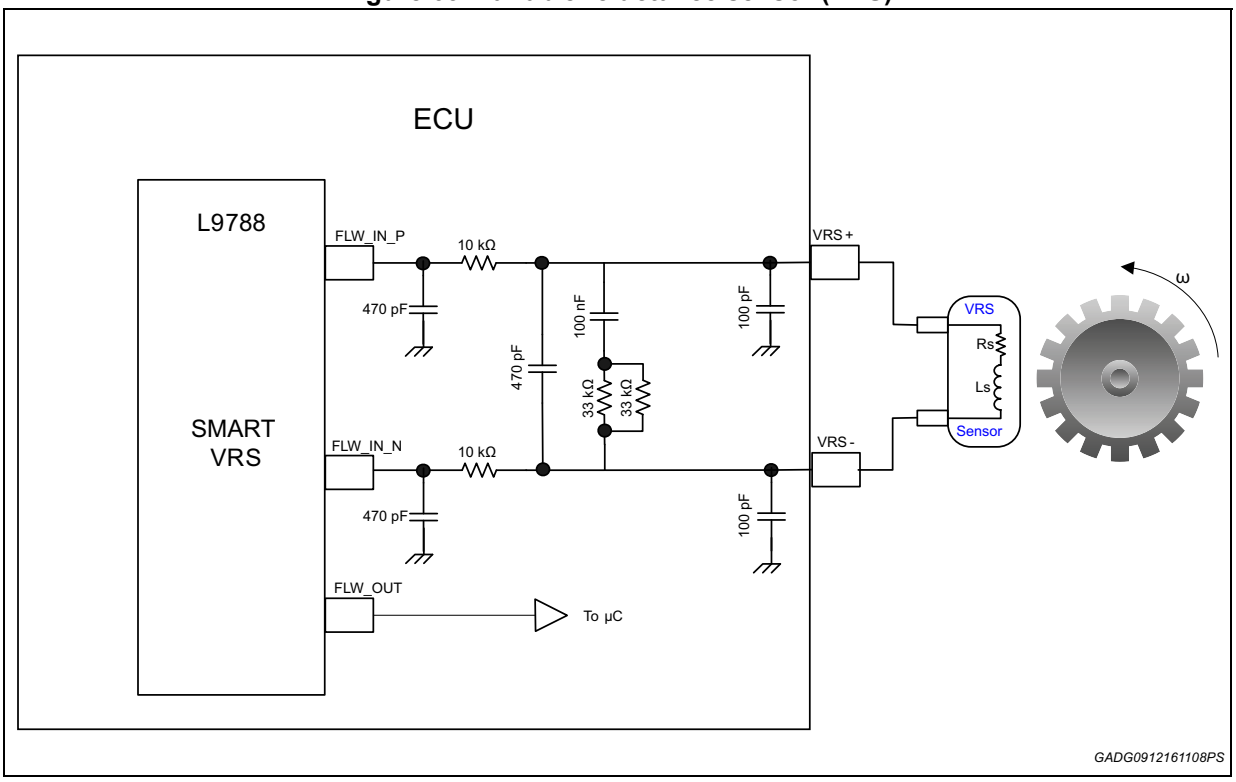


Figure 64. Hall effect sensor configuration 1

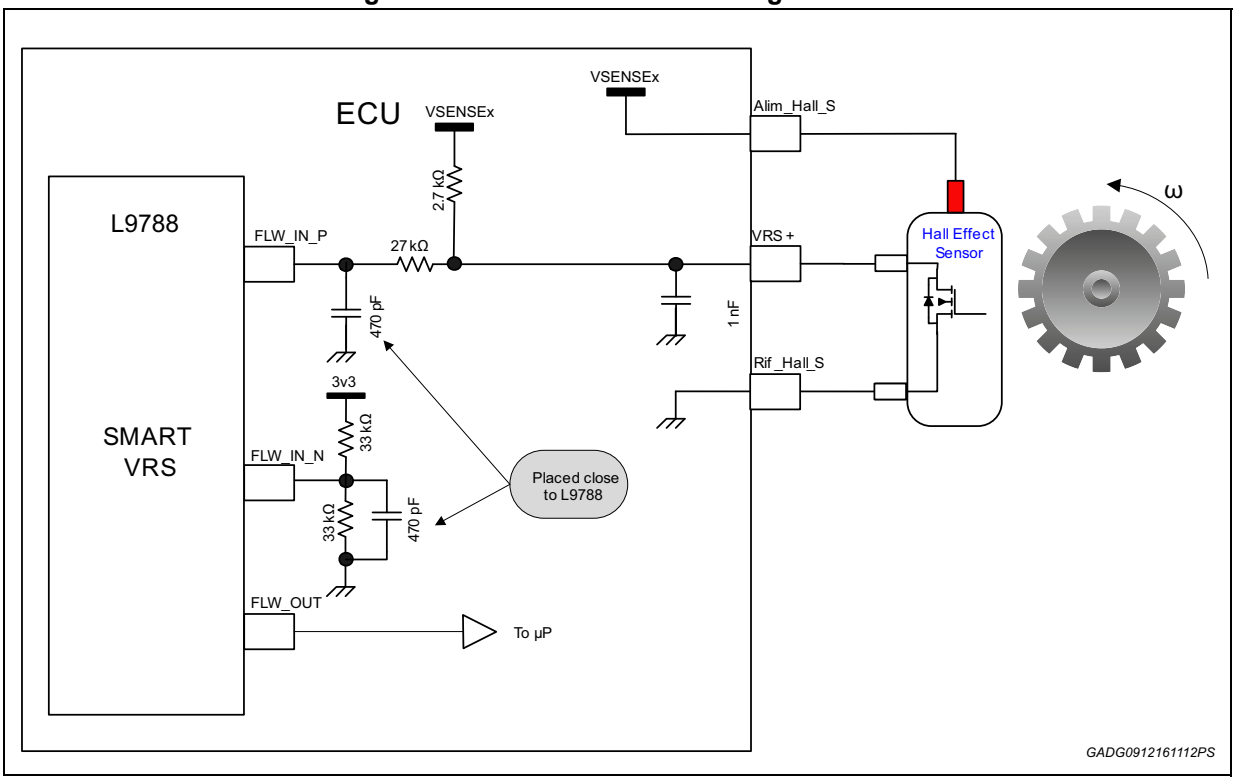
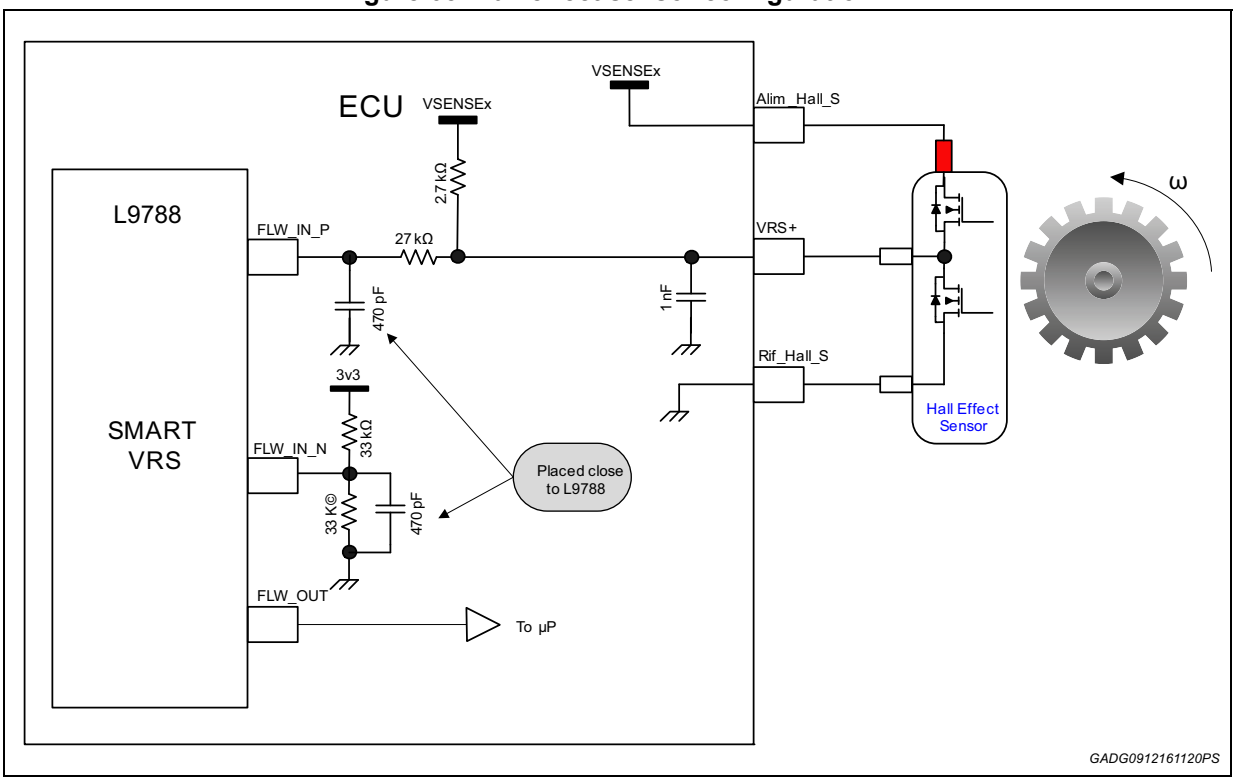


Figure 65. Hall effect sensor configuration 2



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

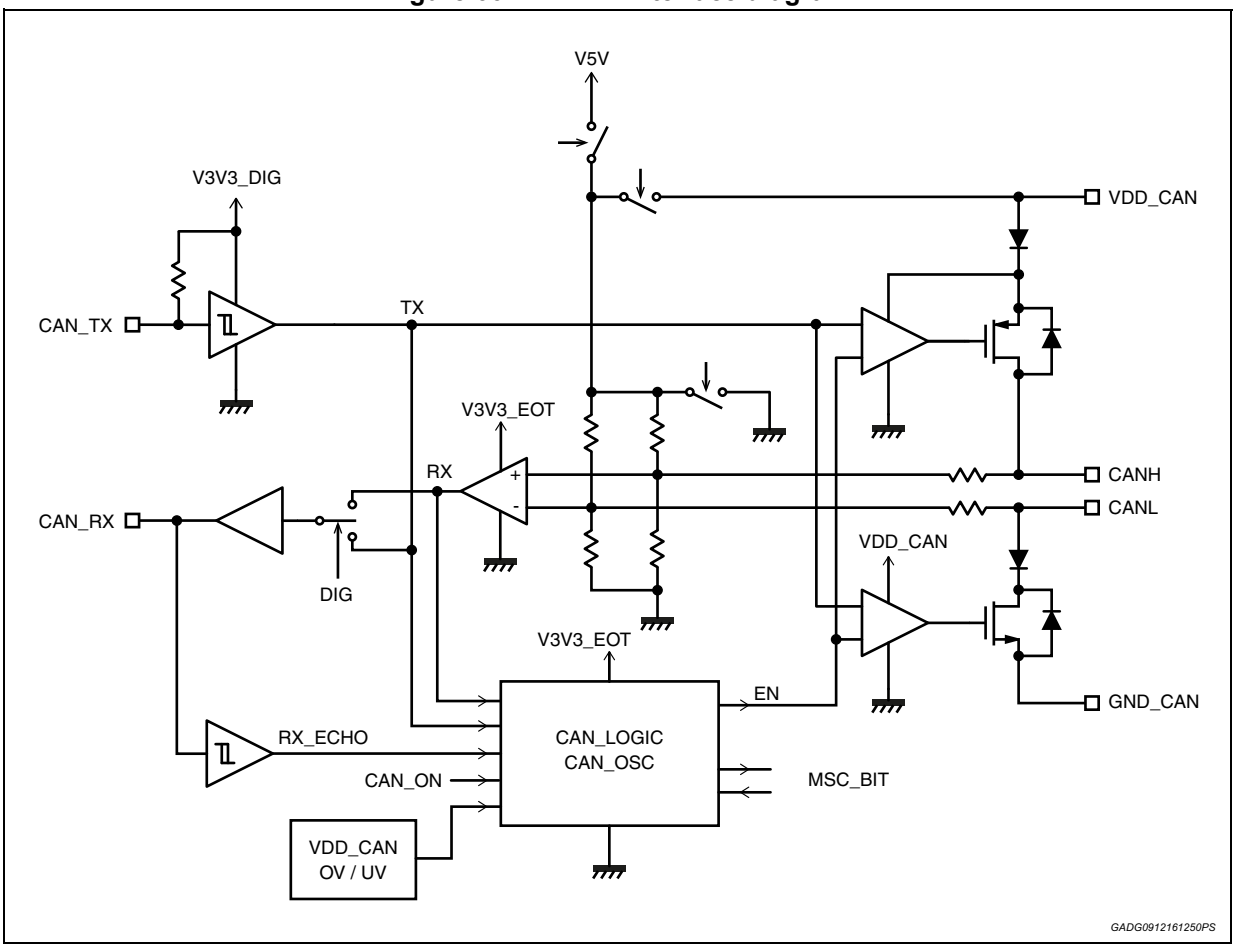
Table 62. Flying wheel interface function - Diagnosis test

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_{iThL}	Input high-to-low differential threshold voltage	-	-50	0	50	mV	FLW_IN_P FLW_IN_N
V_{CM}	Common mode operating range	Not to be tested. It is an application note.	0	1.65	3	V	FLW_IN_P FLW_IN_N
V_{clpH}	Input high clamping voltage	|I_FLW_IN_P|=|I_FLW_IN_N|= 20 mA, device ON	3.3 -0.3	-	3.3 +0.3	V V	FLW_IN_P FLW_IN_N
V_{clpH}	Input high clamping voltage	|I_FLW_IN_P|=|I_FLW_IN_N|= 20 mA, device OFF	1	-	2.8	V	FLW_IN_P FLW_IN_N
V_{clpL}	Input low clamping voltage	|I_FLW_IN_P|=|I_FLW_IN_N|= 20 mA	-1.5	-	-0.3	V	FLW_IN_P FLW_IN_N
$V_{openload}$	Output open load voltage	FLW_IN_P = FLW_IN_N = $V_{openload}$	1.5	(3.3) /2	1.8	V	FLW_IN_P FLW_IN_N
I_{bvrsp}	Input bias current Vrsp	VRS_INP -> FLW_IN_P	-	-	2	µA	FLW_IN_P FLW_IN_N
I_{bvrsm}	Input bias current Vrsm	FLW_IN_N = $V_{openload}$	-	-	2	µA	FLW_IN_P FLW_IN_N
V_{OL}	Output Low Voltage	VDD5 = 5 V or 3.3 V $I_{sink\ current}$ = 2 mA	-	-	0.5	V	FLW_OUT
V_{OH}	Output High Voltage	VDD5 = 5 V or 3.3 V $I_{source\ current}$ = 2 mA	VDD5 -0.5	-	-	V	FLW_OUT
I_{lk_outvrs}	Input leakage current to GND	-	-	-	1	µA	FLW_OUT
I_{lk_outvrs}	Input leakage current to VDD5	-	-	-	8	µA	FLW_OUT
Td_on_outvrs	Delay on falling edge	Test Ext cap = 300 pF	-	-	1	µs	FLW_OUT
Td_off_outvrs	Delay on rising edge	Input signal=4ms	-	-	150	µs	FLW_OUT
T_r_Out_vrs	MRX Rise Time	Test Ext cap = 300 pF	-	-	150	ns	FLW_OUT
T_f_Out_vrs	MRX Fall Time	Test Ext cap = 300 pF	-	-	150	ns	FLW_OUT
$V_{outdiag}$	Output diag voltage	FLW_IN_P = open; diag mode	0.9	(3.3)/3	1.3	V	FLW_OUT
$I_{outdiag}$	Output diag Current	FLW_IN_P = open; FLW_IN_N= GND; diag mode	50	65	80	µA	FLW_OUT
V_{outsh} $V_{bdiagth}$	Output Short-circuit range to VBAT Open Load threshold	FLW_IN_P = open; FLW_IN_N = Vramp; diag mode	2.8	3	3.2	V	FLW_OUT
$V_{outshgnddiagth}$	Output Short-to GND range threshold	FLW_IN_P = open; FLW_IN_N = Vramp; diag mode	1.1	1.3	1.5	V	FLW_OUT

Note: When FLW_IN_P and FLW_IN_N are both in input high clamping condition, the clamp voltage of FLW_IN_N is 30 mV (typical) higher than FLW_IN_P.

12 CAN FD interface

Figure 66. CAN FD interface diagram



The pins related to this block are:

- CANH;
- CANL;
- CANTX;
- CANRX;
- GND_CAN;
- VB_CAN;
- VDD_CAN

VDD_CAN= 5V is the supply for the CAN transceiver block. The voltage on this pin is monitored and if the voltage is below VDD_CAN_SUP_LOW for a $t_{cansuplow}$ filter time an undervoltage fault on VDD_CAN is detected. The fault is latched in a dedicated MSC flag *CAN_SUP_LOW* until an MSC Upstream Read14 is given. While the undervoltage fault is detected on VDD_CAN the CAN transmitter stays disabled (not MSC read clear access is necessary to restore the transmitter just the fault detection expiration).

If VDD_CAN is above VDD_CAN_SUP_OV for a *tcansuphigh* filter time an overvoltage fault on VDD_CAN is detected. The fault is latched in a dedicated MSC flag *VDD_CAN_OV* until an MSC Upstream Read14 is given during the MSC flag VDD_CAN_OV stays set the CAN transmitter is disabled

During a VDD_CAN overvoltage or undervoltage detected fault the biasing voltage is switched from VDD_CAN to a pre-regulated internal voltage (2.5V) supplied by VB_STBY. When the fault ends the biasing voltage switches again on VDD_CAN. The msc flag *VDD_CAN_OV or CAN_SUP_LOW* remains latched until an MSC Upstream Read14 is given.

The biasing voltage is switched from VDD_CAN to a pre-regulated internal voltage (2.5V) supplied by VB_STBY also in CAN_BIAS_ON and CAN_BIAS_OFF.

VB_CAN is the signal that enables CAN cell; if this pin is connected to VB_STBY the CAN is enabled while if it's connected to GND the CAN is disabled

12.1 Functional description

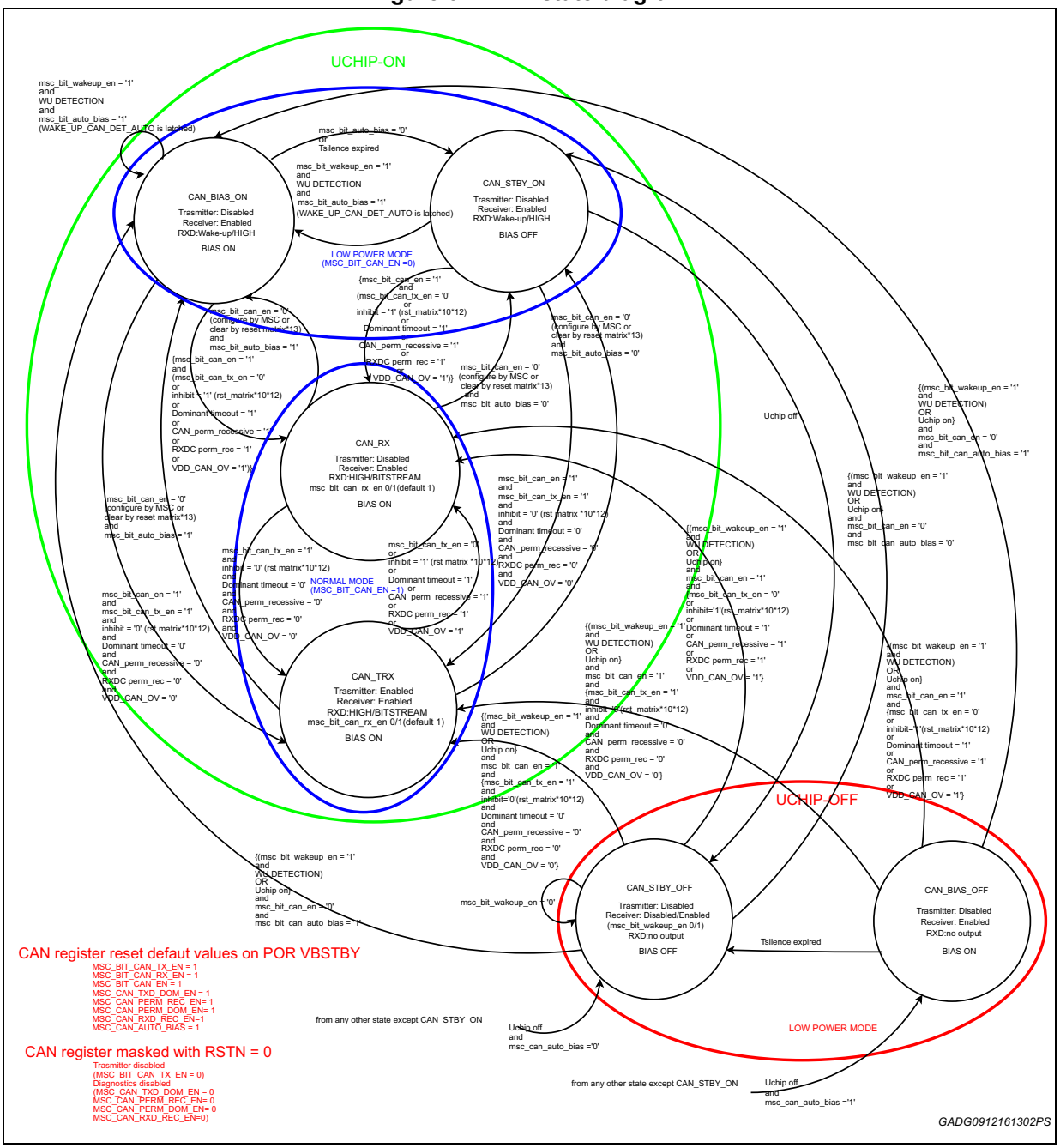
General requirements:

- Compliant with C&S CAN FD certification(ISO16845-2:2015);
- Communication Speed up to 2 Mbit/s. (up to 5Mbit/s in "programming" mode);
- Function range from -27 V to +40 V DC at CAN Pins;
- GND disconnection fail safe at module level;
- GND shift operation at system level;
- Microcontroller interface with CMOS compatible I/O Pins;
- Matched output slopes and propagation delay;
- Receive-only mode available.

In order to further reduce the current consumption in low-power mode, the integrated CAN bus interface offers an ultra low current consumption state when the u-chip is off called Sleep mode.

12.2 CAN state diagram

Figure 67. CAN state diagram



12.3 CAN normal mode

If *CAN_EN* bit MSC_CONFIG-REG17-1[2] is set and the U-chip is in ON state the CAN transceiver is in normal mode (referring to state diagram, CAN_RX or CAN_TRX state). In this state the transmitter and receiver can be configured by MSC (CAN_TX_EN, *CAN_RX_EN*) as follows:

- TRX Standby: transmitter disabled and CAN_RX pin masked to 1(*CAN_TX_EN = '0', CAN_RX_EN = '0'*);
- TRX Listen: transmitter disabled, receiver enabled (**CAN_TX_EN = '0', CAN_RX_EN = '1'**);
- TRX transmit: transmitter enabled CAN_RX pin masked to 1 (*CAN_TX_EN = '1', CAN_RX_EN = '0'*);
- TRX Normal (default): transmitter enabled receiver enabled (*CAN_TX_EN = '1', CAN_RX_EN = '1'*)

In normal mode the CAN biasing is always active

Wake up by CAN disabled option is allowed only for the application that does not require the transceiver (CANH/L not connected to any bus).

12.4 CAN low-power mode

When L9788 is ON it is possible to deactivate the CAN transceiver setting the MSC bit *CAN_EN* (MSC_CONFIG-REG17_1[2]) to zero, sending the CAN in Low-power Mode. The CAN transceiver remains deactivated until it will be activated again setting the *CAN_EN* bit. When L9788 is OFF the CAN transceiver is always in Low-power Mode independently from any other configuration bit except *CAN_WAKEUP_EN*, which if set to zero, sends it to Sleep mode once the transceiver goes to CAN_STBY_OFF state. In Low-power mode the biasing can be active or inactive depending on *CAN_AUTO_BIAS* bit value and from the CAN bus activity (see state diagram), furthermore the transmitter is always disabled and the CAN_RX pin is always masked to recessive. When biasing is disabled the receiver input termination will be biased at zero volt.

12.5 CAN Sleep Mode

When the CAN transceiver goes in CAN_STBY_OFF with *CAN_WAKEUP_EN = '0'* it falls in an ultra low current consumption state called Sleep mode. In this state for the L9788 is impossible to detect Wake-up activity on CAN bus and consequently no power-up is done for a CAN detection (pattern or no pattern).

12.6 CAN error handling

CAN Driver HS and LS are supplied by a dedicated pin (VDD_CAN) to avoid disturbances of CAN activity on main supply lines. After internal power on reset of VB_STBY the CAN transceiver is configured according to the configuration register bit default values. When the

CAN transceiver is in normal mode, the transmitter is disabled and its state changes to CAN_RX in case of at least one of the following events:

- Dominant TxDC time out and *CAN_TXD_DOM_EN MSC bit = 1*;
- CAN permanent recessive *CAN_PERM_REC_EN MSC bit = 1*;
- RxDC permanent recessive *CAN_RXD_REC_EN MSC bit = 1*;
- VDD_CAN overvoltage detection (MSC bit *VDD_CAN_OV = 1*);
- VDD_CAN undervoltage detection active;
- MSC bit *CAN_TX_EN = 0*;
- Reset matrix Conditions *10*12 (see Reset Matrix section).

The CAN receiver is not disabled in case of any failure condition.

The device provides the following 4 error handling features; the CAN error handling function can be disabled by setting the dedicated corresponding MSC bit. The error handling must be also enabled by setting the *CAN_EN* bit MSC_CONFIG-REG17-1[2].

12.6.1 Dominant CAN_TX time out

If CAN_TX is in dominant state (low) for t > $t_{TXDC\_DOM\_TO}$ the transmitter will be disabled, CAN_TXD_DOM status bit will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared or until the state returns recessive according to the setting of the bit *CAN_TX_DOM_ERR_CFG* MSC CONFIG-REG21 [0]. The detection of this error is enabled by the *CAN_TXD_DOM_EN* bit MSC_CONFIG_REG21[3] and by the *CAN_TX_EN* bit MSC_CONFIG_REG17_1[3].

12.6.2 CAN permanent recessive

If CAN_TX changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter will be disabled, *CAN_PERM_REC* status bit will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared. The detection of this error is enabled by the CAN_PERM_REC_EN bit MSC_CONFIG_REG21[4] and by the *CAN_TX_EN* bit MSC_CONFIG_REG17_1[3].

12.6.3 CAN permanent dominant

If the bus state is dominant (low) for t > t_{dom} a permanent dominant status will be detected. *CAN_PERM_DOM* status bit is latched and can be read and cleared by MSC. The transmitter will not be disabled. The detection of this error is enabled by the *CAN_PERM_DOM_EN* bit MSC_CONFIG_REG21[5].

12.6.4 CAN_RX permanent recessive

If CAN_RX Pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if CAN_RX does not follow CAN_TX for 4 times the transmitter will be disabled. *CAN_RXD_REC* status bit will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared. The detection of this error is enabled by the *CAN_RXD_REC_EN* bit MSC_CONFIG_REG21[6] and by the *CAN_TX_EN* bit MSC_CONFIG_REG17_1[3].

12.6.5 Smart reset RSTN effects

In order to avoid spurious interference on CAN Bus and false CAN error detection, during the power-up sequence, as long the Smart Reset RSTN pin signal stays low the following CAN configuration registers are masked to zero:

- *CAN_TX_EN* (transmitter disabled);
- *CAN_TXD_DOM_EN* (Dominant TxDC Time Out disabled);
- *CAN_PERM_REC_EN* (CAN Permanent Recessive disabled);
- *CAN_PERM_DOM_EN* (CAN Permanent Dominant disabled);
- *CAN_RXD_REC_EN* (CAN RXDC Permanent Recessive disabled).

12.7 Wake up With U-Chip OFF

When the U-chip is off with CAN wake up option enabled (*CAN_WAKEUP_EN = '1'*), the CAN transceiver can detect wake up activity on bus and then wake up the device. In this situation the MSC bit *WAKE_UP_CAN_DET* is latched (MSC UPSTREAM READ 12, Frame3). If the U-chip is off with CAN wake up option disabled (*CAN_WAKEUP_EN = '0'*) and automatic voltage biasing disabled (*CAN_AUTO_BIAS* = '0') the transceiver goes in Sleep mode. Otherwise if the U-chip is off with CAN wake up option disabled (*CAN_WAKEUP_EN = '0'*) and automatic voltage biasing enabled (*CAN_AUTO_BIAS* = '1') the transceiver goes in CAN_BIAS_OFF state and after a period greater than $T_{silence}$ without activity on bus goes in Sleep mode.

12.8 Wake up with U-Chip ON

When the U-chip is on and the CAN transceiver is in low power mode (*CAN_EN bit* = '0') and the wake up option is enabled (*CAN_WAKEUP_EN* = '1'), the CAN Transceiver can detect wake up activity on bus. In this situation the MSC bit *WAKE_UP_CAN_DET_AUTO* is latched (MSC UPSTREAM READ 13, Frame3) and a dominant pulse of t_{dom_pulse} is sent on pad CAN_RX. If the *CAN_AUTO_BIAS* bit MSC_CONFIG_REG21[7] is set and the CAN transceiver is in the state CAN_STBY_ON the detection of a wake up activity will bring the transceiver in the state CAN_BIAS_ON

12.8.1 Wake up options

For the wake up feature the device logic differentiates different Wake-up detection conditions.

12.8.2 Normal pattern wake up

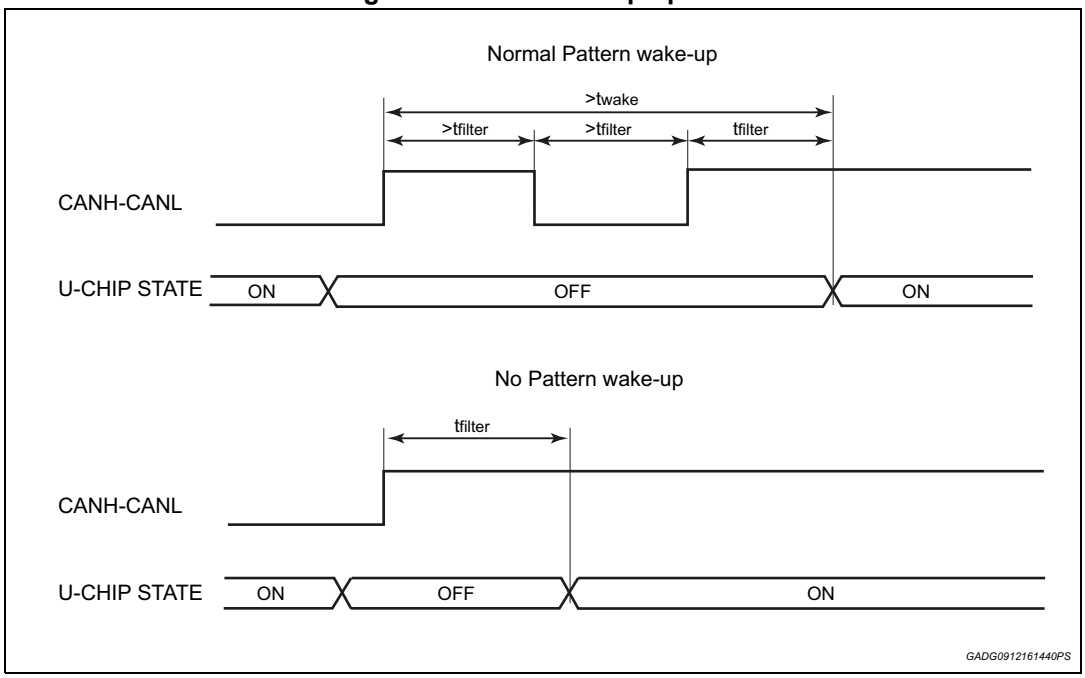
Normal pattern wake up can occur when CAN pattern wake up option is enabled (*CAN_PATTERN_EN* = '1'), the wake up enable bit is set (*CAN_WAKEUP_EN* = '1') and the CAN transceiver is in low-power mode. In order to have a Wake-up detection, the following criteria must be fulfilled:

- The CAN interface wake up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than t_{filter};
- The distance between 2 pulses must be longer than t_{filter};
- The two pulses must occur within a time frame of t_{wake}.

12.8.3 No pattern wake up

If the CAN pattern wake up option is disabled (*CAN_PATTERN_EN* = '0') and the wake up enable bit is set (*CAN_WAKEUP_EN* = '1') and the transceiver is in Low-power mode, a dominant state on CAN BUS for more than t_{filter} will cause a Wake-up detection.

Figure 68. CAN wake up options



12.9 Automatic voltage biasing

If the CAN transceiver is in Low-power mode (*CAN_EN* = 0 or U-CHIP OFF) and the automatic voltage biasing is active (*CAN_AUTO_BIAS* = '1', MSC_CONFIG-REG21[7] if there has been no activity on the bus for longer than $t_{SILENCE}$, the bus lines are biased towards 0 V via the receiver input resistors RCANH/RCANL (biasing disabled) and the MSC flag *CAN_SILENT* is set to 1. If the wake up option is enabled (*CAN_WAKEUP_EN* = '1') and a wake-up activity on the bus lines is detected (wake-up pattern or no pattern), the bus lines are biased to VCANHrec respectively VCANLrec via the internal receiver input resistors RCANH/RCANL also the MSC bit *WAKE_UP_CAN_DET_AUTO* is latched (MSC UPSTREAM READ 12, Frame3). The biasing is activated not later than t_{Bias}.

12.10 CAN reset matrix

In the reset matrix table there is a row dedicated to CAN.

Reset matrix *12 source means that at least one of the following faults is active:

- VDD5_OV;
- OSC FAULT;
- TNL;
- RST_N.

When the CAN transceiver is in normal mode and at least one of the above faults occurs the transmitter is disabled.

Reset matrix *10 source means that at least one of the following faults is active and the *CAN_TDI* bit is set:

- *ERR_CNT*>4;
- *ERR_CNT*>7;
- RST_PRL;

When the CAN transceiver is in normal mode and at least one of the above faults occurs the transmitter is disabled.

Reset matrix *13 source means that at least one of the following faults is active:

1. VB_STBY_UV
2. VB_OV t>TBOV2
3. VB_UV
4. V3V3A_OV, V3V3A_UV, V3V3D_OV and V3V3D_UV
5. VDD5_UV
6. VDDIO_UV

When the CAN transceiver is in normal mode and at least one of the above faults occurs the MSC bit *CAN_EN* is cleared sending the CAN transceiver in Low-power Mode.

12.11 CAN looping mode

If the proper configuration bit (*CAN_LOOP_EN*) in control register is set the TxDC input is mapped directly to the RxDC Pin. This mode can be used in combination with the CAN receive-only mode, to run diagnosis for the CAN protocol handler of the microcontroller.

Figure 69. CAN_TX input structure

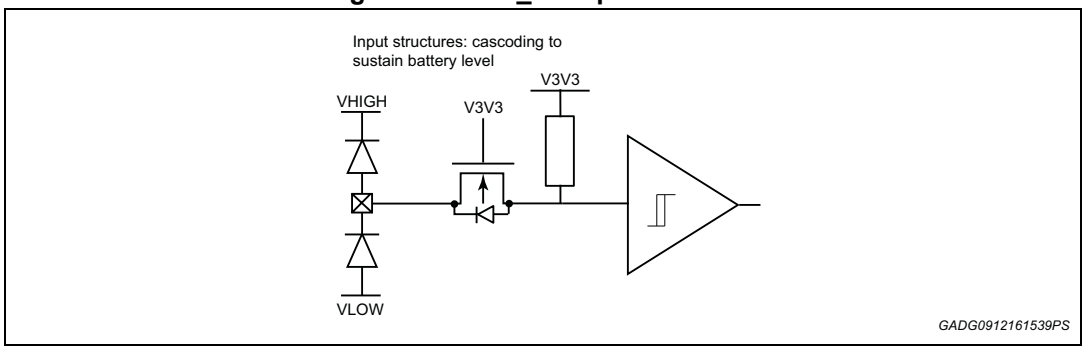
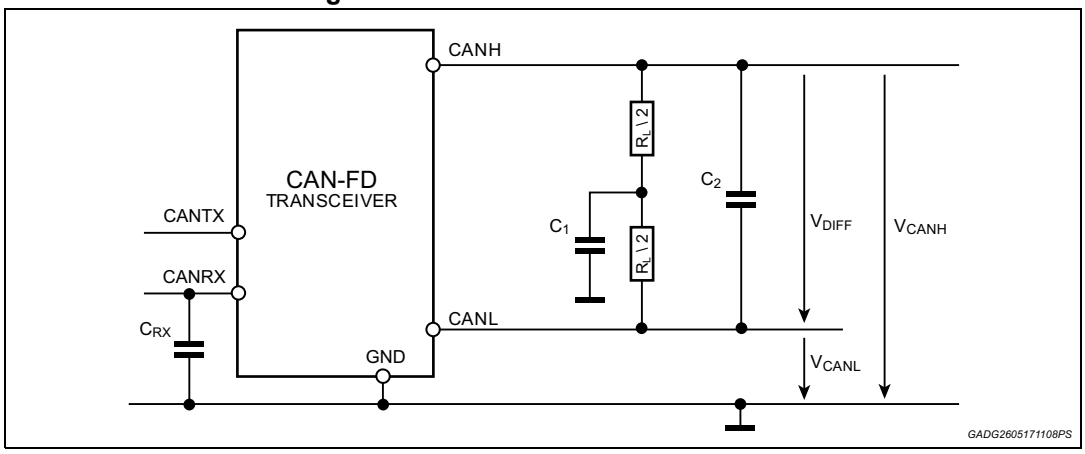


Figure 70. CAN transceiver test circuit



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, 4.5 V ≤ VDD_CAN ≤ 5.5 V, 5 V ≤ VB_STBY ≤ 18 V, T_j -40 to 175 °C unless otherwise specified;

Table 63. CAN threshold related Low supply voltage flag

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD_CAN_SUP_LOW	Threshold to detect CAN Supply low	VDD_CAN decreasing	4.5	4.65	4.8	V	-
VB_CAN_TH(1)	Threshold for CAN cell enable	Not tested For information only	0.8	-	2.2	V	-
VDD_CAN_SUP_OV	Threshold to detect CAN Supply over-voltage	VDD_CAN increasing	6.1	6.85	7.5	V	-

1. Below this threshold all CAN functions are disabled. In case CAN functionality is requested by application VB_CAN has to be shorted to VB_stby, otherwise it should be put to GND to disable CAN block.

Table 64. CAN communication operating range

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD_CAN	Supply Voltage operating range for CAN transceiver	-	4.5	-	5.5	V	-
VCANHL,CM	Common mode Bus voltage (VCANH + VCANL) / 2	Measured with respect to the ground of the CAN transceiver	-12	-	12	V	-
ITRCV_REC(1)	Transceiver current consumption during normal mode from VDD_CAN, Recessive State	$V_{TXDC} = V_{TXDCHIGH}$	-	-	10	mA	-

Table 64. CAN communication operating range (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ITRCV_DOM(1)	Transceiver current consumption during normal mode from VDD_CAN Dominate State	V_{TXDC} = 0 V	-	-	60	mA	-
ITRCV_short	Transceiver current consumption during output short from VDD_CAN	R_L = 50 Ω to 65 Ω; VCANH =- 3 V or VCANL = 40 V	-	-	120	mA	-
ITRCVLPbias	Transceiver current consumption during low-power mode; biasing active from VDD_CAN	R_L = 50 Ω to 65 Ω; V_{TXDC} = $V_{TXDCHIGH}$;	-	-	350	µA	-
ITRCVLP	Transceiver current consumption during low-power mode; biasing inactive from VDD_CAN	RL = 50 Ω to 65 Ω; V_{TXDC} = $V_{TXDCHIGH}$;	-	-	50	µA	-
ITR_VB	Transceiver current consumption from VB_CAN	-	-	-	5	µA	-
BR	Supported Bit-rates	Supported bit-rates at which all requirements are fulfilled Application info	5	-	-	Mb/s	-

1. To be confirmed after ATE measurements.

Table 65. CAN transmit data input: Pin TxDC

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ileak_cantx	Input leakage current	CAN_TX = VDDIO – 1 V	-	-	10	µA	CAN_TX
VTXDCLOW	Input voltage dominant level	-	0.9	-	1.4	V	CAN_TX
VTXDCHIGH	Input voltage recessive level	-	1.45	-	2	V	CAN_TX
VTXDCHYS	VTXDCHIGH-VTXDCLOW	-	0.1	-	0.4	V	CAN_TX
RTXDCPU	TxDC pull up resistor	-	20	50	100	kΩ	CAN_TX
td,TXDC(dom-rec)	TxDC - CANH,L Delay Time dominant - recessive	R_L = 60 Ω (±1%); C2 = 100 pF (±1%); 70% VTXD – VDIFF = 0.5 V; TXDC rise time = 10 ns (10% - 90%) Guaranteed by bench correlation	0	-	140	ns	-

Table 65. CAN transmit data input: Pin TxDC (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
td,TXDC(rec-diff)	TxDC - CANH,L Delay Time recessive - dominant	R_L = 60 Ω (±1%); C2=100pF (±1%); 30% VTXD – VDIFF = 0.9 V; TXDC fall time = 10ns (90% - 10%) Guaranteed by bench correlation	0	-	120	ns	-
tTXDC_DOM_TO	TxDC dominant time-out	-	0.8	2	5	ms	-

Table 66. CAN transmit data output: Pin RxDC

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VRXDCLOW	Output voltage dominant level	Active mode, IRXDC = 2 mA	(0)	0.2	0.5	V	CAN_RX
VRXDCHIGH	Output voltage recessive level	Active mode, IRXDC = -2 mA	VDDIO-0.5	VDDIO -0.2	VDDIO	V	CAN_RX
tr, RXDC	RxDC rise time	CRX = 15 pF, 30% – 70% VRXDC Guaranteed by bench correlation	0	-	25	ns	-
tf, RXDC	RxDC fall time	CRX = 15 pF, 70% – 30% VRXDC Guaranteed by bench correlation	0	-	25	ns	-
td, RXDC (dom-rec)	CANH,L – RxDC Delay Time dominant - recessive	CRX = 15 pF, VDIFF = 0.5V – 70% VRXDC Guaranteed by bench correlation	0	-	120	ns	-
td, RXDC (rec - dom)	CANH,L – RxDC Delay Time recessive - dominant	CRX = 15 pF, VDIFF = 0.9 V – 30% VRXDC	0	-	120	ns	-

Table 67. CAN transmitter dominant output characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VCANHdom	Single Ended CANH voltage level in dominant state	$V_{TXDC} = V_{TXDCLOW}$; R_L = 50 Ω to 65 Ω;	2.75	3.5	4.5	V	-
VCANLdom	Single Ended CANL voltage level in dominant state	$V_{TXDC} = V_{TXDCLOW}$; R_L = 50 Ω to 65 Ω;	0.5	1.5	2.25	V	-

Table 67. CAN transmitter dominant output characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDIFF, dom	Differential output voltage in dominant state: VCANHdom-VCANLdom	$V_{TXDC} = V_{TXDCLOW}$; R_L = 50 Ω to 65 Ω;	1.5	2.0	3	V	-
VDIFF, dom_extR	Differential output voltage in dominant state: VCANHdom-VCANLdom at extended termination resistor range	$V_{TXDC} = V_{TXDCLOW}$; R_L = 45 Ω to 70 Ω;	1.4	-	3.3	V	-
VDIFF, dom_Arb	Differential output voltage in dominant state: VCANHdom-VCANLdom during arbitration	$V_{TXDC} = V_{TXDCLOW}$; R_L = 2240 Ω;	1.5	-	5	V	-
VSYM	Driver Symmetry: VSYM = (VCANHdom + VCANLdom)/VDD_CAN VDD_CAN = 5V	Measured over one 1 MHz period (1 µs) R_L = 60 Ω (±1%) f_{TXDC} = 1MHz (square wave, 50% duty cycle); C1 = 4.7nF (±5%)	0.9	1	1.1	V	-
IOCANH, dom (-3 V)	CANH output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; VCANH = -3 V;	-115	-		mA	-
IOCANL, dom (16 V)	CANL output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; VCANL = 16 V;	-	-	115	mA	-
IOCANH, dom (40 V)	CANH output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; VCANH = 40 V; Vs = 40 V	0	-	-5	mA	-
IOCANL, dom (40 V)	CANL output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; VCANL = 40 V; Vs = 40 V	(0)	-	115	mA	-

Table 68. CAN transmitter recessive output characteristics, normal mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VCANHrec	CANH voltage level in recessive state (Normal mode)	$V_{TXDC} = V_{TXDCHIGH}$; No Load	2	2.5	3	V	-
VCANLrec	CANL voltage level in recessive state (Normal mode)	$V_{TXDC} = V_{TXDCHiGH}$; No Load	2	2.5	3	V	-
VDIFF, recOUT	Differential output voltage in recessive state (Normal mode): $V_{CANHrec}$-$V_{CANLrec}$	$V_{TXDC} = V_{TXDCHIGH}$; No Load	-50	-	50	mV	-

Table 69. CAN transmitter recessive output characteristics, low power mode, biasing active

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VCANHrecLPbias	CANH voltage level in recessive state	$V_{TXDC} = V_{TXDCHIGH}$; No Load 5.5 V ≤ VB_STBY ≤ 18 V	2	2.5	3	V	-
VCANLrecLPbias	CANL voltage level in recessive state		2	2.5	3	V	-
VDIFF, recOUTLPbias	Differential output voltage in recessive state $V_{CANHrec}$-$V_{CANLrec}$		-50	-	50	mV	-

Table 70. CAN transmitter recessive output characteristics, low-power mode, biasing inactive

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VCANHrecLP	CANH voltage level in recessive state	$V_{TXDC} = V_{TXDCHiGH}$; No Load	-0.1	0	0.1	V	-
VCANLrecLP	CANL voltage level in recessive state	$V_{TXDC} = V_{TXDCHiGH}$; No Load	-0.1	0	0.1	V	-
VDIFF, recOUTLP	Differential output voltage in recessive state VCANHrec - VCANLrec	$V_{TXDC} = V_{TXDCHiGH}$; No Load	-50	-	50	mV	-

Table 71. CAN Receiver input characteristics during normal mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VTHdom	Differential receiver threshold voltage recessive to dominant state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	(0.5)	-	0.9	V	-
VTHrec	Differential receiver threshold voltage dominant to recessive state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	0.5	-	(0.9)	V	-

Table 72. CAN Receiver input characteristics during low power mode, biasing active

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VTHdomLPbias	Differential receiver threshold voltage recessive to dominant state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	(0.5)	-	0.9	V	-
VTHrecLPbias	Differential receiver threshold voltage dominant to recessive state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	0.5	-	(0.9)	V	-

Table 73. CAN Receiver input characteristics during low power mode, biasing inactive

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VTHdomLP	Differential receiver threshold voltage recessive to dominant state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	(0.5)	-	1.05	V	-
VTHrecLP	Differential receiver threshold voltage dominant to recessive state	-12 V ≤ V_{CANH} ≤ +12 V, -12 V ≤ V_{CANL} ≤ +12 V	0.4	-	(0.9)	V	-

Table 74. CAN Receiver input resistance

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Rdiff	Differential internal resistance	V_{TXDC} = $V_{TXDCHiGH}$; No Load	12	-	100	kΩ	-
RCANH, CANL	Single Ended Internal resistance	V_{TXDC} = $V_{TXDCHiGH}$; No Load	6	-	50	kΩ	-
mR	Internal Resistance matching RCANH,CANL	Biasing active; VTXDC=VTXDCHIGH; no load R = 2 x (RCAN_H - RCAN_L) / (RCAN_H + RCAN_L)	-0.03	-	0.03	-	-
Cin	Internal capacitance	Guaranteed by design	-	-	66	pF	-
Cin, diff	Differential internal capacitance	Guaranteed by design	-	-	33	pF	-

Table 75. CAN transceiver delay

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Pin
tLOOP,hl	Loop delay TXDC to RXDC (High to Low)	R_L = 60 Ω (±1%); C2 = 100pF (±1%); 30% VTXDC – 30% VRXDC; TXDC fall time = 10ns (90% - 10%); CRX = 15 pF	-	-	255	ns	-
tLOOP,lh	Loop delay TXDC to RXDC (Low to High)	R_L = 60 Ω (±1%); C2 = 100pF (±1%); 70% VTXD – 70% VRXD; TXDC fall time = 10ns (10% - 90%); CRX = 15 pF	-	-	255	ns	-
TBit(RXD) ≤ 1 Mb/s	Recessive bit symmetry at RXDC	R_L = 60 Ω (±1%); VDIFF: 0.5 V(falling) - 0.9 V(rising); C2 = 100pF (±1%); CRX = 15 pF; TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%); Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width. Rectangular pulse signal TTXDC= 6000ns, high pulse 1000ns, low pulse 5000ns	745	1000	1255	ns	-

Table 75. CAN transceiver delay (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Pin
TBit(RXD) ≤ 2Mb/s	Recessive bit symmetry at RXDC	Rectangular pulse signal TTXDC= 3000ns, high pulse 500ns, low pulse 2500ns	400	500	550	ns	-
TBit(RXD) ≤ 5Mb/s	Recessive bit symmetry at RXDC	Rectangular pulse signal TTXDC = 1200 ns, high pulse 200 ns, low pulse 1000 ns	120	200	220	ns	-
TBit(BUS) ≤ 1Mb/s	Recessive bit symmetry at CAN-Bus	R_L = 50 Ω to 65 Ω; VDIFF: 0.5 V(falling) - 0.9 V(rising); CL = 100 pF; CRXD = 15 pF; TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%); Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width Rectangular pulse signal TTXDC = 6000 ns, high pulse 1000 ns, low pulse 5000 ns	800	1000	1100	ns	-
TBit(BUS) ≤ 2Mb/s	Recessive bit symmetry at CAN-Bus	Rectangular pulse signal TTXDC = 3000 ns, high pulse 500 ns, low pulse 2500 ns	435	500	530	ns	-
TBit(BUS) ≤ 5Mb/s	Recessive bit symmetry at CAN-Bus	Rectangular pulse signal TTXDC = 1200 ns, high pulse 200 ns, low pulse 1000 ns; Guaranteed by bench correlation	155	200	210	ns	-
ΔtREC ≤ 2Mb/s	Receiver Timing Symmetry (TBit(RXD) - TBit(BUS))	Rectangular pulse signal TTXDC = 3000 ns, high pulse 500 ns, low pulse 2500 ns; Guaranteed by bench correlation	-65	-	40	ns	-
ΔtREC ≤ 5Mb/s	Receiver Timing Symmetry (TBit(RXD) - TBit(BUS))	Rectangular pulse signal TTXDC = 1200 ns, high pulse 200 ns, low pulse 1000 ns; Guaranteed by bench correlation	-45	-	15	ns	-
Tdom	CAN permanent dominant time-out	Guaranteed by scan	500	700	1000	µs	-
tWUP-RXD	time between WUP(1) on the CAN bus until RXD is active (i.e. the CAN signal is represented at the RXD output)	Wake-Up according to ISO11898-5 RXD output enabled; Guaranteed by scan	0	-	1	ms	-

1. Time starts with the end of last dominant phase of the WUP.

Table 76. Maximum leakage currents on CAN_H and CAN_L, unpowered

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ILeakage, CANH	Input leakage current CANH	Unpowered device; VCANH = 5V ; VCANL = 5 V; VDD_CAN, VB_STBY connected via 0 Ω to GND VDD_CAN, VB_STBY connected via 47 kΩ to GND	-10	-	10	µA	-
ILeakage, CANL	Input leakage current CANL	Unpowered device; VCANH = 5V ; VCANL = 5 V; VDD_CAN, VB_STBY connected via 0 Ω to GND VDD_CAN, VB_STBY connected via 47 kΩ to GND	-10	-	10	µA	-

Table 77. Biasing control timings

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
tfilter	CAN activity filter time	Guaranteed by scan	0.5		1.8	µs	
twake	Wake-up time out	Guaranteed by scan	0.35	1	5	ms	
tSilence	CAN timeout	Guaranteed by scan	600	700	1200	ms	
tBIAS	Bias Reaction Time	R_L = 60 Ω (±1%); C2 = 100 pF (±1%); C1 = 100 pF (±1%); VTXDC = VTXDCLOW; 50% VDIFF; VSYM = 0.1(1); Transition bias inactive to bias active; Guaranteed by scan	-	-	220	µs	-
tcansuphigh	CAN_SUP_LOW filter time	Guaranteed by scan	8.5	10	11.5	µs	-
tcansuplow	VDD_CAN_OV filter time	Guaranteed by scan	8.5	10	11.5	µs	-
tdom_pulse	Dominant interrupt pulse	Guaranteed by scan	47.6	56	64.4	µs	-

1. Measured from the start of a dominant-recessive-dominant sequence (each phase 6µs) until $V_{SYM} \geq 0.1$

Table 78. Standby current consumption (Battery line @RT)

Total quiescent current consumption(1)	Max value	Unit
EOT disabled and CAN block enabled, CAN wake up disabled	60	µA
EOT disabled and CAN block enabled, CAN wake up enabled	70	µA
EOT enabled and CAN block enabled, CAN wake up disabled	70	µA
EOT enabled and CAN block enabled, CAN wake up enabled	80	µA

1. L9788 Total quiescent current consumption at pins VB_STBY, VB_IN, VB_IN_SW, VB_SENSE, CP (through 100 nF capacitor), VB_CAN, MRD, RLY1, LED2, STR2_DRN, PDR1_DRN connected to battery. The total current was measured at battery line @RT.

Table 79. Standby current consumption (Battery line @HT)

Total quiescent current consumption(1)	Max value	Unit
EOT disabled and CAN block enabled, CAN wake up disabled	140	µA

1. L9788 Total quiescent current consumption at pins VB_STBY, VB_IN, VB_IN_SW, VB_SENSE, CP (through 100 nF capacitor), VB_CAN, MRD, RLY1, LED2, STR2_DRN, PDR1_DRN connected to battery. The total current was measured at battery line @HT.

Expected additional current due to bias ON is:

Table 80. can_auto_bias = 1 and can_wakeup_en = 1

-	27 °C, I(VB_STBY)	150 °C, I(VB_STBY)
TYP	548 µA	576 µA
MAX	650 µA	675 µA

Table 81. can_auto_bias = 1 and can_wakeup_en = 0

-	27 °C, I(VB_STBY)	150 °C, I(VB_STBY)
TYP	563 µA	591 µA
MAX	660 µA	690 µA

13 LIN/K-LINE interface

13.1 Functional description

This interface is adapted to *“LIN Specification Rev.2.1”,* and it is also adapted to “*K-LINE Specification (ISO9141)”*.

The Chip has over-voltage protection, loss of ground protection from -27 V to 40 V. -27 V AMR is guaranteed at room & hot temperature. +40 V AMR is guaranteed in all temp range.Short Circuit to Battery or Ground Protection is provided. If the bus line is short circuit to battery, the over current protection is protected by current limitation function. Upon return of connection, normal operation resumes without any intervention on the LIN bus line.

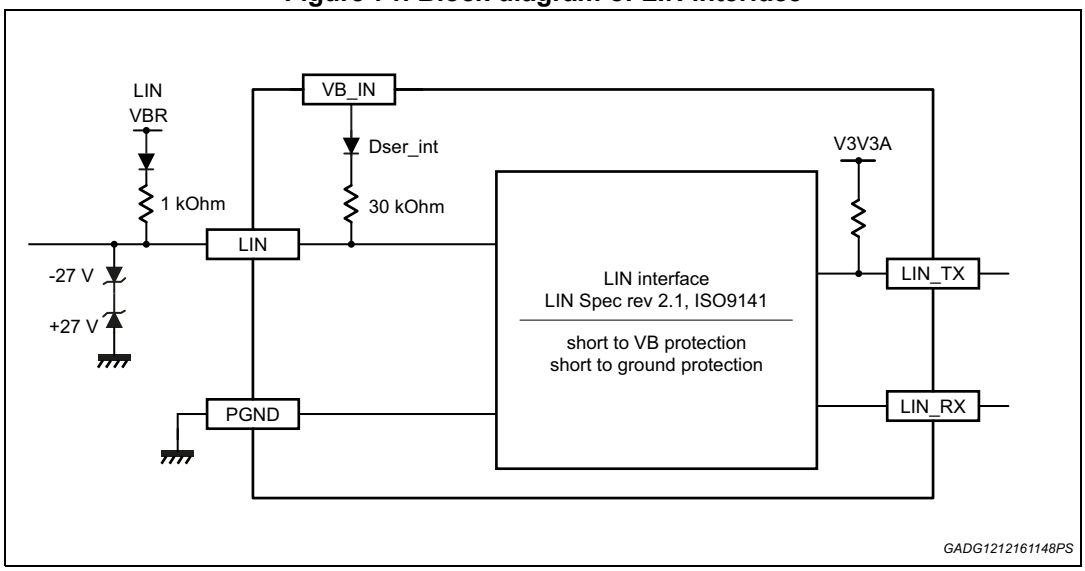
In case of power loss (VB_IN pin disconnected or power off) or ground loss (GND pin disconnected) or LIN block in receive only mode (Transmition function disabled), the LIN driver will not disturb the communication of the remaining transceivers connected to LIN or KLINE bus. Upon return of connection, normal operation will resume without any intervention on the LIN bus line.

LIN-TX is internally pulled up to internal 3.3 V.

All values in this section apply to the entire operating temperature and life of the U-chip.

The LIN block MAX baudrate is 20 Kbit/s.

Figure 71. Block diagram of LIN interface



13.2 LIN receive only mode

There is a MSC bit (*LIN_TX_EN* CONFIG-REG 11) to put the LINE block in receive only mode (Transmition function disabled). Refer to reset matrix for the conditions to enter receive only mode.

13.3 LIN thermal shut down

The LIN block has a dedicated thermal sensor to protect itself.

To protect LIN block from temperature overheat (high battery range of operation, soft short conditions, etc.) a dedicated thermal sensor placed close to power mos is present in the layout sensing FET temperature; one threshold is implemented (T_SD_H) with Hysteresis (T_SD_hys). When the T_SD_H threshold is detected the Driver switches OFF. Once the power stage has been switched-off for over-temperature detection, it will be able to switch on again when temperature is decreased below thermal shut down threshold plus hysteresis value to avoid high frequency on-off cycling.

13.4 LIN error handling

The Chip provides the following 3 error handling features which are not described in the standard LIN Spec Rev2.1, but are realized in different stand alone LIN Interface / microcontrollers to switch the application back to normal operation mode.

The error handling features can be disabled through the *LIN_ERR_EN[2:0]* (CONFIG-REG 11 D1~D3)bit.

13.4.1 LIN dominant TXD timeout

If TXDC is in dominant state (low) for t > t TXDC_DOM_TO=12ms(typ) the transmitter will be disabled, status bit *LIN_TXD_DOM* (Upstream Bit Map Read15 frame 1) will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared or until the state returns recessive, according to MSC configuration bit *LIN_TX_DOM_ERR_CFG*.

13.4.2 LIN permanent recessive

In case TXD changes to dominant (low level) state but RxD signal does not follow within tLIN1: 40 us (typ), the transmitter is disabled. The status bit *LIN_PERM_REC* (Upstream Bit Map Read15 frame 1) is latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared.

13.4.3 LIN Permanent Dominant

In case the bus state is dominant (low level) for more than tLIN2: 12 ms (typ) a permanent dominant status is detected. The status bit *LIN_PERM_DOM* (Upstream Bit Map Read15 frame 1) is latched and can be read and cleared by MSC. The transmitter is not switched off.

Figure 72. LIN TimeOut function

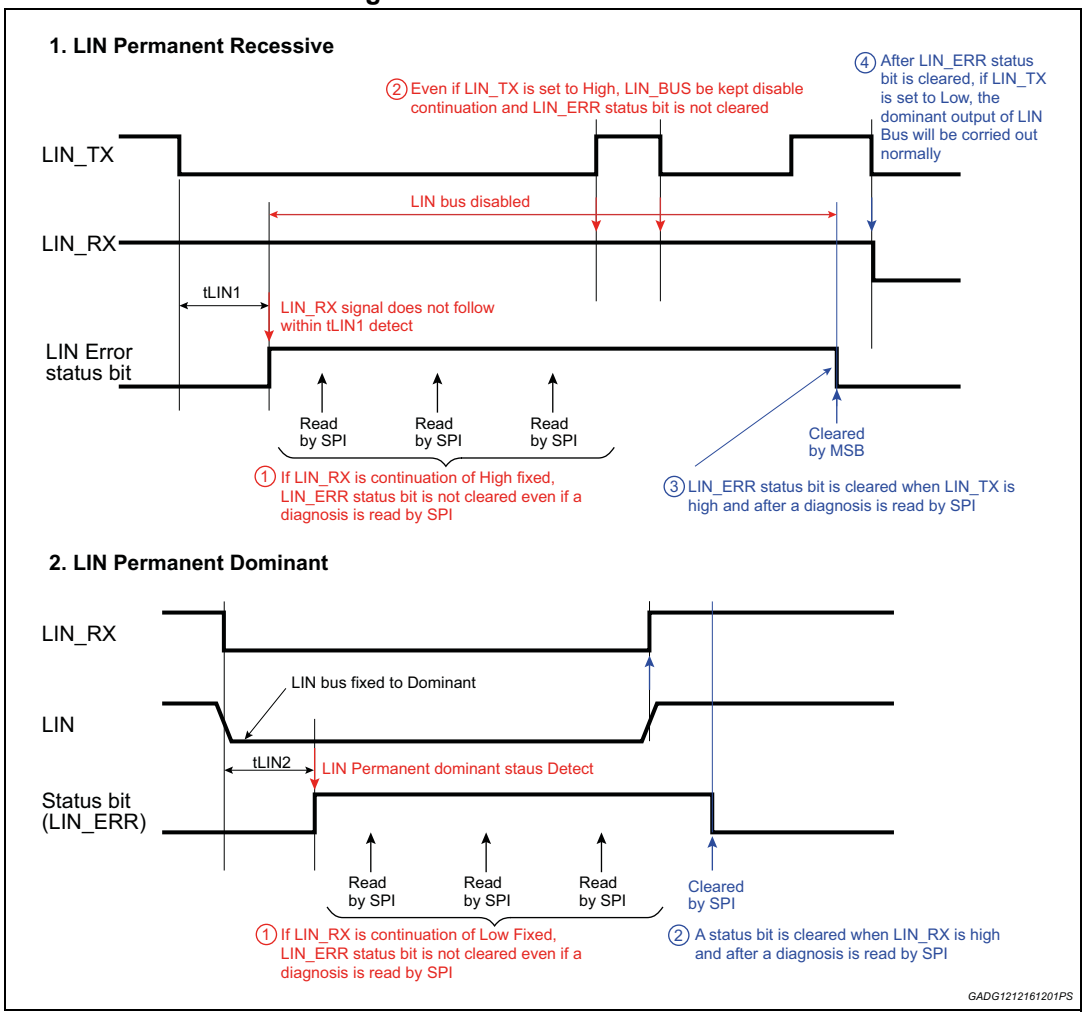
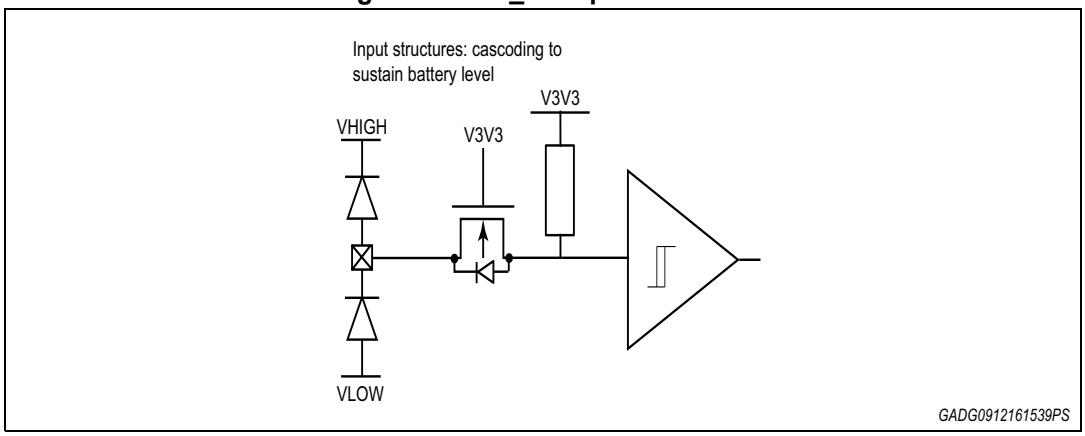


Figure 73. LIN_TX input structure



Conditions:

7 V ≤ VB_IN ≤ 18 V, T_j -40 to 175 °C unless otherwise specified; VB_IN = 18 to 27 V, Tj ≤ 50°C, all specs in limit. In the rest of supply range, parameters are degraded or reset.

If an ECU is not intended to transmit on the LIN bus (e.g. transmit input of a LIN transceiver is recessive), the LIN driver will not drive the LIN bus to dominant state.If the LIN bus is in recessive state, the LIN receiver output will provide a recessive state.

Table 82. Electrical characteristics of LIN interface

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ileak_lintx	Input leakage current	LIN_TX = VDDIO-1 V	-	-	10	µA	LIN_Tx
VIH_T_X	HIGH_level Input voltage	-	1.45	-	2	V	LIN_Tx
VIL_T_X	LOW_level Input voltage	-	0.9	-	1.4	V	LIN_Tx
VHYS_T_X	Input voltage hysteresis	-	0.1	-	0.4	V	LIN_Tx
PULL_T_X	Pull-up resistance	Lin_TX = 0 V	50	100	200	kΩ	LIN_Tx
VOH_R_X	HIGH-level output voltage	Isource = 2 mA	VDDIO -0.6	VDDIO -0.2	-	V	LIN_Rx
VOL_R_X	LOW-level output voltage	Isink = 2 mA	-	0.2	0.5	V	LIN_Rx
VOL_LIN	LOW-level output voltage	Pull up =500 Ω, LIN_Tx = 0 V	-	-	0.2 VB_IN	V	LIN
VOH_LIN	HIGH-level output voltage	Pull up =500 Ω, LIN_Tx = HIGH	0.8 VB_IN	-	VB_IN	V	LIN
I_{bus_dom}	Dominant Source Current	LIN_Tx = HIGH, VB_IN = 12 V, LIN = 0 V	-600	-	0	µA	LIN
I_{bus_res}	Resessive sink current	LIN_Tx=HIGH,VB_IN=8~18V, LIN=8~18V,LIN≥VB_IN	0	-	20	µA	LIN
I_{bus_stby}	Standby current	VB_IN=8~18V, LIN=8~18V,LIN≥VB_IN	0	-	20	µA	LIN
IOVC	Current limitation	LIN=18V, LIN_Tx=0V	70	-	150	mA	LIN
$R_{l\text{-}g\_iso}$	LIN bus to Ground isolation resistance	-	500K	-	-	Ω	LIN
ILK_NG1	Ground loss leakage current	VB_IN=12V, GND = Open, LIN=0~18V	-100	-	100	µA	LIN
ILK_NB1	VB_IN Loss Leakage Current	VB_IN = Open, LIN = 0~18 V	-23	-	23	µA	LIN
t TXDC_DOM_TO	TXDC dominant time-out	-	9	12	15	ms	LIN

Table 82. Electrical characteristics of LIN interface (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
tLIN1 (Time Out)	LIN permanent recessive	-	30	40	50	µs	LIN
tLIN2	LIN permanent dominant	-	9	12	15	ms	LIN
ViD_LIN	Input voltage for dominant state	Application information	-	-	0.4 VB_IN	V	LIN(Bus Receiver)
Vth_DOM	Input voltage for dominant threshold	Application information	0.4 VB_IN	0.45 VB_IN	0.5 VB_IN	V	LIN(Bus Receiver)
ViR_LIN	Input voltage for recessive state	-	0.6 VB_IN	-	VB_IN	V	LIN(Bus Receiver)
Vth_REC	Input voltage for recessive threshold	-	0.5 VB_IN	0.55 VB_IN	0.6 VB_IN	V	LIN(Bus Receiver)
Vth_CNT = (Vth_REC + Vth_DOM) / 2	Input receiver tolerance center voltage	-	0.475 VB_IN	0.5 VB_IN	0.525 VB_IN	V	LIN(Bus Receiver)
Vth_HYS = Vth_REC - Vth_DOM	Input voltage hysteresis voltage	-	0.07 VB_IN	0.1 VB_IN	0.175 VB_IN	V	LIN(Bus Receiver)
tdly(LIN)HL	Output delay time HtoL	Cbus = 10 nF, Pull up = 500 Ω	-	-	50	µs	LIN(Bus Receiver)
tdly(LIN)LH	Output delay time LtoH	Cbus = 10 nF, Pull up = 500 Ω	-	-	50	µs	LIN(Bus Receiver)
tDLY_HL	Input delay time HtoL	CRXD=20pF	-	-	6	µs	LIN(Bus Receiver)
tDLY_LH	Input delay time LtoH	CRXD=20pF	-	-	6	µs	LIN(Bus Receiver)
tDLY	Input delay time	tDLY_HL- tDLY_LH	-2	-	2	µs	LIN(Bus Receiver)
D1	Duty Cycle	$T_{hresmax}$ = 0.744VB_IN, $T_{hdommax}$ = 0.581VB_IN, VB_IN = 7-18 V, tbit = 50 µs, D1 = t_{bus_resmin}/(2xtbit)	0.396	-	-	-	LIN(Bus Receiver)
D2	Duty Cycle	$T_{hresmin}$ = 0.422VB_IN, $T_{hdommin}$ = 0.284VB_IN, VB_IN = 7.6-18V, tbit = 50 µs, D2 = t_{bus_resmax}/(2xtbit)	-	-	0.581	-	LIN(Bus Receiver)
D3	Duty Cycle	$T_{hresmax}$ = 0.778VB_IN, $T_{hdommax}$ = 0.616VB_IN, VB_IN = 7-18 V, tbit = 96 µs, d3 = t_{bus_resmin}/(2xtbit)	0.417	-	-	-	LIN(Bus Receiver)

Table 82. Electrical characteristics of LIN interface (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
D4	Duty Cycle	$T_{hresmin}$ = 0.389 VB_IN, $T_{hdommin}$ = 0.251 VB_IN, VB_IN = 7.6-18 V, tbit=96µs, D4 = t_{bus_resmax}/(2xtbit)	-	-	0.59		LIN(Bus Receiver)
trise_LIN	Slew Rate(LIN)	Cbus = 2.2nF, Rbus = 1kΩ, 40-60%,VB_IN=13.5V	1	2	3	V/µs	LIN(Bus Receiver)
Tfall_LIN	Slew Rate(LIN)	Cbus = 2.2nF, Rbus = 1kΩ, 40-60%,VB_IN=13.5V	0.8	2	3	V/µs	LIN(Bus Receiver)
trise_K_LINE	Slew Rate(K_LINE)	Cbus = 7.2 nF + 2 nF, Rbus = 510 Ω, 20-80%,VB_IN = 18 V	1.2	-	5	V/µs	LIN(Bus Receiver)
Tfall_K_LINE	Slew Rate(K_LINE)	Cbus = 7.2 nF + 2 nF, Rbus = 510 Ω, 20-80%,VB_IN = 18 V	1.2	-	11	V/µs	LIN(Bus Receiver)
T_SD_HIGH	Temperature shut down	-	185	-	200	°C	LIN
T_SD_LOW	Temperature shut down recover	-	175	-	190	°C	LIN
T_SD_hys	Temperature shut down hysteresis	-	5	-	10	°C	LIN
-	Thermal shutdown analog filter time	Guaranteed by design	1.5	-	4	µs	LIN
-	Digital deglitch filter time on Temperature shut down detection	Guaranteed by scan	-	10	-	µs	LIN
Rslave(1)	-	-	20	30	60	kΩ	LIN
VserDiode(1)	Diode drop + pull-up resistor drop	Ibias = 10 µA	0.4	0.7	1.0	V	LIN
VserDiode_drop	Diode drop	Ibias= 550 µA Guaranteed by design	0.4	0.7	1.0	V	LIN
C_{LINIO}	LINIO input capacitance	Guaranteed by design	-	-	25	pF	LIN

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13.4.4 Timing diagram

Figure 74. LIN transmission timing chart

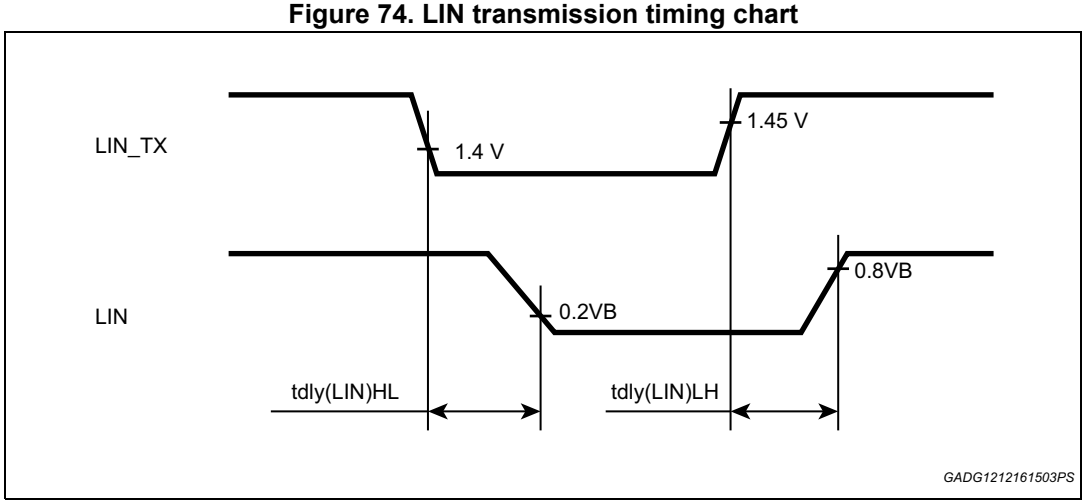


Figure 75. LIN reception timing chart

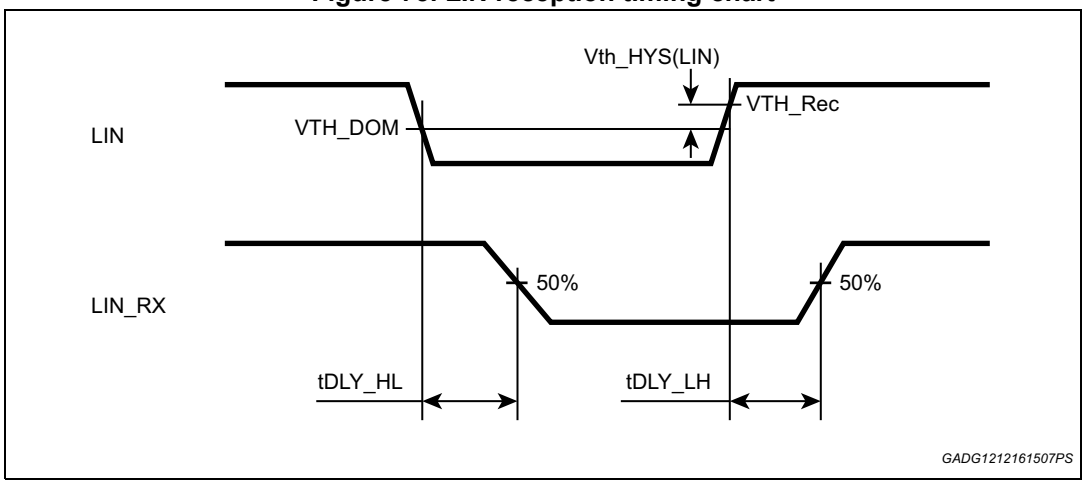


Figure 76. LIN duty cycle timing chart

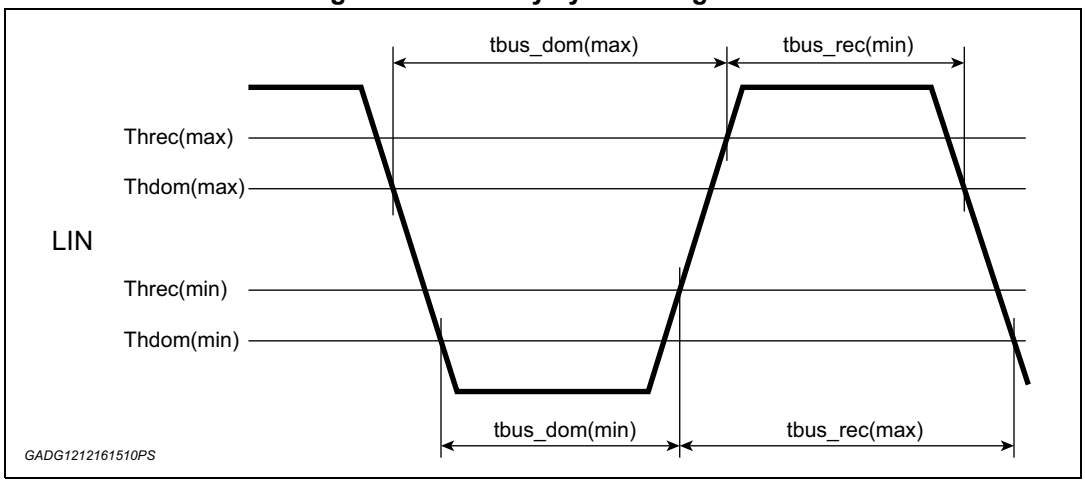


Figure 77. LIN slew rate timing chart

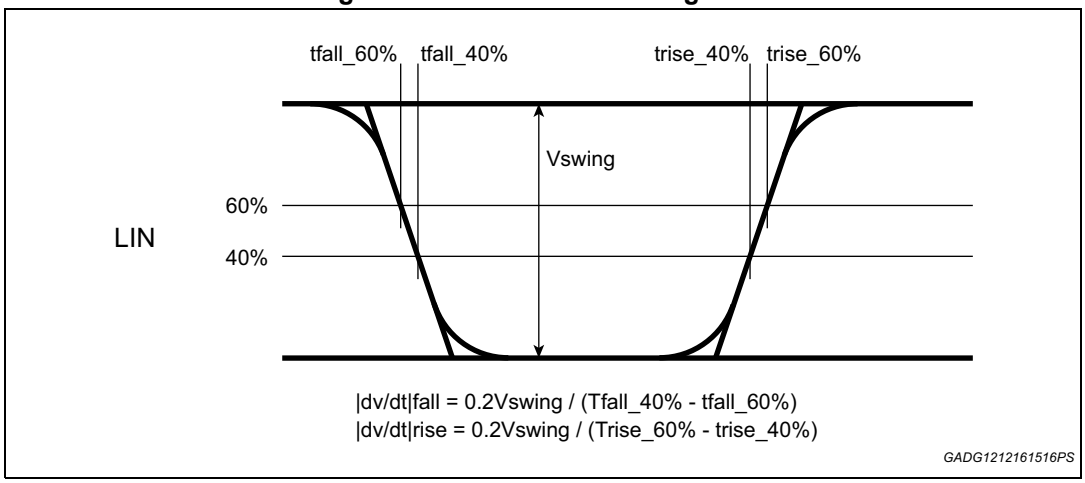
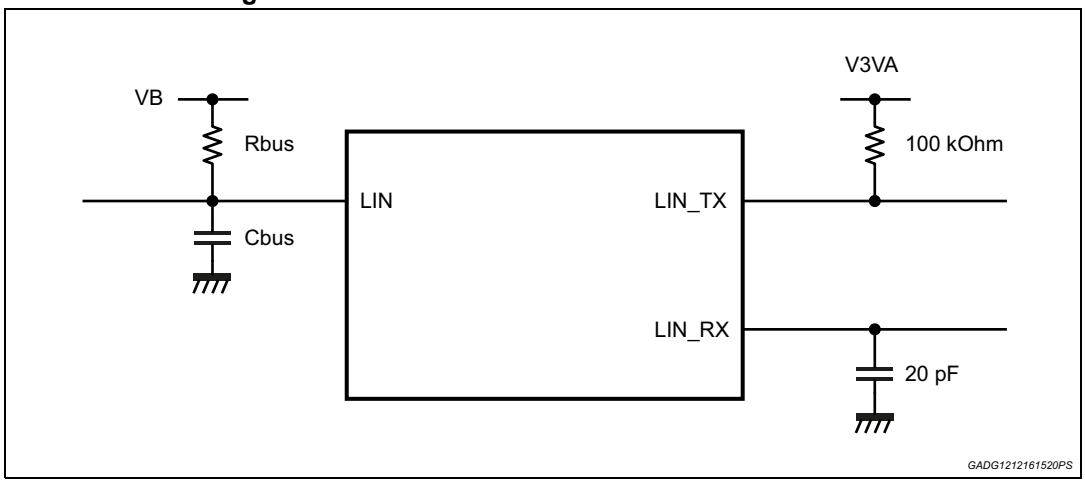


Figure 78. Test circuit for measurement of slew rate



14 Built in self test

14.1 Power supply independency and voltage monitors

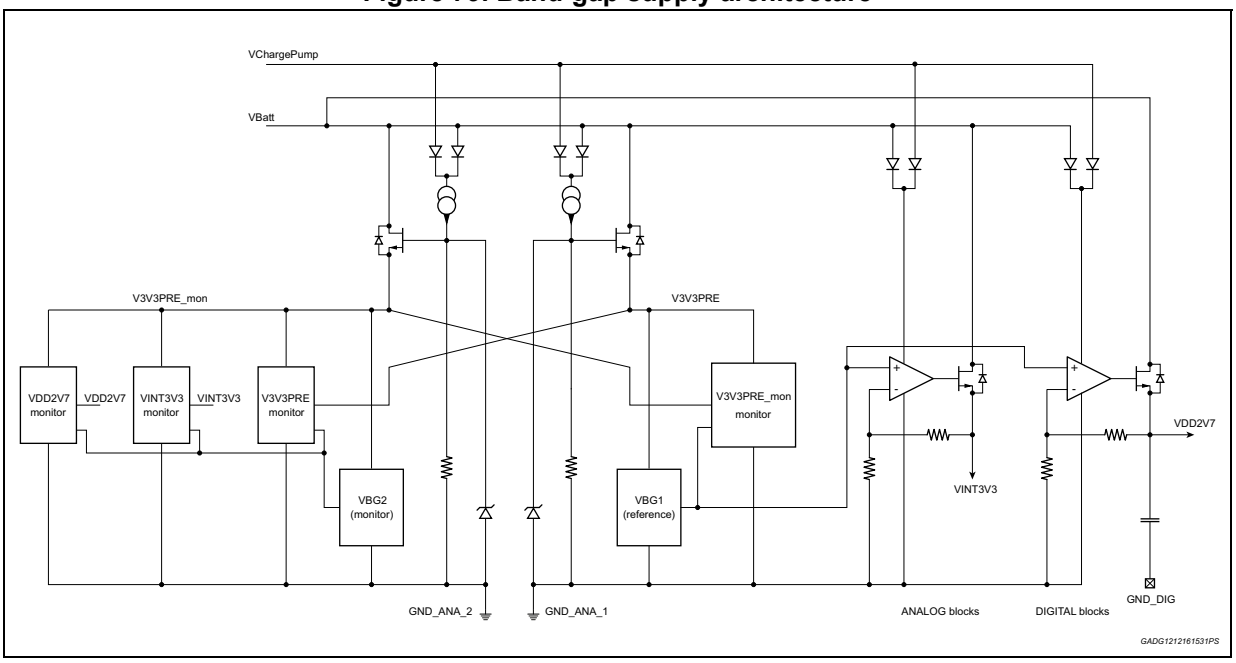
In order to guarantee independence between monitor functions of the L9788 and monitored functions of the same L9788 two independent band-gap references are used; a simple field of application of this concept is the under/over voltage detection of MCU power supply generated by the same L9788.

The basic schematic of the band-gap used to generate the main function and of the band-gap used to monitor it, including their own supply architecture, is shown in *Figure 79*.

Two band-gaps VBG1 and VBG2 are generated starting from protected battery line: VBG1 is used as reference voltage to generate internal analog and digital supply lines and to generate external power supply voltages; VBG2 is used as reference for the uv/ov monitors of these supplies.

The concept to guarantee independence between the two references is that both of them have independent supply and ground architectures to ensure that a single point failure in one of the two structures will not affect the other; independence is achieved by means of physical isolation between the two band-gaps and their supply circuits (A and B areas), isolation is done layouting the circuits in different floor plan areas and by usage of deep trench isolation in between.

Figure 79. Band-gap supply architecture



A cross-referenced monitor is used to detect eventual failures in any of the band-gap supply and enter a safe state: VBG1 is used as reference for the monitor of the supply of VBG2 and VBG2 is used as monitor of the supply of VBG1.

The concept is needed to solve dependencies of band-gap voltage from the supply line: let us suppose that V3V3PRE_mon in the above picture has a fault impacting VBG2 voltage reference, since V3V3PRE_mon is also the supply for monitor circuits a failure in this region

will cause the loss of monitor functionality with an undetected latent fault; the insertion of a monitor supplied from V3V3PRE and referenced to VBG1 allows the detection of this latent. The same concept applies on the vice-versa.

The remaining common points of the internal architecture can be summarized as:

- protected battery line,
- charge pump supply,
- V3V3PRE_mon monitor input (netA),
- V3V3PRE monitor input (netB)

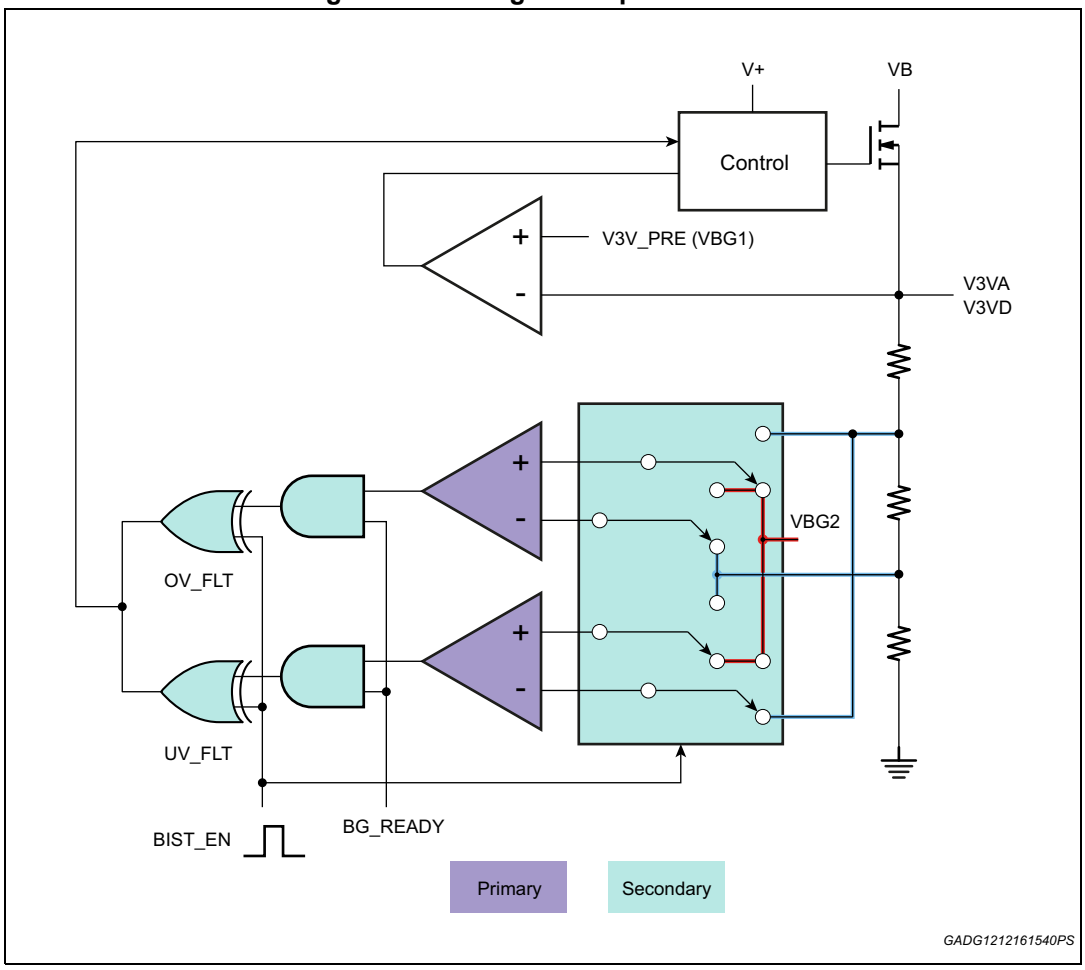
The above points can be tolerated because:

- Protected battery line is the main supply of the L9788, used to generate supply for analog and digital core. All the circuits connected to this rail are capable of high voltage operation, in case the connection is lost no logic supply can be generated and the device will be stuck in reset condition.
- Charge pump is used to guarantee proper functionality during battery cranking only and is useless in normal mode. All the circuits connected to this line are capable of high voltage, in case the line is open it can be detected by dedicated monitor (not shown here) during normal operation or at power-up of the device.
- In case netA is shorted to ground there is fault detection while short to supply line is normal condition, short to VBG1 through V3V3PRE_mon monitor inputs is not possible since the inputs are cascaded; in case a double fault is present (shorted cascade) it will cause an increase in analog and digital supply lines (VINT3V3 and VDD2V7) detected by their monitors using VBG2 reference and triggering safety switch-off path for safety relevant outputs.
- In case netB is shorted to ground there is fault detection while short to supply line is normal condition, short to VBG2 through V3V3PRE monitor inputs is not possible since the inputs are cascaded; in case a double fault is present (shorted cascade) it will cause a failure on the monitor circuit only, without affecting normal functionality until a third fault occurs.

14.2 Analog comparators BIST

For all the safety relevant monitors a self test is implemented to verify that the comparator can detect a variation of the monitored signal applied at its input. The basic implementation scheme is shown in *Figure 80*: comparator inputs are choppered by a diagnostic clock and the output of the comparator is xored with diagnostic clock itself: if the comparator is not able to toggle due to fault condition (internal or external) its output will start toggling following diagnostic clock and causing a self test failure.

Figure 80. Analog bist implementation



The analog bist is applied to the following analog comparators:

V3V3A_OV, V3V3A_UV, V3V3D_OV, V3V3D_UV (internal supply monitors) VDD5_OV, VDD5_UV (VDD5 monitors)

The bist is run on MSC command *BIST_EN*. The result is *read and clear by MSC*.

- On driver section BIST is implemented for diagnostic of main outputs:
- OVC, OPL, STG comparators (injectors)
- STG comparator (igniter)
- The bist is run on MSC command. The result is read and cleared by MSC.

15 Stand-by memory

This memory is a general purpose memory registers array for microcontroller-data which is supposed to be saved during standby when ECU is switched off. Intention is to reduce the number of write cycles in microcontroller-flash.

In case of standby-power-supply failure the data is no longer valid. This condition can be detected reading flag *VB_STBY_UV* MSC_READ13.FRAME2[0].

As long as the standby-power-supply is valid, no data is lost.

There are 15 memory-registers which can be used for application data. The 16th register is an address-register which cannot be used for application data.

Before writing application data into one of the memory-registers, the address of the memory-register must be written into the address-register with the *STBY_NVM_ADD_REG* command.

After setting the address a *STBY_NVM_ADD_REG* command can write the corresponding array byte.

Using the *STBY_NVM_ADD_REG* command and thus updating the address-register is not necessary in case the previously written address is still correct, e.g. when application writes consecutively to the same register.

The memory-register-addresses can have values from 0 to 14. Value 15 is not used for write commands. This means *STBY_NVM_ADD_REG* commands will have no effect when writing to address 15.

The application data is written with mentioned *STBY_NVM_ADD_REG* command which writes one byte (8bit) of application data into the memory-register. To write more than one register, *STBY_NVM_ADD_REG* and *STBY_NVM_ADD_REG* sequences are necessary.

As the other registers above, the upstream reading of the registers is not done register-wise but in blocks of four registers. *MEM_REG1 … 4, MEM_REG5 … 8, MEM_REG9 … 12 and MEM_REG13* … 15 are grouped in the four upstream blocks of Read16.

The address-register MEM_ADR_REG16 is located at the end of the memory and is the 16th register. As mentioned, it cannot be used for application data. It is the fourth byte of the upstream Read16 and can be read back with a read command for this block.

Before upstream-reading, the register-address must be set with the *STBY_NVM_ADD_REG* command. If the previously written address is already the correct one, the *STBY_NVM_ADD_REG* command is not necessary.

For upstream reading of the *MEM_REGx and MEM_ADR_REG16* registers, the command RD_COMMAND16 is used. The RD_COMMAND16 command is the same for all four upstream blocks as the block to be read is defined via the address-register. The read-command will not only read the addressed register, but will read the complete four-byte upstream-block which contains the addressed register.

The *STBY_NVM_ADD_REG* command allows to write a *MEM_VALID* bit (D6) that can be set to 1 by the microcontroller to signal that the memory has been written and validated reading back data. If standby-power-supply is removed *MEM_VALID* bit is reset.

16 DAC

Device integrates a 2-bit DAC, with 4 possible output voltages between 0V and VDD5_IN. The selected level is determined by 2 bits DAC[0:1] into *CONFIG_REG_7*.

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, 4.75 V ≤ VDD_IO ≤ 5.25 V, T_j -40 to 175 °C unless otherwise specified.

Table 83. DAC electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V00	Output voltage 00	-	0.7		1	V	AD_TEST
V01	Output voltage 01	-	1.5		1.8	V	AD_TEST
V10	Output voltage 10	-	2.2		2.8	V	AD_TEST
V11	Output voltage 11	-	3.6		4.7	V	AD_TEST
t_{rise}	Rising time	Transition from 00 to 11 10%-90% open	-	-	10	µs	AD_TEST
t_{fall}	Falling time	Transition from 11 to 00 90%-10% open	-	-	10	µs	AD_TEST

17 ADC

A 10-bit ADC converter is integrated into the device in order to give information about silicon temperature.

A 10-bit conversion can be read with *READ_COMMAND12* MSC frame. Conversion formula is T=MSCcode*290/1024 - 63 (°C).

Conditions:

5.5 V ≤ VB_IN ≤ 18 V, 4.75 V ≤ VDD_IO ≤ 5.25 V, T_j -40 to 175 °C unless otherwise specified.

Table 84. ADC electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ADC_bits	ADC effective number of bits	Guaranteed by design	-	10	-	-	-
T_{range}	Internal junction temperature range	Guaranteed by design	-50	-	200	°C	-
T_{acc}	Temperature accuracy	Guaranteed by design	-10	-	10	°C	-

18 Micro second channel (MSC) interface

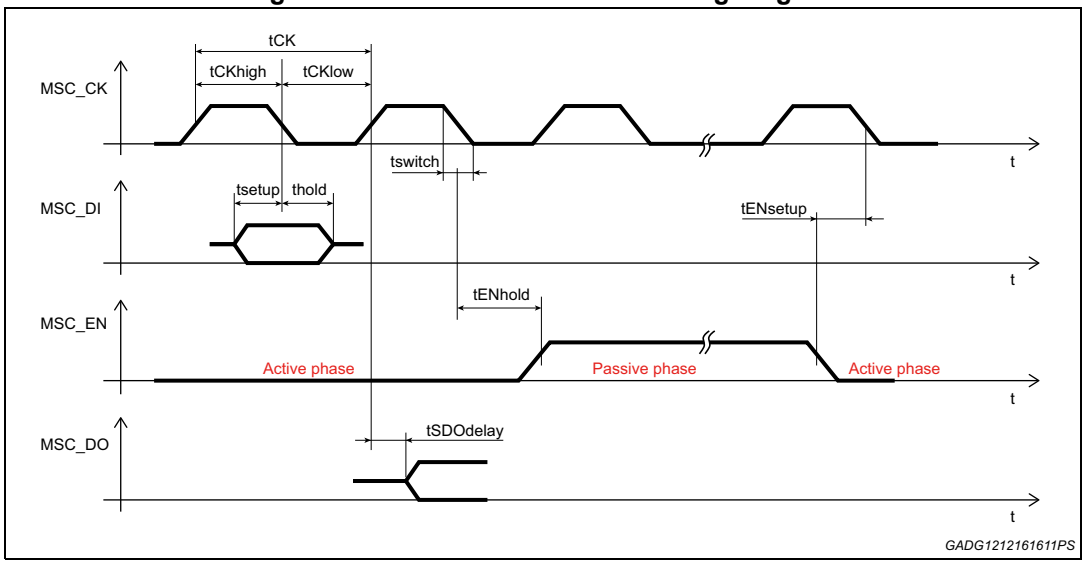
18.1 Function description

The Micro Second Channel interface is an adapted high performance serial bus for power switch device.

L9788 has one Micro Second Channel slave controller capable of receiving up to 35 MHz downstream and transmitting up to 2.18 MBaud upstream.

MSC Clock is supported with synchronous continuous mode. Master clock and data are implemented by LVDS. Slave data out signal is implemented by LVTTL.

Figure 81. MSC communication timing diagram



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, 4.75 V ≤ VDD_IO ≤ 5.25 V, T_j -40 to 175 °C unless otherwise specified.

Table 85. MSC communication timing parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{CK}	Cycle time	Tested by SCAN/	25	-	-	ns	-
t_{setup}	Data setup time	Tested by SCAN/	5	-	-	ns	-
t_{hold}	Data hold time	Tested by SCAN/	5	-	-	ns	-
t_{switch}	Switching time switching time for CL, EN and SI measured between 0.1*VVDD3 and 0.9*VVDD3	Tested by SCAN/	-	-	3	ns	-
t_{CKlow}	CK low time	Tested by SCAN/	7.5	-	-	ns	-
t_{CKhigh}	CK high time	Tested by SCAN/	7.5	-	-	ns	-

Table 85. MSC communication timing parameters (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{ENsetup}$	EN setup time (i.e. time between falling edge of EN and next falling edge of CK)	Tested by SCAN/	5	-	-	ns	-
t_{ENhold}	EN hold time (i.e. time between falling edge of CK and next rising edge of EN)	Tested by SCAN/	5	-	-	ns	-
t_{SDO} /t_{CK}	Data out cycle time F_DO_SEL (CONFIG_REG2 [1:2]) = “11” F_DO_SEL = “10” F_DO_SEL = “01” F_DO_SEL = “00”	Tested by SCAN/	-	128 64 32 16	-	-	-
f_{CK}	Clock range at CK as long as there is a clock at pins MSC_CK_P, MSC_CK_N. $t_{CPP} \geq 2 * t_{CL}$	Tested by SCAN/	-	-	35	MHz	-
	Clock range at CK as long as there is a clock at pins MSC_CK_P, MSC_CK_N. $t_{CPP} \geq 4 * t_{CL}$	Tested by SCAN/	-	-	40	MHz	-
-	tSDOdelay	Tested by SCAN/	-	-	160	ns	-

The MSC is used to receive the input command and data from CPU and to transmit an output data to CPU. Four signals are used according to the timing chart of *Figure 81*:

EN: Bus Enable

There is one input for chip select at pin [EN] This signal is LVTTL Interface from Master to Slave. MSC uses inverted polarity for EN: a logic '1' is a 'passive level' and a logic '0' is a 'active level'. It is possible to drive multiple power devices with shared CL and DI lines and individual EN signal.

CL: Synchronous Serial Clock

The clock pins are [CLP] and [CLN], the differential clock. [CLP]-[CLN] is referred to as CL. The maximum downstream clock rate is CL= 35 MHz.There is an internal resistor between pins [CLP] and [CLN].This signals are LVDS Interface from Master to Slave.

DI: Serial Input Data

Differential inputs for downstream data are pins [DIP] and [DIN]; the differential input signal

[DIP]-[DIN] is referred to as DI. There is an internal resistor between pins [DIPP] and [DIN]. These signals are LVDS Interface from Master to Slave

DO: Serial Output Data

There is one push-pull output for upstream data at pin [DO]. Upstream is done with a lower clock rate fDO, selectable by the microcontroller; after a reset the upstream clock rate is fDO = fCL/32.The upstream clock is synchronous with CL since it is derived from a clock divider.Therefore the CL signal must be always running independently whether a downstream transmission is running or not.This signal is LVTTL Interface from Slave to Master.

Figure 82. Communication diagram between µC and U-CHIP

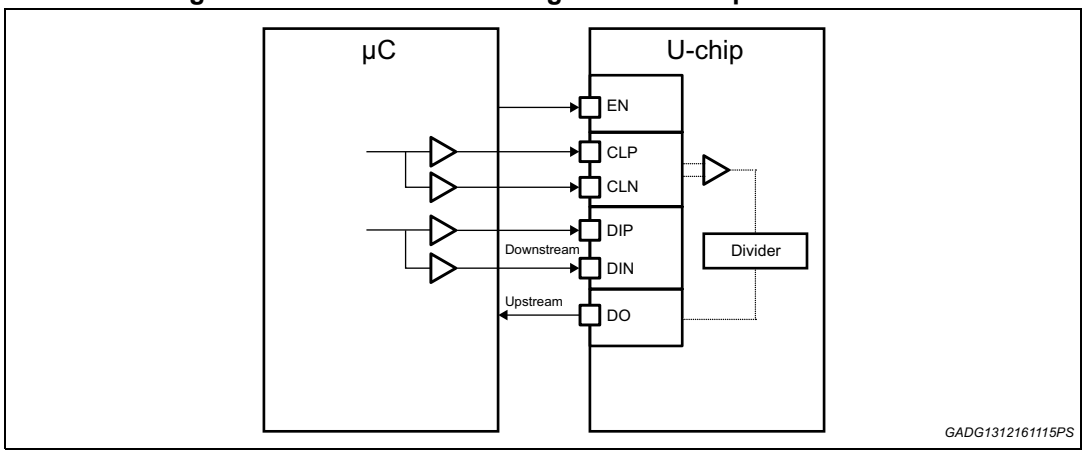
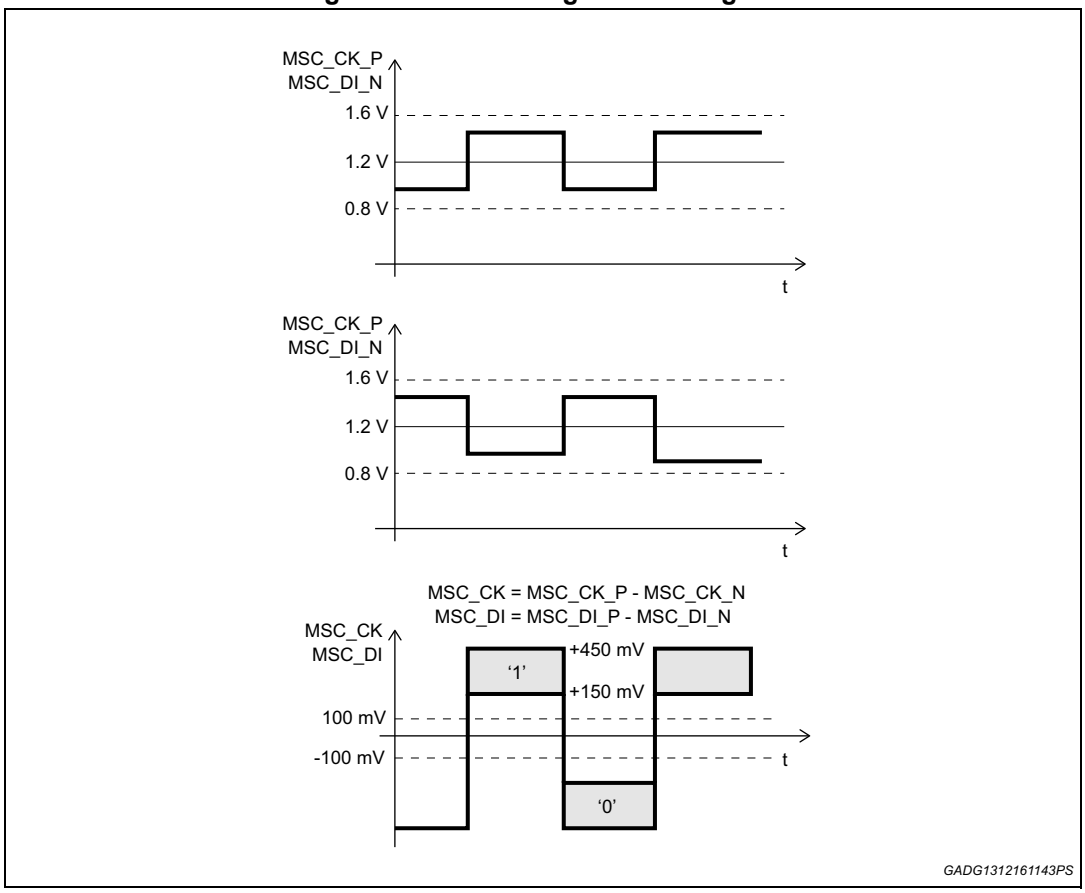


Figure 83. MSC voltage levels diagram



Conditions:

5.5 V ≤ VB_IN ≤ 18 V, 4.75 V ≤ VDD_IO ≤ 5.25 V, T_j -40 to 175 °C unless otherwise specified.

Table 86. MSC electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VCK_P,VCK_N	Input voltage range	Not to be tested. It is an application note.	0.8	-	1.6	V	MSC_CK_P MSC_CK_N
VCKdiff	Differential input voltage VCKdiff =|VCK_P – VCK_N|	Not to be tested. It is an application note.	150	-	450	mV	MSC_CK_P MSC_CK_N
VCKoff	Input voltage offset VCKoff =0.5*(VCK_P + VCK_N)	Not to be tested. It is an application note.	1	-	1.4	V	MSC_CK_P MSC_CK_N
Rck	EXTERNAL Resistor between CK_P and CK_N	Not to be tested. It is an application note.		100	-	Ω	MSC_CK_P MSC_CK_N
Rpu_N	Internal pull-up resistor	-	100	200	400	kΩ	MSC_CK_P MSC_CK_N
Rpd_P	Internal pulldown resistor	-	100	200	400	kΩ	MSC_CK_P MSC_CK_N
VCK_high	Differential input high detection level VCK_high= VCK_P_high – VCK_N_high	-	-	-	100	mV	MSC_CK_P MSC_CK_N
VCK_low	Differential input low detection level VCK_low= VCK_P_low – VCK_N_low	-	-100	-	-	mV	MSC_CK_P MSC_CK_N
VDI+,VDI-	Input voltage range	Not to be tested. It is an application note.	0.8	-	1.6	V	MSC_DI_P MSC_DI_N
VDIdiff	Differential input voltage VDIdiff =|VDI_P-VDI_N|	Not to be tested. It is an application note.	150	-	450	mV	MSC_DI_P MSC_DI_N
VDIoff	Input voltage offset VDIoff =0.5*(VDI_P +VDI_N)	Not to be tested. It is an application note.	1	-	1.4	V	MSC_DI_P MSC_DI_N
Rcl	Resistor between DI_P and DI_N	Not to be tested. It is an application note.	-	100	-	Ω	MSC_DI_P MSC_DI_N
Rpu_N	Internal pull-up resistor	-	100	200	400	kΩ	MSC_DI_P MSC_DI_N
Rpd_P	Internal pulldown resistor	-	100	200	400	kΩ	MSC_DI_P MSC_DI_N
VDI_high	Differential input high detection level VDI_high= VDI_P_high-VDI_N_high	-	-	-	100	mV	MSC_DI_P MSC_DI_N

Table 86. MSC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDI_low	Differential input low detection level VDI_low= VDI_P_low-VDI_N_low	-	-100	-	-	mV	MSC_DI_P MSC_DI_N
VDO_L	DO output low level	VDDIO=5V or 3.3V Isink current=2mA	-	-	0.5	V	MSC_DO
VDO_H	DO output high level	VDDIO =5V or 3.3V Isink current=2mA	VDDIO -0.5	-	-	V	MSC_DO
fDO	Maximum frequency	Tested by SCAN	fCK/128	fCK/64	fCK/16	MHz	MSC_DO
ENL	Low input level	-	-0.3	-	1.1	V	MSC_EN
ENH	High input level	-	2.3	-	VDD5 +0.3	V	MSC_EN
VHYST	Hysteresis	-	0.1	-		V	MSC_EN
IIN	Input current	-		-	32	µA	MSC_EN
RPU	Pull up resistor	-	50	-	250	kΩ	MSC_EN

18.2 Downstream communication

The enable input is active with inverted polarity - i.e. ‘low level' during the active phases of command or data frames. An active enable signal validates the DI input signal. Outside the active phase (enable line is at high level) invalid data may occur at DI. The active phase of a downstream frame starts with the falling edge of the enable signal and ends with the rising edge of the enable signal. The enable signal changes its state with the rising edge of the clock CL. DI changes its state on rising edge and it is latched by L9788 on the falling edge of CL. Downstream frames are synchronous serial frames. They support enable signal and command/data selection bit as part of the frame. Command/data selection bit allows distinguishing frames as command and data frames in the receiver circuit. Command frames and data frames may be sent in any sequence with a passive phase of at least 2 CL-cycles after each frame.

18.2.1 Command frame

A command frame always starts with a high level bit (command selection bit). The number of the command bit of the active phase of a command frame NCB is fixed to 16. If the number of the command bit is not equal to NCB = 16 the frame will be ignored, the command will not be executed and the error flag (*TRANS_L*) will be set. If the MSC command frame has an invalid command the flag "*CMD_ERROR*" is set but no action on outputs is taken. The command frame is ignored.

The length of the command frame's passive phase tCPP must be a minimum of 2 * tCL.

Figure 84. MSC Command Frame bit stream

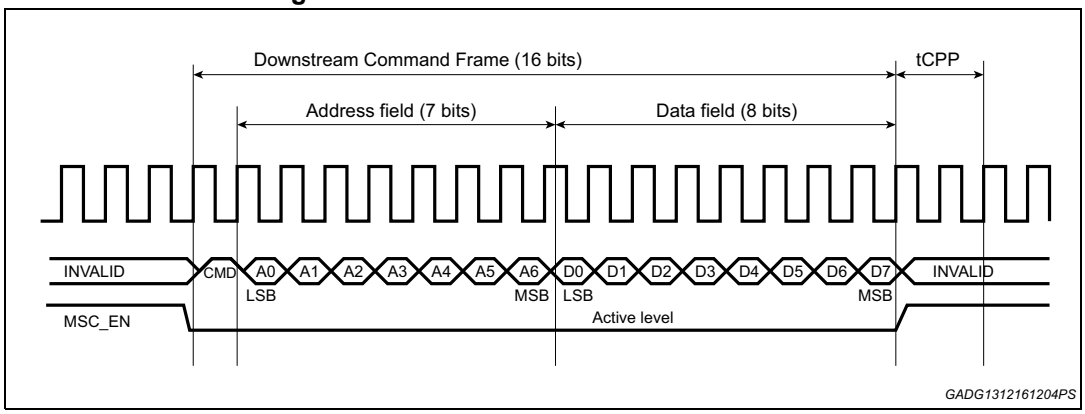


Table 87. MSC Interface command frame

bit	Description
0	=’1’: command selection bit
1-7	Command. LSB first!
8-15	Data for the command. LSB first!

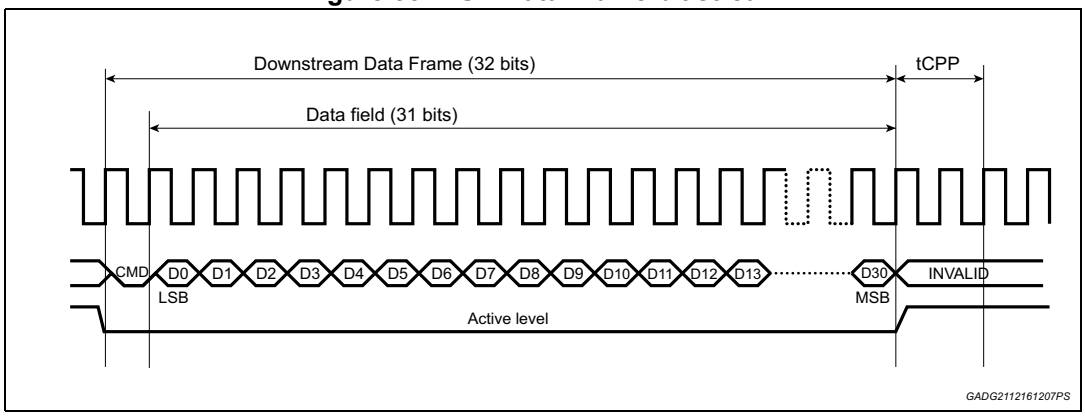
18.2.2 Data frame

A data frame always starts with a low level bit (data selection bit). The number of the data bit of the active phase of a data frame NDB is fixed to 31 bits:

If the number of the data bit is not equal to NDB = 31 the frame will be ignored and the error flag (*TRANS_L*) will be set, but no action on outputs is taken.

The length of the data frame's passive phase tCPP must be a minimum of 2 * tCL.

Figure 85. MSC Data Frame bit stream



Content of DATA frame (transmitted LSB first)

Table 88. MSC Interface Data frame

bit	Description
0	=’0’:DATA selection bit
1-31	D0-D30 CONTROL REGISTER LSB first!

Table 89. Control register

Control Register							
D0	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
LSD-INJ1	LSD-INJ2	LSD-INJ3	LSD-INJ4	LSD-O2H1	-	LSD-O2H2	-
D8	**D9**	**D10**	**D11**	**D12**	**D13**	**D14**	**D15**
LSD-SOL1	LSD-SOL2	LSD-LED1	LSD-LED2	LSD-RLY1	LSD-RLY2	LSD-RLY3	LSD-RLY4
D16	**D17**	**D18**	**D19**	**D20**	**D21**	**D22**	**D23**
LSD-RLY5	LSD-HSD-STR1	LSD-HSD-STR2	LSD-HSD-STR3	FET-PRD1	FET-PRD2	FET-PRD3	FET-PRD4
D24	**D25**	**D26**	**D27**	**D28**	**D29**	**D30**	-
FET-PRD5	IGN1	IGN2	IGN3	IGN4	IGN5	IGN6	-

Note: If RLY4, STR2, STR3 are not configured as starter their status is controlled by the data in control register.

If they are configured as starter their status is controlled by MSC dedicated command.

18.3 Upstream communication

The serial data output [DO] is the synchronous serial data signal of the upstream channel.

The polarity for [DO] is ‚normal polarity'- i.e. a low level bit at [DO] is stored in the µC as a logic ‚0', and a high level bit at [DO] is stored in the µC as a logic ‚1'. The serial data output is single-ended.

The frequency is derived from fCL by an internal divider to typ. fDO = fCL/32. It can be adjusted via *MSC* to fDO = fCL/16... fCL/128. The time for a bit is TSDO = 1/fDO.

Each upstream frame consists of 16 bit:

- 1 start bit, always '0'
- 4-bit-upstream address field (A[0..3] with LSB first)
- 8 bit data upstream data field (D[0..7] with LSB first)
- 1 upstream parity bit (with even parity for the complete data frame)
- 2 fDO stop bit, always '1'.

There are 16 commands to perform read accesses.

All the read command READ-N Upstream Block are composed of 4 continued frames sent to µC.

Within the execution of these read commands an upstream data frame is sent after the 2 stop bits of the prior upstream data frame and one additional interframe bit waiting time. If a new read command is received while the up-stream communication is active, the 16 bit up-stream on-going is completed and the new read command is canceled. At the end of the upstream frame the latched flags contained in the register are cleared automatically, if the frame is interrupted by new read command, flags will not be cleared. The time from the read command to the first upstream frame of the answer is less than 100 µs.

Outside the upstream frame the DO output is high impedance

Figure 86. MSC upstream

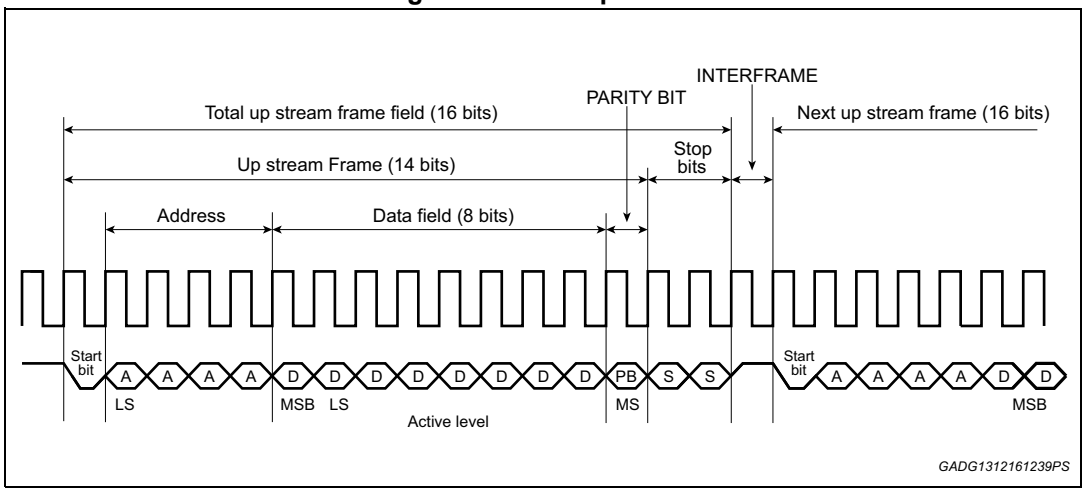
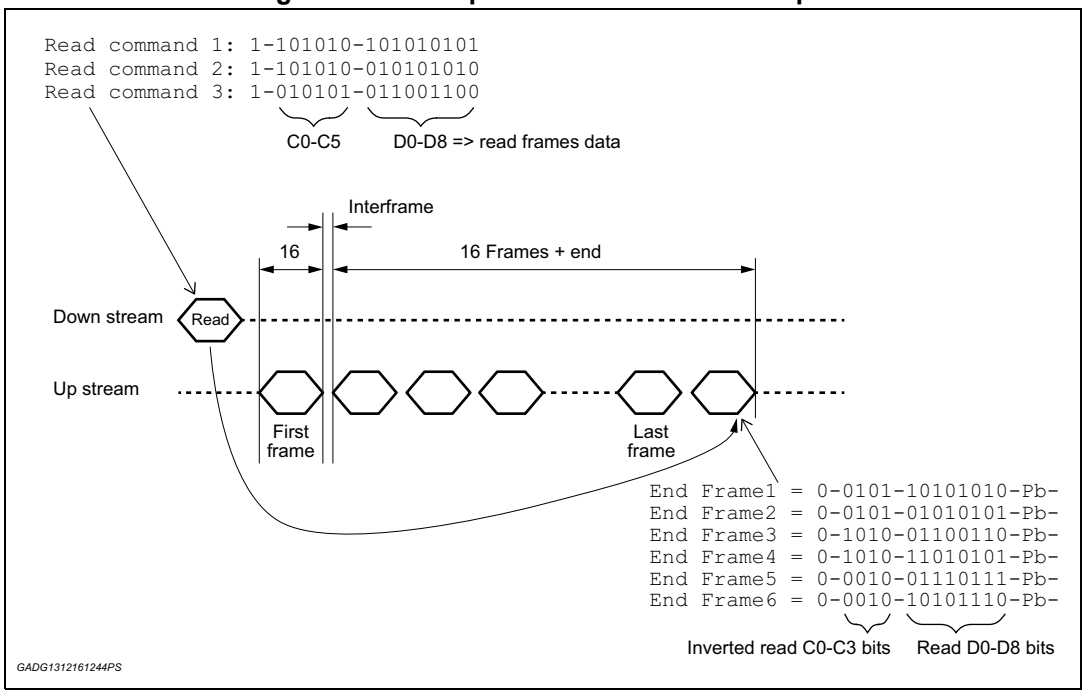


Figure 87. MSC upstream commands example



18.4 Micro Second Channel activity watchdog

MSC data frames are monitored to be sent in intervals shorter than tMSC_mon. If L9788 receives no valid data frame for longer than tMSC_mon, it will switch off all the drivers, removing driver enable command, and the error flag (*TRANS_F*) is set to 1 and internal signal "OUT_DIS" will be set to "0". Note: OUT_DIS = *driver_en* (Read11 frame 1); tMSC_mon is the time needed to send OUT_DIS, it is different from time needed to turn off drivers (which can be different depending on driver type, the maximum time to turn off all drivers is about 300 µs).

To enable again the outputs, the µC has to read the *TRANS_F* and then send the command Enable_Driver, and then outputs are reactivated with the first correct data frame. If the fault flag is not cleared the Enable_Driver command is ignored.

By default the Micro Second Channel activity watch dog is enabled and the monitoring time will start after writing of the internal signal OUT_DIS bit by Enable_Driver command. Each time L9788 receives a valid data frame the tMSC_on timer is reset. This means that micro controller can drive the outputs only when the monitoring module is active.

It is also possible to enable /disable the Micro Second Channel activity watch dog through *MSC_ACT_EN* bit (CONFIG_REG2 D0), 0= disable and 1 = enable (reset value).

Figure 88. MSC activity watchdog time diagram

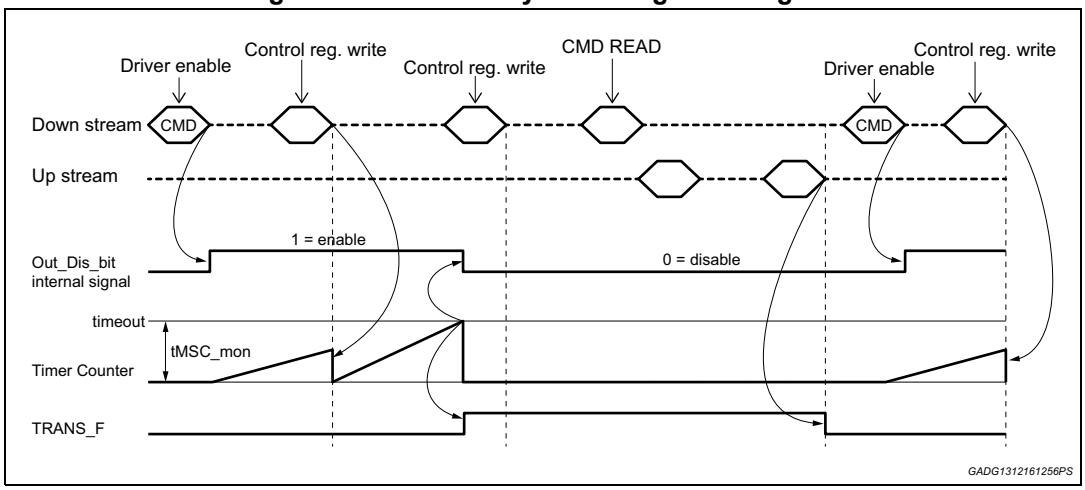


Table 90. MSC Interface Micro Second Channel activity watchdog

Parameter	min	typ	max	unit
tMSC_mon	100	142	185	µs

18.5 Downstream frame Bit Map

MSC Interface DOWN STREAM FRAME Bit Map

Table 91. MSC Interface DOWN STREAM FRAME Bit Map

	ADDRESS							DATA							
	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
RD_COMMAND1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
RD_COMMAND2	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
RD_COMMAND3	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
RD_COMMAND4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
RD_COMMAND5	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1
RD_COMMAND6	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
RD_COMMAND7	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1
RD_COMMAND8	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
RD_COMMAND9	1	0	1	0	1	0	1	1	1	1	0	1	1	1	0
RD_COMMAND10	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1
RD_COMMAND11	0	1	0	1	0	1	0	1	1	1	0	1	1	1	0
RD_COMMAND12	0	1	0	1	0	1	0	0	0	0	1	0	0	0	1
RD_COMMAND13	1	0	1	0	1	0	1	0	1	1	1	0	1	1	1
RD_COMMAND14	1	0	1	0	1	0	1	1	0	0	0	1	0	0	0
RD_COMMAND15	0	1	0	1	0	1	0	0	1	1	1	0	1	1	1
RD_COMMAND16	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0
CONFIG-REG 1	0	0	1	1	1	1	1	PHOLD_EN	PHOLD_TIME[0:1]		LED1_PD_EN	LED2_PD_EN	BOOST_EN	WAKE_UP_TIMER_START_STOP[0:1]	
CONFIG-REG 2	0	1	1	1	1	0	1	MSC_ACT_EN	F_DO_SEL[0:1]		VRS_MODE_SEL	IGN_CURRENT_CFG	IGN_DIAG	IPUPD_EN	IPUPD_MODE

Table 91. MSC Interface DOWN STREAM FRAME Bit Map (continued)

	ADDRESS							DATA							
	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 3	1	1	1	1	0	0	1	RLY4_DLY_OFF_EN	LSD/HSD_DRV1-CFG	LSD/HSD_DRV2-CFG	LSD/HSD_DRV3-CFG	SRT2_EN	STR3_EN	T_SEO_DELAY[0:1]	
CONFIG-REG 4	1	1	0	0	0	0	1	PRD1_IDRV[0:1]		PRD2_IDRV[0:1]		PRD3_IDRV[0:1]		PRD4_IDRV[0:1]	
CONFIG-REG 5	0	0	0	0	1	1	1	PRD5_IDRV[0:1]		PRD1_VDS[0:2]			PRD2_VDS[0:2]		
CONFIG-REG 6	1	1	0	0	1	1	1	PRD3_VDS[0:2]			PRD4_VDS[0:2]			EOT_MODE	IGN_LSD_DIS
CONFIG-REG 7	0	0	1	1	0	0	1	PRD5_VDS[0:2]			TRK_EN[1]	TRK_EN[2]	TRK_EN[3]	DAC[0:1]	
CONFIG-REG 8	1	0	1	1	0	1	1	VRS_DIAG	VRS _MODE[0:1]		VRS _HYS2[0:2]			EN_FALLING_FILT	HYS_FB_SEL
CONFIG-REG 9-0	0	1	0	0	1	0	1	0	1	WDA_RESPTIME[0:5]					
CONFIG-REG 9-1	0	1	0	0	1	0	1	1	0	WDA_WIN_SEL	WDA_INIT				
CONFIG-REG 10	0	0	0	1	1	0	1	WDA_RESP[0:7]							
CONFIG-REG 11	0	1	1	0	1	1	1	LIN/KLINE SEL	LIN_ERR_EN[0]	LIN_ERR_EN[1]	LIN_ERR_EN[2]	LIN_TX_EN	LIN_TX_DIS_FOR_WDA_ERR	VDD5_OF_SEL	O2H2_OC_FLT
CONFIG-REG 12	1	0	0	1	0	0	1	TNL_RST_EN	VB_IN_OV_RST_EN	VDD5_OV_RST_EN	O2H1_OC_FLT	FILTER_MODE	WAKE_UP_CAN_RST	WAKE_UP_EOT_RST	WK_IN_RST
CONFIG-REG 13	1	1	0	1	1	0	1		WDA_PWR_CNT_OFF_DIS	IPUPD_EN_HLS1 IPUPD_EN_STR1	IPUPD_EN_HLS2 IPUPD_EN_STR2	IPUPD_EN_HLS3 IPUPD_EN_STR3	IDIAG_HIGH_INJ	IDIAG_HIGH_SOL	IDIAG_HIGH_PDRV
CONFIG-REG 14	1	1	1	0	0	1	1	RLY1_UC	RLY2_UC	RLY3_UC	RLY4_UC	RLY5_UC	STR1_UC	STR2_UC	STR3_UC
CONFIG-REG15-0 (WUPT_0)	1	0	0	0	0	1	1	0	0	Wake up timer_SET_0[0:5]					

Table 91. MSC Interface DOWN STREAM FRAME Bit Map (continued)

	ADDRESS							DATA							
	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG15-1 (WUPT_1)	1	0	0	0	0	1	0	0	1	Wake up timer_SET_1[6:11]					
CONFIG-REG15-2 (WUPT_2)	1	0	0	0	0	1	0	1	0	Wake up timer_SET_2[12:17]					
CONFIG-REG15-2 (WUPT_3)	1	0	0	0	0	1	1	1	1	Wake up timer_SET_3[18:23]					
CONFIG-REG16-0	0	0	1	0	0	1	1	0	1	PRD1_BLK[0:1]		PRD2_BLK[0:1]		PRD3_BLK[0:1]	
CONFIG-REG16-1	0	0	1	0	0	1	1	1	0	PRD4_BLK[0:1]		PRD5_BLK[0:1]		O2H_PDRV_1	O2H_PDRV_3
CONFIG-REG17-0	0	0	1	0	0	1	0	0	0		O2H1_SR	O2H1_OC_TH		O2H2_SR	O2H2_OC_TH
CONFIG-REG17-1	0	0	1	0	0	1	0	1	1	CAN_EN	CAN_TX_EN	CAN_WAKEUP_EN	CAN_PATTERN_EN	CAN_RX_EN	CAN_2_5_MB
STBY_NVM_ADD_REG	0	1	0	0	1	1	0	0	1	STBY_NVM_ADD[0:3]				MEM_VALID	
STBY_NVM_DATA_REG	1	0	1	1	0	0	0	STBY_NVM_DATA[0:7]							
CONFIG-REG20	1	1	1	1	1	1	0	BIST_EN	FIN_WAKE	WAKE_UP_TIMER_EN_SEL	KEY_OC_RERTY_MAX_EN	CAN_LOOP_EN	CAN_TDI	LIN_TX_DOM_ERR_CFG	PDRV_O2H_DLY
CONFIG-REG21	0	0	0	0	0	0	1	CAN_TX_DOM_ERR_CFG	OL_RED	BUCK_SLOW_SR	CAN_TXD_DOM_EN	CAN_PERM_REC_EN	CAN_PERM_DOM_EN	CAN_RXD_REC_EN	CAN_AUTO_BIAS
LOCK	1	0	0	1	1	1	1	0	1	0	1	0	1	0	1
UNLOCK	1	0	0	1	1	1	1	1	0	1	0	1	0	1	0
WDA_EN	1	0	0	1	1	1	1	0	1	1	0	0	1	1	0
WDA_DIS	1	0	0	1	1	1	1	1	0	0	1	1	0	0	1
SW-RESET	1	0	1	1	1	0	1	0	1	1	0	1	1	0	1

Table 91. MSC Interface DOWN STREAM FRAME Bit Map (continued)

	ADDRESS							DATA							
	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
EN-DRIVERS	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1
DISABLE-DRIVERS	0	1	1	0	0	0	1	0	1	1	0	0	1	1	0
MRD_ON	0	1	1	0	0	0	1	1	1	0	0	0	1	1	1
MRD_OFF	0	1	1	0	0	0	1	0	0	1	1	1	0	0	0
MRD_UC	0	1	1	0	0	0	1	1	1	0	1	1	0	1	1
STR2_ON	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0
STR2_OFF	0	1	0	0	1	0	0	1	1	0	1	0	1	0	1
STR3_ON	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0
STR3_OFF	0	1	0	0	1	0	0	1	1	1	1	0	0	1	1
RLY4_ON	0	1	0	0	1	0	0	0	0	1	1	0	0	1	1
RLY4_OFF	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0

Legenda:

Locked bit	Bit generated as pulse	Address	Default value	Bit in satellite logic, not affected by reset matrix clear conditions

Locked bit: Bit generated as pulse Bit in satellite logic, not affected by reset matrix clear conditions.

18.5.1 CONFIG-REG 1

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 1	0	0	1	1	1	1	1	PHOLD_EN	PHOLD_TIME[0:1]		LED1_PD_EN	LED2_PD_EN	BOOST_EN	WAKE_UP_TIMER_START_STOP[0:1]	
RW	DEFAULT							0	0	0	0	0	1	1	0
	RESET SOURCE							D0:D5 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN D6:D7 the read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[6:7] WAKE_UP_TIMER_START_STOP [0:1]

Start/stop Wake_up_timer counter

10: (stop) wake up timer stops (default)

01: (start) → 10 (stop) wake up timer counter value hold

10: (stop) → 01 (start) wake up timer starts from h'000001

01: (start) wake up timer counter is running

Application note: after a start/stop command 500us must be waited to have the command be effective in the EOT clock domain.

[5] BOOST_EN

Boost enable.

1: enabled (default)

0: disabled

[4] LED2_PD_EN

Enable the pull down current (open load diagnosis not available) for LED2 driver

0: pull down current disabled (LED mode enabled) (default)

1: enable

[3] LED1_PD_EN

Enable the pull down current (open load diagnosis not available) for LED1 driver

0: pull down current disabled (LED mode enabled) (default)

1: enable

[2:1] PHOLD_TIME[1:0]

Set the power hold timeout.

00: timeout disabled (default)

01: 500 ms

10: 5 minutes

11: 20 minutes

[0] PHOLD_EN

Enable the power hold function.

0: disabled (default)

1: enabled

18.5.2 CONFIG-REG 2

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 2	0	1	1	1	1	0	1	MSC_ACT_EN	F_DO_SEL[0:1]		VRS_MODE_SEL	IGN_CURRENT_CFG	IGN_DIAG	IPUPD_EN	IPUPD_MODE
RW	DEFAULT							1	1	0	0	0	0	0	1
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7] IPUPD_MODE

Enable the fast charge current I_LS_PU1 required by driver fast off diagnosis.

0: fast charge current disabled

1: fast charge current enabled (default)

[6] IPUPD_EN

Enable the driver off diagnosis and the currents I_LS_PU2, I_LS_PD1 required by it.

0: off diagnosis disabled (default)

1: off diagnosis enabled

[5] IGN_DIAG.

0: IGN diagnosis off (default)

1: IGN diagnosis on

[4] IGN_CURRENT_CFG.

0: I1_HS_IGN current selected 15-30 mA (default)

1: I2_HS_IGN current selected 5-15 mA

[3] VRS_MODE_SEL: VRS mode

0: limited adaptive (default)

1: full adaptive

[2:1] F_DO_SEL [1:0] Upstream clock ratio selection.

00: fDO= fCL/ 16

01: fDO= fCL/ 32(default)

10: fDO= fCL/ 64

11: fDO= fCL/ 128

[0] MSC_ACT_EN: MSC activity monitoring enable

0: MSC activity monitoring function is disabled

1: MSC activity monitoring function is enabled (default)

18.5.3 CONFIG-REG 3

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 3	1	1	1	1	0	0	1	RLY4_DLY_OFF_EN	LSD/HSD_DRV1-CFG	LSD/HSD_DRV2-CFG	LSD/HSD_DRV3-CFG	SRT2_EN	STR3_EN	T_SEO_DELAY[0:1]	
RW	DEFAULT							1	1	1	1	1	1	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							locked bits							

[7:6] SEO_DELAY_DELAY[1:0]

Delay from KEY_OFF for SEO function activation.

00: 100 ms (default)

01: 200 ms

10: 400 ms

11: 800 ms

[5] STR3_EN

0: disable

1: starter functions (DELAY OFF) enable for driver STR[3] (default)

[4] STR2_EN

0: disable

1: starter functions (DELAY OFF) enable for driver STR[2] (default)

[3] LSD/HSD_DRV3-CFG

1: LOW-SIDE configuration for STR3 driver (default)

0: HIGH-SIDE configuration for STR3 driver

[2] LSD/HSD_DRV2-CFG

1: LOW-SIDE configuration for STR2 driver (default)

0: HIGH-SIDE configuration for STR2 driver

[1] LSD/HSD_DRV1-CFG

1: LOW-SIDE configuration for STR1 driver (default)

0: HIGH-SIDE configuration for STR1 driver

[0] RLY4_DLY_OFF_EN

Enable delay off for RLY4 driver.

0: disabled

1: enabled (default)

18.5.4 CONFIG-REG 4

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 4	1	1	0	0	0	0	1	PRD1_IDRV[0:1]		PRD2_IDRV[0:1]		PRD3_IDRV[0:1]		PRD4_IDRV[0:1]	
RW	DEFAULT							0	0	0	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7:6] PRD4_IDRV[1:0]

MOSFET pre-driver current driving strength

00: IDRV_00 20mA (default)

01: IDRV_01 10mA

10: IDRV_10 4mA

11: IDRV_11 2mA

[5:4] PRD3_IDRV[1:0]

MOSFET pre-driver current driving strength

00: IDRV_00 20mA (default)

01: IDRV_01 10mA

10: IDRV_10 4mA

11: IDRV_11 2mA

[3:2] PRD2_IDRV[1:0]

MOSFET pre-driver current driving strength

00: IDRV_00 20mA (default)

01: IDRV_01 10mA

10: IDRV_10 4mA

11: IDRV_11 2mA

[1:0] PRD1_IDRV[1:0]

MOSFET pre-driver current driving strength

00: IDRV_00 20mA (default)

01: IDRV_01 10mA

10: IDRV_10 4mA

11: IDRV_11 2mA

18.5.5 CONFIG-REG 5

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 5	0	0	0	0	1	1	1	PRD5_IDRV[0:1]		PRD1_VDS[0:2]			PRD2_VDS[0:2]		
RW	DEFAULT							0	0	0	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7:5] PRD2_VDS[2:0]

MOSFET pre-driver VDS threshold

000: VTH_DS_000 150mV (default)

001: VTH_DS_001 245mV

010: VTH_DS_010 325mV

011: VTH_DS_011 405mV

100: VTH_DS_100 525mV

101: VTH_DS_101 660mV

110: VTH_DS_110 950mV

[4:2] PRD1_VDS[2:0]

MOSFET pre-driver VDS threshold

000: VTH_DS_000 150mV (default)

001: VTH_DS_001 245mV

010: VTH_DS_010 325mV

011: VTH_DS_011 405mV

100: VTH_DS_100 525mV

101: VTH_DS_101 660mV

110: VTH_DS_110 950mV

[1:0] PRD5_IDRV[1:0]

MOSFET pre-driver current driving strength

00: IDRV_00 20mA (default)

01: IDRV_01 10mA

10: IDRV_10 4mA

11: IDRV_11 2mA

18.5.6 CONFIG-REG 6

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 6	1	1	0	0	1	1	1	PRD3_VDS[0:2]			PRD4_VDS[0:2]			EOT_MODE	IGN_LSD_DIS
RW	DEFAULT							0	0	0	0	0	0	1	1
	RESET SOURCE							D0:D5, D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN D6 the read bit is from satellite logic on VB_STBY and is not affected by reset matrix							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							D0:D7 not locked bits							

[7] IGN_LSD_DIS

Disable for LSD stage in igniter driver to be used with IGBT load

0: LSD enable

1: LSD disabled (default)

[6] EOT_MODE

Bit going to Wake Up Timer Logic

Selection for EOT function

0: counter without wake up function EOT function 1

1: counter with wake up function EOT function 2 (default)

Application note: EOT_MODE bit can be written only when *WAKE_UP_TIMER_EN_SEL*=0 (CONFIG_REG20 D2, MSC Start/Stop) and *WAKE_UP_TIMER_START_STOP[0:1]*=10 (CONFIG_REG1 D7-D6, Stop condition) when *WAKE_UP_TIMER_START_STOP[0:1]* is effective in EOT clock domain

[5:3] PRD4_VDS[2:0]

MOSFET pre-driver VDS threshold

000: VTH_DS_000 150mV (default)

001: VTH_DS_001 245mV

010: VTH_DS_010 325mV

011: VTH_DS_011 405mV

100: VTH_DS_100 525mV

101: VTH_DS_101 660mV

110: VTH_DS_110 950mV

[2:0] PRD3_VDS[2:0]

MOSFET pre-driver VDS threshold

000: VTH_DS_000 150mV (default)

001: VTH_DS_001 245mV

010: VTH_DS_010 325mV

011: VTH_DS_011 405mV

100: VTH_DS_100 525mV

101: VTH_DS_101 660mV

110: VTH_DS_110 950mV

18.5.7 CONFIG-REG 7

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 7	0	0	1	1	0	0	1	PRD5_VDS[0:2]			TRK_EN[1]	TRK_EN[2]	TRK_EN[3]	DAC[0:1]	
RW	DEFAULT							0	0	0	1	1	1	1	1
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7:6] DAC

A/D test output voltage selection

00: 0.25*Vref

01: 0.50*Vref

10: 0.75*Vref

11: 1.0*Vref (default)

[5] TRK_EN[3]

Enable for tracking regulator 3

0: disabled

1: enabled (default)

[4] TRK_EN[2]

Enable for tracking regulator 2

0: disabled

1: enabled (default)

[3] TRK_EN[1]

Enable for tracking regulator 1

0: disabled

1: enabled (default)

[2:0] PRD5_VDS[2:0]

MOSFET pre-driver VDS threshold

000: VTH_DS_000 150mV (default)

001: VTH_DS_001 245mV

010: VTH_DS_010 325mV

011: VTH_DS_011 405mV

100: VTH_DS_100 525mV

101: VTH_DS_101 660mV

110: VTH_DS_110 950mV

18.5.8 CONFIG-REG 8

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 8	1	0	1	1	0	1	1	VRS_DIAG	VRS_MODE[0:1]		VRS_HYS2[0:2]			EN_FALLING_FILT	HYS_FB_SEL
RW	DEFAULT							0	0	1	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7] HYS_FB_SEL:

0: VRS hyst. Feedback connected before adaptive filter (default)

1: VRS hyst. Feedback connected after adaptive filter

[6] EN_FALLING_FILT:

0: Falling edge filter disabled (default)

1: Falling edge filter enabled

[5:3] VRS_HYST[2:0]

000: Hys current = 17 µA (Hys VRS = 347 mV with 10 kΩ ext resistors) (default)

001: Hys current = 5 µA (Hys VRS=100mV with 10 kΩ ext resistors)

010: Hys current = 10 µA (Hys VRS=200mV with 10 kΩ ext resistors)

011: Hys current = 17 µA (Hys VRS=347mV with 10 kΩ ext resistors)

100: Hys current = 32 µA (Hys VRS=644mV with 10 kΩ ext resistors)

101: Hys current = 51 µA (Hys VRS=967mV with 10 kΩ ext resistors)

110: Hys current = 17 µA (Hys VRS=347mV with 10 kΩ ext resistors)

111: Hys current = 0 µA (used only for test purpose)

[2:1] VRS_MODE[1:0]

Internal auto-adaptive hysteresis OFF allows to configure hysteresis by MSC. Internal auto-adaptive hysteresis ON selects higher hysteresis between the one configured by MSC and the one internally computed by peak voltage.

Internal auto-adaptive filter time ON works properly only in full adaptive mode, in limited adaptive mode filter time ON is fixed to 4 us. Internal auto-adaptive filter time OFF allows to bypass the filter in both modalities.

00: Internal auto-adaptive hysteresis OFF, internal auto-adaptive filter time OFF

01: Internal auto-adaptive hysteresis ON, internal auto-adaptive filter time OFF

10: Internal auto-adaptive hysteresis OFF, internal auto-adaptive filter time ON (default)

11: Internal auto-adaptive hysteresis ON, internal auto-adaptive filter time ON

[0] VRS_DIAG: VRS diagnosis enable, only for full adaptive mode

0: diagnosis function is disabled (default)

1: diagnosis function is enabled

18.5.9 CONFIG-REG 9

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 9_0	0	1	0	0	1	0	1	0	1	WDA_RESPTIME[0:5]					
RW	DEFAULT									1	1	1	1	1	1
	RESET SOURCE							D2:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_ov, vdd5_uv, vddio_uv, err_cnt>7, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D2:D7 bits active as level							
	CONTROL ACCESS							D2:D7 not locked bits							

[7:2] WDA_RESPTIME[5:0]

Response-time = WDA_RESPTIME[5:0]) *1.6 ms

The error counter is incremented by one on a controller write access to this register

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 9_1	0	1	0	0	1	0	1	1	0	WDA_WIN_SEL	WDA_INIT				
RW	DEFAULT									1	0				
	RESET SOURCE							D2:D3 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_ov, vdd5_uv, vddio_uv, err_cnt>7, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D2:D3 bits active as level							
	CONTROL ACCESS							D2:D3 locked bits							

[3] WDA_INIT

Monitoring module reset

0: disabled (default)

1: enabled

[2] WDA_WIN_SEL

Select the time base for window watchdog generation

0: 39 kHz

1: 64 kHz (default)

18.5.10 CONFIG-REG 10

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 10	0	0	0	1	1	0	1	WDA_RESP[0:7]							
RW	DEFAULT							0	0	0	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_ov, vdd5_uv, vddio_uv, err_cnt>7, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							D0:D7 not locked bits							

WDA_RESP[0:7]

Q&A WD response according to *Table 21.*

18.5.11 CONFIG-REG 11

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 11	0	1	1	0	1	1	1	LIN/KLINE SEL	LIN_ERR_EN[0]	LIN_ERR_EN[1]	LIN_ERR_EN[2]	LIN_TX_EN	LIN_TX_DIS_FOR_WDA_ERR	VDD5_OFF_SEL	O2H2_OC_FLT
RW	DEFAULT							0	0	0	0	0	1	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							D0:D7 not locked bits							

[7] O2H2_OC_FLT

Select the OVC filter time for O2H2.

0: select I_LS_ocv_flt (default)

1: select I_LS_ocv_flt x 2

[6] VDD5_OFF_SEL

VDD5 disabled by VB_IN UV:

0 VDD5 depends on VB_IN (default)

1: VDD5 does not depend on VB_IN

[5] LIN_TX_DIS_FOR_WDA_ERR

Disable the LIN transmitting when Watchdog ERR_CNT>4

0: LIN transmitting stays enabled when Watchdog ERR_CNT>4

1: LIN transmitting disabled when Watchdog ERR_CNT>4 (default)

[4] LIN_TX_EN

Enable the LIN transmission function

0: disabled (default)

1: enabled

[3] LIN_ERR_EN[2]

LIN error handling permanent dominant

0; LIN error handling disabled (default)

1; LIN error handling enabled

[2] LIN_ERR_EN[1]

LIN error handling permanent recessive

0; LIN error handling disabled (default)

1; LIN error handling enabled

[1] LIN_ERR_EN[0]

LIN error handling permanent TX timeout

0; LIN error handling disabled (default)

1; LIN error handling enabled

[0] LIN/KLIN SEL

Select between LIN/K-LINE sel

0: LIN Mode (default)

1: K-LINE Mode

18.5.12 CONFIG-REG 12

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 12	1	0	0	1	0	0	1	TNL_RST_EN	VB_IN_OV_RST_EN	VDD5_OV_RST_EN	O2H1_OC_FLT	FILTER_MODE	WAKE_UP_CAN_RST	WAKE_UP_EOT_RST	WK_IN_RST
RW	DEFAULT							1	1	1	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							not locked bits							

[7] WK_IN_RST

Activation of WK_IN_RST, active on level

1: clearing of WK_IN_DET

0: no functionality (default)

[6] WAKE_UP_EOT_RST

Activation of WAKE_UP_EOT_RST, active on level

1: clearing of WAKE_UP_EOT_DET

0: no functionality (default)

[5] WAKE_UP_CAN_RST

Activation of WAKE_UP_CAN_RST, active on level

1: clearing of WAKE_UP_CAN_DET

0: no functionality (default)

[4] FILTER_MODE

Select the filter time (Tflt_diagoff) of all the drivers.

0: selected Tflt_diagoff1 (100us) (default)

1: selected Tflt_diagoff2 (600us)

[3] O2H1_OC_FLT

Select the OVC filter time for O2H1.

0: select I_LS_ocv_flt (default)

1: select I_LS_ocv_flt x 2

[2] VDD5_OV_RST_EN

Enable the contribution of VDD5_OV in the reset matrix

0: disabled

1: enabled (default)

[1] VB_IN_OV_RST_EN

Enable the contribution of VB_IN_OV on BUCK /VDD5/ VTRK regulator in the reset matrix

0: disabled

1: enabled (default)

[0] TNL_RST_EN

enable the RSTN activation for TNL time on the positive edge of KEY_IN

1: enable (default)

0: disable

18.5.13 CONFIG-REG 13

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 13	1	1	0	1	1	0	1		WDA_PWR_CNT_OFF_DIS	IPUPD_EN_STR1	IPUPD_EN_STR2	IPUPD_EN_STR3	IDIAG_HIGH_INJ	IDIAG_HIGH_SOL	IDIAG_HIGH_PDRV
RW	DEFAULT							0	0	0	0	0	1	1	1
	RESET SOURCE							D1:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D1:D7 bits active as level							
	CONTROL ACCESS							D1 locked bit D2:D7 not locked bits							

[7] IDIAG_HIGH_PDRV

Increase the currents required for pre-drivers off diagnosis.

0: I_LS_PU2 (40 µA (min) I_LS_PD1(60 µsA (min))

1: I_LS_PU3 (100 µA (min) I_LS_PD2(350 µsA (min)) (default)

[6] IDIAG_HIGH_SOL

Increase the currents required for Solenoids off diagnosis.

0: I_LS_PU2 (40 µA (min) I_LS_PD1(60 µsA (min))

1: I_LS_PU3 (100 µA (min) I_LS_PD2(350 µsA (min)) (default)

[5] IDIAG_HIGH_INJ

Increase the currents required for Solenoids off diagnosis.

0: I_LS_PU2 (40 µA (min) I_LS_PD1(60 µsA (min))

1: I_LS_PU3 (100 µA (min) I_LS_PD2(350 µsA (min)) (default)

[4] IPUPD_EN_STR3

Enable the driver off diagnosis and the currents required by it.

0: off diagnosis disabled (default)

1: off diagnosis enabled

[3] IPUPD_EN_STR2

Enable the driver off diagnosis and the currents required by it.

0: off diagnosis disabled (default)

1: off diagnosis enabled

[2] IPUPD_EN_STR1

Enable the driver off diagnosis and the currents required by it.

0: off diagnosis disabled (default)

1: off diagnosis enabled

[1] WDA_PWR_CNT_OFF_DIS

Disable the power down due to watchdog pwr_cnt overflow.

0: enabled (default)

1: disabled

[0] Not used

18.5.14 CONFIG-REG 14

	C0	C1	C2	C3	C4	C5	C6	D0		D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 14	1	1	1	0	0	1	1	RLY1_UC		RLY2_UC	RLY3_UC	RLY4_UC	RLY5_UC	STR1_UC	STR2_UC	STR3_UC
RW	DEFAULT							0		0	0	0	0	0	0	0
	RESET SOURCE							D0:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN								
	ACTIVATION							D0:D7 bits active as pulse								
	CONTROL ACCESS							D0:D7 not locked bits								

[7] STR3_UC

0→1: micro command for fast diagnostic activation for relay driver STR3

0: no functionality (default)

1: no functionality

[6] STR2_UC

0→1: micro command for fast diagnostic activation for relay driver STR2

0: no functionality (default)

1: no functionality

[5] STR1_UC

0→1: micro command for fast diagnostic activation for relay driver STR1

0: no functionality (default)

1: no functionality

[4] RLY5_UC

0→1: micro command for fast diagnostic activation for relay driver RLY5

0: no functionality (default)

1: no functionality

[3] RLY4_UC

0→1: micro command for fast diagnostic activation for relay driver RLY4

0: no functionality (default)

1: no functionality

[2] RLY3_UC

0→1: micro command for fast diagnostic activation for relay driver RLY3

0: no functionality (default)

1: no functionality

[1] RLY2_UC

0→1: micro command for fast diagnostic activation for relay driver RLY2

0: no functionality (default)

1: no functionality

[0] RLY1_UC

0→1: micro command for fast diagnostic activation for relay driver RLY1

0: no functionality (default)

1: no functionality

18.5.15 CONFIG-REG 15

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG15-0 (WUPT_0)	1	0	0	0	0	1	1	0	0	Wake up timer_SET_0[0:5]					
RW	DEFAULT									0	0	0	0	0	0
CONFIG-REG15-1 (WUPT_1)	1	0	0	0	0	1	0	0	1	Wake up timer_SET_1[6:11]					
RW	DEFAULT									0	0	0	0	0	0
CONFIG-REG15-2 (WUPT_2)	1	0	0	0	0	1	0	1	0	Wake up timer_SET_2[12:17]					
RW	DEFAULT									0	0	0	0	0	0
CONFIG-REG15-3 (WUPT_3)	1	0	0	0	0	1	1	1	1	Wake up timer_SET_3[23:18]					
RW	DEFAULT									0	0	0	0	0	0
	RESET SOURCE							D2:D7 The read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D2:D7 bits active as level							
	CONTROL ACCESS							D2:D7 not locked bits							

Application note: the minimum time distance between two consecutive accesses to the Wake up timer SET registers is 2.5 µs.

Wake up timer_SET_x Bits go to, and are stored, in Wake Up Timer Logic.

Wake up timer_SET_x regs can be written only when *WAKE_UP_TIMER_EN_SEL*=0 (CONFIG_REG20 D2, MSC Start/Stop) and *WAKE_UP_TIMER_START_STOP*[0:1]=10 (CONFIG_REG1 D6-D7, Stop condition).

18.5.16 CONFIG-REG 16

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 16-0	0	0	1	0	0	1	1	0	1	PRD1_BLK[0:1]		PRD2_BLK[0:1]		PRD3_BLK[0:1]	
RW	DEFAULT									1	0	1	0	1	0
CONFIG-REG 16-1	0	0	1	0	0	1	1	1	0	PRD4_BLK[0:1]		PRD5_BLK[0:1]		O2H_PDRV_1	O2H_PDRV_3
RW	DEFAULT									1	0	1	0	0	0
	RESET SOURCE							D2:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D2:D7 bits active as level							
	CONTROL ACCESS							D2:D7 not locked bits							

[7] O2H_PDRV_3

VDS comparator selection for ON diagnosis

0: PDRV3 takes VDS3 comparator and PDRV4 works as independent driver

1: PDRV3 takes VDS4 comparator and PDRV4 driver cannot be used

[6] O2H_PDRV_1

VDS comparator selection for ON diagnosis

0: PDRV1 takes VDS1 comparator and PDRV2 works as independent driver

1: PDRV1 takes VDS2 comparator and PDRV2 driver cannot be used

PRDx_BLK[1:0]

Blanking time on VDS detection in ON state for Predriver

00: 6 µs

01: 12 µs (default)

10: 18 µs

11: 24 µs

18.5.17 CONFIG-REG 17

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 17_0	0	0	1	0	0	1	0	0	0		O2H1_SR	O2H1_OC_TH		O2H2_SR	O2H2_OC_TH
RW	DEFAULT									0	0	1	0	0	1
	RESET SOURCE							D2:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN							
	ACTIVATION							D2:D7 bits active as level							
	CONTROL ACCESS							D2:D7 not locked bits							

[7] O2H2_OC_TH

Select OVC threshold

0: threasold1 I_ovc1_o2h 4.5A typ

1: threasold2 I_ovc2_o2h 10A typ (default)

[6] O2H2_SR

Select SR threshold

0: typ 0,5 V/us (default)

1: typ 4 V/us

[4] O2H1_OC_TH

Select OVC threshold

0: threasold1 I_ovc1_o2h 4.5A typ

1: threasold2 I_ovc2_o2h 10A typ (default)

[3] O2H1_SR

Select SR threshold

0: typ 0,5 V/µs (default)

1: typ 4 V/µs

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 17_1	0	0	1	0	0	1	0	1	1	CAN_EN	CAN_TX_EN	CAN_WAKEUP_EN	CAN_PATTERN_EN	CAN_RX_EN	CAN_2_5_MB
RW	DEFAULT									1	1	1	1	1	0

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
	RESET SOURCE							D2:D7 The read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D2:D7 bits active as level							
	CONTROL ACCESS							D2:D6 not locked bits D7 locked bit							

[7] CAN_2_5_MB

CAN mode selection:

0: CAN with 2Mbaud (default)

1: CAN FD with 5Mbaud with reduced EMC performance.

[6]CAN_RX_EN:

CAN Receiver enable:

0: disable

1: enable (default)

[5] CAN_PATTERN_EN

Normal pattern wake up enable:

0: disable

1: enable (default)

[4] CAN_WAKEUP_EN

Enable wake up by CAN:

0: disable

1: enable (default)

[3] CAN_TX_EN

CAN Transmitter enable:

0: disable

1: enable (default)

[2] CAN_EN

CAN enable

0: disable

1: enable (default)

All Bits go to and are stored in CAN Logic

18.5.18 CONFIG-REG STBY_NVM

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
STBY_NVM_ADD_REG	0	1	0	0	1	1	0	0	1	STBY_NVM_ADD[0:3]				MEM_VALID	
RW	DEFAULT									0	0	0	0	0	
	RESET SOURCE							D2:D6 The read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D2:D6 bits active as level							
	CONTROL ACCESS							D2:D6 not locked bits							

[6] MEM_VALID

STBY NVM memory valid bit:

0: not valid (default)

1: valid

[5:2] STBY_NVM_ADD

STBY NVM write address

0000: address of the byte to write (default)

All Bits go to and are stored in Wake Up Timer Logic

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
STBY_NVM_DATA	1	0	1	1	0	0	0	STBY_NVM_DATA[0:7]							
RW	DEFAULT							0	0	0	0	0	0	0	0
	RESET SOURCE							D0:D7 The read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D0:D7 bits active as level							
	CONTROL ACCESS							D0:D7 not locked bits							

[7:0] STBY_NVM_ADD

Byte to write in STBY NVM

All Bits go to and are stored in Wake Up Timer Logic

18.5.19 CONFIG-REG 20

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 20	1	1	1	1	1	1	0	BIST_EN	FIN_WAKE	WAKE_UP_TIMER_EN_SEL	KEY_OC_RETRY_MAX_EN	CAN_LOOP_EN	CAN_TDI	LIN_TX_DOM_ERR_CFG	PDRV_O2H_DLY
RW	DEFAULT							0	0	0	0	0	0	0	0
	RESET SOURCE							D0:D1; D4:D7 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN D2:D3 the read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	ACTIVATION							D0 bit active as pulse D1:D7 bits active as level							
	CONTROL ACCESS							D0:D3 not locked bits D4:D7 locked bits							

[7] PDRV_O2H_DLY

Selection of delay time for switching from low to high current in predriver on/off transitions in o2h configuration.

0: 150µs selected (default)

1: 300µs selected

[6] LIN_TX_DOM_ERR_CFG

LIN Tx enable after dominant error timeout:

0: re-enable as soon as Tx become recessive (default)

1: wait for error flag read

[5] CAN_TDI

CAN transmission depends on WDA:

0: WDA does not affect CAN (default)

1: disable transmission if WDA_INT active

[4] CAN_LOOP_EN

CAN looping mode enable:

0: disable (default)

1: enable

[3] KEY_OC_RETRY_MAX_EN

Enable a maximum number of retry after OVC, when wake up by key:

0: disable (default)

1: enable

Bits going to Wake Up Timer Logic

[2] WAKE_UP_TIMER_EN_SEL

Select the source of activation for the wake_up_timer

0: from MSC start/stop commands (default)

1: from KEY_IN 1->0

Bits going to Wake Up Timer Logic

[1] FIN_WAKE

0: satellite logics execute auto clear 1 second after power up (default)

1: micro confirmed power up, no auto clear after 1 second

[0] BIST_EN

Bist enable for regulators

0: disable (default)

1: enable

18.5.20 CONFIG-REG 21

	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
CONFIG-REG 21	0	0	0	0	0	0	1	CAN_TX_DOM_ERR_CFG	OL_RED	BUCK_SLOW_SR	CAN_TXD_DOM_EN	CAN_PERM_REC_EN	CAN_PERM_DOM_EN	CAN_RXD_REC_EN	CAN_AUTO_BIAS
RW	DEFAULT							0	0	0	1	1	1	1	1
	ACTIVATION							D0:D2 v3v3a_ov, v3v3a_uv, v3v3d_ov, v3v3d_uv, vdd5_uv, vddio_uv, sw_reset, after_run_reset, RSTN_IN D3:D7 the read bits are from satellite logic on VB_STBY and are not affected by reset matrix							
	CONTROL ACCESS							D0:D7 bits active as level							
	RESET SOURCE							D0 locked bit D1:D7 not locked bits							

[7] CAN_AUTO_BIAS

0: auto biasing disabled

1: auto biasing enabled (default)

[6] CAN_RXD_REC_EN

0: error handling disable

1: error handling enable (default)

[5] CAN_PERM_DOM_EN

0: error handling disable

1: error handling enable (default)

[4] CAN_PERM_REC_EN

0: error handling disable

1: error handling enable (default)

[3] CAN_TXD_DOM _EN

0: error handling disable

1: error handling enable (default)

All Bits going to CAN Logic

[2] BUCK_SLOW_SR

0: fast slew rate selected (default)

1: slow slew rate selected

[1] OL_RED

Select open load current:

0:0.8 mA max (default)

1: 0.2 mA max

[0] CAN_TX_DOM_ERR_CFG

CAN Tx enable after dominant error timeout:

0: re-enable as soon as Tx become recessive (default)

1: wait for error flag read

18.5.21 Commands

RD_COMMAND1.. RD_COMMAND16

These commands allow the reading of information that will be output on Upstream.

Table 92. Commands

Name	ADDRESS							DATA							
	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
RD_COMMAND1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
RD_COMMAND2	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
RD_COMMAND3	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
RD_COMMAND4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
RD_COMMAND5	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1
RD_COMMAND6	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
RD_COMMAND7	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1
RD_COMMAND8	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
RD_COMMAND9	1	0	1	0	1	0	1	1	1	1	0	1	1	1	0
RD_COMMAND10	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1
RD_COMMAND11	0	1	0	1	0	1	0	1	1	1	0	1	1	1	0
RD_COMMAND12	0	1	0	1	0	1	0	0	0	0	1	0	0	0	1
RD_COMMAND13	1	0	1	0	1	0	1	0	1	1	1	0	1	1	1
RD_COMMAND14	1	0	1	0	1	0	1	1	0	0	0	1	0	0	0
RD_COMMAND15	0	1	0	1	0	1	0	0	1	1	1	0	1	1	1
RD_COMMAND16	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0

Lock Command

Registers that have this function are locked as default.

Registers are unlocked by the UNLOCK command and locked again by the LOCK command. Before the LOCK command the registers stay unlocked.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
LOCK	1	0	0	1	1	1	1	0	1	0	1	0	1	0	1

Unlock Command

Enables the write right to registers under lock.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
UNLOCK	1	0	0	1	1	1	1	1	0	1	0	1	0	1	0

Question and Answer Watch Dog Enable command

WD is enabled as default.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
WDA_EN	1	0	0	1	1	1	1	0	1	1	0	0	1	1	0

Question and Answer Watch Dog Disable command

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
WDA_DIS	1	0	0	1	1	1	1	1	0	0	1	1	0	0	1

SW-Reset command

This command generates internal reset initiated by the CPU's software that clears all the configuration and diagnostic registers and switches off all the drivers.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
SW-RESET	1	0	1	1	1	0	1	0	1	1	0	1	1	0	1

EN_Drivers command

The command Enable Drivers sets the bit Drivers_EN to "1" (UPS1 Frame 10 bit D1).

With Drivers_EN =1 all drivers controlled through control register can be activated using the Data Frame.

After a reset or command Disable Drivers_EN = "0" and all drivers are disabled.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
EN-DRIVERS	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1

Disable Driver

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
DISABLE-DRIVERS	0	1	1	0	0	0	1	0	1	1	0	0	1	1	0

Main relay Driver ON

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
MRD_ON	0	1	1	0	0	0	1	1	1	0	0	0	1	1	1

Main relay Driver OFF

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
MRD_OFF	0	1	1	0	0	0	1	0	0	1	1	1	0	0	0

MRD_OFF_UC command

The Main Relay Driver is switched off for the time required to perform the off diagnosis and then switched on again. The command can be activated if firstly is unlocked.

W	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4	D5	D6	D7
MRD_UC	0	1	1	0	0	0	1	1	1	0	1	1	0	1	1

STR2 driver ON/OFF

It has effect only if delay-off function for this driver is active (Config3[4] = 1).

STR2_ON	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0
STR2_OFF	0	1	0	0	1	0	0	1	1	0	1	0	1	0	1

STR3 driver ON/OFF

It has effect only if delay-off function for this driver is active (Config3[5] = 1).

STR3_ON	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0
STR3_OFF	0	1	0	0	1	0	0	1	1	1	1	0	0	1	1

RLY4 driver ON/OFF

It has effect only if delay-off function for this driver is active (Config3[0] = 1).

RLY4_ON	0	1	0	0	1	0	0	0	0	1	1	0	0	1	1
RLY4_OFF	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0

18.6 Upstream frame

See downstream paragraph for configuration register bits description. Bits highlighted in orange are clear on read. Bits highlighted in green come from satellite logics, they need VB_STBY in order to be correctly read.

18.6.1 Upstream Bit Map Read1 (CONFIG-REG 1-4)

Table 93. MSC Interface Upstream Bit Map Read1

	ADDRESS				DATA							
	A0	**A1**	**A2**	**A3**	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
FRAME1	0	0	0	0	CONFIG-REG 1							
FRAME2	0	0	1	0	CONFIG-REG 2							
FRAME3	0	0	0	1	CONFIG-REG 3							
FRAME4	0	0	1	1	CONFIG-REG 4							
source					logic on VB_IN (main logic)							
access					read							

Frame[1]

[7:6] WAKE_UP_TIMER_START_STOP:

Read start "10" or stop "01" status, (never read "00" or "11").

These bits are valid only if WUT is driven by MSC.

18.6.2 Upstream Bit Map Read2 (CONFIG-REG 5-8)

Table 94. MSC Interface Upstream Bit Map Read2

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	**CONFIG-REG 5**							
FRAME2	0	0	1	0	**CONFIG-REG 6**							
											EOT_MODE(1)	
FRAME3	0	0	0	1	**CONFIG-REG 7**							
FRAME4	0	0	1	1	**CONFIG-REG 8**							
source	FRAME[1][3][4] FRAME[2]D[0:5] FRAME[2]D[7] logic on VB_IN (main logic) FRAME[2]D[6] logic on VB_STBY(Wake Up Timer logic)											
access	read											

1. Bit in satellite logic.

18.6.3 Upstream Bit Map Read3 (CONFIG-REG 11-13, 16-0)

Table 95. MSC Interface Upstream Bit Map Read3

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	CONFIG-REG 11							
FRAME2	0	0	1	0	CONFIG-REG 12							
FRAME3	0	0	0	1	CONFIG-REG 13							
FRAME4	0	0	1	1	STR_DELAY_OFF_STATUS		CONFIG-REG 16-0					
					STR2	STR3						
source					logic on VB_IN (main logic)							
access					read							

FRAME[4]:

[1] 1:STR3 delay-off function active

0: STR3 delay-off function inactive

[0] 1: STR2 delay-off function active

0: STR2 delay-off function inactive

18.6.4 Upstream Bit Map Read4 (CONFIG-REG 16-1 + Wake up timer_SET)

Table 96. MSC Interface Upstream Bit Map Read4

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	RLY4_DELAY_OFF_STATUS	MRD_STATUS	CONFIG-REG 16_1					
					RLY4	MRD						
					Wake up timer_SET [23:0]							
FRAME2	0	0	1	0	Wake up timer_SET_0[0:7](1)							
FRAME3	0	0	0	1	Wake up timer_SET_1[8:15](1)							
FRAME4	0	0	1	1	Wake up timer_SET_2[16:23](1)							
source					FRAME[1][0:7] logic on VB_IN (main logic) FRAME[2:4]D[0:7] logic on VB_STBY (Wake Up Timer logic)							
access					read							

1. Bit in satellite logic.

FRAME[1]:

[1] 1: Main Relay Driver On

0: Main Relay Driver Off

[0] 1: RLY4 delay-off function active

0: RLY4 delay-off function inactive

FRAME[2:4]: Wake Up Timer setting

Bits coming from WUT Logic

18.6.5 Upstream Bit Map Read5 (CONFIG-REG 17-0, WAKE_UP_TIMER VALUE)

Table 97. MSC Interface Upstream Bit Map Read5

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0		TNL	CONFIG-REG 17_0					
						TNL_RESET(1)						
					TIMER CONT VALUE[23:0]							
FRAME2	0	0	1	0	Wake up timer _CNT_0[0:7](2)							
FRAME3	0	0	0	1	Wake up timer _CNT_1[8:15](2)							
FRAME4	0	0	1	1	Wake up timer _CNT_2[16:23](2)							
source					FRAME[1]D[0:7] logic on VB_IN (main logic) FRAME[2:3]D[0:7] logic on VB_STBY (Wake Up Timer logic)							
access					FRAME[1]D[1] clear-on-read FRAME[1]D[0] FRAME[1]D[2:7] FRAME[2:4]D[0:7] read							

1. Clear on Read.
2. Bit in satellite logic.

FRAME[1]:

[1] 1: After run reset (TNL) happened

0: After run reset (TNL) not happened, clear on read

FRAME[2:4]: Wake Up Timer counting

18.6.6 Upstream Bit Map Read6 (DRIVER DIAGNOSIS)

Table 98. MSC Interface Upstream Bit Map Read6

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	DIAG INJ1				DIAG INJ2			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME2	0	0	1	0	DIAG INJ3				DIAG INJ4			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME3	0	0	0	1	DIAG O2H1							
					STA	STG	OPL	OVC				
FRAME4	0	0	1	1	DIAG O2H2							
					STA	STG	OPL	OVC				
source					logic on VB_IN (main logic)							
access					clear-on-read							

Clear on Read

FRAME[1:4]: Driver diagnosis for driver

STA: driver diagnosis: error in driver status

The driver status is detected by reading the STG comparator in on and off, it should be aligned with command (msc command and enabling).

0: aligned, no error

1: not aligned, error

STG/STB: driver diagnosis: short to ground/battery

0: no fault (default)

1: for low-side and igniter drivers: short to ground fault

for high-side driver: short to battery fault

OPL: driver diagnosis: open load

0: no fault (default)

1: open load fault

OVC: driver diagnosis: over current

0: no fault (default)

1: over current faul

18.6.7 Upstream Bit Map Read7 (DRIVER DIAGNOSIS)

Table 99. MSC Interface Upstream Bit Map Read7

	ADDRESS				READ3 DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	DIAG LED1				DIAG LED2			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME2	0	0	1	0	MRD DIAG				DIAG RLY1			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME3	0	0	0	1	DIAG RLY2				DIAG RLY3			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME4	0	0	1	1	DIAG RLY4				DIAG RLY5			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
source					logic on VB_IN (main logic)							
access					clear-on-read							

Clear on Read

18.6.8 Upstream Bit Map Read8 (DRIVER DIAGNOSIS)

Table 100. MSC Interface Upstream Bit Map Read8

	ADDRESS				READ4 DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	DIAG STR1				DIAG STR2			
					STA	STG/STB	OPL	OVC	STA	STG/STB	OPL	OVC
FRAME2	0	0	1	0	DIAG STR3				DIAG PRD1			
					STA	STG/STB	OPL	OVC	STA	STG	OPL	OVC
FRAME3	0	0	0	1	DIAG PRD2				DIAG PRD3			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME4	0	0	1	1	DIAG PRD4				DIAG PRD5			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
source					logic on VB_IN (main logic)							
access					clear-on-read							

Clear on Read

18.6.9 Upstream Bit Map Read9 (DRIVER DIAGNOSIS)

Table 101. MSC Interface Upstream Bit Map Read9

	ADDRESS				READ4 DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	DIAG IGN1				DIAG IGN2			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME2	0	0	1	0	DIAG IGN3				DIAG IGN4			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME3	0	0	0	1	DIAG IGN5				DIAG IGN6			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
FRAME4	0	0	1	1	DIAG SOL1				DIAG SOL2			
					STA	STG	OPL	OVC	STA	STG	OPL	OVC
source					logic on VB_IN (main logic)							
access					clear-on-read							

Clear on Read

18.6.10 Upstream Bit Map Fast Read10 (SAFETY WDA)

Table 102. MSC Interface Upstream Bit Map Read10

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	WDA REQULO							
					REQU[0:3]				ERR_CNT[0:2]			WDA_INT
FRAME2	0	0	1	0	WDA REQUHI							
					RESP_TOO_EARLY	NO_RESP	W_RESP	CHRT	RESP_Z0	RESP_ERR	RESP_CNT[0 :1]	
FRAME3	0	0	0	1	WDA PWR_RST_CNT							
					RST_CNT[0 :2]			PWR_CNT[0:2]				WDA_RST
FRAME4	0	0	1	1	WDA RESPTIME							
					RESPTIME[0:5]						WDA_WIN_SEL	WDA_INIT
source	logic on VB_IN (main logic)											
access	FRAME[1]D[0:7] FRAME[2]D[0] FRAME[2]D[2] FRAME[2]D[4:7] FRAME[3]D[0:7] FRAME[4]D[0:7] read FRAME[2]D[1] FRAME[2]D[3] clear-on-read											

Clear on Read

FRAME[1]: WATCHDOG REQULO

[7] WDA_INT

1: ERR_CNT[2:0]>4

Default: 1

[6:4] ERR_CNT[2:0]

Value of ERR_CNT[2:0]

Default: 0x6

[3:0] REQU[3:0]

4-bit question

FRAME[2]: WATCHDOG REQUHI

[7:6] RESP_CNT[1:0]

Counter for receiving the 4 response bytes

Default: 0xC

[5] RESP_ERR

1: 1 byte of 32-bit response is incorrect: one of the response bytes in the current sequencer run is wrong, reading WDA status register after the 4th byte write implies that this flag will always be read as 0.

reset to zero at each sequencer-run

[4] RESP_Z0

1: Controller set response time to 0ms

a correct response within the time window nevertheless increments the error counter by one
0: Response-time is greater than 0ms

[3] CHRT

1: Controller has changed response time

reset to zero after a read access and after the next sequencer run

[2] W_RESP

1: if one of the RESP_BYTEx was incorrect during the previous sequencer run;

0: otherwise

[1] NO_RESP

1: in case of no response at all timer is restarted automatically

reset to zero after a read access

[0] RESP_TOO_EARLY

1: in case the 4 response bytes arrive before time window starts during the previous sequencer run;

Reset to zero at each sequencer run

FRAME[3]: WATCHDOG PWR_RST_CNT

[7] WDA_RST

See reset matrix

[5:3] PWR_CNT[2:0]

Current value of PWR_CNT register

[2:0] RST_CNT[2:0]

Current value of RST_CNT register

FRAME[4]: WATCHDOG RESPTIME

[7:6] CONFIG-REG9_1

[5:0] RESPTIME[5:0]

CONFIG-REG9_0

18.6.11 Upstream Bit Map Read11 (SAFETY+BIST+VRS+LIN+ASIC_REV)

Table 103. MSC Interface Upstream Bit Map Read11

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	SAFETY/VRS							
					TRANS_L	TRANS_F	CMD_ERR	FREQ_ERR	CLK_MON_FAULT	OSC_STUCK	OL_RED	VRS_DIAG
FRAME2	0	0	1	0	BIST							
					V3V3	VDD5	IGN1	IGN2	IGN3	IGN4	IGN5	IGN6
FRAME3	0	0	0	1	BIST/LIN							
					BIST_END	INJ1	INJ2	INJ3	INJ4	DRIVER_EN	LIN/KLINE STATUS	LOCK
FRAME4	0	0	1	1	ASIC REVISION[0:7]							
					1	1	0	0	0	1	0	0
source	logic on VB_IN (main logic)											
access	FRAME[1]D[6] FRAME[3][5:7] FRAME[4]D0:7] read FRAME[1]D[0:5] FRAME[1]D[7] FRAME[2]D[0:7] FRAME[3]D[0:4] clear-on-read											

Clear on Read

FRAME[1]: SAFETY/VRS

[0] TRANS_L

Wrong command frame or data frame down stream length (longer than 16 bits)

0: no fault (default)

1: down stream frame length incorrect

[1] TRANS_F

No valid the data frame for longer than tMSC_mon

0: no fault (default)

1: no data stream within tMSC_mon time out

[2] CMD_ERR

This bit is address error(C0-C5) of previous command Frame

0: no fault (default)

1: command error

[3] FREQ_ERR

Main OSC and checker OSC running with more than +/- 20% freq difference

0: no fault (default)

1: clocks out of frequency or stucked

[4] CLK_MON_FAULT

Main OSC and checker OSC running with more than +/- 30% freq difference

0: no fault (default)

1: clocks out of frequency or stucked (drivers disabled)

[5] OSC_STUCK

Main OSC or checker OSC stuck

0: no fault (default)

1: clocks stucked (drivers disabled)

[6] OL_RED

CONFIG_REG21 BIT 1

[7] VRS_DIAG

VRS diagnosis result

0: no fault detected (default)

1: generic fault detected

FRAME[2]: BIST

[0] BIST_V3V3

Bist result for V3V3 regulator

0: bist pass (default)

1: bist fail

[1] BIST_VDD5

Bist result for VDD5 regulator

0: bist pass (default)

1: bist fail

[2:7] BIST_IGN

Bist result for Igniter drivers

0: bist pass (default)

1: bist fail

FRAME[3]: BIST/LIN

[0] BIST_END

End of Bist operation

0: bist not end

1: bist end

[1:4] BIST_INJ

Bist result for INJECTOR drivers

0: bist pass (default)

1: bist fail

[5] DRIVER_EN

Drivers enabled or disabled by MSC command

0: drivers disabled (default)

1: drivers enabled

[6] LIN_KLINE_STATUS

LIN / K-LINE Mode (CONFIG-REG11 [0])

0: LIN mode (default)

1: KLINE mode

[7] MSC LOCK

MSC command and bit lock

0: unlocked

1: locked (default)

FRAME [4]: ASIC REVISION FOR BC

[0:7] ASIC_REVISION

18.6.12 Upstream Bit Map Read12 (PHOLD+POWER_UP+ADC)

Table 104. MSC Interface Upstream Bit Map Read12

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	PHOLD							
					PHOLD_TIME STATUS	PHOLD TIMER [0]	PHOLD TIMER [1]	PHOLD TIMER [2]	PHOLD TIMER [3]	PHOLD TIMER [4]	PHOLD TIMER[5]	PHOLD TIMER[6]
FRAME2	0	0	1	0	PHOLD							
					PHOLD TIMER [7]	PHOLD TIMER [8]	PHOLD TIMER [9]	PHOLD TIMER [10]	PHOLD TIMER [11]	PHOLD TIMER [12]	PHOLD TIMER [13]	PHOLD TIMER [14]
FRAME3	0	0	0	1	POWER UP					EOT_STATUS	ADC	
					KEY_IN_DET	WK_IN_DET	WAKE_UP_EOT_DET	WAKE_UP_CAN_DET	FAULT_WARN	EOT(1)	ADC[0]	ADC[1]
FRAME4	0	0	1	1	ADC							
					ADC[2]	ADC[3]	ADC[4]	ADC[5]	ADC[6]	ADC[7]	ADC[8]	ADC[9]
source					FRAME[1]D[0:7] FRAME[2]D[0:7] FRAME[3]D[0:4] FRAME[3]D[6:7] FRAME[4]D[0:7] logic on VB_IN (main logic) FRAME[3]D[5] logic on VB_STBY (Wake Up Timer logic)							
access					read							

1. Bit in satellite logic.

FRAME[1:2]: POWER_HOLD TIMER

It is the counter used to reach the timeout selected by PHOLD_TIME[0:1] configuration bits.

The run time is derived from the PHOLD_TIMER[14:0] according to the formula:

run time = PHOLD_TIMER[14:0] * 279 ms

FRAME[3]: POWER_UP

[0] KEY_IN_DET

Latch status of activation of KEY_IN signal

0: low level detected on KEY_IN signal

1: high level on KEY_IN signal

[1] WK_IN_DET

Latch status of activation of WK_IN signal.

0: no positive edge detected on WK_IN signal

1: positive edge on WK_IN signal

[2] WAKE_UP_EOT_DET

Latch status of activation of Wake_Up_Timer counter

0: Wake_Up_Timer end counting not detected

1: Wake_Up_Timer end counting detected

[3] WAKE_UP_CAN_DET

Latch status of activation of CAN signal

0: no wake up activity detected on CAN

1: wake up activity detected on CAN

[4] FAULT_WARN

0: no fault warning active

1: at least one of fault warning contributors (oscillator fault, v3v3pre_mon_ov, v3v3pre_mon_uv, v3v3pre_ov, v3v3pre_uv, v3v3ana_ov, v3v3ana_uv, v3v3dig_ov, v3v3dig_uv, gnd_dig_loss) is active.

[5] EOT_STATUS:

1: EOT active (WAKE_UP_TIMER_START_STOP[0:1] = 01, start)

0: EOT inactive (WAKE_UP_TIMER_START_STOP[0:1] = 10, stop)

[6:7] ADC[0:1]

FRAME[4]

[0:7] ADC[2:9]

Temperature= (ADC[9:0] * 293 / 1024) - 63 [°C]

18.6.13 Upstream Bit Map Read13 (SUPPLY UV/OV)

Table 105. MSC Interface Upstream Bit Map Read13

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME 1	0	0	0	0	SUPPLY OVERVOLTAGE/UNDERVOLTAGE							
						V3V3A_ UV	V3V3A_ OV	V3V3D_ UV	V3V3D_ OV	VB_IN_ UV	VB_IN_ OV 1	VB_IN_ OV 2
FRAME 2	0	0	1	0	SUPPLY OVERVOLTAGE/UNDERVOLTAGE							
					VB_STBY_UV(1)	GND_ DIG_ LOSS	VDDIO_ UV	VDD5_ UV	VDD5_ OV	VPRE_ UV	VPRE_ OV	
FRAME 3	0	0	0	1	SUPPLY OVERVOLTAGE/UNDERVOLTAGE							
					WAKE_ UP_CAN _DET_ AUTO	TRIM_ VALID	TRK_ STB[1]	TRK_ STB[2]	TRK_ STB[3]	TRK_ OVC[1]	TRK_ OVC[2]	TRK_ OVC [3]
FRAME 4	0	0	1	1	SUPPLY OVERVOLTAGE/UNDERVOLTAGE							
					EXT_ TRK_UV	INT_ TRK_ UV[1]	INT_ TRK_ UV[2]	INT _TRK_ UV[3]	EXT_ TRK_OV	INT_ TRK_OV [1]	INT_ TRK_O V[2]	INT_ TRK_ OV[3]
source					FRAME[1]D[0:7] FRAME[2]D[1:7] FRAME[3]D[0:7] FRAME[4]D[0:7] logic on VB_IN (main logic) FRAME[2]D[0] logic on VB_STBY (Wake Up Timer logic)							
access					FRAME[3]D[1] read FRAME[1]D[0:7] FRAME[2]D[0:7] FRAME[3]D[0] FRAME[3]D[2:7] FRAME[4]D[0:7] clear-on-read							

1. Bit in satellite logic.

Clear on Read

FRAME[1:4]: SUPPLY OVERVOLTAGE/UNDERVOLTAGE

0: no fault (default)

1: overvoltage/undervoltage detected on the corresponding pin

VB_STBY_UV is functional only if VB_STBY is present, if VB_STBY is totally disconnected no diagnosis related to VB_STBY will be available (bit latched in wut logic).

GND_DIG_LOSS comparator for digital ground level

0: the digital ground supply is connected to ground.

1: the digital ground supply is disconnected from ground.

TRIM_VALID

0: trimming content not written or not valid (parity check fail) (default)

(in this case the trimming content is anyway used)

1: trimming content written and valid

WAKE_UP_CAN_DET_AUTO

0: No Wakeup pattern detected in sleep mode with UCHIP-ON and CAN_AUTO_BIAS = 1(CONFIG-REG 21 D7) (default)

1: Wakeup pattern detected

18.6.14 Upstream Bit Map Read14 (THERMAL WARNING AND CAN)

Table 106. MSC Interface Upstream Bit Map Read14

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	OVERTEMPERATURE							
					OVT[1]	OVT[2]	OVT[3]	OVT[4]	OVT[5]	OVT[6]	OVT[7]	OVT[8]
FRAME2	0	0	1	0	OVERTEMPERATURE							
					OVT[9]	OVT[10]	OVT[11]	OVT[12]	OVT[13]	OVT[14]	OVT[15]	OVT[16]
FRAME3	0	0	0	1	OVERTEMPERATURE				CONFIG-REG 17_1			
					OVT[17]	OVT[18]	OVT[19]	VDD_CAN_OV (1)	CAN_EN (1)	CAN_TX_EN(1)	CAN_RX_EN (1)	CAN_WAKEUP_EN(1)
FRAME4	0	0	1	1	CONFIG-REG 17_1		CAN DIAG					
					CAN_PATTERN_EN(1)	CAN_2_5_MB (1)	CAN_TXD_DOM (1)	CAN_PERM_REC(1)	CAN_PERM_DOM(1)	CAN_RXD_REC(1)	CAN_SILENT (1)	CAN_SUP_LOW(1)
source					FRAME[1]D[0:7] FRAME[2]D[0:7] FRAME[3]D[0:2] logic on VB_IN (main logic) FRAME[3]D[4:7] FRAME[4]D[0:7] logic on VB_STBY (Can logic)							
access					FRAME[3]D[4:7] FRAME[4]D[0:1] read FRAME[1]D[0:7] FRAME[2]D[0:7] FRAME[3]D[0:3] FRAME[4]D[2:7] clear on read							

1. Bit in satellite logic.

Clear on Read

FRAME[1:3]: OVERTEMPERATURE

0: no fault (default)

1: overtemperature detected on the corresponding block

FRAME[3:4]:

[3]: VDD_CAN_OV

0: no fault

1: VDD_CAN _OV overvoltage detected

CONFIG_REG 17-1

FRAME[4]: CAN DIAG, see CAN section for detailed description.

18.6.15 Upstream Bit Map Read15 (MEM_STBY_CONFIG+CONFIG_REG20+UCs)

Table 107. MSC Interface Upstream Bit Map Read15

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	LIN_ERROR			STBY_NVM_ADD_REG				
					LIN_ PERM_ REC	LIN_ PERM_ DOM	LIN_ TXD_ DOM	STBY_NVM_ADD[0:3](1)				MEM_ VALID(1)
FRAME2	0	0	1	0	CONFIG_REG_21							
					BUCK_ SLOW_ SR	CAN_ TXD_ DOM _EN(1)	CAN_ PERM_ REC_ EN(1)	CAN_ PERM_ DOM_ EN(1)	CAN_ RXD_ REC_EN(1)	CAN_ AUTO_ BIAS(1)	KEY_ IN_PIN _FLT	WAKE_ IN_PIN_ FLT
FRAME3	0	0	0	1		CONFIG-REG 20						
					CAN_TX_ DOM_ ERR_ CFG(1)	FIN_W AKE	WAKE_ UP_TI MER_E N_SEL (1)	KEY_O C_RER TY_MA X_EN(1)	CAN_LO OP_EN	CAN_TDI	LIN_TX _DOM_ ERR_C FG	PDRV_ O2H_ DLY
FRAME4	0	0	1	1	CONFIG-REG 14 (UCOMMANDS STATUS)							
					RLY1_UC	RLY2_ UC	RLY3_ UC	RLY4_U C	RLY5_UC	STR1_UC	STR2_ UC	STR3_ UC
source					FRAME[1]D[0:2] FRAME[2]D[0] FRAME[2]D[6:7] FRAME[3]D[1] FRAME[3][4:7] FRAME[4]D[0:7] logic on VB_IN (main logic)							
access					FRAME[1]D[3:7] FRAME[2]D[0:7] FRAME[3]D[0:7] FRAME[4]D[0:7] read FRAME[1]D[0:2] clear-on-read							

1. Bit in satellite logic.

Clear on Read

FRAME [1]

[7] MEM_VALID (see 4.19)

1: memory has been written and validated by micro by reading back data.

0: memory was not validated or standby-power-supply is removed

[6:3] STBY_NVM_ADD

[2] 1: LIN TxD dominant timeout error occurs

0: no LIN TxD dominant timeout error occurs

Clear on read

[1] 1: LIN permanent dominant error occurs

0: no LIN permanent dominant error occurs

Clear on read

[0] 1: LIN permanent recessive error occurs

0: no LIN permanent recessive error occurs

Clear on read

FRAME[2]

[7] 1: The WK_IN pin (filtering on low to high transition) is at high state.

0: The WK_IN pin (filtering on high to low transition) is at low state.

[6] 1: The KEY_IN pin (filtering on low to high transition) is at high state.

0: The KEY_IN pin (filtering on high to low transition) is at low state.

FRAME[3]

FRAME[4]

[7:0] µcommands:

1 if driver µcommand is still active and driver is off, 0 otherwise

0 if driver µcommand is still active and driver is on, 1 otherwise

See driver section for detailed description of µcommands.

18.6.16 Upstream Bit Map Read16 (MEM_STBY_DATA)

Table 108. MSC Interface Upstream Bit Map Read16

	ADDRESS				DATA							
	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
FRAME1	0	0	0	0	MEM_STBY_DATA(Byte0)(1)							
FRAME2	0	0	1	0	MEM_STBY_DATA(Byte1)(1)							
FRAME3	0	0	0	1	MEM_STBY_DATA(Byte2)(1)							
FRAME4	0	0	1	1	MEM_STBY_DATA(Byte3)(1)							
source					logic on VB_STBY (Wake Up Timer logic)(1)							
access					read							

1. Bit in satellite logic.

FRAME[1:4]: BYTES READ FROM MEM+STBY

19 Package information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

19.1 LQFP100 (14x14x1.4 mm exp. pad down) package information

Figure 89. LQFP100 (14x14x1.4 mm exp. pad down) package outline

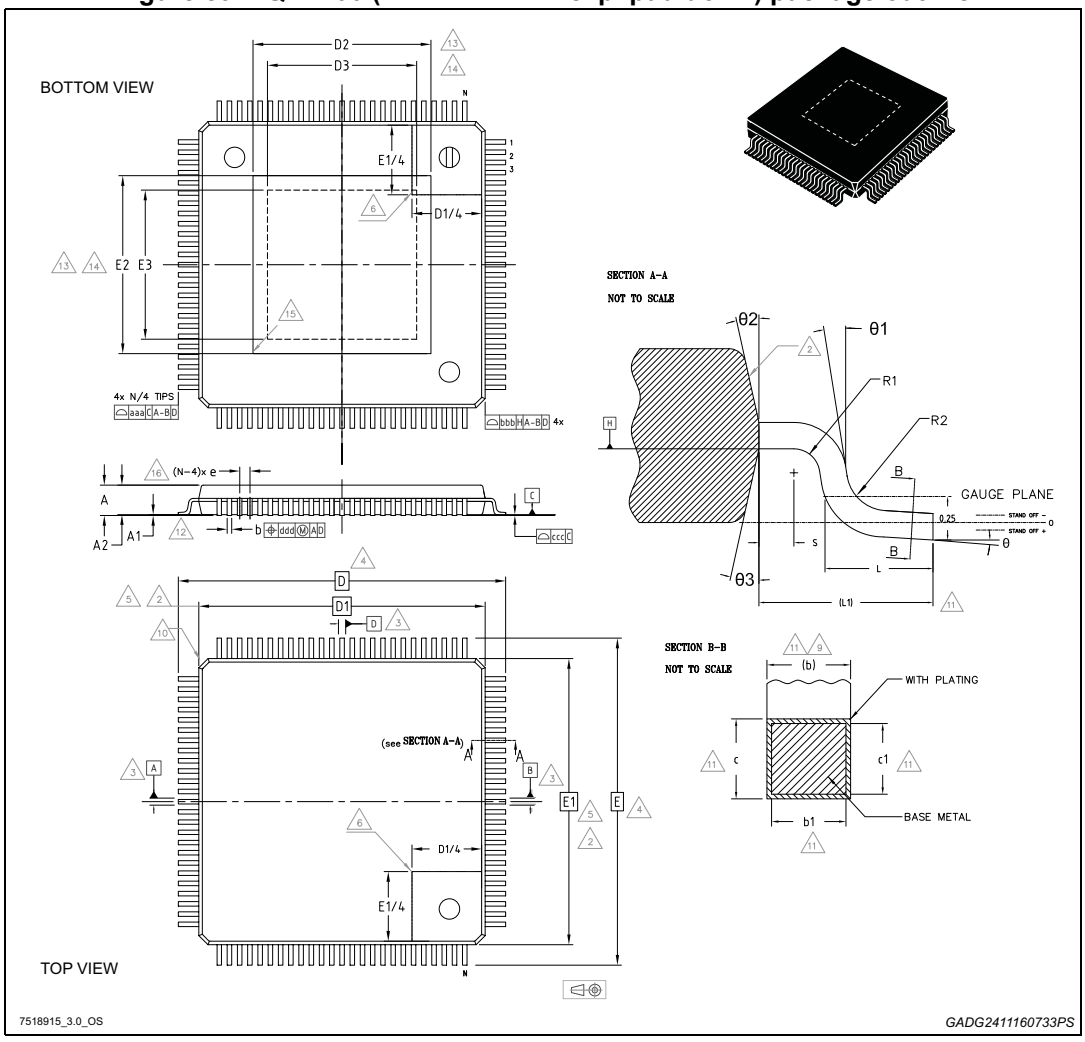


Table 109. LQFP100 (14x14x1.4 mm exp. pad down) package mechanical data

Symbol	Dimensions in mm			Notes:
	Min.	Typ.	Max.	
Θ	0°	3.5°	6°	-
Θ1	0°	-	-	-
Θ2	10°	12°	14°	-
Θ3	10°	12°	14°	-
A	-	1.40	1.60	15
A1	0.05	-	0.15	12
A2	1.35	1.40	1.45	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.20	0.23	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	16.00 BSC			4
D1	16.00 BSC			5, 2
D2	VARIATIONS			13
D3	VARIATIONS			14
e	0.50 BSC			-
E	16.00 BSC			4
E1	14.00 BSC			5, 2
E2	VARIATIONS			13
E3	VARIATIONS			14
L	0.45	0.60	0.75	-
L1	1.00 REF			-
N	100			16
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
Tolerance of form and position				
aaa	0.20			1, 7
bbb	0.20			
ccc	0.08			
ddd	0.08			

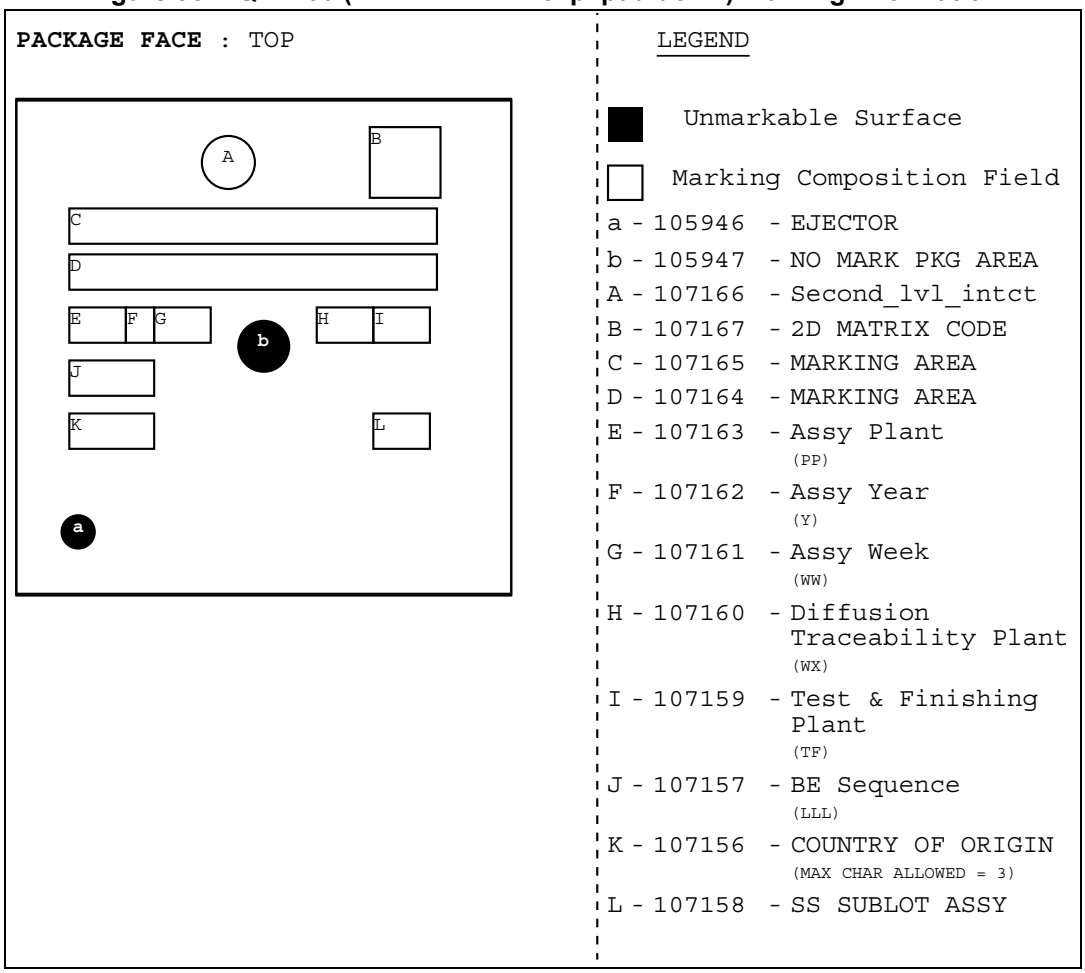
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.

5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

19.2 LQFP100 (14x14x1.4 mm exp. pad down) marking information

Figure 90. LQFP100 (14x14x1.4 mm exp. pad down) marking information



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Appendix A Device behavior

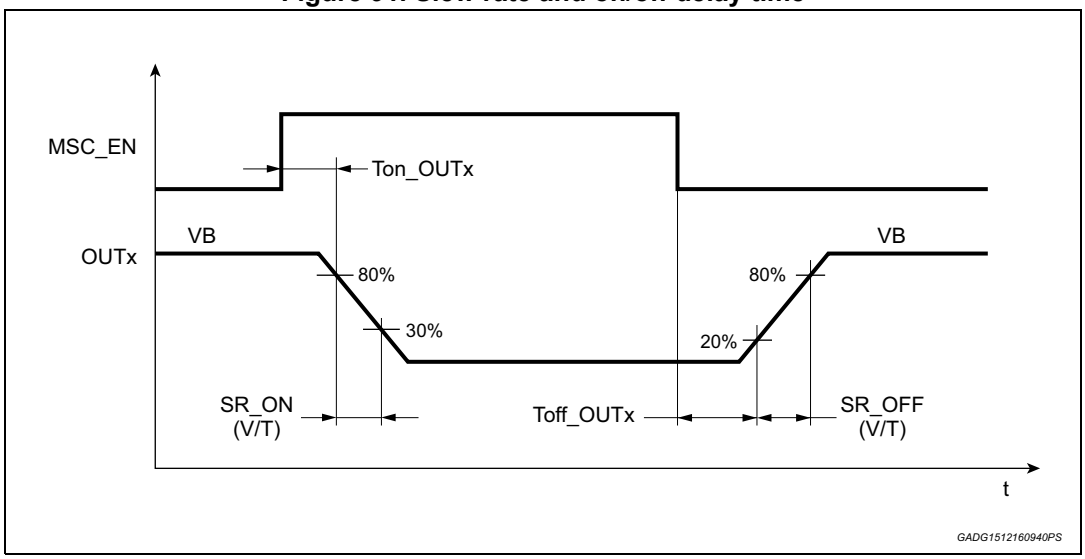
A.1 Summary of all drivers block

Table 110. Summary of all drivers block

Drivers		Min OVC value (A)	Rdson (Ω)	Vclamp Typ (V)	STB	STG	OPL	OVC
INJ		3	0.6	55	√	√	√	√
SOL		3	0.47	55	√	√	√	√
O2H		3/7.8	0.2	50	√	√	√	√
RLY		1	1.5	50	√	√	√	√
HSLS	HS	1	1.5	-3.5	√	√	√	√
	LS	1	1.5	45	√	√	√	√
LED		0.07	20	45	√	√	√	√
MRD		1	-	50	√	√	√	√
IGN		0.1	7	-	√	√	√	
PreMOS		-	-	-	√	√	√	√

A.2 Slew rate and on/off delay time

Figure 91. Slew rate and on/off delay time



Ton_OUTX is the on delay time of OUTX;

Toff_OUTX is the off delay time of OUTX;

SR_ON is the on slew rate of OUTX;

SR_OFF is the off slew rate of OUTX.

A.3 Power up/down scenarios

Figure 92. Power up and power down with deglitch concept (not permanent battery)

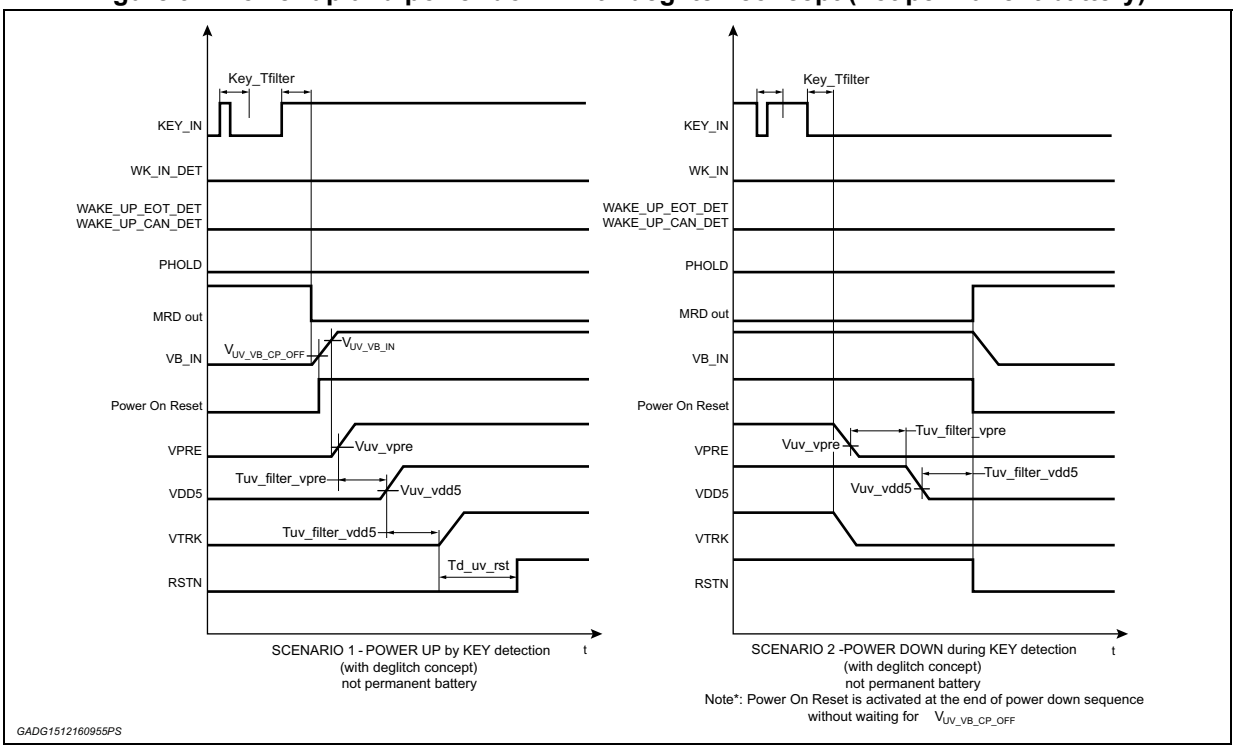


Figure 93. Power up and power down with boost (permanent battery)

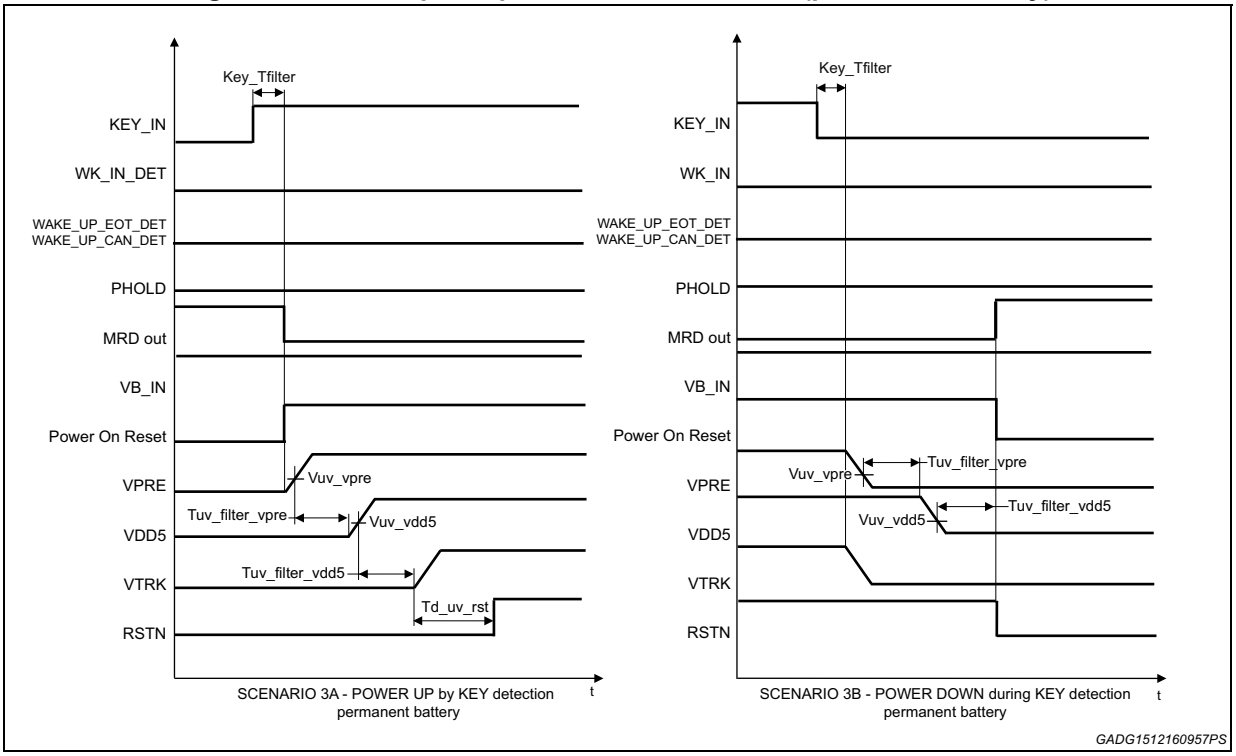


Figure 94. Power up permanent battery without boost and cranking

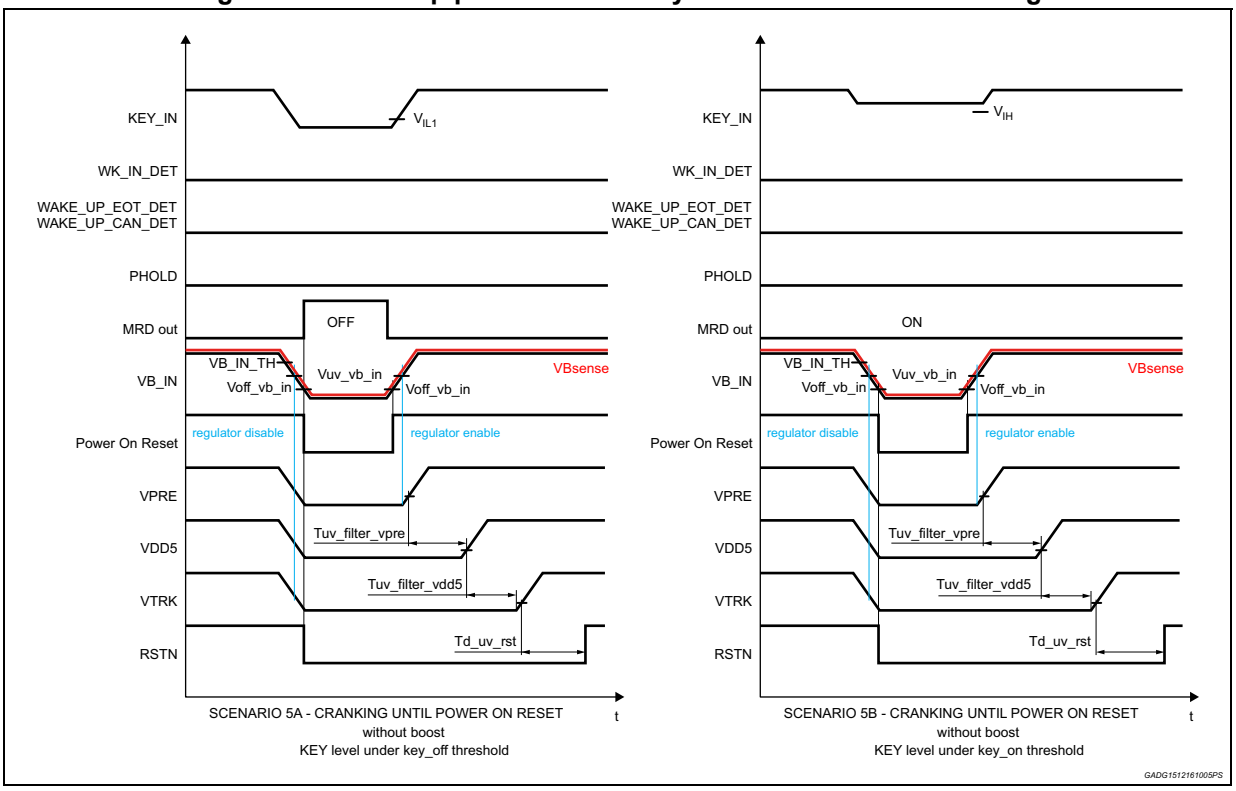


Figure 95. Power up permanent battery with boost and cranking

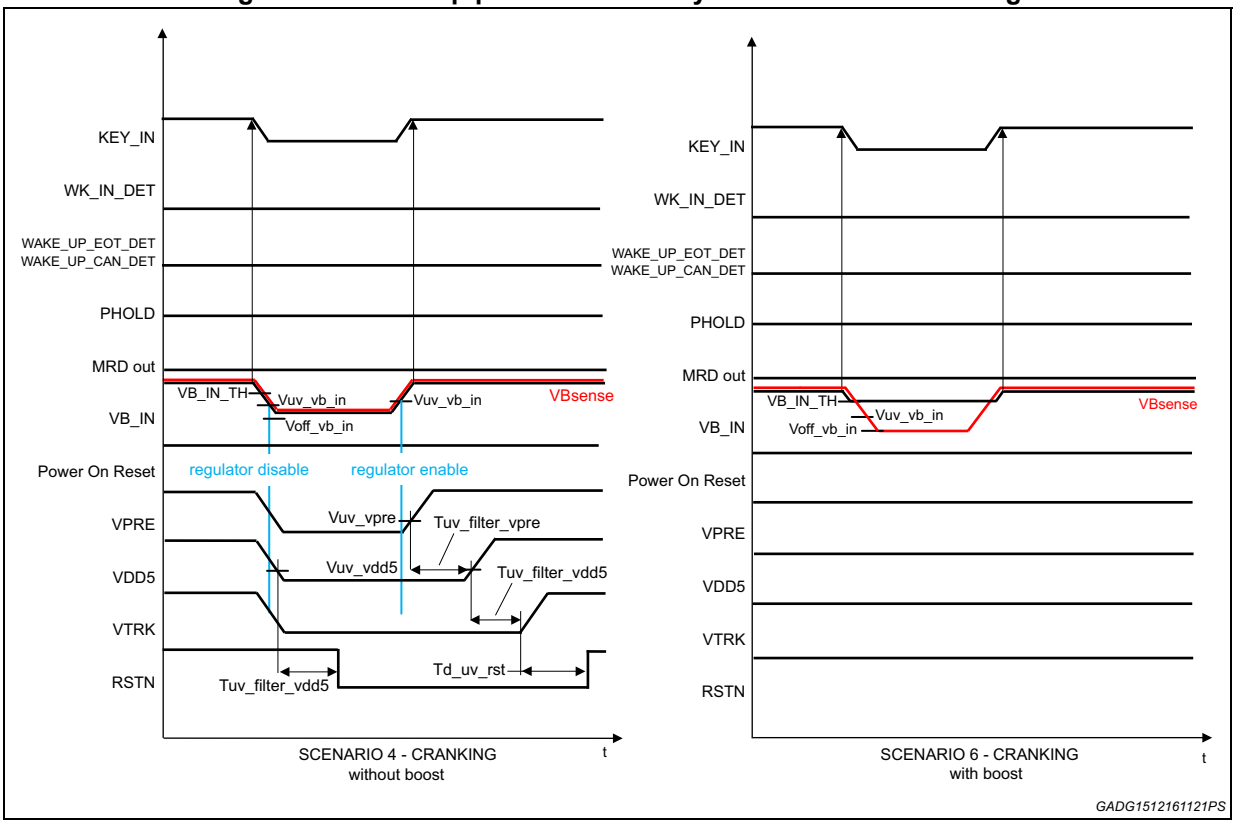


Figure 96. Power up with WK_IN and power down with WK_IN in not permanent battery condition

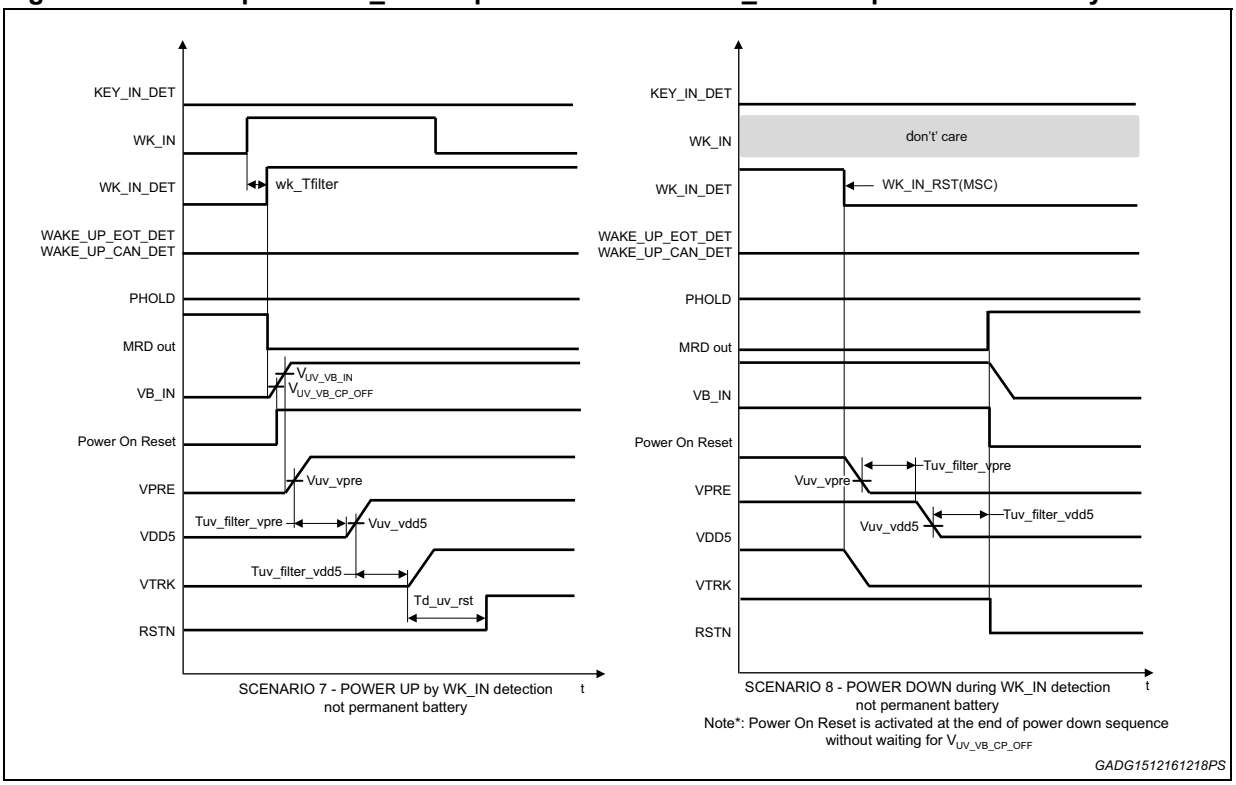


Figure 97. Power up with WK_IN and power down with WK_IN in permanent battery condition

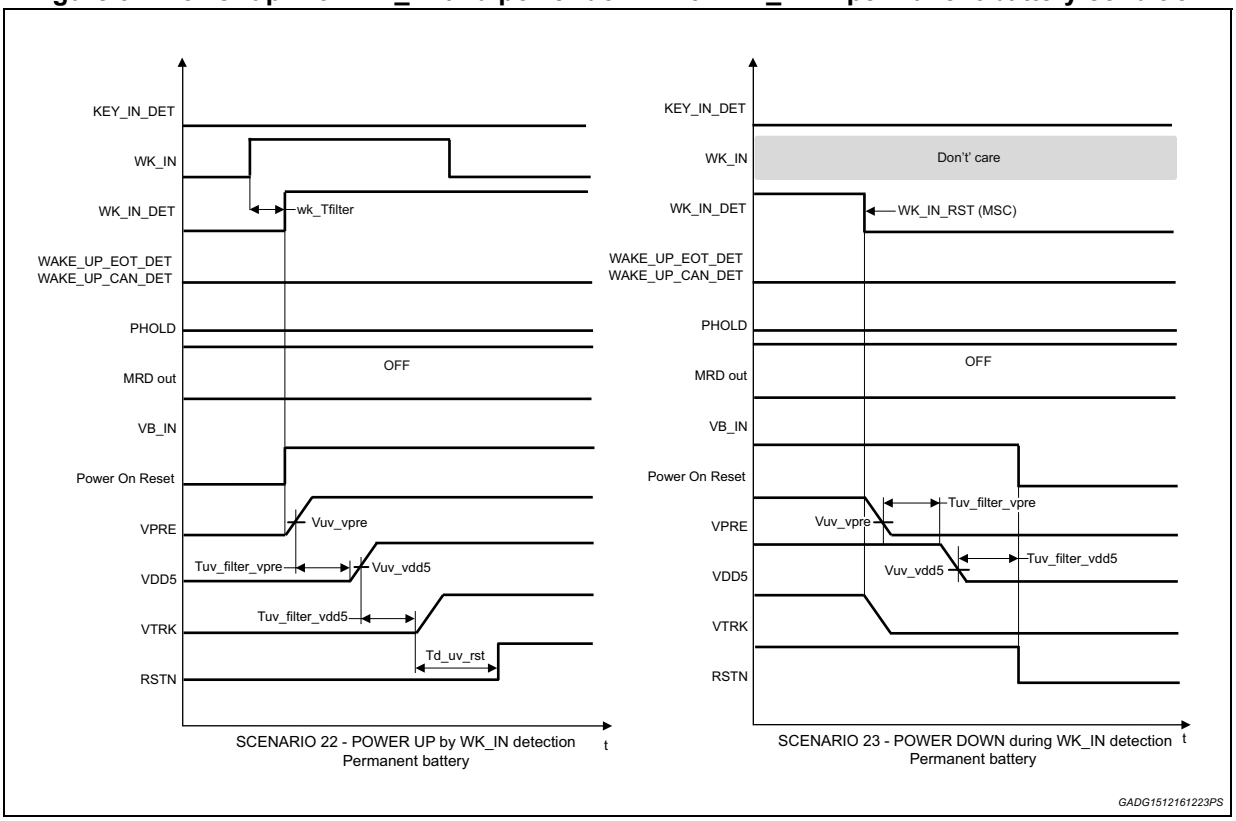


Figure 98. Power up with WAKE_UP_EOT/CAN and power down with WAKE_UP_EOT/CAN (Scenario 9 and 10)

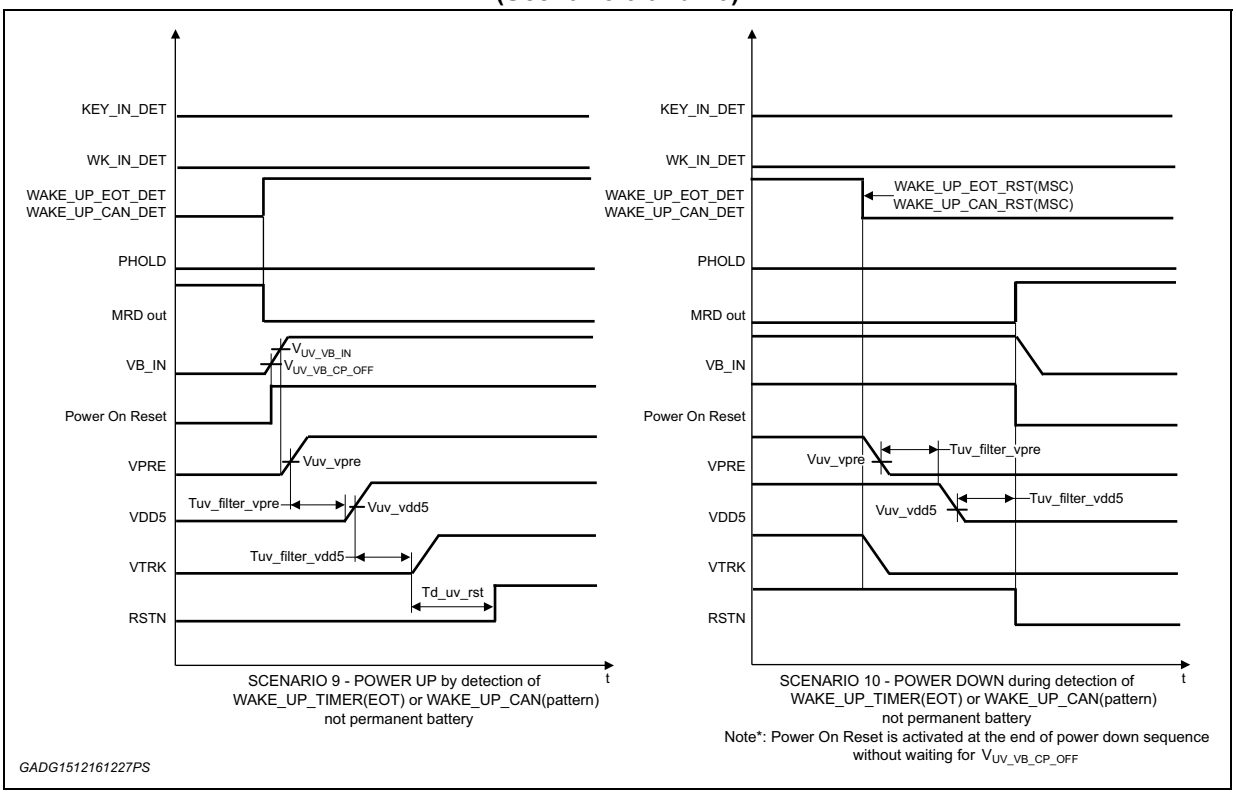


Figure 99. Power up with WAKE_UP_EOT/CAN and power down with WAKE_UP_EOT/CAN (Scenario 24 and 25)

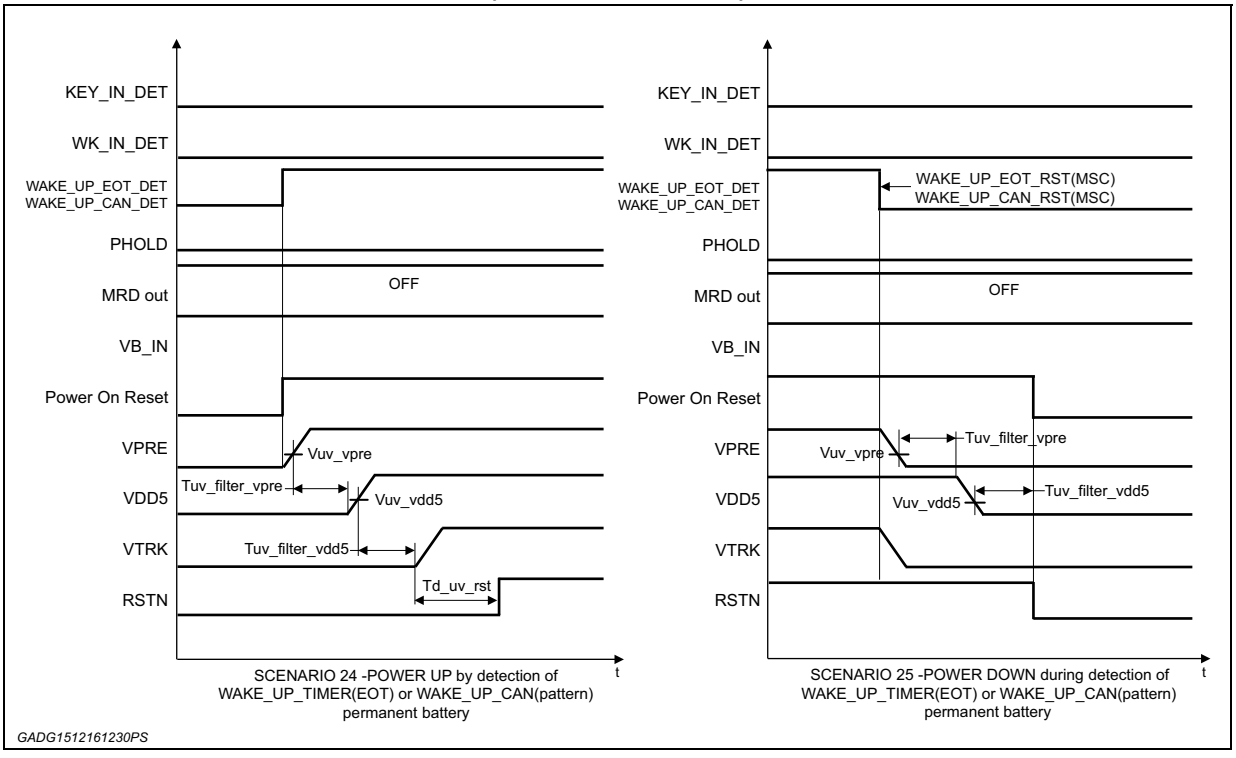


Figure 100. Main relay driver timeout

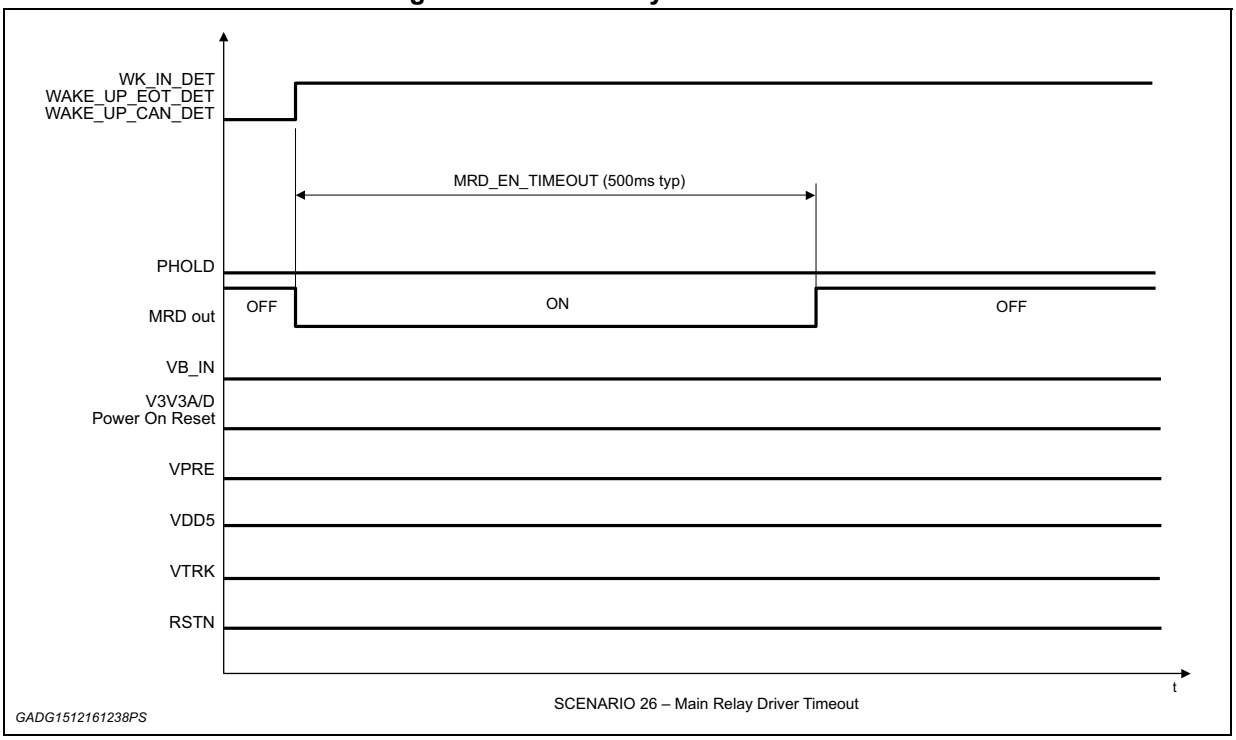
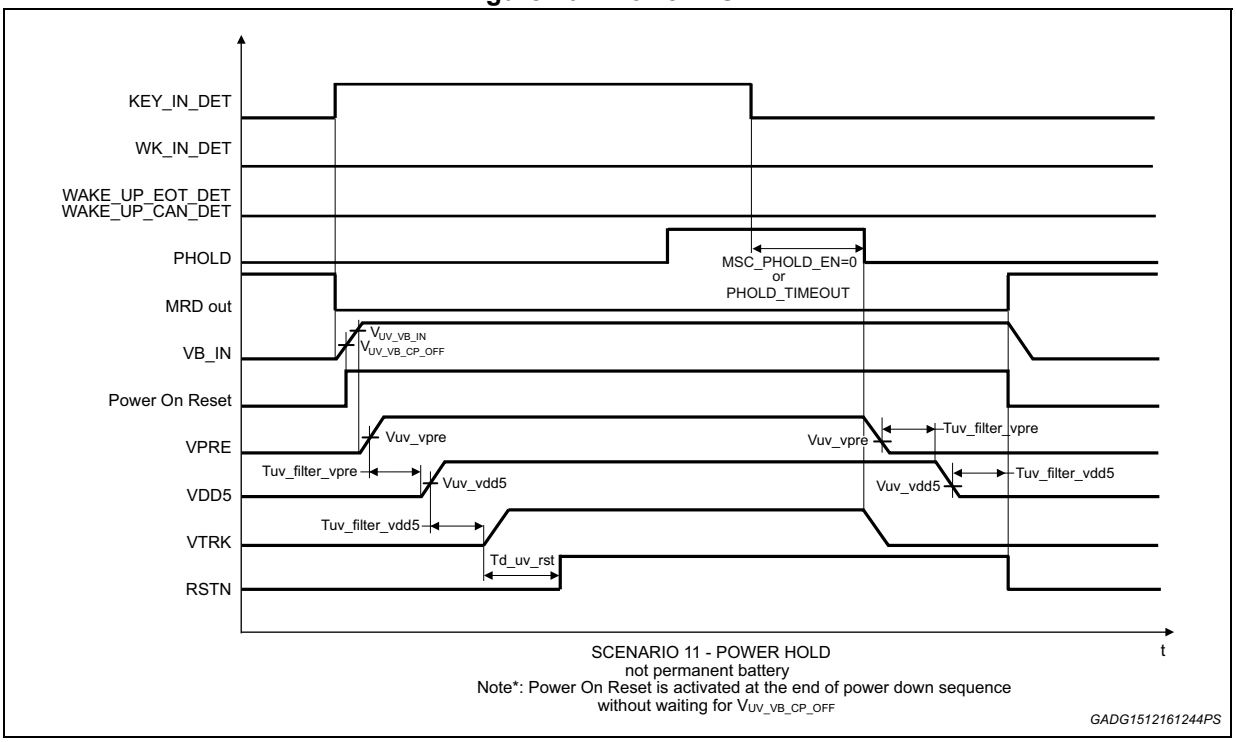


Figure 101. Power HOLD



According to reset matrix power down is also produced by Watchdog PWR_CNT counter overflow during KEY_IN low. In these cases the power down sequence is actuated without considering VDD5 undervoltage.

A.4 Main relay scenario

Figure 102. Overcurrent OVC removed before VB present with KEY_IN high and Overcurrent OVC removed before VB present with KEY_IN stays high

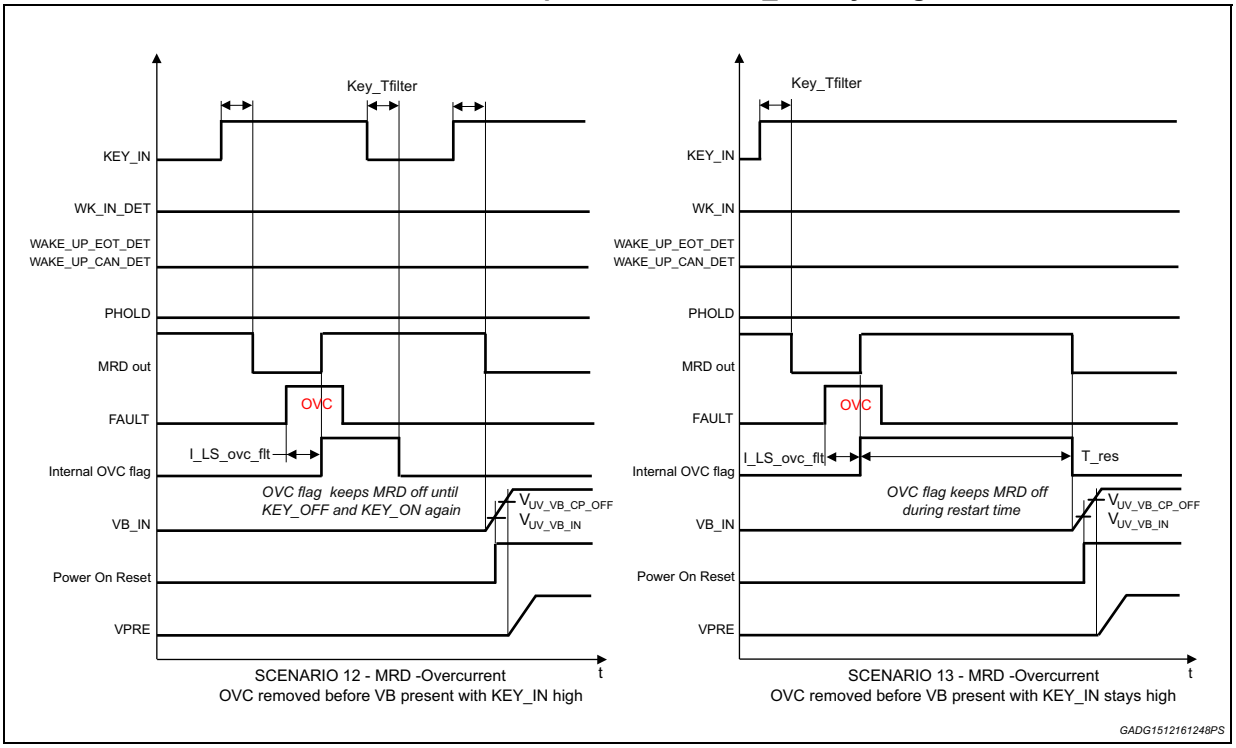


Figure 103. Overcurrent OVC permanent after VB present with KEY_IN high

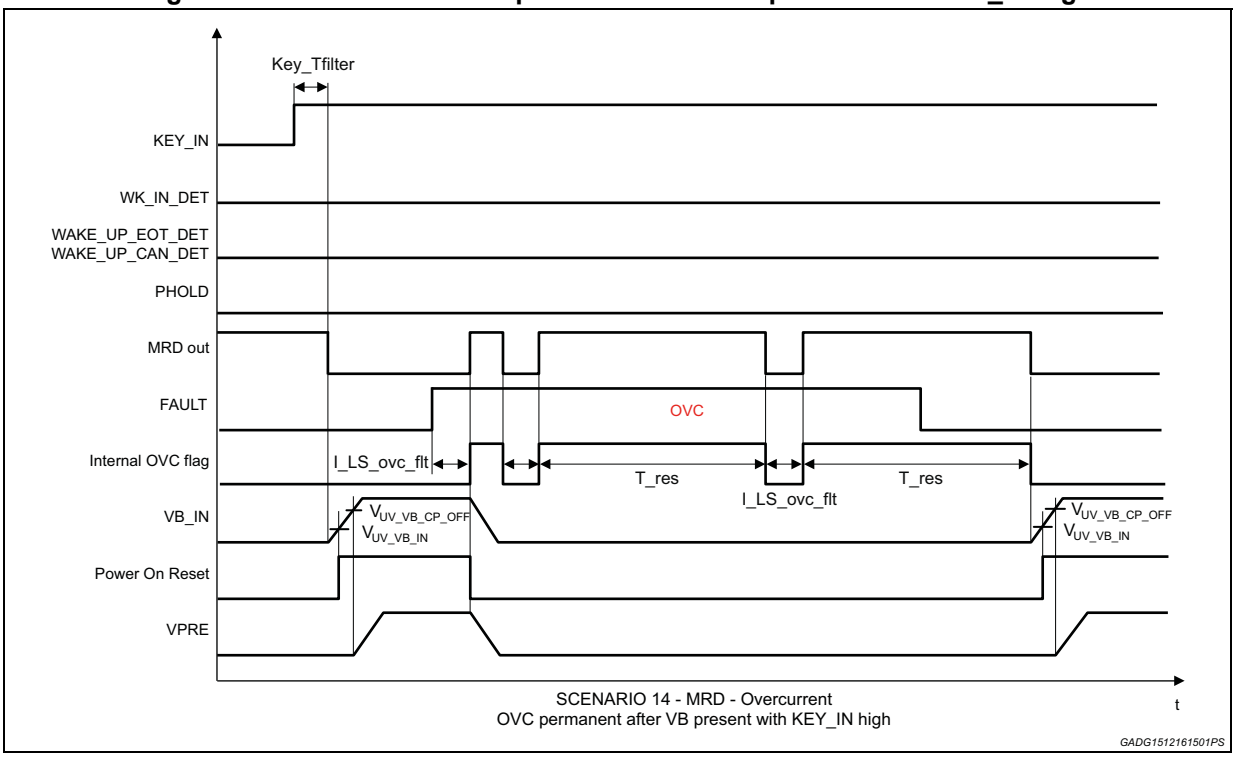


Figure 104. Overcurrent OVC permanent after VB present with KEY_IN high - unlimited retry

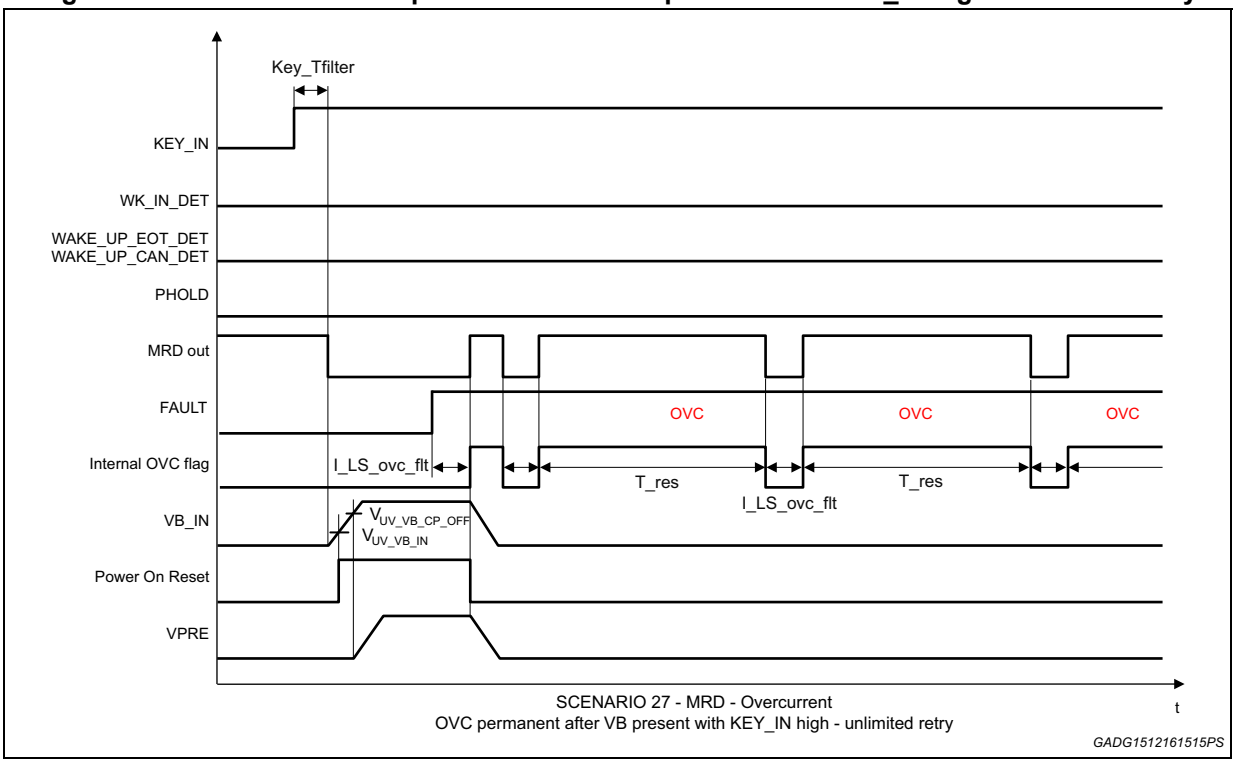


Figure 105. Overcurrent OVC removed before Tres activation with KEY_IN high and Overcurrent OVC permanent in PHOLD

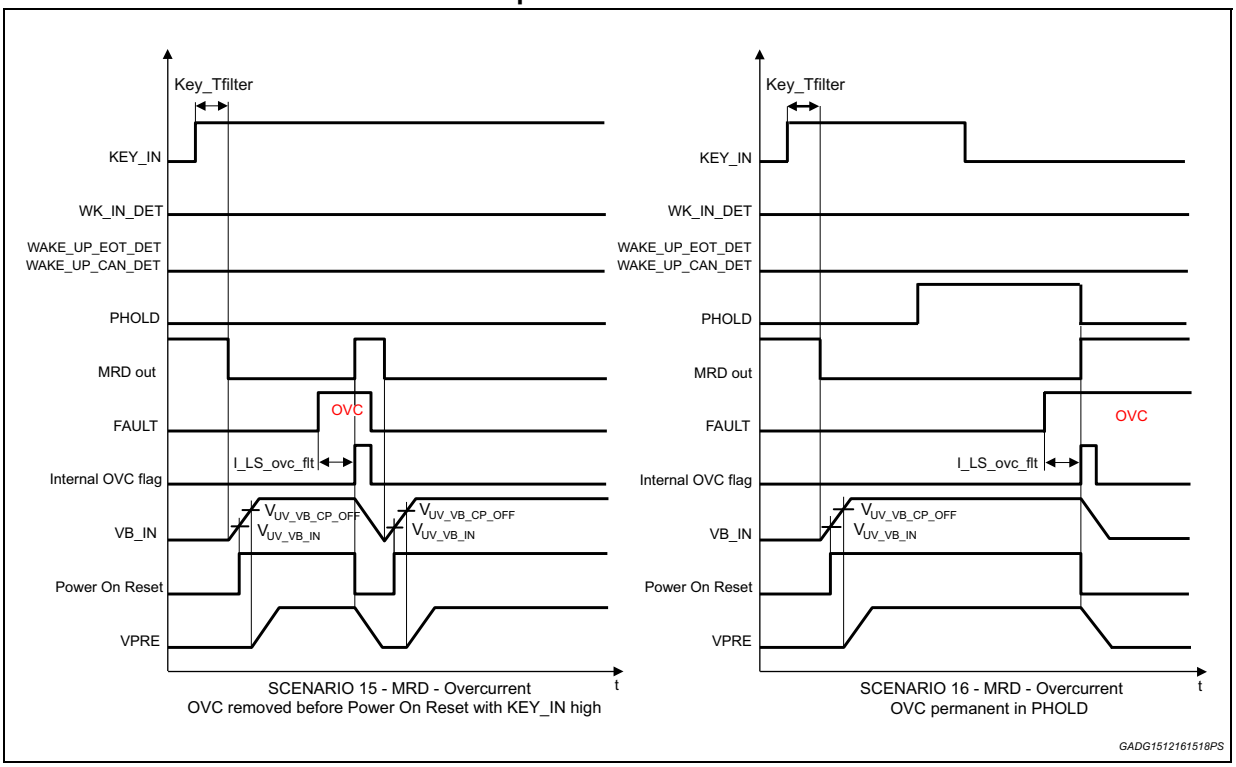


Figure 106. Overcurrent not permanent battery OVC not permanent before VB present with WK_IN/WAKE_UP_EOT/CAN detection (scenario 17)

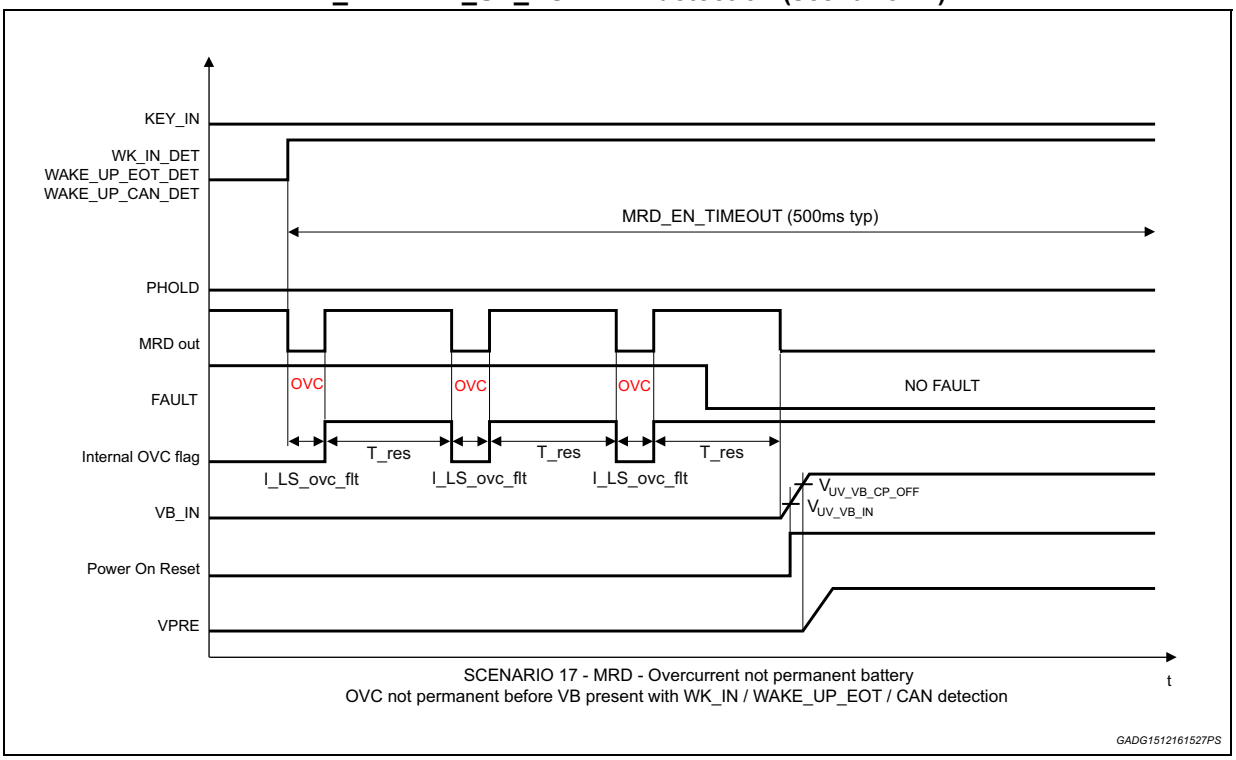


Figure 107. Overcurrent not permanent battery OVC not permanent before VB present with WK_IN/WAKE_UP_EOT/CAN detection (scenario 18)

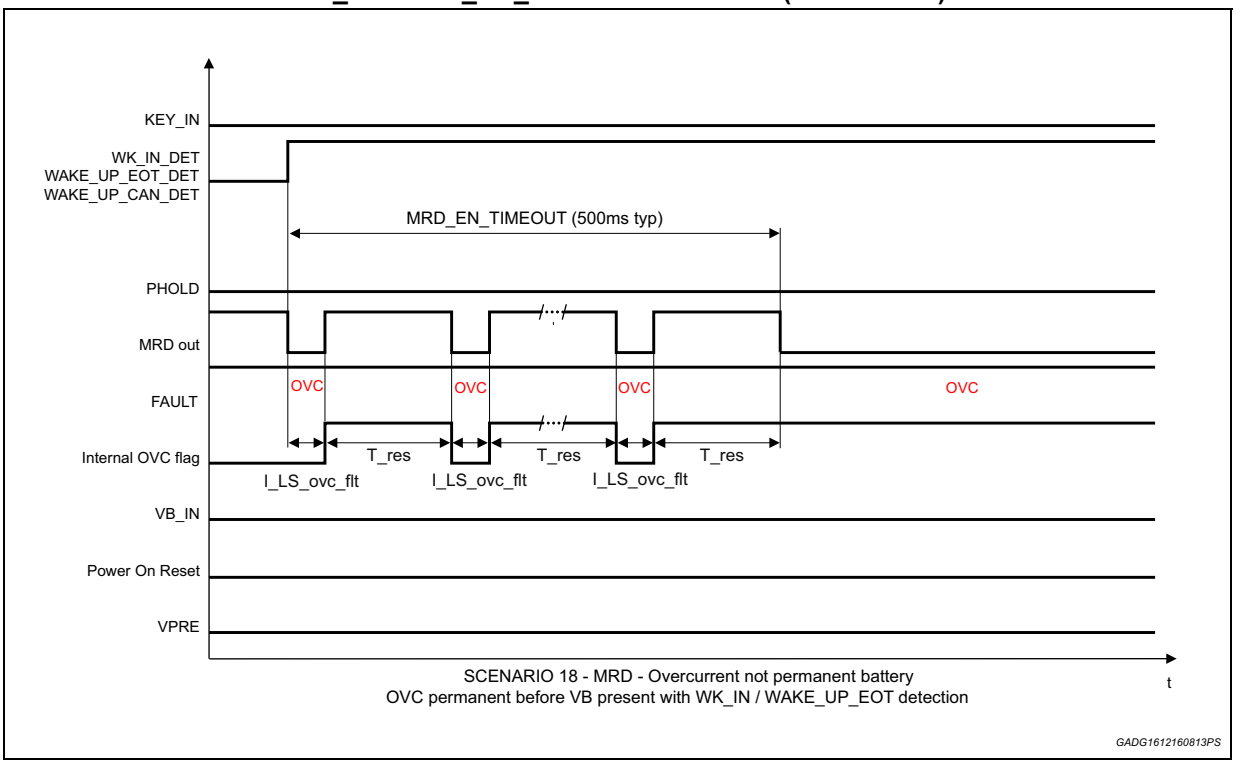


Figure 108. Overcurrent not permanent battery OVC not permanent after VB present with WK_IN/WAKE_UP_EOT/CAN detection - no retry

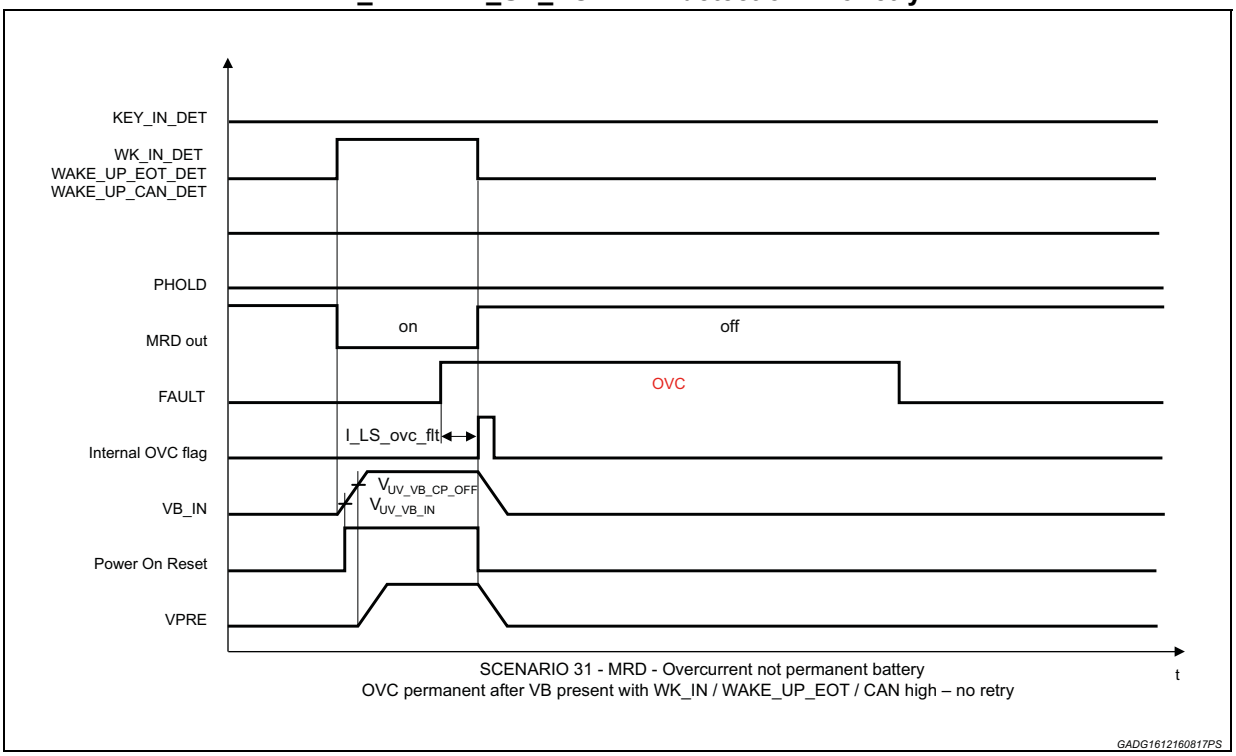
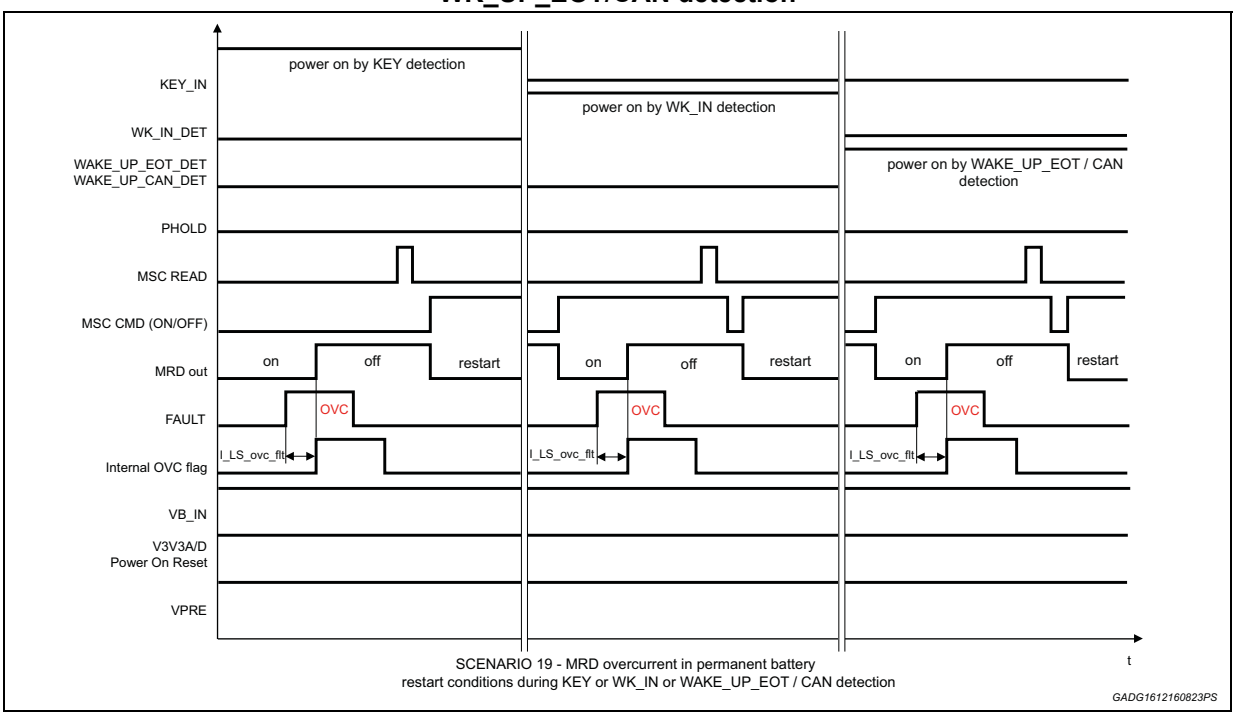


Figure 109. Overcurrent in permanent battery restart conditions during KEY or WK_IN or WK_UP_EOT/CAN detection



Note: In permanent battery when power on by KEY the MSC CMD can only restart driver after OVC. The MSC CMD OFF has no effect.

Figure 110. Overcurrent in permanent battery PHOLD

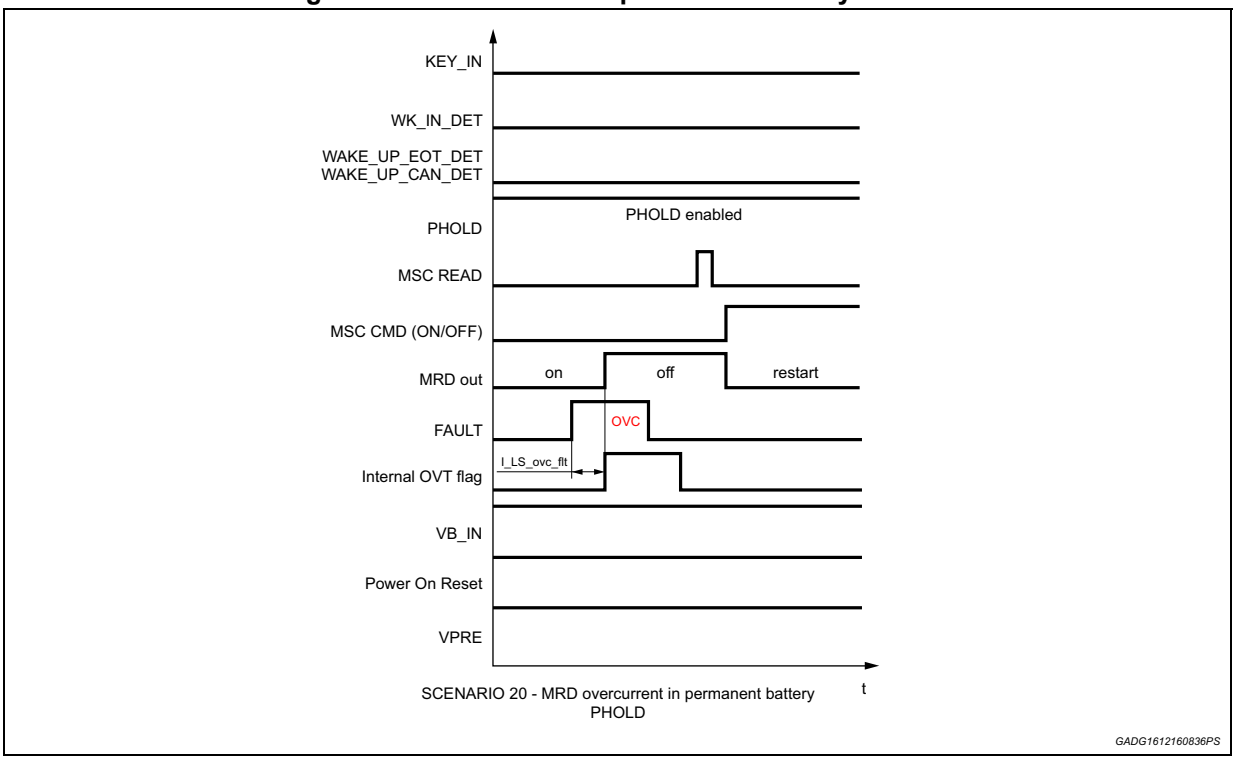


Figure 111. Overtemperature in permanent battery restart conditions during KEY or WK_IN or WAKE_UP_EOT/CAN detection

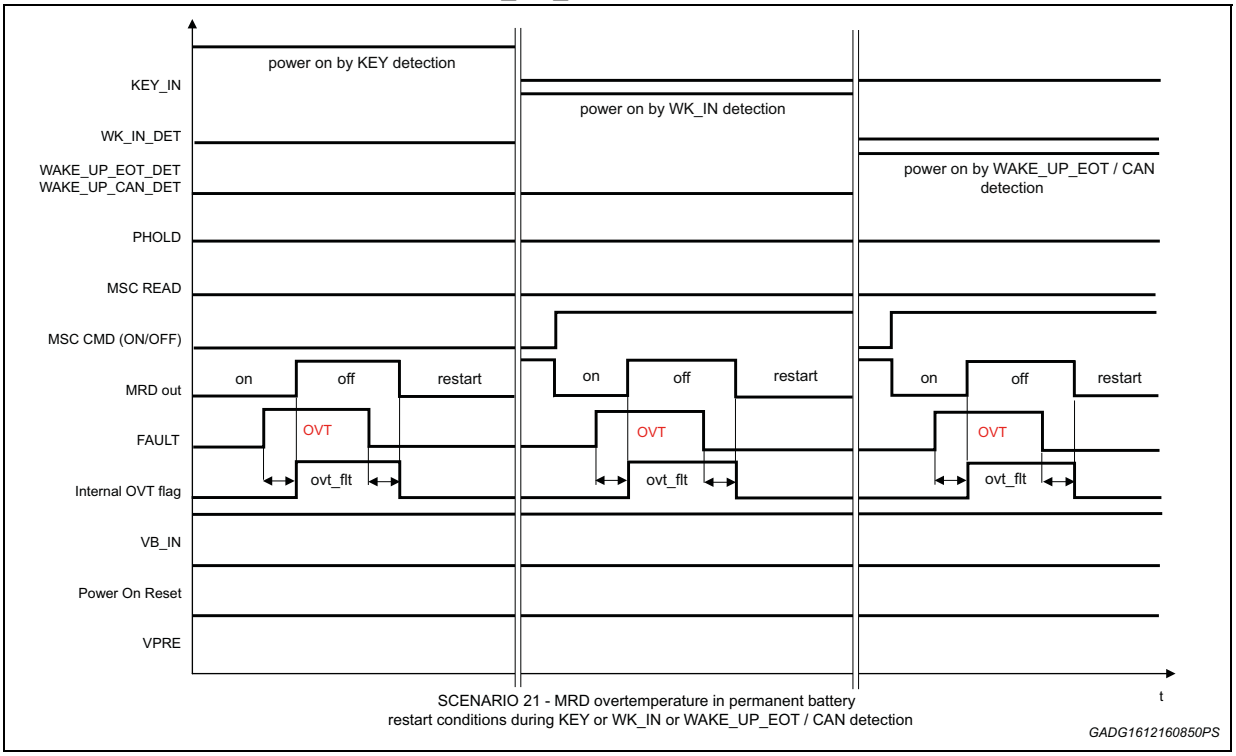


Figure 112. Overtemperature in permanent battery PHOLD

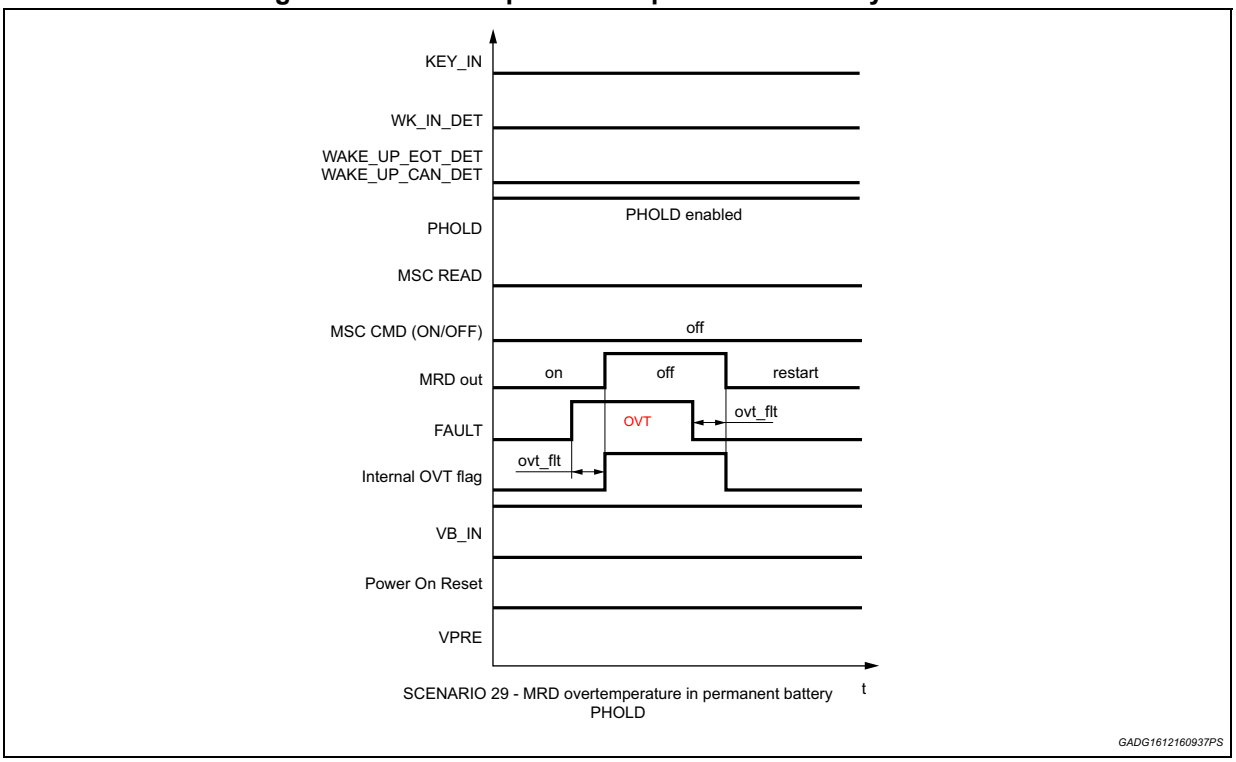


Figure 113. Overtemperature (permanent fault) in not permanent battery Power on by KEY detection

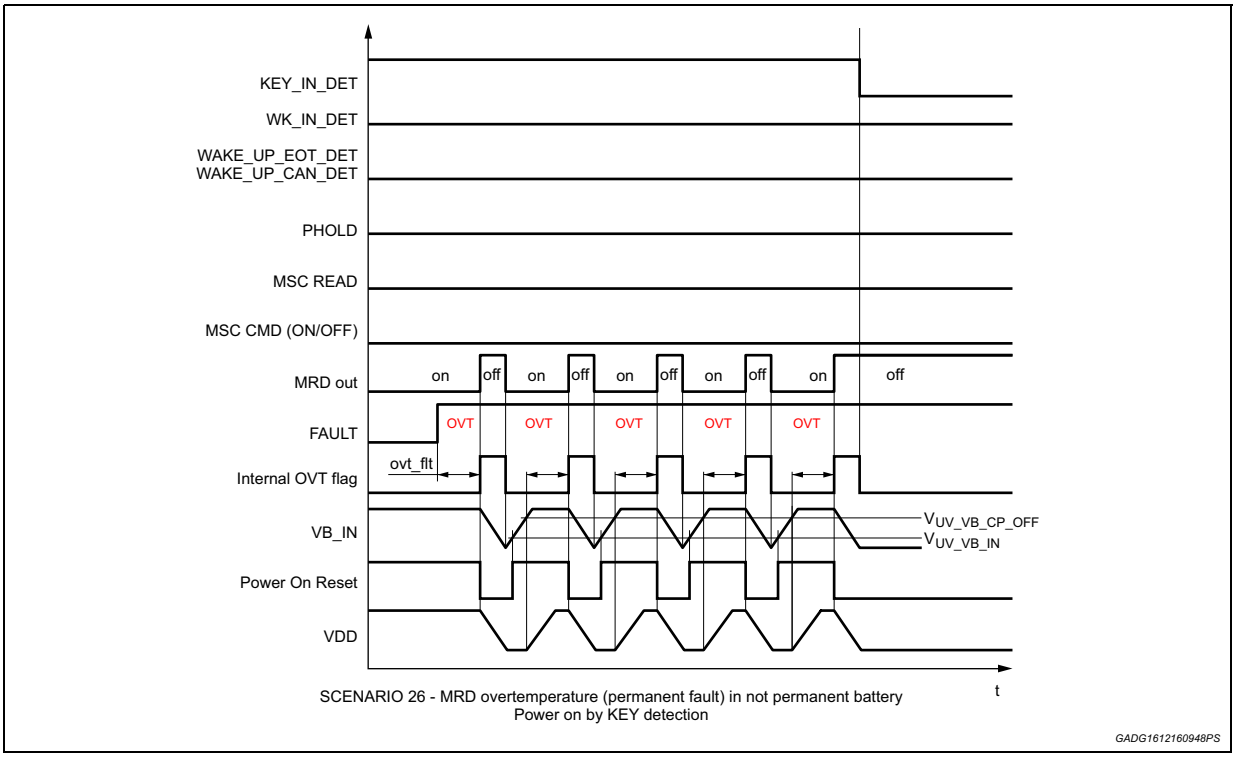


Figure 114. Overtemperature (not permanent fault) in not permanent battery Power on by KEY detection

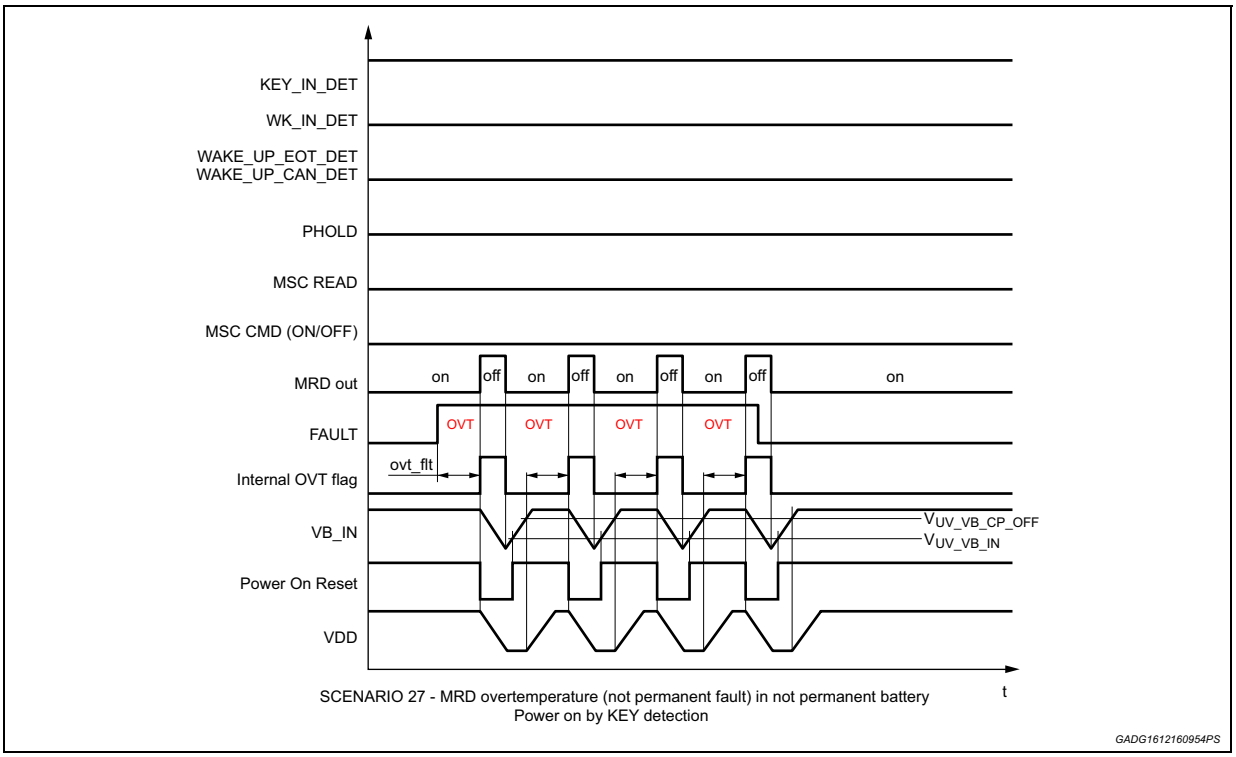


Figure 115. Overtemperature in not permanent battery Power on by WK_IN or WAKE_UP_EOT/CAN detection

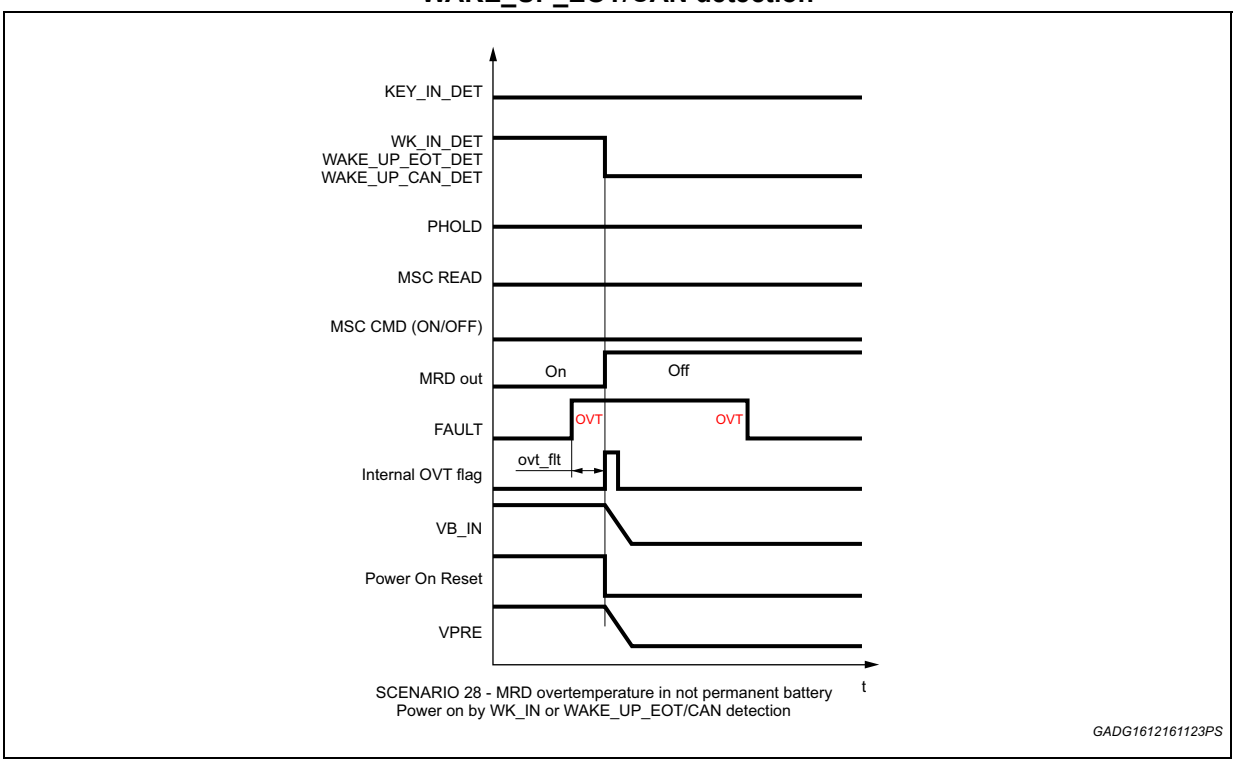
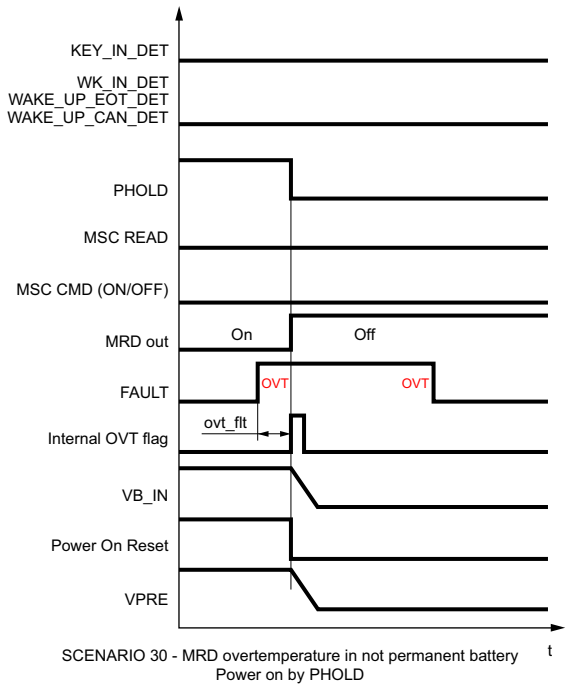


Figure 116. Overtemperature in not permanent battery Power on by PHOLD



Appendix B Application diagrams

Figure 117. Driver/predriver section application diagram

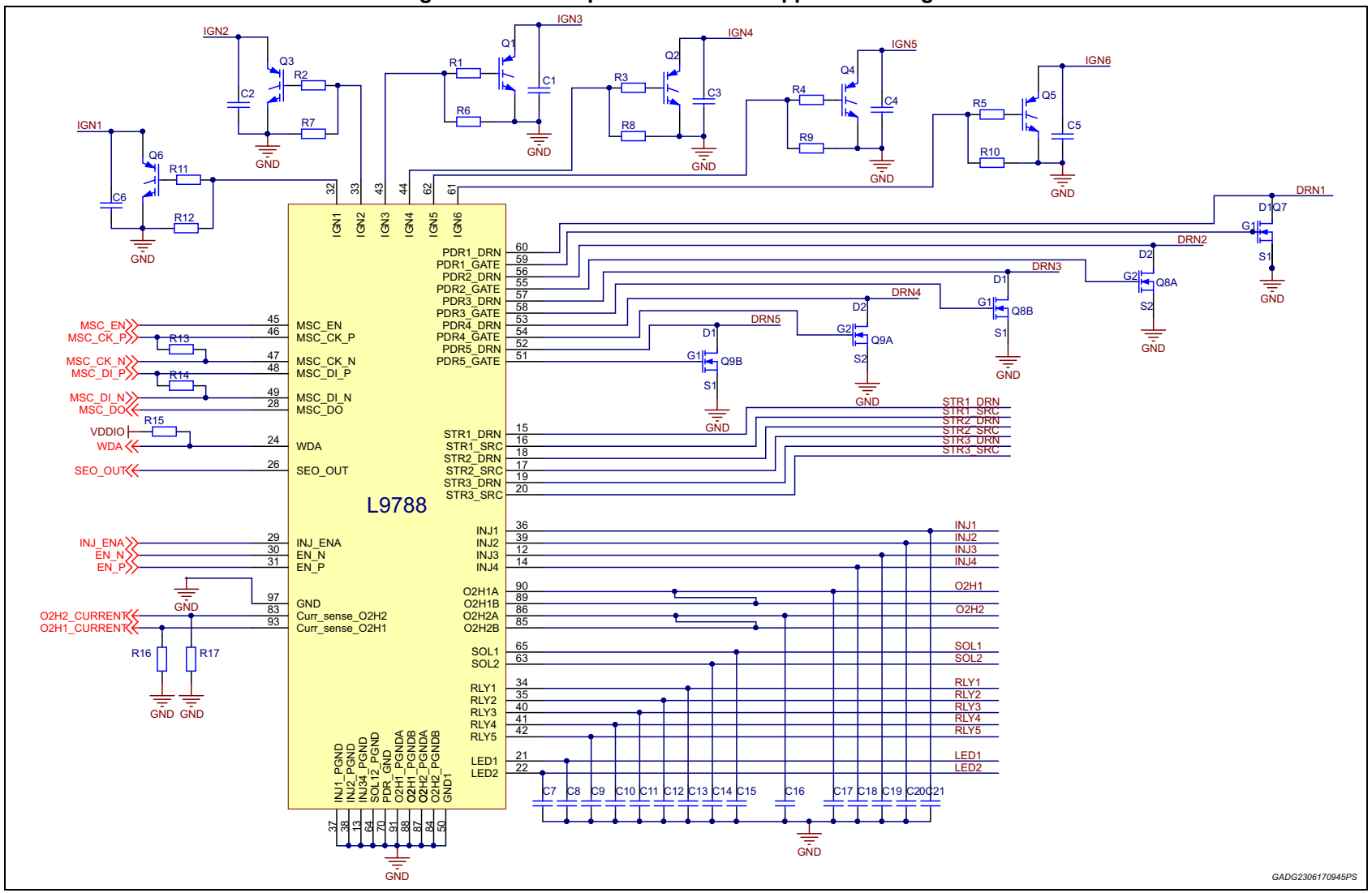
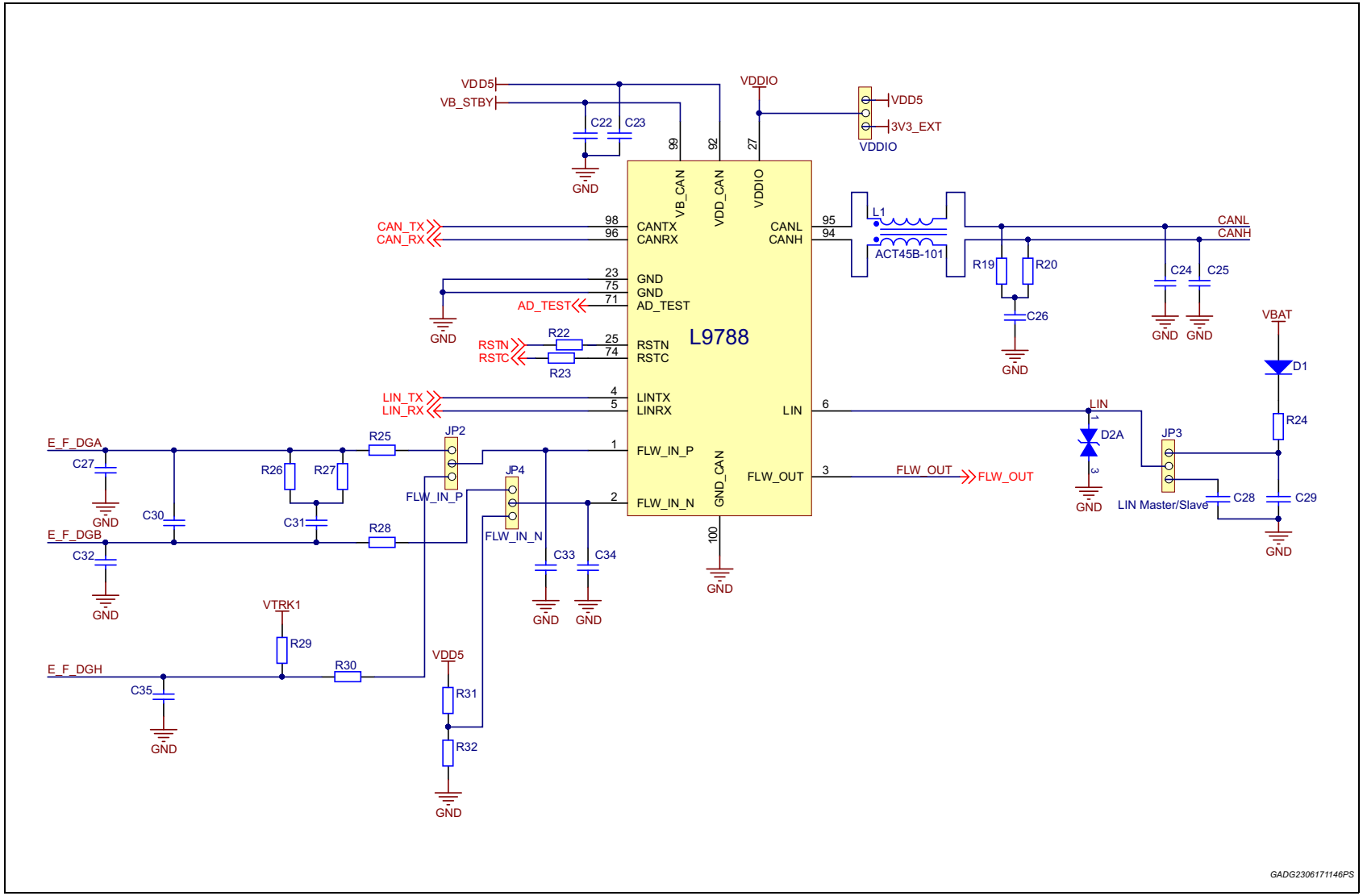


Figure 118. Interface section application diagram



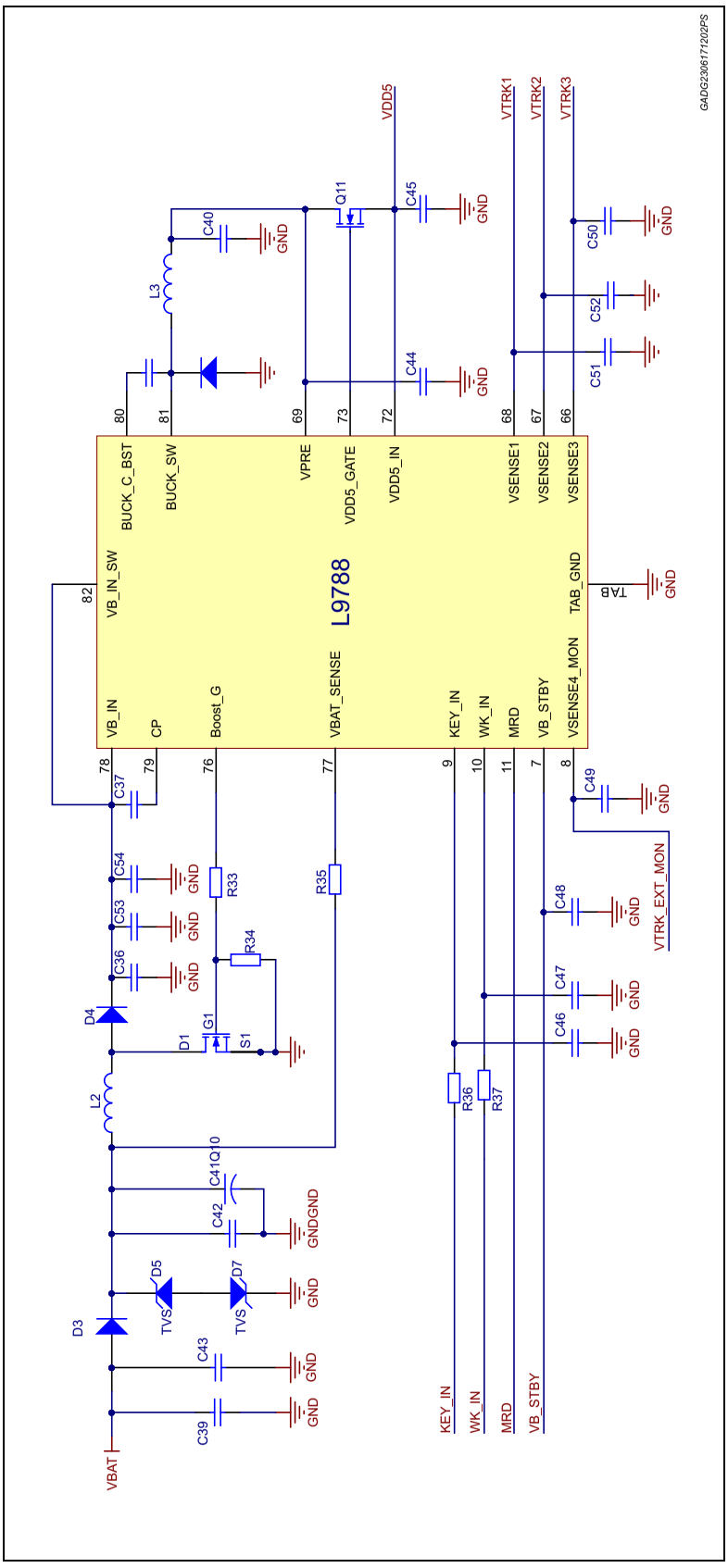


Figure 119. Multi regulator supply section application diagram

B.1 Bill of material

Table 111. Bill of material

Symbol	Parameter	Min	Typ	Max	Unit	Note
C39	Battery filter capacitor	-	4.7	-	nF	-
D3	Reverse battery protection diode	-	-	-	-	Choice: STTH4R02
D5,D7	TVS diode	-	-	-	-	Choice: TPSMB36A
C42	battery decoupling capacitor	-	100		nF	
C41	battery decoupling capacitor	-	100		µF	
L2	Boost inductance	-	-	-	-	see *Table 28*
Q10	Boost MOSFET	-	-	-	-	choice: STD20NF06L see *Table 27* and *Table 28*
D4	Boost diode	-	-	-	-	choice: STPS10H100C see *Table 28*
C36	Cout_boost	36	40	150	µF	see *Table 28*
C53	Cout_boost_ALU	0	330	470	µF	see *Table 28*
R33	Rg	-	2.2	-	Ω	see *Table 28*
R34	Rg_pd	-	150	-	kΩ	see *Table 28*
C37	External charge pump capacitor	80	100	120	nF	see *Table 39*
R35	Rsense	10	22	30	kΩ	see *Table 28*
C43	filter capacitor	-	100	-	nF	Optional
R36	KEY_IN protection resistor	-	1	-	kΩ	-
R37	WK_IN protection resistor	-	1	-	kΩ	-
C46, C47, C48, C49,C44, C54	filter capacitor	-	100	-	nF	-
C38	CBST	-	47	-	nF	see *Table 30*
L3	Lvpre	15	22	29	µH	see *Table 30*
D6	Dvbuck_CTRL	-	-	-	-	Choice: STPS5L60-Y see *Table 30*
C40	Cvpre	15	40	150	µF	see *Table 30*
Q11	-	-	-	-	-	choice: STD20NF06L see *Table 34* and *Table 35*
C45	CVDD5	5	20	60	µF	see *Table 35*

Table 111. Bill of material (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Note
C50,C51,C52	CVS1/2/3	0.38	0.47	20	µF	see *Table 32*
R1,R2,R3,R4,R5, R11	IGBT gate resistor	-	1	-	kΩ	-
R6,R7,R8,R9,R10, R12	IGBT Gate discharge resistor	-	4.7	0	kΩ	-
C1,C2,C3,C4,C5,C6	filter capacitor	-	1.5	-	nF	-
R13,R14	MSC differential line adapting resistor	-	100	-	Ω	-
R15	WDA pull-up external resistor	50	-	250	kΩ	See *Table 24*
Q7, Q8A, Q8B, Q9A, Q9B	-	-	-	-	-	choice: STL15DN4F
C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21	filter capacitor	-	4.7	-	nF	-
R16, R17	-	-	5.1	-	kΩ	See *Table 46*
C22,C23	decoupling capacitor	-	100	-	nF	-
R22,R23	protection resistor	-	1	-	kΩ	-
C27, C32	filter capacitor (VRS sensor configuration)	-	100	-	pF	-
C30	filter capacitor (VRS sensor configuration)	-	470	-	pF	-
R26,R27	filter resistor (VRS sensor configuration)	-	33	-	kΩ	-
C31	filter capacitor (VRS sensor configuration)	-	100	-	nF	-
R25,R28	Protection and reference resistors (VRS sensor configuration)	-	10 1%	-	kΩ	see *Section 11.2*
C35	filter capacitor (Hall sensor configuration)	-	1	-	nF	-
R29	pull-up resistor (Hall sensor configuration)	-	27	-	kΩ	-
R30	Protection and reference resistor (Hall sensor configuration)	-	27	-	kΩ	-
R31,R32	Protection and reference resistor (Hall sensor configuration)	-	33	-	kΩ	-
C33,C34	filter capacitor	-	470	-	pF	place close to pin
L1	CAN Choke	-	-	-	-	choice: ACT45B-101

Table 111. Bill of material (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Note
R19, R20	CAN termination resistor	-	60	-	Ω	-
C26	CAN termination capacitor	-	4.7	-	nF	-
C24,C25	-	-	47	-	pF	-
D2A	-	-	-	-	-	27V TVS
D1	Vser Diode	-	-	-	-	Choice: BAS21
R24	Lin pull-up resistor	-	1	-	kΩ	-
C28	-	-	-	-	-	Choice: 220pF
C29	-	-	-	-	-	Choice: 1 nF (K-Line), 680 pF (LIN)

Revision history

Table 112. Document revision history

Date	Revision	Changes
30-Jan-2018	1	Initial release.
20-Jun-2018	2	Updated *Figure 47: Safety switch off on page 121*.
03-Dec-2018	3	Updated: – *Table 11 (parameter IVB_STBY_ EOT_enable and IVB_STBY_EOT_enable*; – *"**DO: Serial Output Data**" on page 178*; – *Section 18.3: Upstream communication on page 184*.
30-May-2022	4	Updated: – *Figure 90: LQFP100 (14x14x1.4 mm exp. pad down) marking information*; – *Table 109: LQFP100 (14x14x1.4 mm exp. pad down) package mechanical data*. Document changed from "Restricted" to "Public".