L8202

MULTIFUNCTION ANALOG ASIC

1 FEATURES

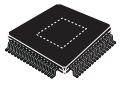
- Flexible Motor Driver configuration
  - 4 DC Motor drivers (1.5A Peak Current) or
  - 2 DC Motor drivers & 1 Dual Full Bridge Stepper Motor driver
- 2 Switching Voltage regulators
- 6 Open Drain Drivers
- Serial Input Port
- 4 Operational amplifiers
- Low voltage Supervisor
- Thermal Protection

2 DESCRIPTION

L8202 is a multifunction analog ASIC designed for MFP Inkjet printer applications.

L8202 integrates 4 full H Bridge drivers, 2 switching Buck type voltage regulators, 4 operational amplifiers, 6 open drain drivers, Reset Generation circuitry and over temperature protection circuitry.

Figure 1. Package



TQFP64

Table 1. Order Codes

Part Number	Package
L8202	TQFP64 (Exposed Pad Down)

The regulated Voltages are: VCC that can be either 3.3V or +5V and VDD, programmable by a resistor divider network from +3V to +17V

It is possible to increase the Output Current capability of the VDD regulator by adding an external discrete Power DMOS.

An internal regulator is present in the IC in order to supply several internal blocks. The 5V output voltage is filtered on pin V5 (Typical filter capacitor = 100nF) .

Figure 2. Block Diagram

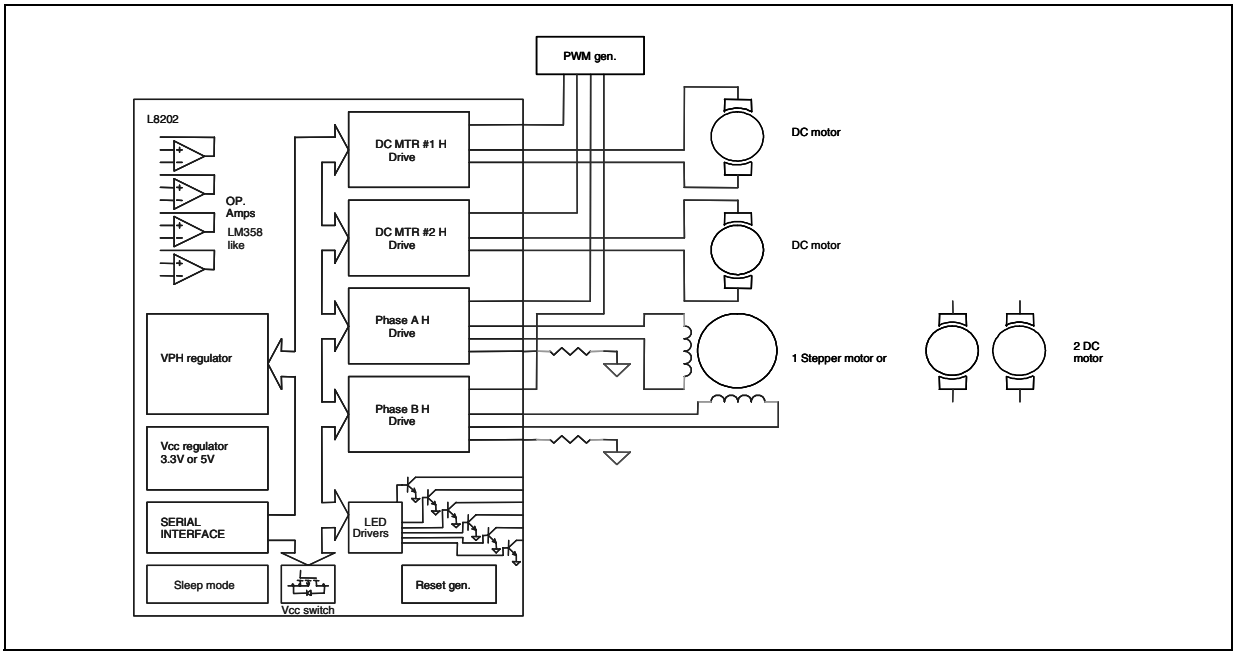


Table 2. Pin Description

N°	Pin	Function
1	PH_A+	Stepper Motor Driver Output A plus
2	R_Sense_A	Phase A Stepper Motor Driver Current Sense Resistor
3	PH_A-	Stepper Motor Driver Output A minus
4		No Connection
5	Test	This pin is used to measure internal Temperature of ASIC.
6	VDD_gate	Gate drive pin for external Power DMOS. N/C when internal FET is used.
7	VDD_source1	Source pin #1 for VDD internal FET. Used as differential input when external Power DMOS is used.
8	VDD_source2	Source pin #2 for VDD internal FET. Used as differential input when external Power DMOS is used.
9	VDD_drain1	Drain pin #1 for VDD internal FET. N/C when an external Power DMOS is used.
10	VDD_drain2	Drain pin #2 for VDD internal FET. N/C when an external Power DMOS is used.
11	Vs(VDD)	VDD regulator Supply voltage.
12	VDD_FB	Feedback for VDD Regulator
13		No Connection
14	PH_B-	Stepper Motor Driver Output B minus
15	R_Sense_B	Phase B Stepper Motor Driver Current Sense Resistor
16	PH_B+	Stepper Motor Driver Output B plus
17	Vs(DC4)	DC4 or Stepper PH_B Supply voltage.
18	Vs(Vcc)	Source pin for Vcc Regulator. Internally tied to other Vs.
19	Vcc_out	Output pin for Vcc Regulator
20	ODD 6	Open Drain Driver #6
21	Vcc_Select	This pin is used to select 5V or 3.3V for Vcc
22	Vcc_FB	Feedback for Vcc Regulator
23	DC4_PWM	PWM input for DC motor driver #4
24	DC3_PWM	PWM input for DC motor driver #3
25	DC1_PWM	PWM input for DC motor driver #1
26	DC2_PWM	PWM input for DC motor driver #2
27	Analog_GND	Analog Ground.
28	Vcc_Switch_Out	Vcc switched output pin.
29	Vcc_In	Vcc input pin.
30	V5	5V output pin.
31		No Connection.
32	Vs(DC1)	DC1 Supply voltage.
33	DC1B	Negative output for DC motor driver #1

Table 2. (continued)

N°	Pin	Function
34	GND(DC1)	DC1 Ground.
35	DC1A	Positive output for DC motor driver #1
36	ODD 5	Open Drain Driver #5.
37	ODD 4	Open Drain Driver #4.
38	ODD 3	Open Drain Driver #3.
39	ODD 2	Open Drain Driver #2.
40	ODD1	Open Drain Driver #1.
41	nCS	Chip Select, active Low
42	SCLK	Serial Clock
43	SDI	Serial Data In
44	nRESET	nRESET pin.
45	GND(Logic)	Logic Ground
46	DC2A	Positive output for DC motor driver #2
47	GND(DC2)	DC2 Ground.
48	DC2B	Negative output for DC motor driver #2
49	Vs(DC2)	DC2 Supply voltage.
50	OA_GND	Ground for Op-Amps
51	OA4-	Inverting Input for Op-Amp #4
52	OA4+	Non-Inverting Input For Op-Amp #4
53	OA4Out	Output for Op-Amp #4.
54	OA3-	Inverting Input for Op-Amp #3
55	OA3+	Non-Inverting Input for Op-Amp #3
56	OA3Out	Output for Op-Amp #3
57	OA2-	Inverting Input for Op-Amp #2
58	OA2+	Non-Inverting Input for Op-Amp #2
59	OA2Out	Output for Op-Amp #2.
60	OA1-	Inverting Input for Op-Amp #1
61	OA1+	Non-Inverting Input for Op-Amp #1
62	OA1Out	Output for Op-Amp #1.
63	OA_Supply	Op Amp Supply voltage.
64	Vs(DC3)	DC3 or Stepper PH_A Supply voltage.

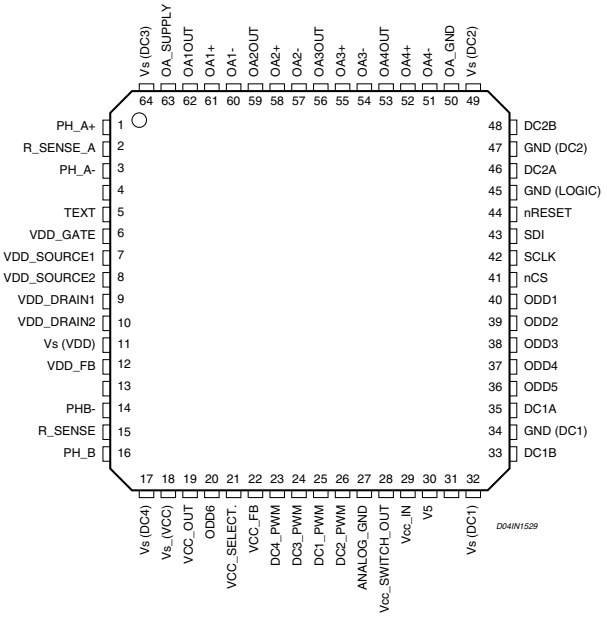
Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vs	Supply voltage, including ripple	44	V
VOD	Differential Voltage between Power pins, Supply pins and Ground	44	V
Vcc_IN, Vcc_FB	VCC	7	V
VDD Max	VDD Voltage (@I_{VDD} = 0.0A)	17	V
I_{VDD}	VDD Output current	3	A
$V_{CCOpAmp}$	Op Amp Supply Voltage	7	V
$V_{DIFF\ OpAmp}$	Op Amp Differential Voltage	7	V
Vmaxrst*	Maximum voltage on nRESET	Vcc_in	V
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

Table 4. Recommended Operating Conditions (T_j = 25°C, V_S= 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vs	Supply voltage, including ripple		24	30	38	V
IVs	Vs Standby Current	In the stand by mode(sleep=1)		3	15	mA
Vcc_IN, Vcc_FB	Vcc voltage	Vcc = 3.3V Vcc = 5.0V	3.15 4.8	3.3 5.0	3.45 5.25	V
Ivcc_in	Vcc input current nReset = 0, Ivcc_switch = 0	Vcc = 3.3V Vcc = 5.0V		2	5	mA

Figure 3. Pin Connections



3 SERIAL INTERFACE

L8202 Analog ASIC integrates an SPI interface (write only) for data exchange with the Digital ASIC.

The Input word is 19 bits long.

3 Input Pins are dedicated to the Serial Interface: nCS (Chip Select, active Low), SDI (Serial Data In), SCLK (Serial Clock). nCS must be pulled low to activate a Serial Input command.

Data present at the SDI pin are shifted into the L8202 on the 19 rising edges of SCLK.

The first bit present at the SDI, after the nCS is pulled low, and shifted into the L8202 at the first SCLK rising edge is the LSB. (SDI will remain at the value presented with the last bit of data). The low to high transition of nCS, after the 19th Sclk rising edge, loads the data into the internal L8202 ASIC input register.

The serial interface is cleared by nRESET.

Figure 4. SPI Operation

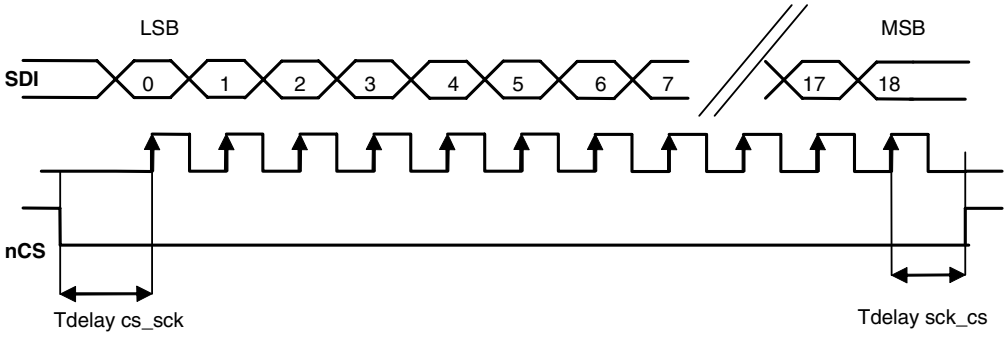


Table 5. SPI Timing specifications

(T_{amb} = 25 °C, V_S = 32 V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fck	Serial clock frequency	6	8	12	MHz
Tckhw	SCLK high width	30			ns
Tcklw	SCLK low width	30			ns
Tdelay_cs-sck	Delay nCS falling to first SCLK rising	10			ns
Tdelay_sck-cs	Delay last SCLK rising edge to nCS rising	10			ns
Tdata_setup	Data valid to SCLK set up time	10			ns
Tdata_hold	Data hold time	10			ns
Tdelay_cs	Delay required from (n-1)CS to nCS	10			ns
Tr_data	SDI rise time	0		20	ns
Tf_data	SDI fall time	0		20	ns
Tr/f_sck	SCLK rise/fall time	0		20	ns

Table 6. SPI Bit Definition

BIT #	Symbol	RESET VALUE	DESCRIPTION
0	STAND_BY	1	A Logic “1” inhibits OpAmps and Motors, and puts the L8202 into a lower power state. Chip must power up with Stand By Mode active. VDD regulators operate independently from Stand By Mode.
1	VDD_EN	0	A logic "1" enables the VDD regulator. Chip must power up with the VDD regulators inactive.
2	MDC1_D	0	Controls the direction of current flow through the DC motor windings. A high level causes current to flow from DC1A(source) to DC1B(sink).
3	MDC2_D	0	Controls the direction of current flow through the DC motor windings. A high level causes current to flow from DC2A(source) to DC2B(sink).
4	VSW_EN	1	A high level causes the 5V switch turn on. Chip must power up with the 5V switch closed.
5	ODD 1	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
6	ODD 2	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
7	ODD 3	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
8	ODD 4	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
9	ODD 5	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
10	ODD 6	0	Controls Open Drain Driver. A high level causes Open Drain Driver Turn On.
11	SEL_MTR	0	Selection of motor type. A high level selects DC motor. A logic 0 level selects Step motor.
12	I1_PH_B	1	This input and I0_PH_B select the output of three comparators to set the current level. Current also depends on the sensing resistor and reference voltage.
13	I0_PH_B	1	See I1_PH_B
14	D_PH_B	0	This TTL-compatible logic input sets the direction of current flow through the load. A high level causs current to flow from OUT A (source) to OUT B(sink). A Schmitt triger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
15	I1_PH_A	1	This input and I0_PH_A select the output of three comparators to set the current level. Current also depends on the sensing resistor and reference voltage.
16	I0_PH_A	1	See I1_PH_A
17	D_PH_A	0	See D_PH_B
18	Test	0	A high level forces the device to enter in Test Mode.

4 DC/DC CONVERTERS SPECIFICATION

L8202 contains 2 DC/DC converters.

VCC converter is programmable by the Vcc_Select pin for an Output Voltage rated at 3.3V or 5V (1.2A max.). VDD voltage is programmable by a resistor divider network to voltages from +3V to +17V.

The switching frequency of the two converters is 200KHz.

The Vcc and the VDD regulators are protected by thermal protection circuit with thermal hysteresys (Output Voltages are switched off during thermal protection event). The output voltages, Vcc and VDD are short circuit protected.

4.1 VCC Regulator

Table 7. Electrical Characteristcs (T_j = 25 °C, V_S = 32 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC_o}	Vcc Regulator Output Voltage. Vcc value selected by Vcc_select pin.	Vcc = 3.3V From 10mA to 1.2A Vcc = 5V From 10mA to 1.2A	3.23 4.90	3.3 5	3.37 5.20	V V
I_{OC_detect}	Over current Threshold level		1.6		4.8	A
I_{OC_BK} time	Blankig time for overcurrent detect			400		ns
I_{Vcc_load}	Vcc external load current		10		1200	mA
f_{ck}	Operating frequency	T_{amb} = 10 to 55°C	175	200	225	KHz

4.2 VDD Regulator

Table 8. Electrical Characteristcs (T_j = 25 °C, V_S = 32 V, unless otherwise specified**)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD_O}	VDD Regulator Output Voltage range	24V≤ Vs ≤ 38V	3		17	V
Vref	Internal reference voltage for error amp		-2%	1.24	+2%	V
I_{VDD_load}	Vcc external load current		0.01		3.0	A
$I_{OC\_det\_SU}$	Over current detect level	During start up	2.0	3.2		A
$I_{OC\_det\_SC}$	Over current detect level	During short circuit	4.0	5.5		A
V_{Sen_VDD}	Current sense voltage	Using external Power DMOS, this is a voltage of Ext. resistor between Vs and VDD_source	-20%	250	+20%	mV
$I_{OC\_BK\ time}$	Blankig time for overcurrent detect			300		ns
V_{GS_C}	Gate to source clamp voltage		Vs-15		Vs-10	V
T_{Full_LOAD}	Transient time after which max load can be applied to VDD regulator	Vs high, ASIC receives command to turn on VDD Reg	75			ms
I_{ST_UP}	Maximum load current appliable during start up.				1.2	A
f_{ck}	Operating Frequency	T_{amb} = 10 to 55°C	175	200	225	KHz

5 DC MOTOR DRIVERS OPERATIONS

L8202 provides PWM bi-directional drive for two DC motors.

The PWM modulation is provided by the MDx_PWM input, and the current direction into the motor by the MDCx_D bit in the serial input port.

The driver is protected versus overloads on the output lines to a max. current of 2 Amps peak.

The current protection circuit is implemented only on the High Side Drivers, so current protection is provided to motor currents only, but not to shorts between Motor Outputs to GND or Vs.

A blanking period following a current turn-on event is included to prevent false current protection.

The H Bridges are protected versus cross-conduction.

Thermal protection with hysteresys is provided to the Motor Drivers.

During thermal protection event the Bridge Outputs are forced into a high impedance status.

If nReset is low the motor drive outputs are forced in high impedance

Table 9. Absolute Maximum Ratings (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{DC_O}	Pulsed Output Current DC Motor Overcurrent Threshold		 2		1.5	A A

Table 10. Electrical Characteristcs (T_j = 25 °C, V_S = 32 V, unless otherwise specified**)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)}$	ON Resistance	I_{LOAD} = -0.75A (from output to GND) or I_{LOAD} = +0.75A (from Vs to output) @T_{amb} =25°		0.31 0.32		W
f_{PWM}	PWM frequency		10		30	KHz
T_{on},$T_{off\ min.}$	Minimum Ton and Toff time		500			ns
DC_{PWM}	PWM Duty Cycle range		1		99	%

Table 11. Truth Table

Internal Thermal Bit	Inputs		Outputs	
	MDCx_D	DCx_PWM	DCxA	DCxB
L	L	L	H	H
	L	H	L	H
	H	L	H	H
	H	H	H	L
H	X	X	All transistors turned off	All transistors turned off

6 STEPPER MOTOR DRIVER OPERATIONS

Two H Bridges are provided to implement current control through the two widings of a Bipolar Stepper Motor.

The phase and current level information are programmed over the serial input port (see Serial Interface Bits definition section).

Four current levels (0%,33%,66%,100%) are programmable through the status of IN0 and IN1 bits in the Input Serial Port.

This drive enters the fast current decay mode when both the I0_PH_X and I1_PH_X inputs set to the high logic level (current is recirculated from GND to Vs supply).

A blanking period following a current turn-on event is included to prevent false current protection.

The H Bridges are protected versus cross-conduction.

Thermal protection with hysteresys is provided to the Motor Drivers.

During thermal protection event the Bridge Outputs are forced into a high impedance status.

Table 12. Absolute Maximum Ratings (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{STEP_O}	Pulsed Output Current				1.5	A

Table 13. Electrical Characteristcs (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)}$	ON Resistance	I_{LOAD} = -0.6 A (from output to GND) or I_{LOAD} = +0.6 A (from Vs to output) @T_{amb} = 25°C		0.55 0.4		W
V_{Comp_HT}	Comparator High Threshold Voltage	I0_PH_x = 0 I1_PH_x = 0		500		mV
V_{Comp_MT}	Comparator Medium Threshold Voltage	I0_PH_x = 1 I1_PH_x = 0		333		mV
V_{Comp_LT}	Comparator Low Threshold Voltage	I0_PH_x = 0 I1_PH_x = 1		167		mV
I_{LEAK_VOFF}	VoOFF Output Leakage Current for Stepper Motor Driver Outputs	VoOFF = 5V I0_PH_x = 1 I1_PH_x = 1		0.5		mA
T_{off}	Off time		20	30	40	µs
T_j	Thermal shutdown		140			°C
$T_{j(enable\_hysterisys)}$	Stepper Motor driver thermal enable junction temperature hysterisys			20		°C

Table 14. Truth Table

I0_PH_x	I1_PH_x	$I_{STEP\_O\_PH\_x}$
L	L	100%
H	L	66 %
L	H	33 %
H	H	0 %

Notes: 1. The 100% current is fixed by the sense resistor, and the Maximum Threshold of the Voltage Comparator

7 OPERATIONAL AMPLIFLIERS

L8202 contains four general purpose Op-Amps,with their own Supply rail and Gnd rail. OpAmps are inhibited when L8202 is in sleep mode

Table 15. Absolute Maximum Ratings (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage		3.2		5.2	V
Vid	Differential Input Voltage				5.2	V

Table 16. Electrical Characteristcs (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vio	Input Offset Voltage	Vinp = Vcc-1.5	-9		9	mV
Avd	Large Signal Voltage Gain			130		V/mV
Vicm	Input Common Mode Voltage Range	Full range	0		Vcc-1.5	V
CMR	Common Mode Rejection Ratio	DC	70			dB
I_{source}	Output Current Source	Vcc = 5/3.3V Vo = Vcc-2V	10	20		mA
I_{sink}	Output Sink Current	Vcc = 5/3.3V, Vo = 2V	10	20		mA
V_{OH}	High Level Output Voltage	Sourcing 2mA, Vcc = 5.2V, full range	Vcc-0.5			V
V_{OL}	Low Level Output Voltage	Sinking 2mA, Vcc=5.2V, full range			0.5	V
SR	Slew Rate	Full Range Cload = 100pF	0.3			V/µs
GBP	Gain Bandwidth Product					

* Guaranted by design

8 OPEN DRAIN DRIVERS

L8202 contains 6 open Drain Drivers. These drivers are controlled by the Serial Interface by the bit ODD1/6, each driver is able to sink 30mA from either 3.3V or 5v Supply.

Table 17. Electrical Characteristics (T_j = 25°C, V_S = 32V, unless otherwise specified)

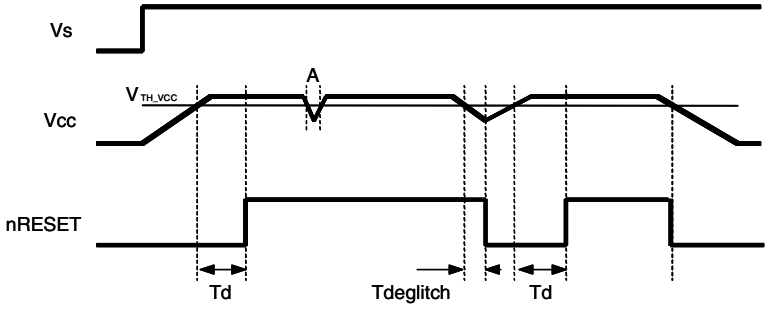
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{ODD_H}	High State Output Current	ODDx = 0, Vcc = 5.0V or 3.3V			1	µA
V_{ODD_L}	Low State Output Voltage	ODDx = 1, Vcc = 5.0V or 3.3V, Iload = 30mA			300	mV

9 VOLTAGE SUPERVISOR

nRESET is an Output/Input signal (active low), that is used both to provide the information about the status of Vcc and Vs supplies, both to provide a Reset signal to the internal logic when driven "low" from an external source for a period > 30µs.
When nRESET is asserted, Motor Drivers and VDD regulator are forced in the inactive state and the Serial Input Port is loaded with the "Reset Value".
To avoid false assertion due to glitches, nRESET is released to the "high" state with a delay of 100ms. Delay period is calculated from the moment Vcc is passing the Vcc threshold.

At power down no delay is present, and nRESET is asserted low by Vcc or Vs falling low respect to their thresholds

Figure 5.



Note A. L8202 ignores very brief transients. This should be less than Tdeglitch

Table 18. Electrical Characteristics (T_j = 25°C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vout_high	High-level output voltage at nRESET	Ioh = -0.1 mA	Vcc-0.5V			V
Vout_low	Low-level output voltage at nRESET	Vcc< V_{TH_VCC} Vs=38V			0.2	V
Rp_up	Internal pull-up resistance between Vcc_in and nRESET		2	3	5	KΩ
V_{TH_VCC}	Threshold voltage at Vcc & Vcc_in	Vcc = 3.3V Vcc_in = 3.3V	2.87 2.82		3.07 3.10	V
		Vcc = 5.0V Vcc_in = 3.3V	4.35 2.87		4.65 3.10	
V_{TH_Vs-}	Low threshold voltage at Vs	Vcc > VTH_VCC Vs decreasing	18.0		20.0	V
V_{TH_Vs+}	High threshold voltage at Vs	Vcc > VTH_VCC Vs increasing	19.25		21.25	V
V_{HYST_Vs}	Hysteresis Voltage	(V_{TH_Vs+}) -(V_{TH_Vs-})		1.2		V

Table 19. Switching Characteristics (T_j = 25 °C, V_S = 32V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Td	nRESET delay	Vcc >= V_{TH_VCC}	70	100	130	ms
Tdeglitch	Vcc out of tolerance persistence time	nRESET deasserted Vcc < V_{TH_VCC}	10	20	30	µs
Trise	Rise Time at nRESET	10 to 90%, 50pF Load			750	ns
Tfall	Fall Time at nRESET	90 to 10%, 50pF Load			50	ns

10 APPLICATION CIRCUIT

Figure 6.

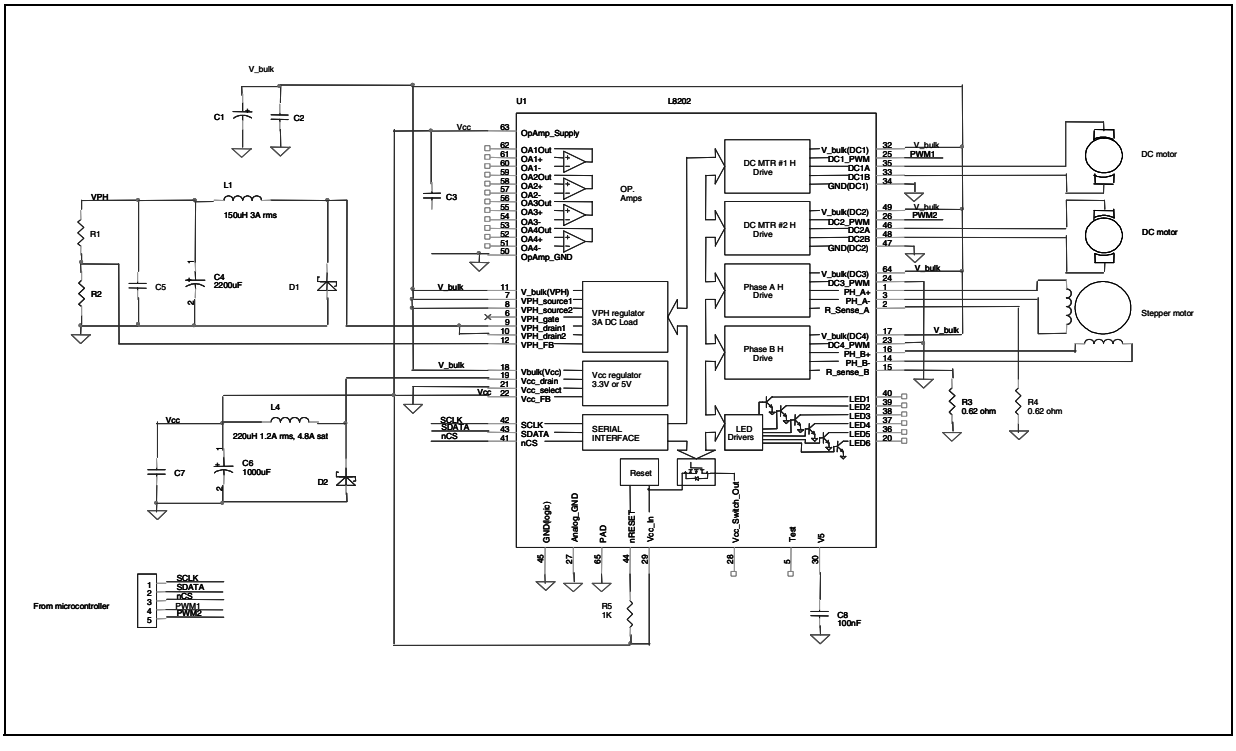


Figure 7.

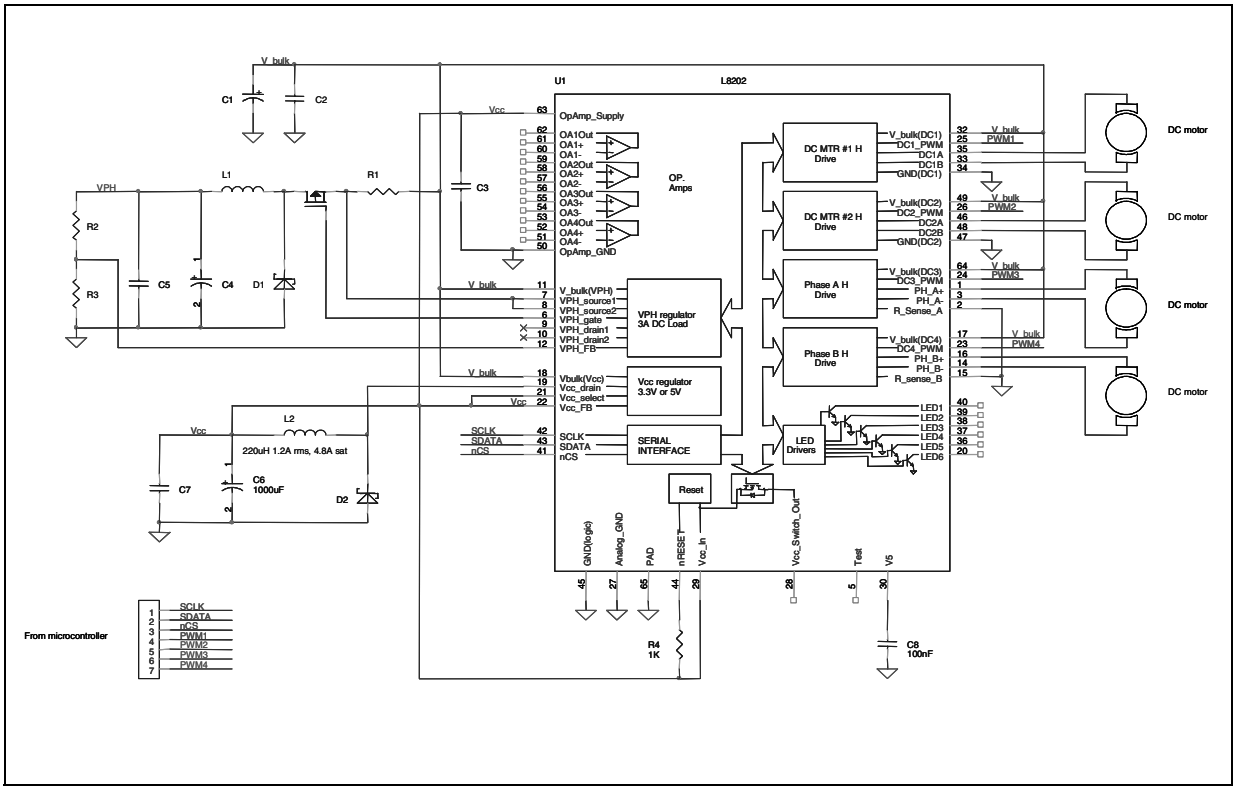
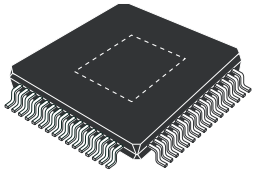


Figure 8. TQFP64 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.0472
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.0374	0.0393	0.0413
b	0.17	0.22	0.27	0.0066	0.0086	0.0086
c	0.09		0.20	0.0035		0.0078
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D2	2.00			0.787		
D3		7.50			0.295	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E2	2.00			0.787		
E3		7.50			0.295	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10x10x1.0mm)
Exposed Pad Down

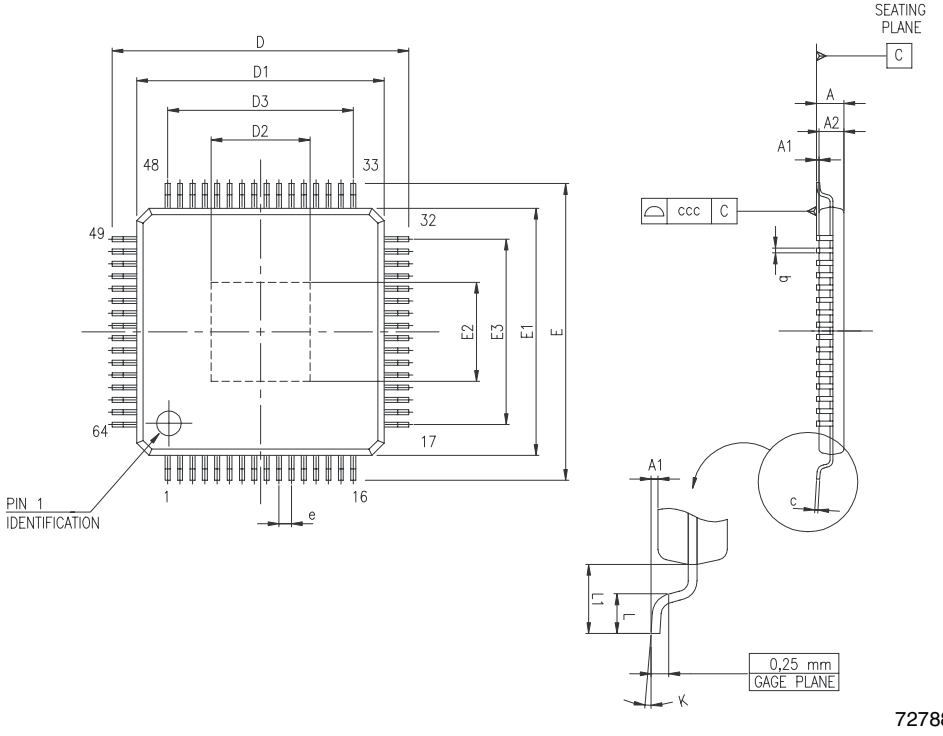


Table 20. Revision History

Date	Revision	Description of Changes
January 2005	1	First Issue
February 2005	2	Changed the maturity from Preliminary Data to Final Datasheet.