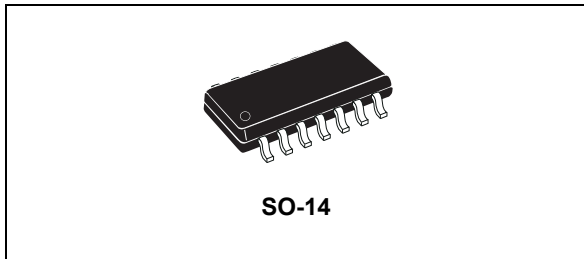


## High voltage high and low-side 4 A gate driver

Datasheet - production data



### Features

- High voltage rail up to 600 V
- $dV/dt$  immunity  $\pm 50$  V/ns in full temperature range
- Driver current capability: 4 A source/sink
- Switching times 15 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Comparator for fault protections
- Smart shutdown function
- Adjustable deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

### Applications

- Motor driver for home appliances, factory automation, industrial drives and fans
- HID ballasts
- Power supply unit
- Induction heating
- Wireless chargers
- Industrial inverters
- UPS

### Description

The L6491 is a high voltage device manufactured with the BCD6 "OFF-LINE" technology. It is a single-chip half-bridge gate driver for N-channel power MOSFET or IGBT.

The high-side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

An integrated comparator is available for fast protection against overcurrent, overtemperature, etc.

**Table 1. Device summary**

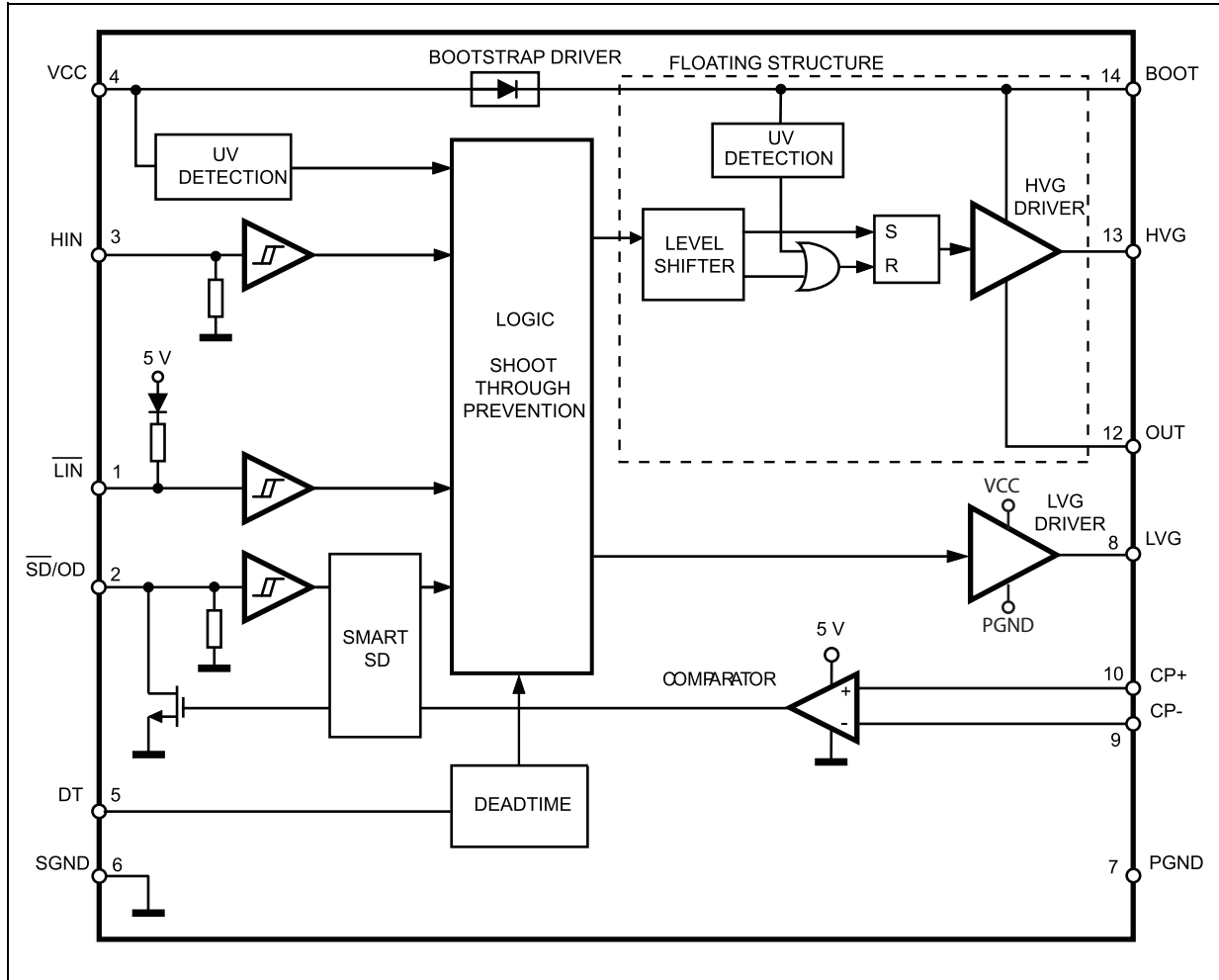
Order code	Package	Packaging
L6491D	SO-14	Tube
L6491DTR	SO-14	Tape and reel

# Contents

<b>1</b>	<b>Block diagram</b> .....	<b>3</b>
<b>2</b>	<b>Pin connection</b> .....	<b>4</b>
<b>3</b>	<b>Truth table</b> .....	<b>5</b>
<b>4</b>	<b>Electrical data</b> .....	<b>6</b>
	4.1 Absolute maximum ratings .....	6
	4.2 Thermal data .....	6
	4.3 Recommended operating conditions .....	7
<b>5</b>	<b>Electrical characteristics</b> .....	<b>8</b>
	5.1 AC operation .....	8
	5.2 DC operation .....	11
<b>6</b>	<b>Waveform definitions</b> .....	<b>14</b>
<b>7</b>	<b>Smart shutdown function</b> .....	<b>15</b>
<b>8</b>	<b>Typical application diagram</b> .....	<b>17</b>
<b>9</b>	<b>Bootstrap driver</b> .....	<b>18</b>
	C <sub>BOOT</sub> selection and charging .....	18
<b>10</b>	<b>Package information</b> .....	<b>20</b>
<b>11</b>	<b>Revision history</b> .....	<b>23</b>

# 1 Block diagram

Figure 1. Block diagram



## 2 Pin connection

Figure 2. Pin connection (top view)

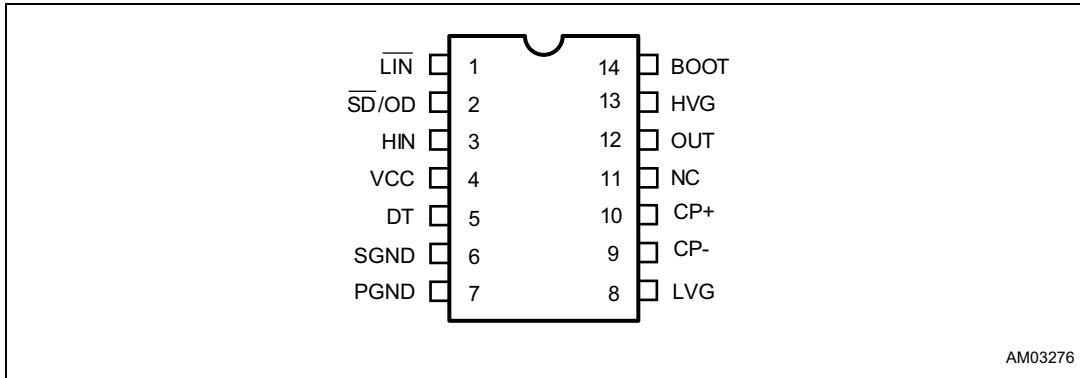


Table 2. Pin description

Pin number	Pin name	Type	Function
1	LIN	I	Low-side driver logic input (active low)
2	SD/OD <sup>(1)</sup>	I/O	Shutdown logic input (active low)/open-drain comparator output
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	SGND	P	Signal ground
7	PGND	P	Power ground
8	LVG <sup>(1)</sup>	O	Low-side driver output
9	CP-	I	Comparator negative input
10	CP+	I	Comparator positive input
11	NC		Not connected
12	OUT	P	High-side (floating) common voltage
13	HVG <sup>(1)</sup>	O	High-side driver output
14	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at  $I_{sink} = 10 \text{ mA}$ ), with  $V_{CC} > 3 \text{ V}$ . This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. When the SD is set low, gate driver outputs are forced low and assure low impedance.

### 3 Truth table

Table 3. Truth table

Input			Output	
$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
L	X <sup>(1)</sup>	X <sup>(1)</sup>	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

1. X: don't care.

## 4 Electrical data

### 4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings<sup>(1)</sup>

Symbol	Parameter	Value		Unit
		Min.	Max.	
V <sub>CC</sub>	Supply voltage	-0.3	21	V
V <sub>PGND</sub>	Low-side driver ground	V <sub>CC</sub> - 21	V <sub>CC</sub> + 0.3	V
V <sub>out</sub>	Output voltage	V <sub>boot</sub> - 21	V <sub>boot</sub> + 0.3	V
V <sub>boot</sub>	Bootstrap voltage	-0.3	620	V
V <sub>hvg</sub>	High-side gate output voltage	V <sub>out</sub> - 0.3	V <sub>boot</sub> + 0.3	V
V <sub>lvg</sub>	Low-side gate output voltage	PGND - 0.3	V <sub>CC</sub> + 0.3	V
V <sub>cp-</sub>	Comparator negative input voltage <sup>(2)</sup>	-0.3	5.5	V
V <sub>cp+</sub>	Comparator positive input voltage <sup>(2)</sup>	-0.3	5.5	V
V <sub>i</sub>	Logic input voltage	-0.3	15	V
V <sub>OD</sub>	Open-drain voltage	-0.3	15	V
dv <sub>out</sub> / dt	Allowed output slew rate		50	V/ns
P <sub>tot</sub>	Total power dissipation (T <sub>A</sub> = 25 °C)		1.0	W
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

1. Each voltage referred to SGND unless otherwise specified.

2. Spikes up to 20 V can be tolerated if the duration is shorter than 50 ns (f<sub>SW</sub> = 120 kHz).

### 4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-14	Unit
R <sub>th(JA)</sub>	Thermal resistance junction to ambient	120	°C/W

### 4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Min.	Max.	Unit
V <sub>CC</sub>	4	Supply voltage		10	20	V
V <sub>PS</sub> <sup>(1)</sup>	7 - 6	Low-side driver ground		-1.5	+1.5	V
V <sub>BO</sub> <sup>(2)</sup>	14 - 12	Floating supply voltage		9.3	20	V
V <sub>out</sub>	12	DC output voltage		- 9 <sup>(3)</sup>	580	V
V <sub>CP-</sub>	9	Comparator negative input pin voltage	V <sub>CP+</sub> ≤ 2.5 V		5 <sup>(4)</sup>	V
V <sub>CP+</sub>	10	Comparator positive input pin voltage	V <sub>CP-</sub> ≤ 2.5 V		5 <sup>(4)</sup>	V
f <sub>sw</sub>		Switching frequency	HVG, LVG load C <sub>L</sub> = 1 nF		800	kHz
T <sub>J</sub>		Junction temperature		-40	125	°C

1. V<sub>PS</sub> = V<sub>PGND</sub> - SGND.

2. V<sub>BO</sub> = V<sub>boot</sub> - V<sub>out</sub>.

3. LVG off. V<sub>CC</sub> = 12.5 V. Logic is operational if V<sub>boot</sub> > 5 V.

4. At least one of the comparator's inputs must be lower than 2.5 V to guarantee proper operation.

## 5 Electrical characteristics

### 5.1 AC operation

Table 7. AC operation electrical characteristics (VCC = 15 V; PGND = SGND; T<sub>J</sub> = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>on</sub>	1 vs. 8	High/low-side driver turn-on propagation delay	OUT = 0 V BOOT = VCC C <sub>L</sub> = 1 nF V <sub>i</sub> = 0 to 3.3 V see <a href="#">Figure 3</a>		85	120	ns
t <sub>off</sub>	3 vs. 13	High/low-side driver turn-off propagation delay			85	120	ns
t <sub>sd</sub>	2 vs. 8, 13	Shutdown to high/low-side driver propagation delay			85	120	ns
t <sub>isd</sub>		Comparator triggering to high/low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+; CP- = 0.5 V		175	220	ns
MT		Delay matching, HS and LS turn-on/off <sup>(1)</sup>				30	ns
DT	5	Deadtime setting range see <a href="#">Figure 4</a>	R <sub>DT</sub> = 0 Ω, C <sub>L</sub> = 1 nF	0.12	0.18	0.24	μs
			R <sub>DT</sub> = 100 kΩ, C <sub>L</sub> = 1 nF, C <sub>DT</sub> = 100 nF	1.2	1.4	1.6	μs
			R <sub>DT</sub> = 200 kΩ, C <sub>L</sub> = 1 nF, C <sub>DT</sub> = 100 nF	2.2	2.6	3	μs
MDT		Matching deadtime <sup>(2)</sup>	R <sub>DT</sub> = 0 Ω, C <sub>L</sub> = 1 nF			50	ns
			R <sub>DT</sub> = 100 kΩ, C <sub>L</sub> = 1 nF, C <sub>DT</sub> = 100 nF			165	ns
			R <sub>DT</sub> = 200 kΩ, C <sub>L</sub> = 1 nF, C <sub>DT</sub> = 100 nF			260	ns
t <sub>r</sub>	8, 13	Rise time	C <sub>L</sub> = 1 nF		15	40	ns
t <sub>f</sub>		Fall time	C <sub>L</sub> = 1 nF		15	40	ns

1. MT = max. (|t<sub>on(LVG)</sub> - t<sub>off(LVG)</sub>|, |t<sub>on(HVG)</sub> - t<sub>off(HVG)</sub>|, |t<sub>off(LVG)</sub> - t<sub>on(HVG)</sub>|, |t<sub>off(HVG)</sub> - t<sub>on(LVG)</sub>|).

2. MDT = |DT<sub>LH</sub> - DT<sub>HL</sub>| (see [Figure 5 on page 14](#)).



Figure 3. Timing

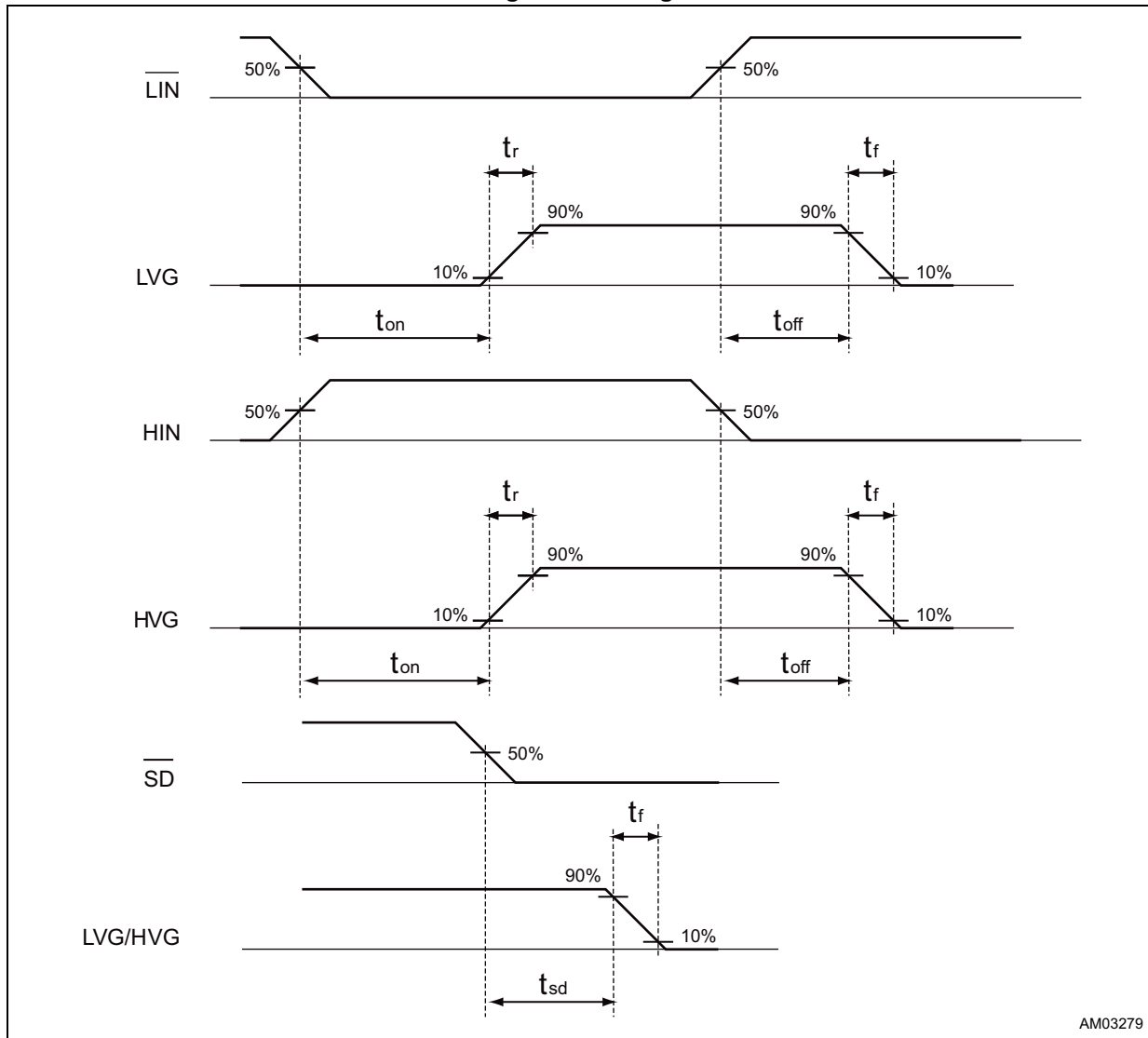
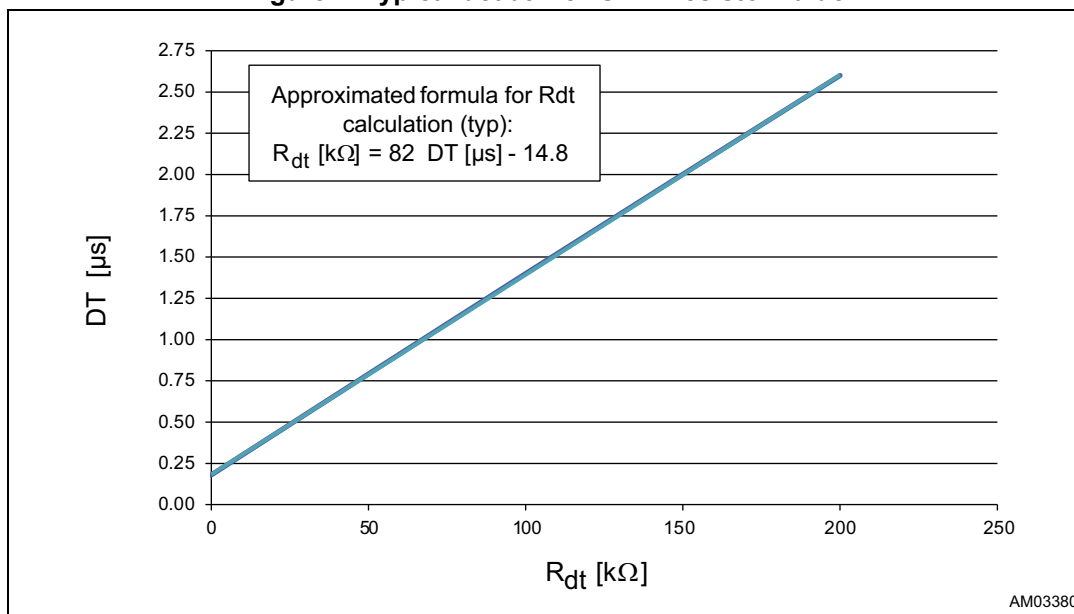


Figure 4. Typical deadtime vs. DT resistor value



## 5.2 DC operation

**Table 8. DC operation electrical characteristics**  
(VCC = 15 V; PGND = SGND; T<sub>J</sub> = + 25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC_hys</sub>	4	VCC UV hysteresis		0.5	0.6	0.72	V
V <sub>CC_thON</sub>		VCC UV turn-ON threshold		8.7	9.3	9.8	V
V <sub>CC_thOFF</sub>		VCC UV turn-OFF threshold		8.2	8.7	9.2	V
I <sub>qccu</sub>		Undervoltage quiescent supply current	VCC = 8 V SD = 5 V; LIN = 5 V; HIN = SGND; R <sub>DT</sub> = 0 Ω; CP+ = SGND; CP- = 5 V		160	210	μA
I <sub>qcc</sub>		Quiescent current	VCC = 15 V SD = 5 V; LIN = 5 V; HIN = SGND; R <sub>DT</sub> = 0 Ω; CP+ = SGND; CP- = 5 V		540	700	μA
<b>Bootstrapped supply voltage section<sup>(1)</sup></b>							
V <sub>BO_hys</sub>	14-12	V <sub>BO</sub> UV hysteresis		0.48	0.6	0.7	V
V <sub>BO_thON</sub>		V <sub>BO</sub> UV turn-ON threshold		8	8.6	9.1	V
V <sub>BO_thOFF</sub>		V <sub>BO</sub> UV turn-OFF threshold		7.5	8.0	8.5	V
I <sub>QBOU</sub>		Undervoltage V <sub>BO</sub> quiescent current	VCC = V <sub>BO</sub> = 7 V SD = 5 V; LIN and HIN = 5 V; R <sub>DT</sub> = 0 Ω; CP+ = SGND; CP- = 5 V		20	30	μA
I <sub>QBO</sub>		V <sub>BO</sub> quiescent current	V <sub>BO</sub> = 15 V SD = 5 V; LIN and HIN = 5 V; R <sub>DT</sub> = 0 Ω; CP+ = SGND; CP- = 5 V		90	120	μA
I <sub>LK</sub>		High voltage leakage current	BOOT = HVG = OUT = 600 V			8	μA
R <sub>DS(on)</sub>		Bootstrap driver on resistance <sup>(2)</sup>			175		Ω

**Table 8. DC operation electrical characteristics  
(VCC = 15 V; PGND = SGND; T<sub>J</sub> = + 25 °C) (continued)**

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Driving buffer section</b>							
I <sub>so</sub>	8, 13	High/low-side source peak current	LVG/HVG ON T <sub>J</sub> = 25 °C	3.5	4		A
			Full temperature range	2.5			A
I <sub>si</sub>		High/low-side sink peak current	LVG/HVG OFF T <sub>J</sub> = 25 °C	3.5	4		A
			Full temperature range	2.5			A
<b>Logic inputs</b>							
V <sub>il</sub>	1, 2, 3	Low level logic threshold		0.95		1.45	V
V <sub>ih</sub>		High level logic threshold voltage		2		2.5	V
V <sub>SSD</sub>	2	SmartSD unlatch threshold				0.8	V
V <sub>il_s</sub>	1, 3	Single input voltage	$\overline{\text{LIN}}$ and HIN connected together and floating			0.8	V
I <sub>HINh</sub>	3	HIN logic "1" input bias current	HIN = 15 V	120	200	260	μA
I <sub>HINl</sub>		HIN logic "0" input bias current	HIN = 0 V			1	μA
I <sub>LINl</sub>	1	$\overline{\text{LIN}}$ logic "0" input bias current	$\overline{\text{LIN}}$ = 0 V	5	10	15	μA
I <sub>LINh</sub>		$\overline{\text{LIN}}$ logic "1" input bias current	$\overline{\text{LIN}}$ = 15 V			1	μA
I <sub>SDh</sub>	2	$\overline{\text{SD}}$ logic "1" input bias current	$\overline{\text{SD}}$ = 15 V	20	40	60	μA
I <sub>SDl</sub>		$\overline{\text{SD}}$ logic "0" input bias current	$\overline{\text{SD}}$ = 0 V			1	μA

- V<sub>BO</sub> = V<sub>boot</sub> - V<sub>out</sub>.
- R<sub>DS(on)</sub> is tested in the following way:  
 $R_{DS(on)} = [(VCC - V_{BOOT1}) - (VCC - V_{BOOT2})] / [I_1(VCC, V_{BOOT1}) - I_2(VCC, V_{BOOT2})]$  where I<sub>1</sub> is pin 14 current when V<sub>BOOT</sub> = V<sub>BOOT1</sub>, I<sub>2</sub> when V<sub>BOOT</sub> = V<sub>BOOT2</sub>.

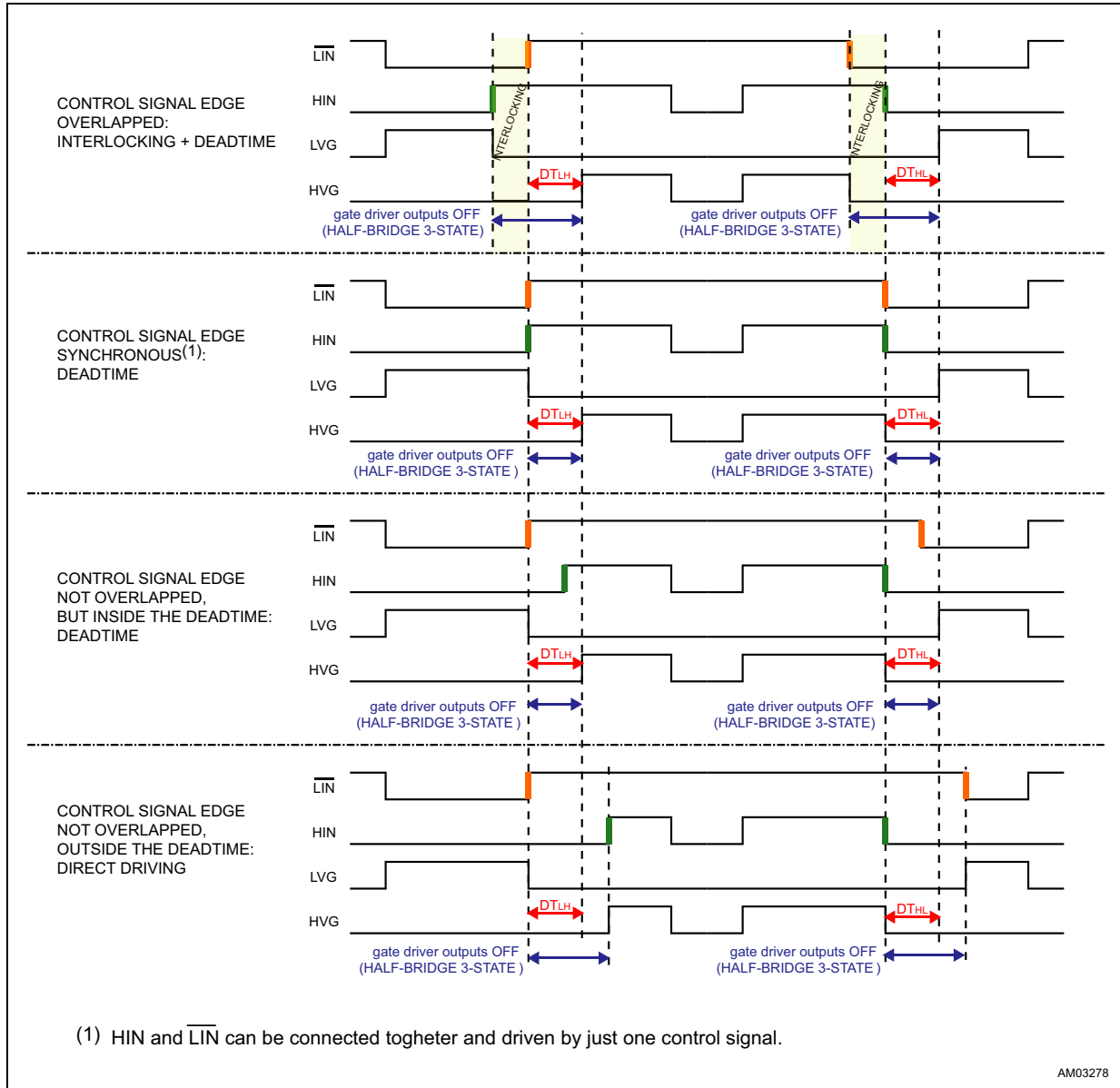
Table 9. Sense comparator<sup>(1)</sup> ( $V_{CC} = 15\text{ V}$ ,  $T_J = +25\text{ °C}$ )

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{io}$	9, 10	Input offset voltage		-15		15	mV
$I_{ib}$	9, 10	Input bias current	$V_{CP+} = 1\text{ V}$ , $V_{CP-} = 1\text{ V}$			1	$\mu\text{A}$
$I_{OD}$	2	Open-drain low level sink current	$SD\backslash OD = 400\text{ mV}$ , $V_{CP+} = 1\text{ V}$ ; $V_{CP-} = 0.5\text{ V}$ ;	13	20	27	mA
$t_{d\_comp}$		Comparator delay	$R_{pu} = 100\text{ k}\Omega$ to $5\text{ V}$ ; $V_{CP-} = 0.5\text{ V}$ ; voltage step on CP+ = 0 to 3.3 V; 50% CP+ to 90% SD		100	155	ns
SR	2	Slew rate	$C_L = 10\text{ nF}$ ; $R_{pu} = 5\text{ k}\Omega$ to $5\text{ V}$ ; 90% SD to 10% SD		10		$\text{V}/\mu\text{s}$

1. Comparator is disabled when VCC is in UVLO condition.

# 6 Waveform definitions

Figure 5. Deadtime and interlocking waveform definitions

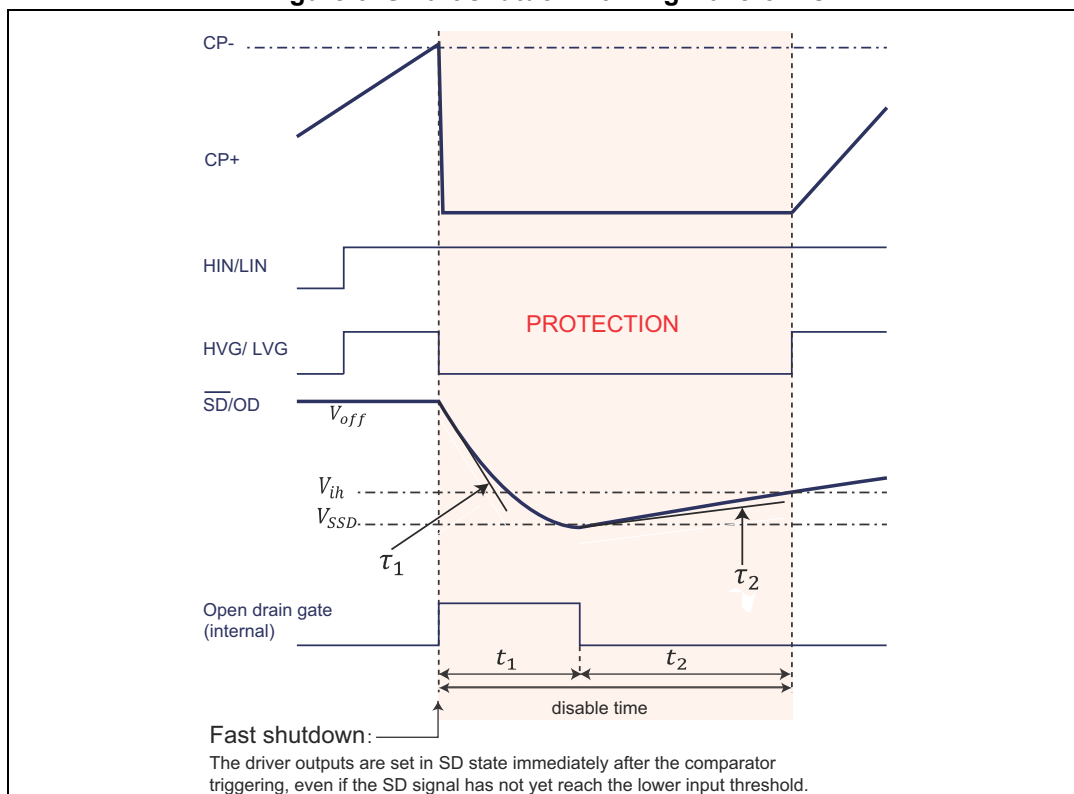


# 7 Smart shutdown function

The L6491 device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open-drain output available on pin 2, shared with the  $\overline{SD}$  input. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leaving the half-bridge in 3-state.

Figure 6. Smart shutdown timing waveforms



An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot \ln \left( \frac{V_{off} - V_{on}}{V_{SSD} - V_{on}} \right)$$

$$t_2 \cong \tau_2 \cdot \ln \left( \frac{V_{SSD} - V_{off}}{V_{ih} - V_{off}} \right)$$

where:

$$\tau_1 = (R_{ON\_OD} // R_{SD}) \cdot C_{SD}$$

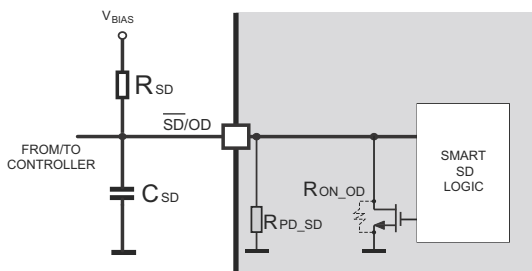
$$\tau_2 = (R_{PD\_SD} // R_{SD}) \cdot C_{SD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{SD}} \cdot V_{BIAS}$$

AM03334

### SHUT DOWN CIRCUIT



In common overcurrent protection architectures, the comparator output is usually connected to the  $\overline{SD}$  input and an RC network is connected to this  $\overline{SD}/OD$  line in order to provide a monostable circuit, which implements a protection time following the fault condition. Differently from the common fault detection systems, the L6491 smart shutdown architecture allows immediate turn-off of the output gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the current output switch-off. In fact the time delay between the fault and the output turn-off is no longer dependent on the RC value of the external network connected to the  $\overline{SD}/OD$  pin. In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time, the internal logic turns on the open-drain output and holds it on until the  $\overline{SD}$  voltage goes below the smartSD unlatch threshold  $V_{SSD}$ . When such threshold is reached, the open-drain output is turned off, allowing the external pull-up to recharge the capacitor. The driver outputs restart following the input pins as soon as the voltage at the  $\overline{SD}/OD$  pin reaches the higher threshold of the  $\overline{SD}$  logic input. The smart shutdown system gives the possibility to increase the time constant of the external RC network (that determines the disable time after the fault event) up to very large values without increasing the delay time of the protection.

Any external signal provided to the  $\overline{SD}$  pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the  $\overline{SD}$  input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.



# 8 Typical application diagram

Figure 7. Typical application diagram

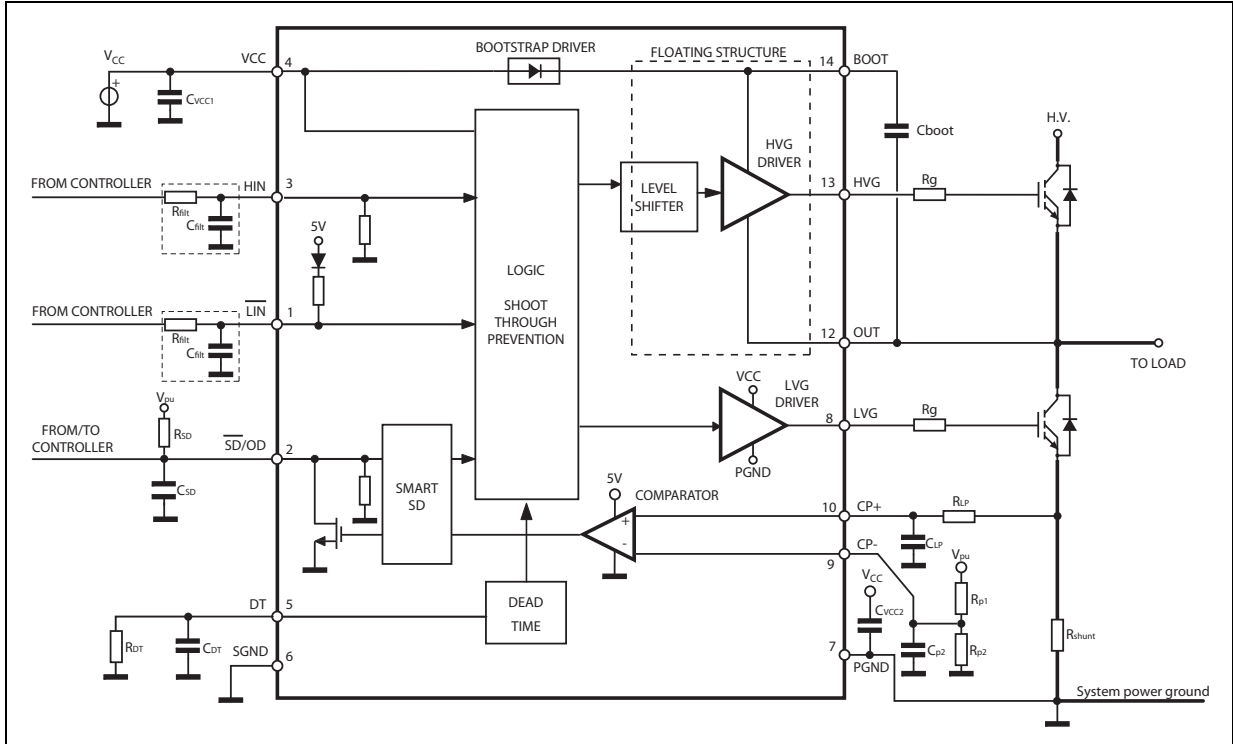
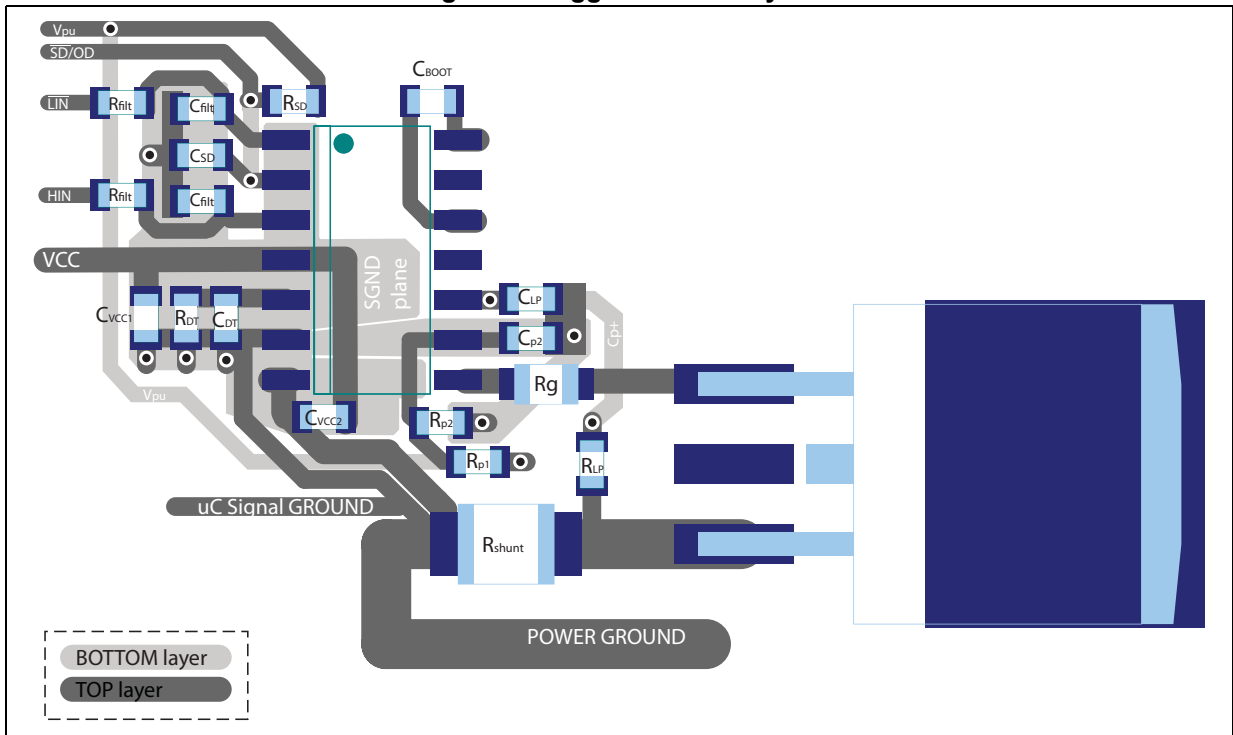


Figure 8. Suggested PCB layout



## 9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode (*Figure 9*). In the L6491 an integrated structure replaces the external diode.

### $C_{BOOT}$ selection and charging

To choose the proper  $C_{BOOT}$  value the external MOS can be seen as an equivalent capacitor. This capacitor  $C_{EXT}$  is related to the MOS total gate charge:

#### Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors  $C_{EXT}$  and  $C_{BOOT}$  is proportional to the cyclical voltage loss. It has to be:

#### Equation 2

$$C_{BOOT} \gg \gg C_{EXT}$$

if  $Q_{gate}$  is 30 nC and  $V_{gate}$  is 10 V,  $C_{EXT}$  is 3 nF. With  $C_{BOOT} = 100$  nF the drop is 300 mV.

If HVG has to be supplied for a long time, the  $C_{BOOT}$  selection has also to take into account the leakage and quiescent losses.

HVG steady-state consumption is lower than 120  $\mu$ A, so if HVG  $T_{ON}$  is 5 ms,  $C_{BOOT}$  has to supply  $C_{EXT}$  with 0.6  $\mu$ C. This charge on a 1  $\mu$ F capacitor means a voltage drop of 0.6 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if  $V_{OUT}$  is close to SGND (or lower) and in the meanwhile the LVG is on. The charging time ( $T_{charge}$ ) of the  $C_{BOOT}$  is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS  $R_{DS(on)}$  (typical value: 175  $\Omega$ ). At low frequency this drop can be neglected. Anyway, the rise of frequency has to take into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

#### Equation 3

$$V_{drop} = I_{charge} R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

where  $Q_{gate}$  is the gate charge of the external power MOS,  $R_{DS(on)}$  is the on resistance of the bootstrap DMOS and  $T_{charge}$  is the charging time of the bootstrap capacitor.

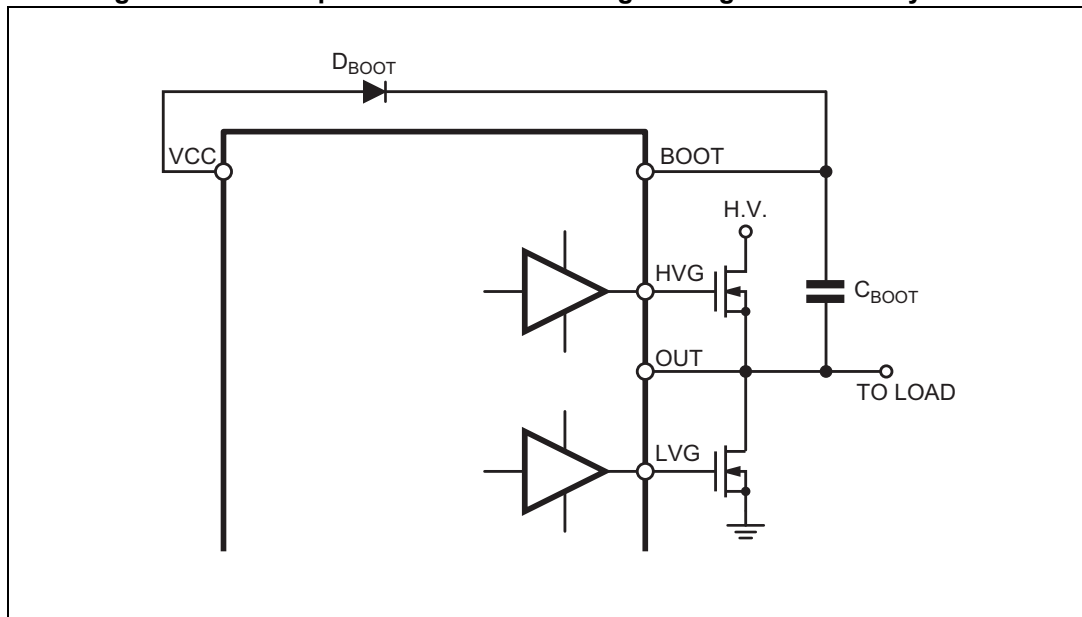
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the  $T_{\text{charge}}$  is 5  $\mu\text{s}$ . In fact:

**Equation 4**

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 175\Omega \sim 1\text{V}$$

$V_{\text{drop}}$  has to be taken into account when the voltage drop on  $C_{\text{BOOT}}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

**Figure 9. Bootstrap driver with external high voltage fast recovery diode**



## 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 10. SO-14 package outline

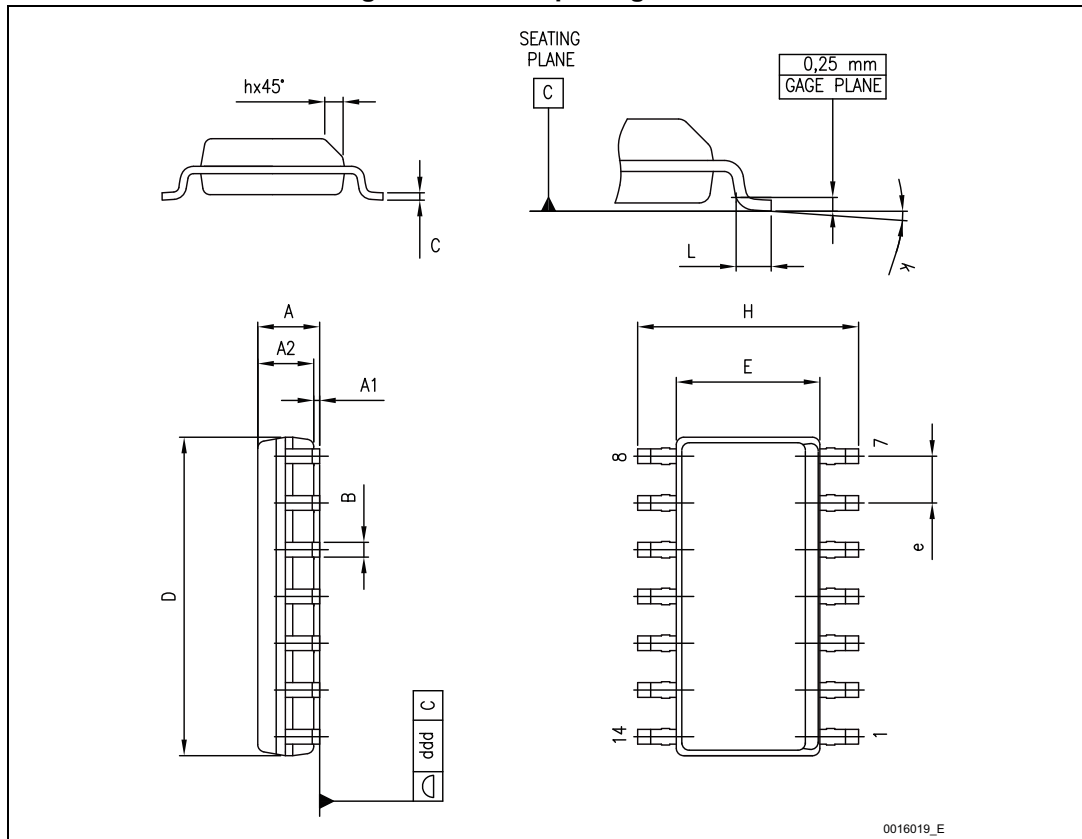
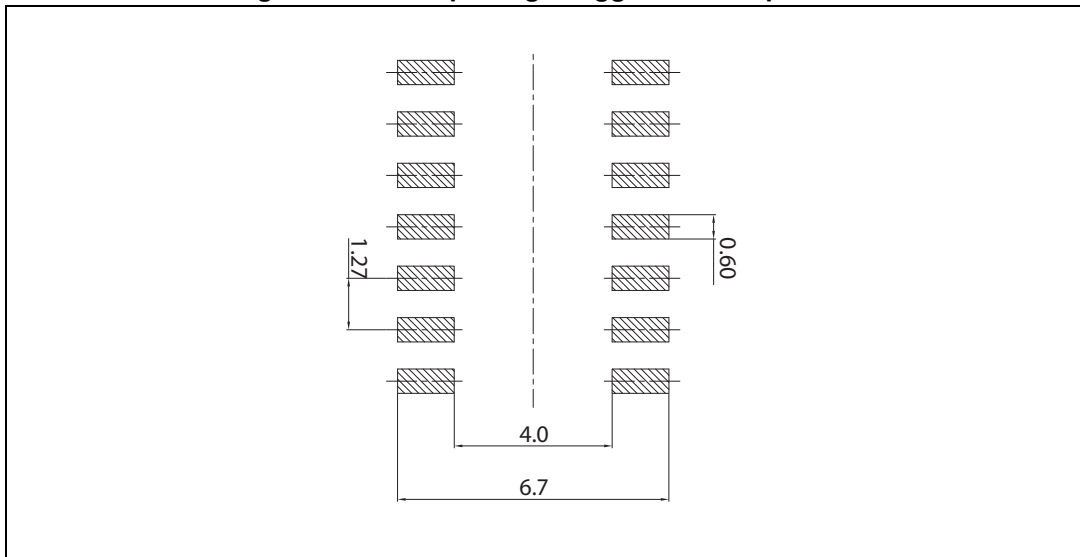


Table 10. SO-14 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	0		8
ddd			0.10

Figure 11. SO-14 package suggested land pattern



## 11 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
11-Mar-2015	1	Initial release.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved