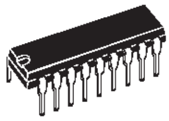
L4973V3.3 - L4973V5.1
L4973D3.3 - L4973D5.1

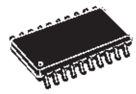
3.5A STEP DOWN SWITCHING REGULATOR

- UP TO 3.5A STEP DOWN CONVERTER
- OPERATING INPUT VOLTAGE FROM 8V TO 55V
- 3.3V AND 5.1V (±1%) FIXED OUTPUT, AND ADJUSTABLE OUTPUTS FROM:
  0V TO 50V (3.3V type)
  5.1V TO 50V (5.1 type)
- FREQUENCY ADJUSTABLE UP TO 300KHz
- VOLTAGE FEED FORWARD
- ZERO LOAD CURRENT OPERATION (min 1mA)
- INTERNAL CURRENT LIMITING (PULSE BY PULSE AND HICCUP MODE)
- PRECISE 5.1V (1.5%) REFERENCE VOLTAGE EXTERNALLY AVAILABLE
- INPUT/OUTPUT SYNCHRONIZATION FUNCTION
- INHIBIT FOR ZERO CURRENT CONSUMPTION (100µA Typ. at V_{CC} = 24V)
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN
- OUTPUT OVERVOLTAGE PROTECTION
- SOFT START FUNCTION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (12+3+3)



SO20(12+4+4)

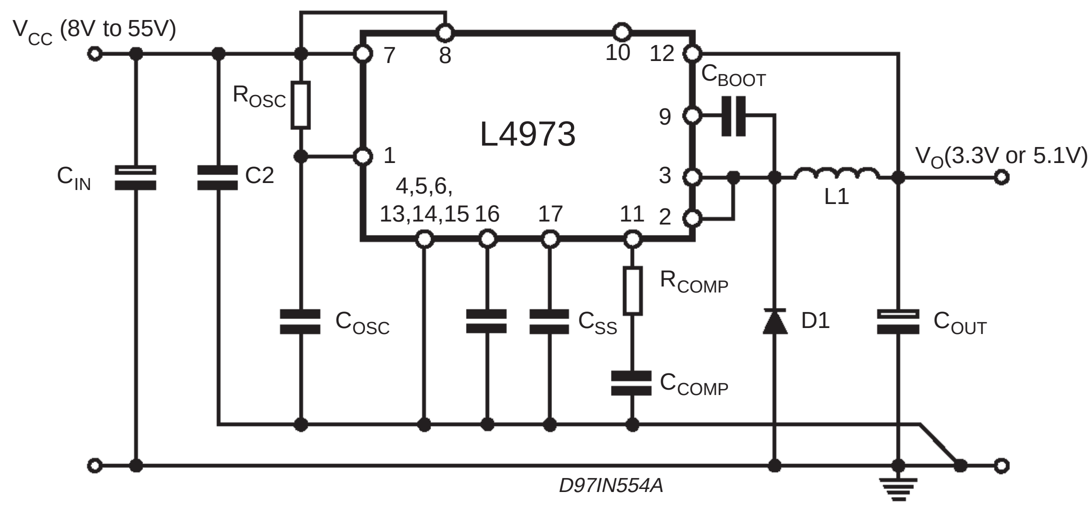
ORDERING NUMBERS:
L4973V3.3 (Powerdip)
L4973D3.3 (SO20)
L4973V5.1 (Powerdip)
L4973D5.1 (SO20)

DESCRIPTION

The L4973 is a step down monolithic power switching regulator delivering 3.5A at fixed voltages of 3.3V or 5.1V and using a simple external divider output adjustable voltage up to 50V.

Realized in BCD mixed technology, the device

TYPICAL APPLICATION CIRCUIT (POWERDIP)



uses an internal power D-MOS transistor (with a typical Rdson of 0.15ohm) to obtain very high efficiency and very fast switching times.

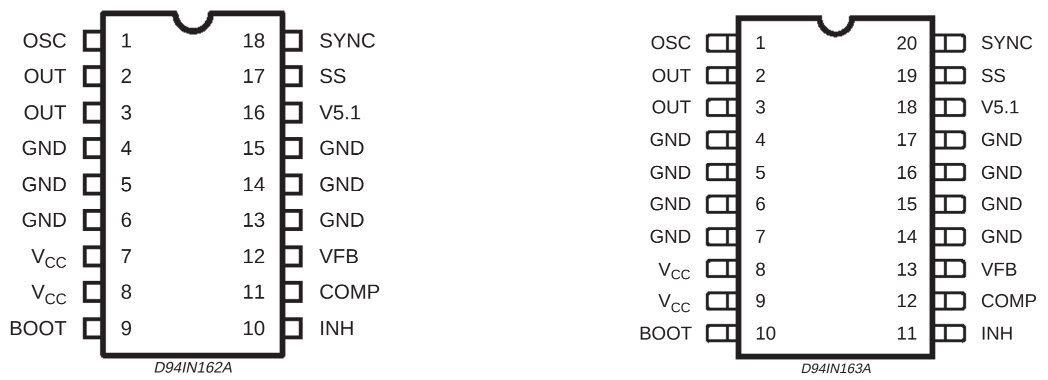
Switching frequency up to 300KHz are achievable (the maximum power dissipation of the packages must be observed).

A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 40V cover the majority of the today applications.

Features of this new generation of DC-DC converter includes pulse by pulse current limit, hiccup mode for output short circuit protection, voltage feed forward regulation, soft start, input/output synchronization, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown.

Packages available are in plastic dual in line, DIP-18 (12+3+3) for standard assembly, and SO20 (12+4+4) for SMD assembly.

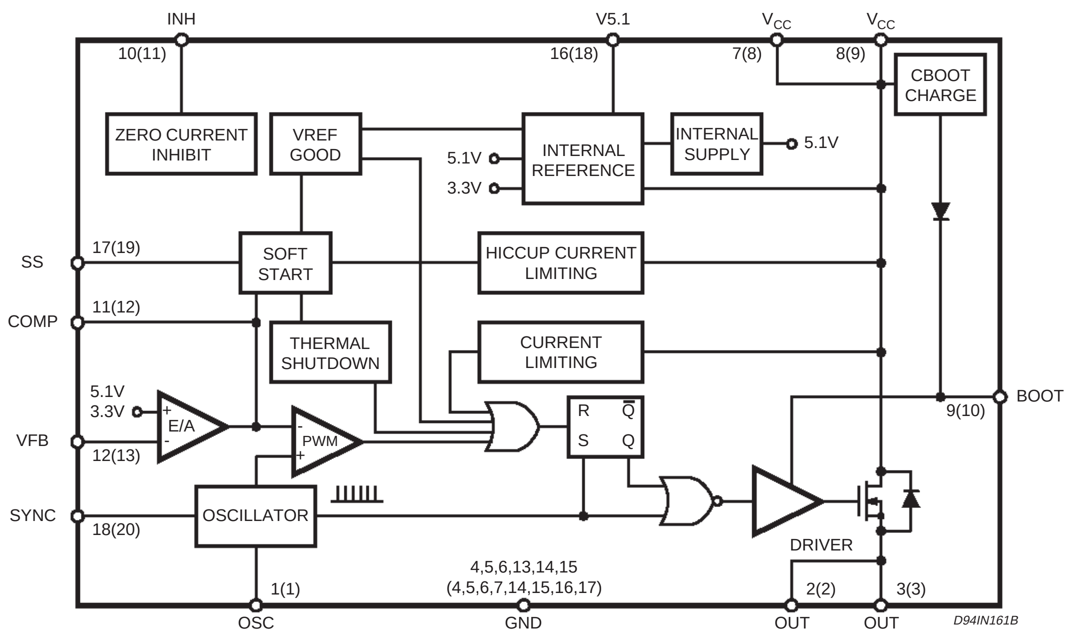
PIN CONNECTIONS (Top view)



POWERDIP (12+3+3)

SO20 (12+4+4)

BLOCK DIAGRAM



Pin x = Powerdip
Pin (x) = S020

THERMAL DATA

Symbol	Parameter		Powerdip	SO20	Unit
$R_{th(j\text{-}pin)}$	Thermal Resistance Junction to pin	Max.	12	15	°C/W
$R_{th(j\text{-}amb)}$	Thermal Resistance to Ambient	Max.	60 (*)	80 (*)	°C/W

(*) Package mounted on board.

ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter		Value	Unit
DIP-18	S0-20				
V_7,V_8	V_9,V_8	Input voltage		58	V
V_2,V_3	V_2,V_3	Output DC voltage Output peak voltage at t = 0.1µs f=200KHz		-1 -5	V V
I_2,I_3	I_2,I_3	Maximum output current		int. limit.	
V_9-V_8	V_{10}-V_8			14	V
V_9	V_{10}	Bootstrap voltage		70	V
V_{11}	V_{12}	Analogs input voltage (V_{CC} = 24V)		12	V
V_{17}	V19	Analogs input voltage (V_{CC} = 24V)		13	V
V_{12}	V_{13}	(V_{CC} = 20V)		6 -0.3	V V
V_{18}	V_{20}	(V_{CC} = 20V)		5.5 -0.3	V V
V_{10}	V_{11}	Inhibit		Vcc -0.3	V V
P_{tot}		Power dissipation a T_{pins} ≤ 90°C (T_{amb} = 70°C no copper area) (T_{amb} = 70°C 4cm copper area on PCB)	DIP 12+3+3	5 1.3 2	W W W
		Power dissipation a T_{pins} = 90°C	SO20	4	W
T_J,T_{STG}		Junction and storage temperature		-40 to 150	°C

PIN FUNCTIONS

Powerdip	SO20	NAME	DESCRIPTION
11	12	COMP	E/A output to be used for frequency compensation
10	11	INH	A logic signal (active high) disables the device (sleep mode operation). If not used it must be connected to GND; if floating the device is disabled.
9	10	BOOT	A capacitor connected between this pin and the output allows to drive the internal D-MOS.
18	20	SYNC	Input/Output synchronization.
7,8	8,9	Vcc	Unregulated DC input voltage
2,3	2,3	OUT	Stepdown regulator output.
12	13	VFB	Stepdown feedback input. Connecting the output directly to this pin results in an output voltage of 3.3V for the L4973V3.3 and 5.1V. An external resistive divider is required for higher output voltages. For output voltage less than 3.3V, see note ** and Figure 32.
16	18	V5.1	Reference voltage externally available.
4,5,6 13,14,15	4,5,6,7 14,15,16,17	GND	Signal ground
1	1	OSC	An external resistor connected between the unregulated input voltage and Pin 1 and a capacitor connected from Pin 1 to ground fixes the switching frequency. (Line feed forward is automatically obtained)

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_{CC} = 24V; T_j = 25°C, C_{OSC} = 2.7nF; R_{OSC} = 20KΩ; unless otherwise specified) ● = specifications referred to T_J from 0 to 125°C.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
	Input Voltage Range (*)	V_O = V_{REF} to 40V; I_O = 3.5A	●	8		55	V
	Output Voltage L4973V5.1	I_O = 1A		5.05	5.1	5.15	V
		I_O = 0.5A to 3.5A		5.00	5.1	5.20	V
		V_{CC} = 8V to 55V	●	4.95	5.1	5.25	V
	Output Voltage L4973V3.3	I_O = 1A		3.326	3.36	3.393	V
		I_O = 0.5A to 3.5A		3.292	3.36	3.427	V
		V_{CC} = 8V to 40V	●	3.26	3.36	3.46	V
	R_{DSON}	V_{CC} = 10.5V			0.15	0.22	Ω
		I_O = 3.5A	●			0.35	Ω
	Maximum Limiting Current	V_{CC} = 8V to 55V	●	4	4.5	5.5	A
η	Efficiency	V_O = 5.1V; I_O = 3.5A			90		%
		V_O = 3.3V; I_O = 3.5A			85		%
	Switching Frequency		●	90	100	110	KHz
	Supply Voltage Ripple Rejection	V_i = V_{CC} +2V_{RMS} V_O = V_{ref}; I_O = 1A; f_{ripple} = 100Hz		60			dB
Δf_{sw}	Switching Frequency Stability vs, Supply Voltage	V_{CC} = 8V to 55V			2	5	%
REFERENCE SECTION							
	Reference Voltage			5.025	5.1	5.175	V
		I_{ref} = 0 to 20mA; V_{CC} = 8 to 55V	●	4.950	5.1	5.250	V
	Line Regulation	I_{ref} = 0mA; V_{CC} = 8 to 55V			5	10	mV
	Load Regulation	V_{ref} = 0 to 5mA; V_{CC} = 0 to 20mA			2 6	10 25	mV mV
	Short Circuit Current			30	65	100	mA
SOFT START							
	Soft Start Charge Current			30	45	60	µA
	Soft Start Discharge Current			15	22	30	µA
INHIBIT							
	High Level Voltage		●	3.0			V
	Low Level Voltage		●			0.8	V
	I_{source} High Level	V_{INH} = 3V	●	10	16	50	µA
	I_{source} Low Level	V_{INH} = 0.8V	●	10	15	50	µA
DC CHARACTERISTICS							
	Total Operating Quiescent Current	Duty Cycle = 50%			4	6	mA
	Quiescent Current	Duty Cycle = 0			2.7	4	mA
	Total stand-by quiescent current	V_{CC} = 24V; V_{INH} = 5V			100	200	µA
		V_{CC} = 55V; V_{INH} = 5V			150	300	µA
ERROR AMPLIFIER							
	High Level Output Voltage			11.0			V
	Low Level Output Voltage					0.65	V
	Source Bias Current			1	2	3	µA
	Source Output Current			200	300	600	µA

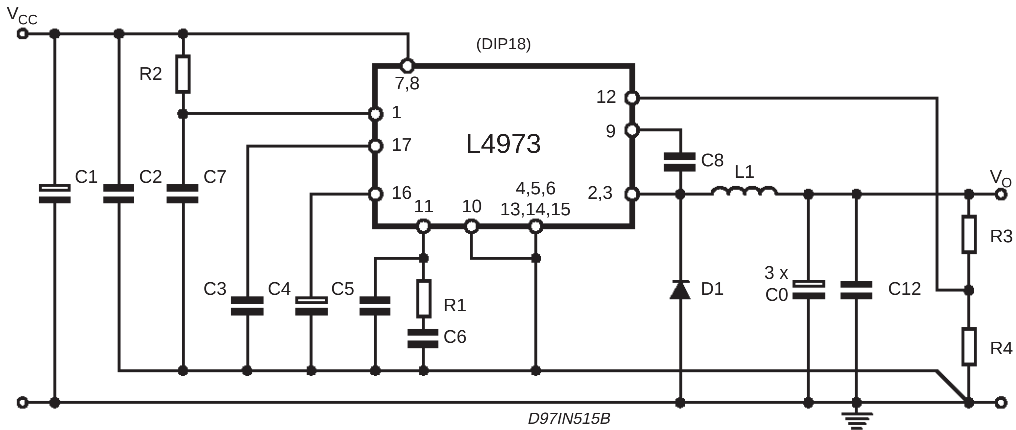
ELECTRICAL CHARACTERISTICS (continued)

	Sink Output Current			200	300		µA
	Supply Voltage Ripple Rejection	V_{COMP} = VFB C_{REF} =4.7µF 1-5mA load current		60	80		dB
	DC Open Loop Gain	$R_L = \infty$		50	60		dB
	Transconductance	I_{comp} = -0.1 to 0.1mA; V_{comp} = 6V			2.5		mS
OSCILLATOR SECTION							
	Ramp valley			0.78	0.85	0.92	V
	Ramp peak	V_{CC} = 8V		1.9	2.1	2.3	V
		V_{CC} = 55V		9	9.6	10.2	V
	Maximum Duty Cycle			95	97		%
	Maximum Frequency	Duty Cycle = 0%; R_{OSC} = 13KΩ; C_{OSC} = 820pF;				500	KHz
SYNC FUNCTION							
	High Input Voltage	V_{CC} = 8V to 55V		3.5			V
	Low Input Voltage	V_{CC} = 8V to 55V				0.9	V
	Slave Sink Current			0.15	0.25	0.45	mA
	Master Output Amplitude	I_{source} = 3mA		4	4.5		V
	Output Pulse Width	no load, V_{sync} = 4.5V		0.20	0.35		µs

(*) Pulse testing with a low duty cycle.

(**) The maximum power dissipation of the package must be observed.

Figure 1. Evaluation Board Circuit



C1=1000µF/63V
C2=220nF/63V
C3=470nF
C4=1µF/50V
C5=220pF
C6=22nF
C7=2.7nF
C8=220nF/63V
C0=100µF/40V(C9,C10,C11)
C12=Optional (220nF)
L1=150µH $K_{OOL\mu}$ 77310 - 40 Turns - 0.9mm
R1=9.1K
R2=20K
D1=GI SB560

L4973 V3.3

V_O(V)	R3(KΩ)	R4(KΩ)
3.3	0	
5.1	2.7	4.7
12	12	4.7
15	16	4.7
18	20	4.7
24	30	4.7

L4973 V5.1

V_O(V)	R3(KΩ)	R4(KΩ)
5.1	0	
12	6.2	4.7
15	9.1	4.7
18	12	4.7
24	18	4.7

Typical Performance (Using Evaluation Board) fsw = 100kHz

Output Voltage	Output Ripple	Efficiency	Line Regulator I_o = 3.5A V_{CC} = 8 to 50V	Load Regulator V_{CC} =35V I_O = 1 to 3.5A
3.3V	20mV	81.5 (%)	3mV	6mV
5.1V	20mV	86.7 (%)	3mV	6mV
12V	30mV	93.5 (%)	3mV (V_{CC} =15 to 50V)	4mV

Figure 1a: Evaluation Board (Components Side)

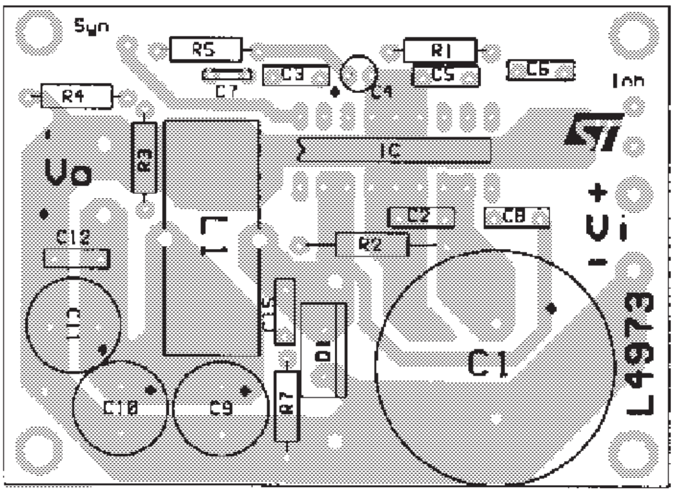


Figure 1b: Evaluation Board (Solder Side)

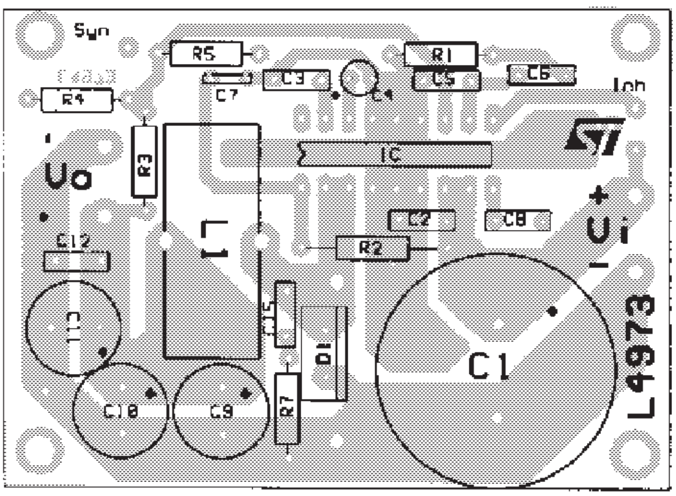


Figure 1c: Application Circuit (see fig. 1 part list)

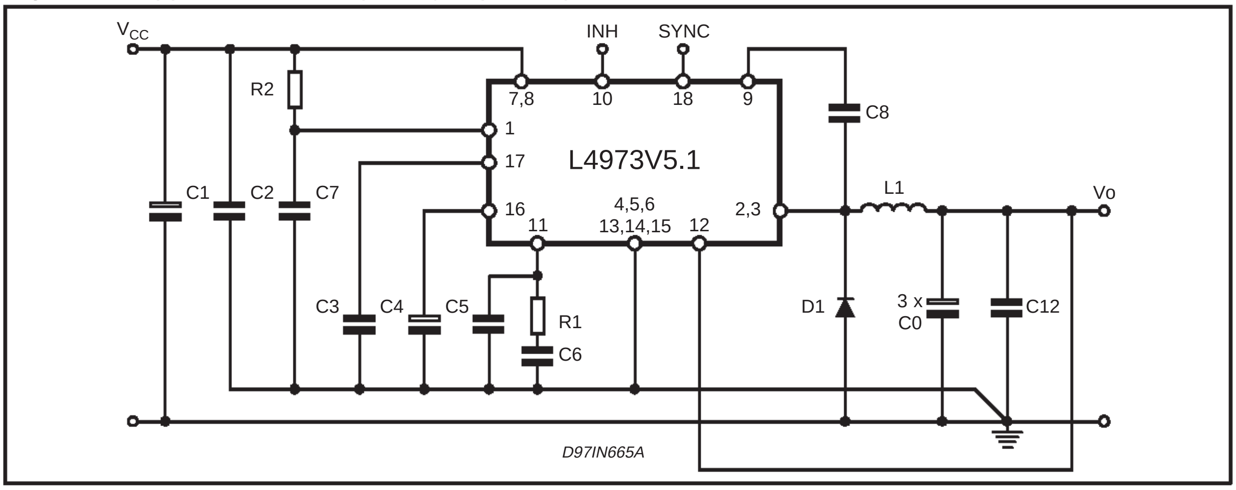


Figure 1d: Application Circuit (see fig. 1 part list)

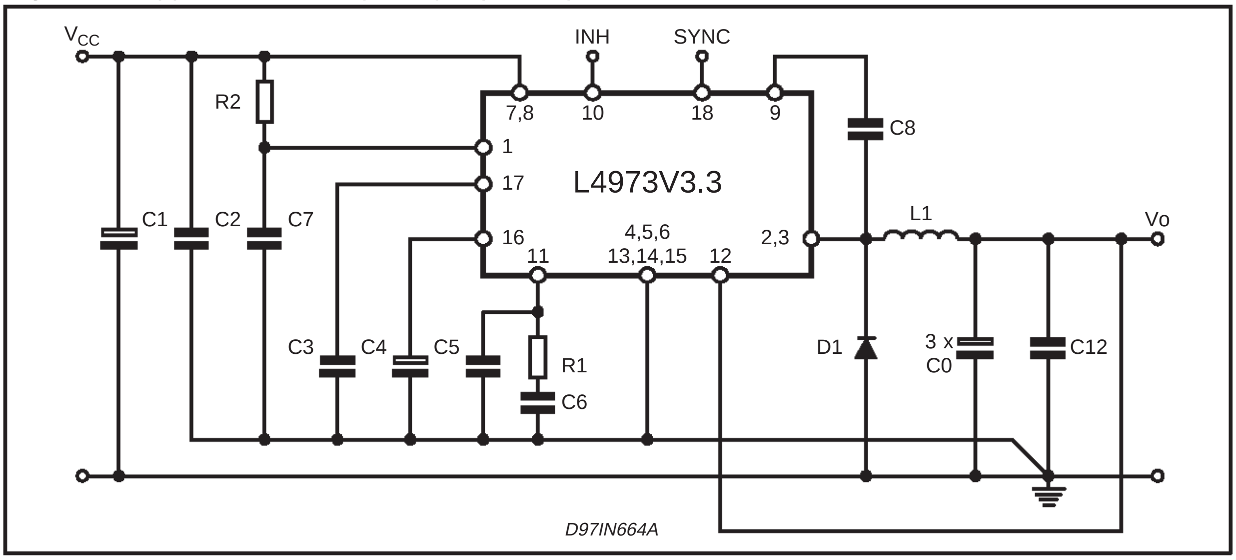


Figure 2: Quiescent Drain Current vs. Input Voltage (0% Duty Cycle)

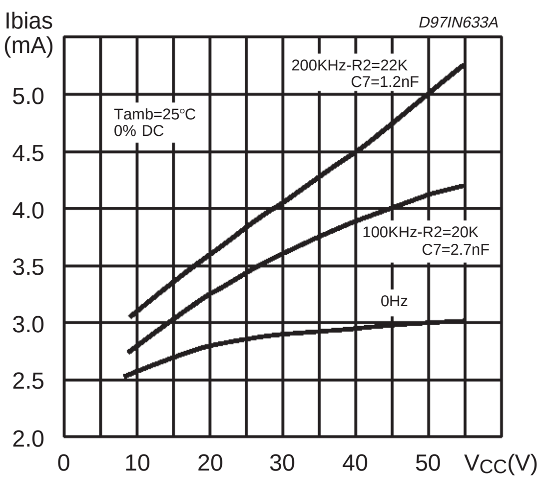


Figure 3: Quiescent Drain Current vs. Junction Temperature

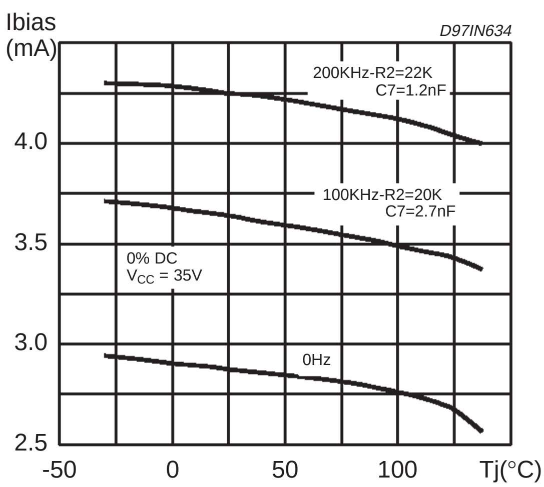


Figure 4: Stand by Drain Current vs. input Voltage

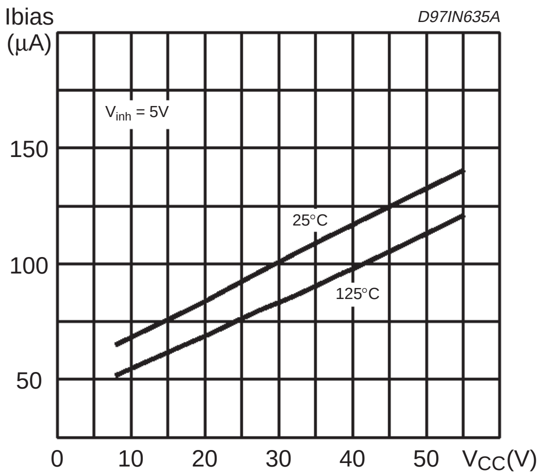


Figure 5: Reference Voltage vs. Junction Temperature (Pin 16)

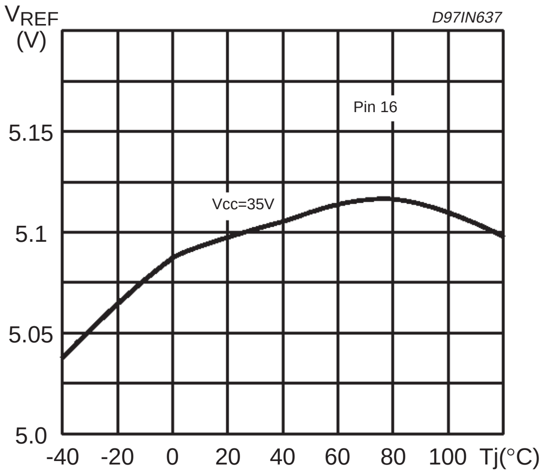


Figure 6: Reference Voltage vs. Input Voltage (Pin 16)

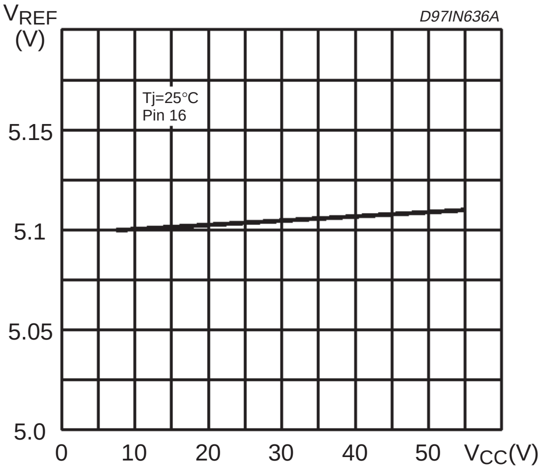


Figure 7: Reference Voltage vs. Reference Input Current

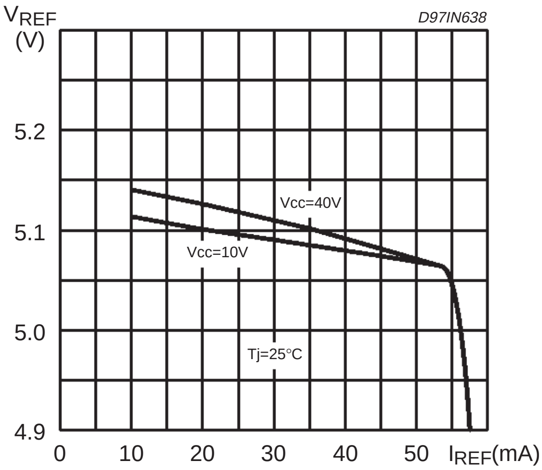


Figure 8: Inhibit Current vs. Inhibit Voltage (Pin 10)

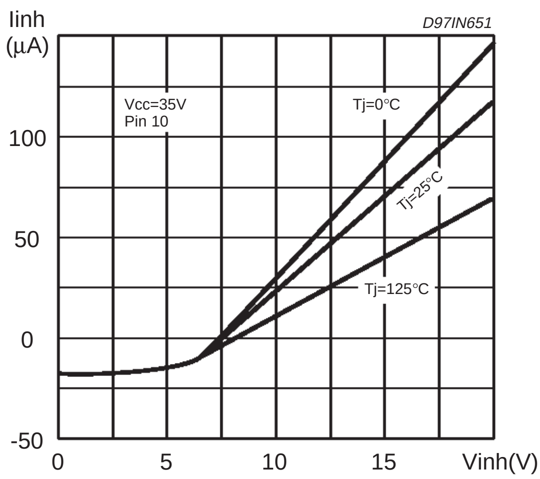


Figure 9: Line Regulation (see fig. 1)

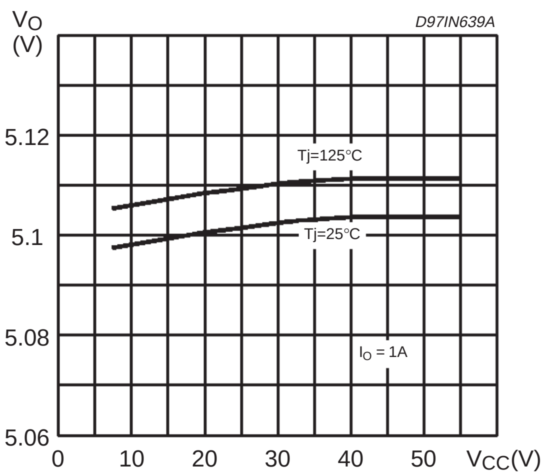


Figure 10: Load Regulation (see fig. 1c)

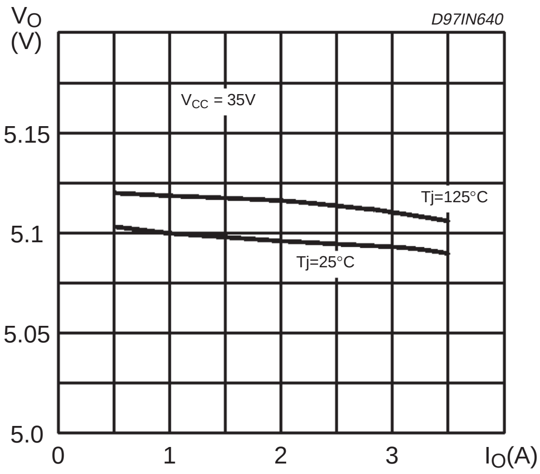


Figure 11: Line Regulation (see fig. 1d)

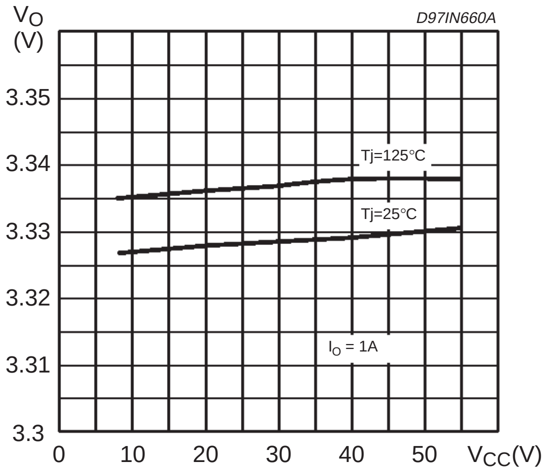


Figure 12: Load Regulation (see fig. 1d)

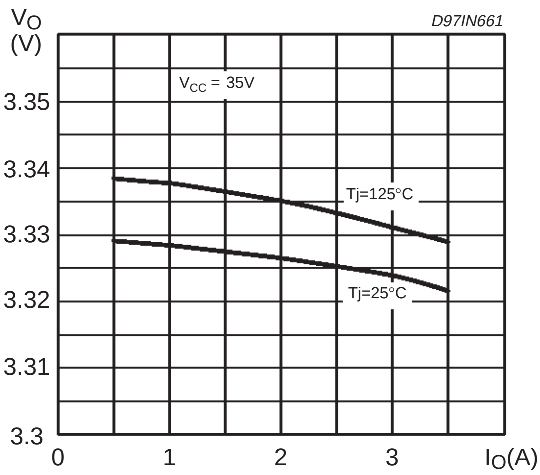


Figure 13: Switching Frequency vs.R2 and C7 (fig. 1)

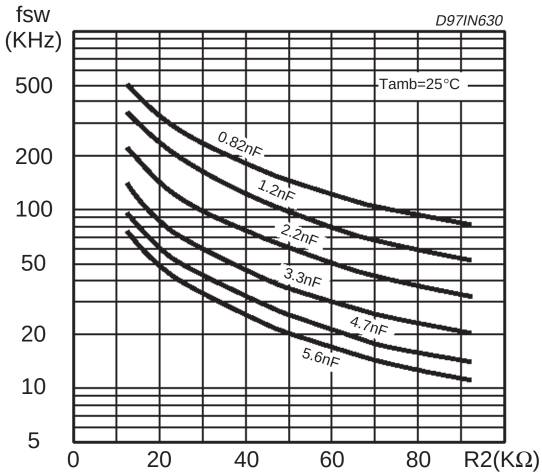


Figure 14: Switching Frequency vs. Input Voltage

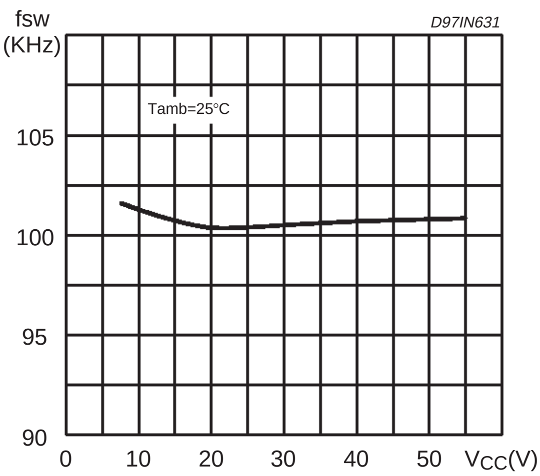


Figure 15: Switching Frequency vs. Junction temperature (see fig. 1)

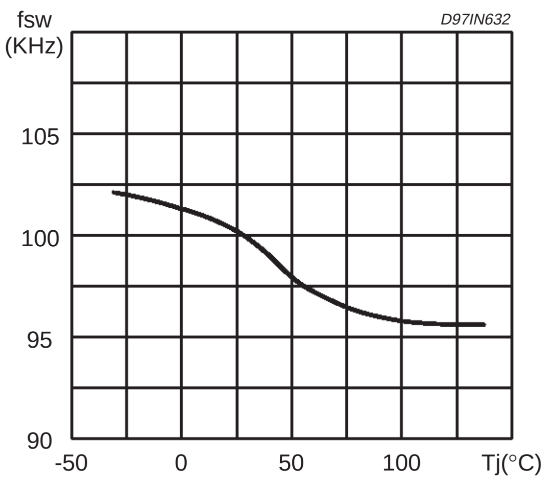


Figure 16: Dropout Voltage Between pin 7,8 and 2,3

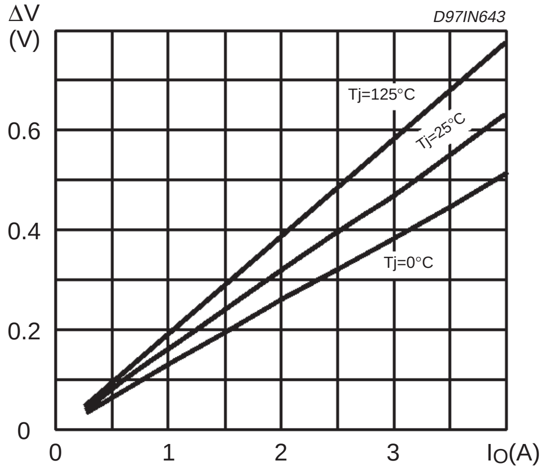


Figure 17: Efficiency vs. Output Voltage (see fig.1)

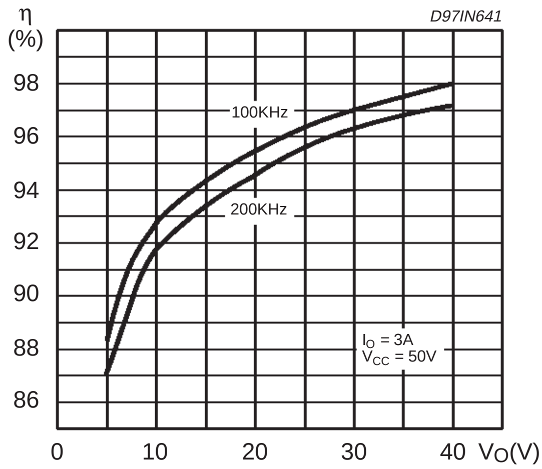


Figure 18: Efficiency vs. Output Voltage (Diode STPS745D)

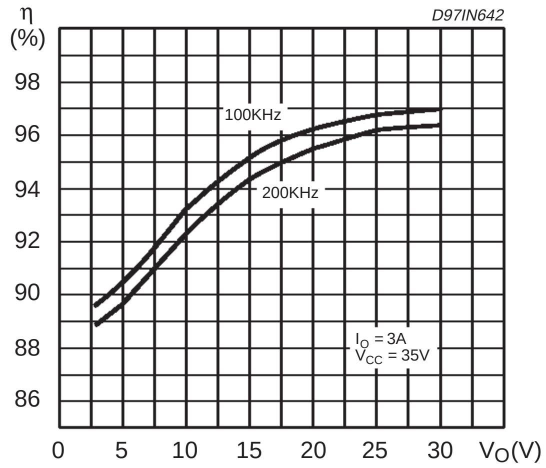


Figure 19: Efficiency vs. Output Current (see fig.1c)

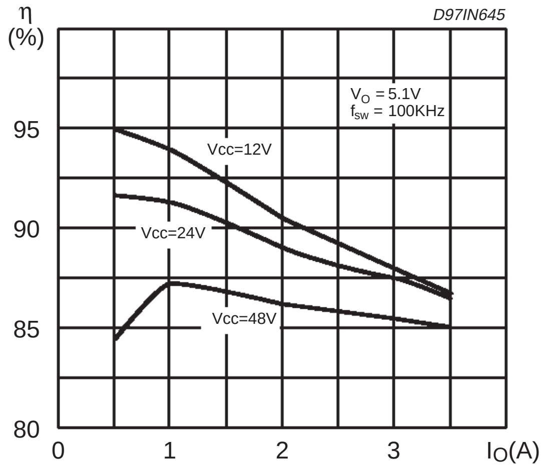


Figure 20: Efficiency vs. Output Current (see fig.1c)

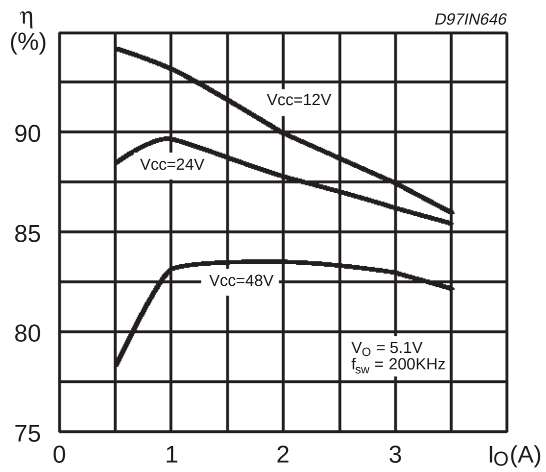


Figure 21: Efficiency vs. Output Current (see fig.1d)

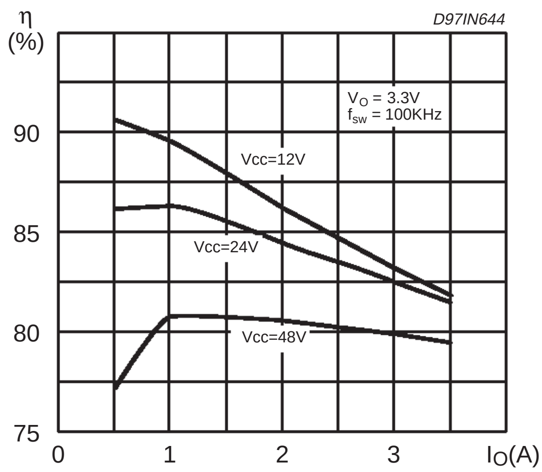


Figure 22: Efficiency vs. Output Current (see fig.1d)

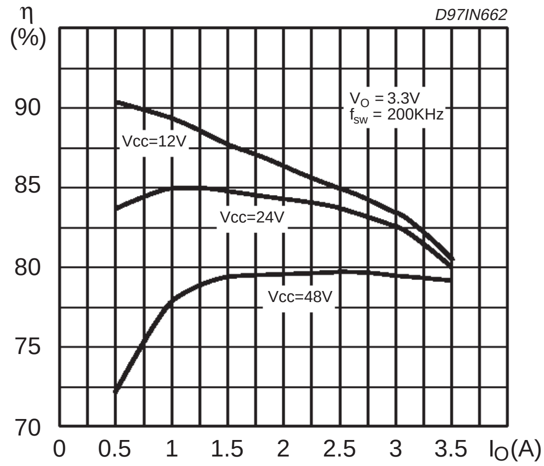


Figure 23: Power dissipation vs. Input Voltage (Device only) (see fig.1c)

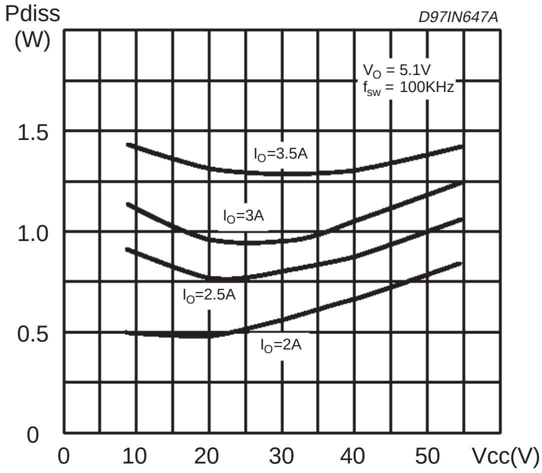


Figure 24: Power dissipation vs. Output Voltage (Device only)

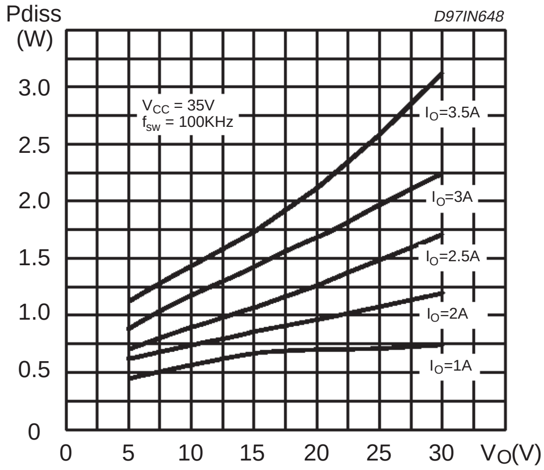


Figure 25: Pulse by Pulse Limiting Current vs. Junction Temperature

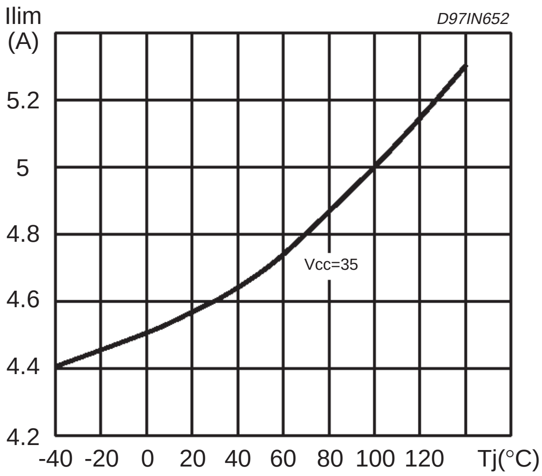


Figure 26: Load Transient

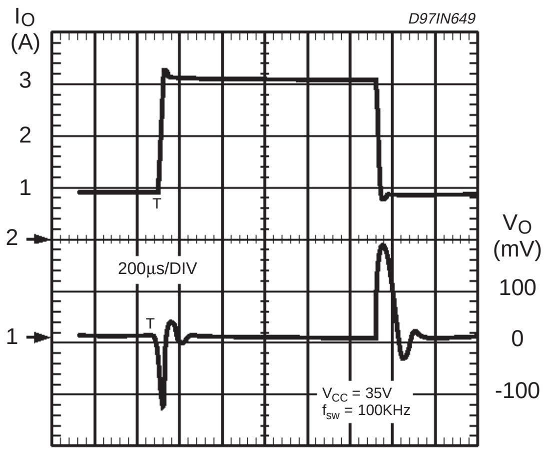


Figure 27: Line Transient

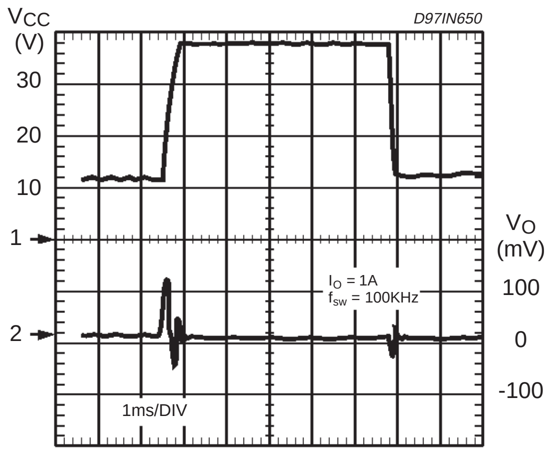


Figure 28: Source Current Rise and Fall Time, pin 2, 3 (See fig1)

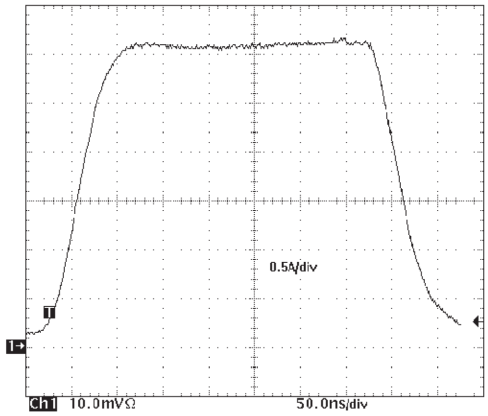


Figure 29: Soft Start Capacitor Selection vs. Inductor and VCC max (ref. AN938)

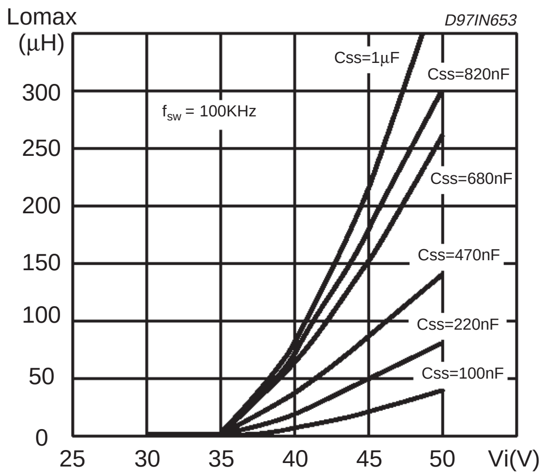


Figure 30: Soft Start Capacitor Selection vs. Inductor and VCC max (ref. AN938)

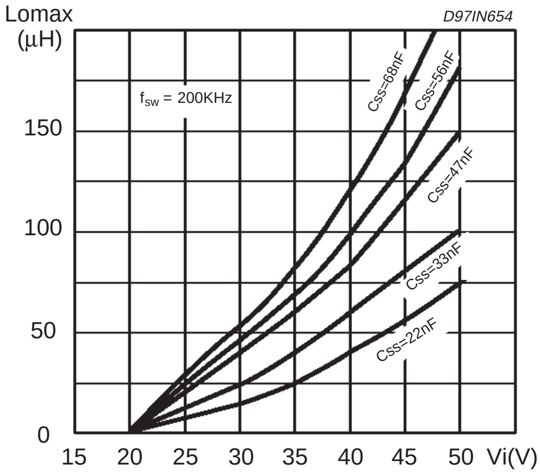


Figure 31: Open Loop Frequency and Phase of Error amplifier

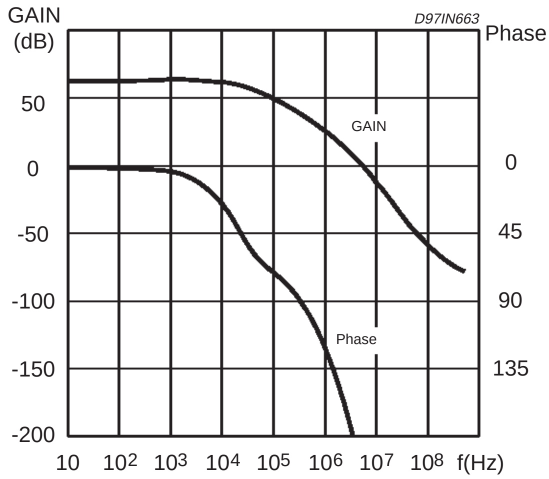


Figure 32: 3.5A at V_O< 3.3V (see part list fig. 1)

V_P	R_5	R_3
1	3.6K	4.7K
1.5	2K	2K
2	4.7K	3.6K
2.5	7.5K	3.6K
3	5.1K	1K

$V_O = 3.36 - 1.74 \bullet \frac{R_3}{R_5}$

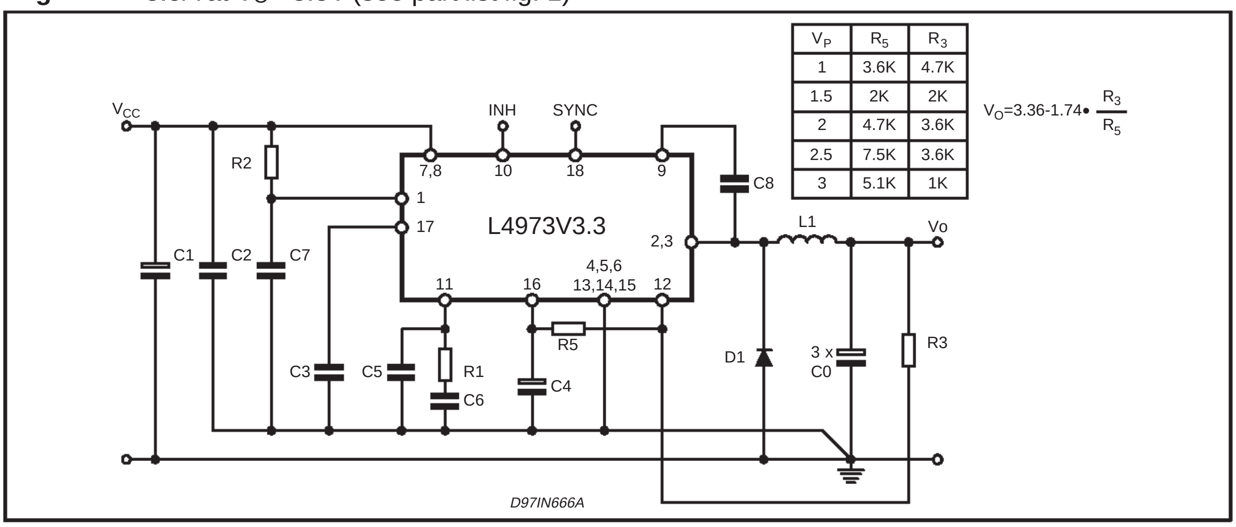


Figure 33: 12V to 3.3V High Performance Buck Converter (f_{SW} = 200kHz)

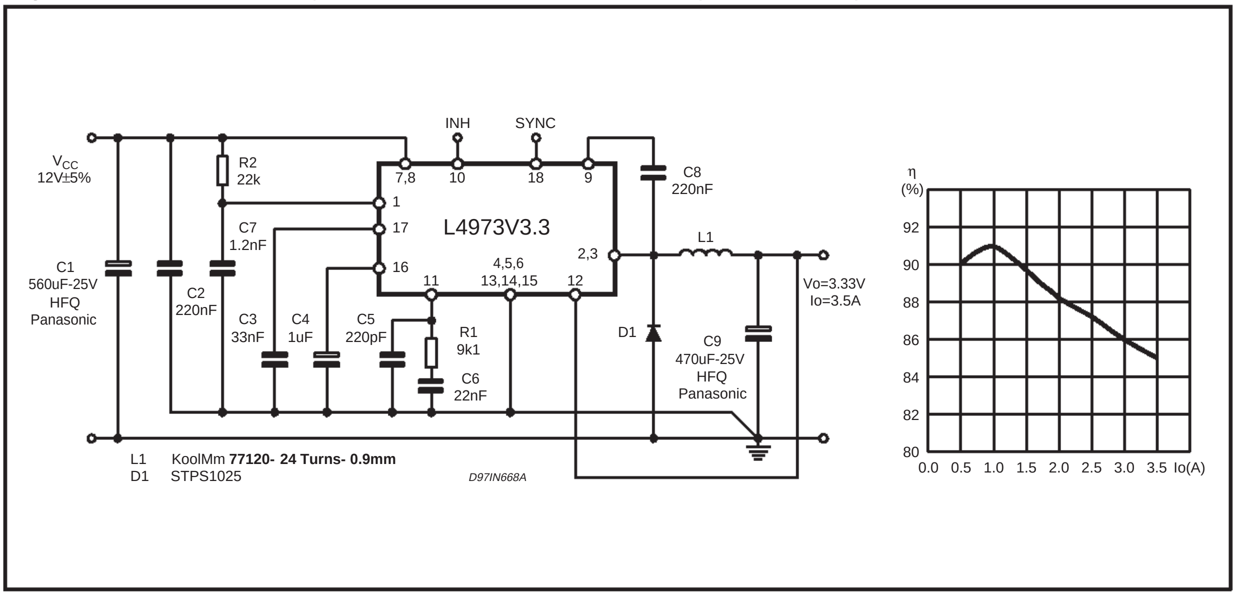


Figure 34: Synchronization Example

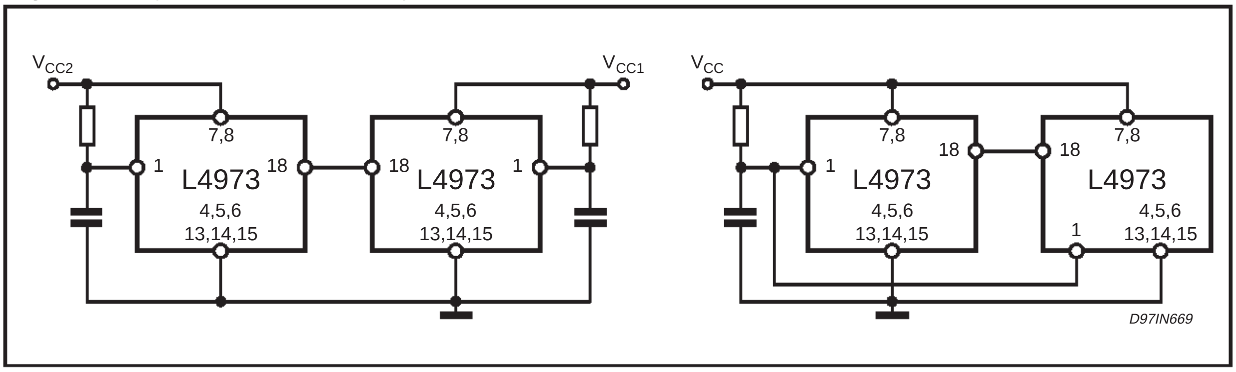
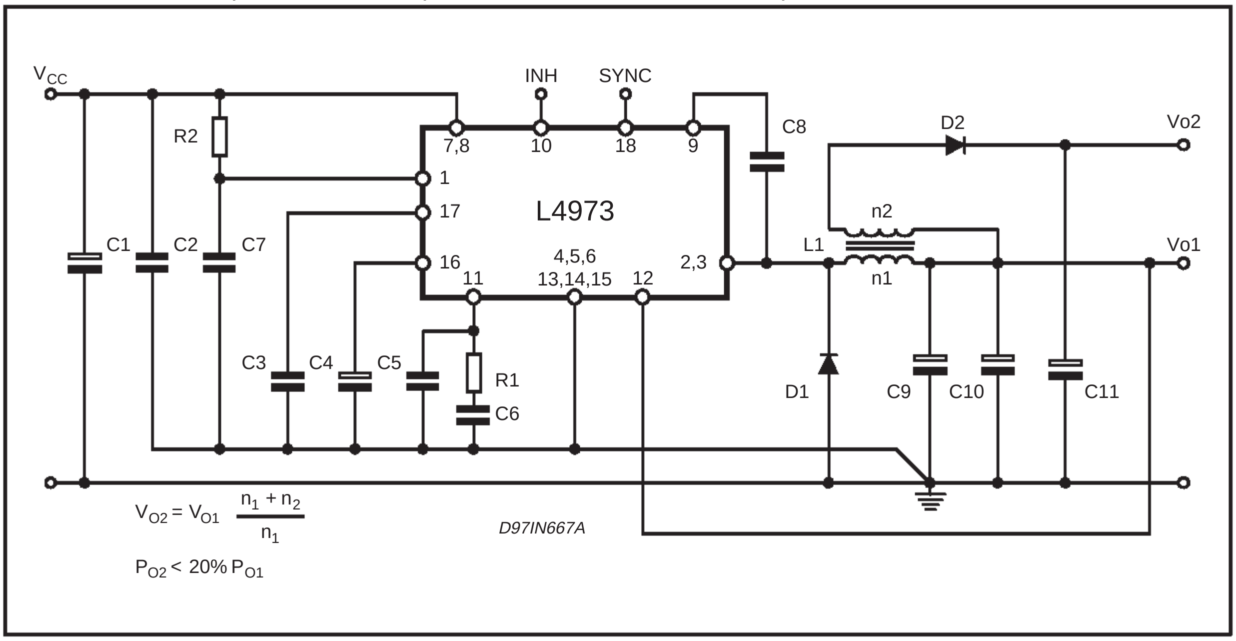
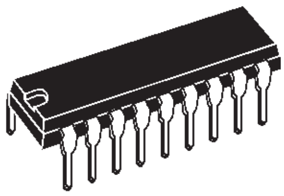


Figure 35: Multioutput not Isolated (Pin out referred to DIP12+3+3)

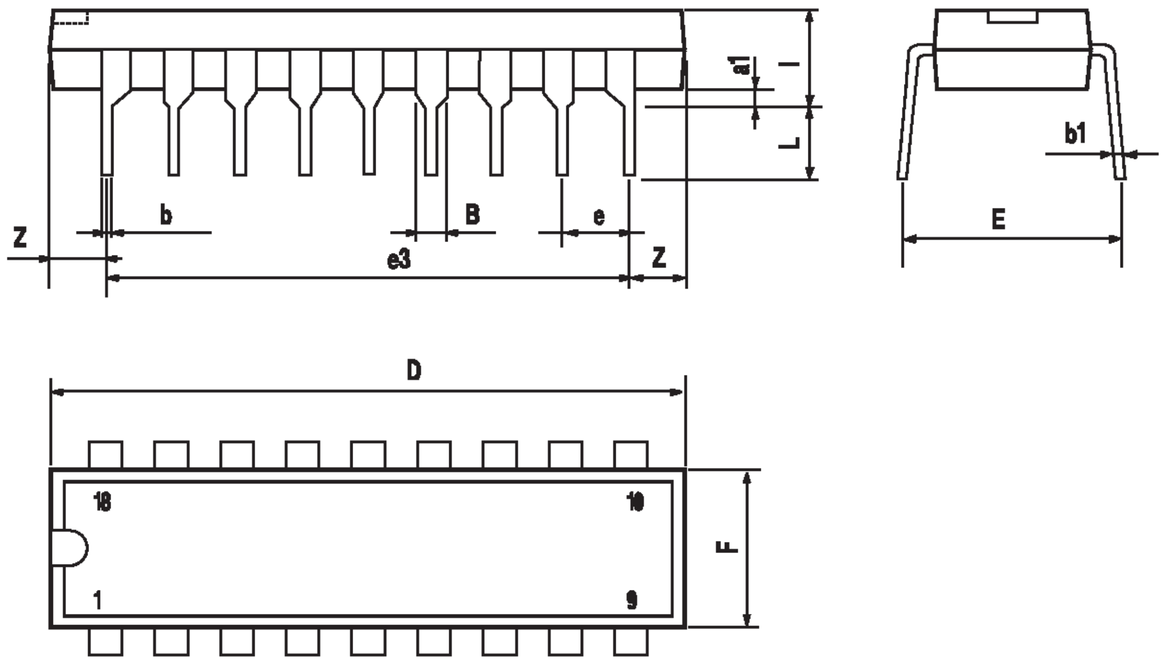


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100

OUTLINE AND MECHANICAL DATA

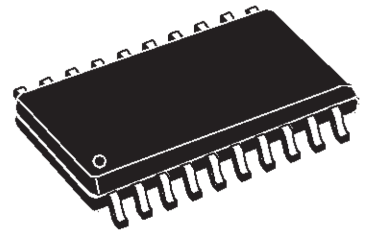


Powerdip 18

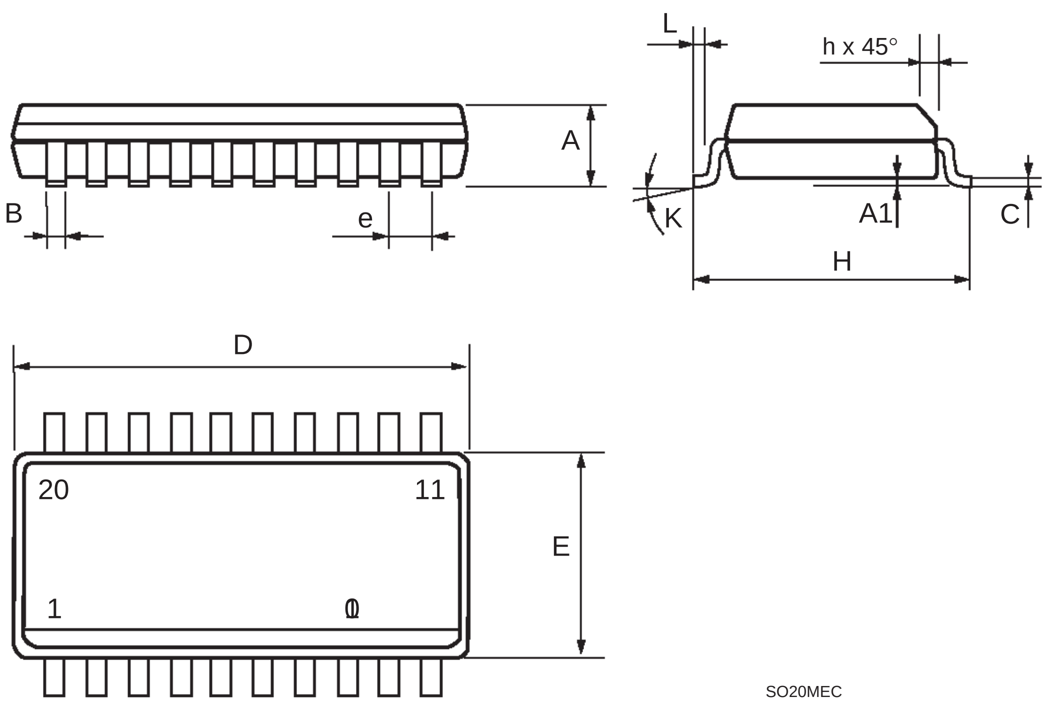


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

OUTLINE AND MECHANICAL DATA



SO20



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