# CoolMOS™ Power Transistor

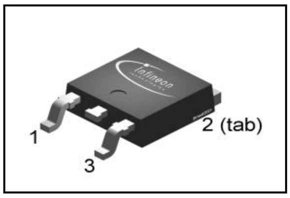
**Product Summary**

| | | |
|---|---|---|
| $V_{DS}$ | 800 | V |
| $R_{DS(on)max}$ @ $T_j$ = 25°C | 2.7 | Ω |
| $Q_{g,typ}$ | 12 | nC |

**Features**

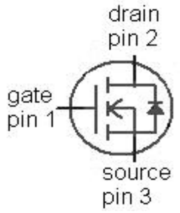
- New revolutionary high voltage technology
- Extreme dv/dt rated
- High peak current capability
- Qualified according to AEC Q101
- Green package (RoHS compliant), Pb-free lead plating, halogen free for mold compound
- Ultra low gate charge
- Ultra low effective capacitances

PG-TO252-3




**CoolMOS™ 800V designed for:**

- Automotive application with high DC bulk voltage
- Switching Application ( i.e. active clamp forward )




| Type | Package | Marking |
|---|---|---|
| IPD80R2k7C3A | PG-TO252-3 | 80C2k7A |

**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous drain current | $I_D$ | $T_C$=25 °C | 2 | A |
| | | $T_C$=100 °C | 1.2 | |
| Pulsed drain current[2)] | $I_{D,pulse}$ | $T_C$=25 °C | 6 | |
| Avalanche energy, single pulse | $E_{AS}$ | $I_D$=1 A, $V_{DD}$=50 V | 90 | mJ |
| Avalanche energy, repetitive $t_{AR}$[2),3)] | $E_{AR}$ | $I_D$=2 A, $V_{DD}$=50 V | 0.05 | |
| Avalanche current, repetitive $t_{AR}$[2),3)] | $I_{AR}$ | | 2 | A |
| MOSFET d$v$/d$t$ ruggedness | d$v$/d$t$ | $V_{DS}$=0…640 V | 50 | V/ns |
| Gate source voltage | $V_{GS}$ | static | ±20 | V |
| | | AC ($f$>1 Hz) | ±30 | |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 42 | W |
| Operating, Storage temperature | $T_j, T_{stg}$ | | -40 ... 150 | °C |

**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous diode forward current | $I_S$ | $T_C$=25 °C | 2 | A |
| Diode pulse current[2] | $I_{S,pulse}$ | | 6 | |
| Reverse diode d*v*/d*t*[4] | d*v*/d*t* | | 4 | V/ns |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Thermal characteristics** | | | | | | |
| Thermal resistance, junction - case | $R_{thJC}$ | | - | - | 3 | K/W |
| Thermal resistance, junction - ambient | $R_{thJA}$ | SMD version, device on PCB, minimal footprint | - | - | 62 | |
| | | SMD version, device on PCB, 6 cm$^2$ cooling area[5] | - | 35 | - | |
| Soldering temperature, reflow soldering | $T_{sold}$ | reflow MSL1 | - | - | 260 | °C |
| **Electrical characteristics,** at $T_j$=25 °C, unless otherwise specified | | | | | | |
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage[1] | $V_{(BR)DSS}$ | $V_{GS}$=0 V, $I_D$=250 µA | 800 | - | - | V |
| Avalanche breakdown voltage | $V_{(BR)DS}$ | $V_{GS}$=0 V, $I_D$=2 A | - | 870 | - | |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=0.12 mA | 2.1 | 3 | 3.9 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=800 V, $V_{GS}$=0 V, $T_j$=25 °C | - | - | 5 | µA |
| | | $V_{DS}$=800 V, $V_{GS}$=0 V, $T_j$=150 °C | - | 25 | - | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=20 V, $V_{DS}$=0 V | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=10 V, $I_D$=1.2 A, $T_j$=25 °C | - | 2.4 | 2.7 | Ω |
| | | $V_{GS}$=10 V, $I_D$=1.2 A, $T_j$=150 °C | - | 5.5 | - | |
| Gate resistance | $R_G$ | *f*=1 MHz, open drain | - | 1.2 | - | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0 V, $V_{DS}$=100 V, $f$=1 MHz | - | 290 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 13 | - | |
| Effective output capacitance, energy related[6] | $C_{o(er)}$ | $V_{GS}$=0 V, $V_{DS}$=0 V to 480 V | - | 11 | - | |
| Effective output capacitance, time related[7] | $C_{o(tr)}$ | | - | 26 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=400 V, $V_{GS}$=0/10 V, $I_D$=2 A, $R_{G,ext}$=47 Ω, $T$j=25 °C | - | 25 | - | ns |
| Rise time | $t_r$ | | - | 15 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 72 | - | |
| Fall time | $t_f$ | | - | 18 | - | |
| **Gate Charge Characteristics** | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=640 V, $I_D$=2 A, $V_{GS}$=0 to 10 V | - | 1.5 | - | nC |
| Gate to drain charge | $Q_{gd}$ | | - | 6 | - | |
| Gate charge total | $Q_g$ | | - | 12 | 16 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 5.5 | - | V |
| **Reverse Diode** | | | | | | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0 V, $I_F$=$I_S$=2 A, $T_j$=25 °C | - | 1 | 1.2 | V |
| Reverse recovery time | $t_{rr}$ | $V_R$=400 V, $I_F$=$I_S$=2 A, d$i_F$/d$t$=100 A/µs | - | 520 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 2 | - | µC |
| Peak reverse recovery current | $I_{rrm}$ | | - | 6 | - | A |

1) For applications with applied blocking voltage > 65% of the specified blocking voltage, we recommend to evaluate the impact of the cosmic radiation effect in early design phase. For assessment please contact local Infineon sales office.

2) Pulse width $t_p$ limited by $T_{j,max}$

3) Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

4) $I_{SD} \leq I_D$, di/dt≤400A/µs, $V_{DClink}$ = 400V, $V_{peak}<V_{(BR)DSS}$, $T_j<T_{jmax}$, identical low side and high side switch

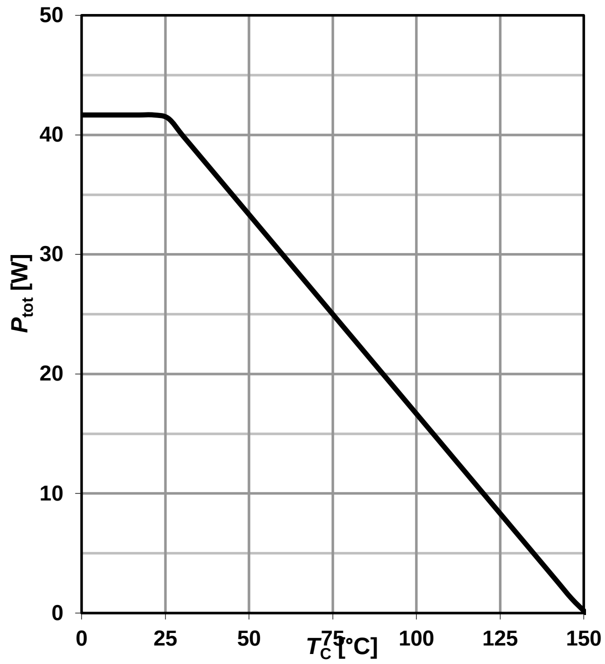
5) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air

6) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

7) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

## 1 Power dissipation

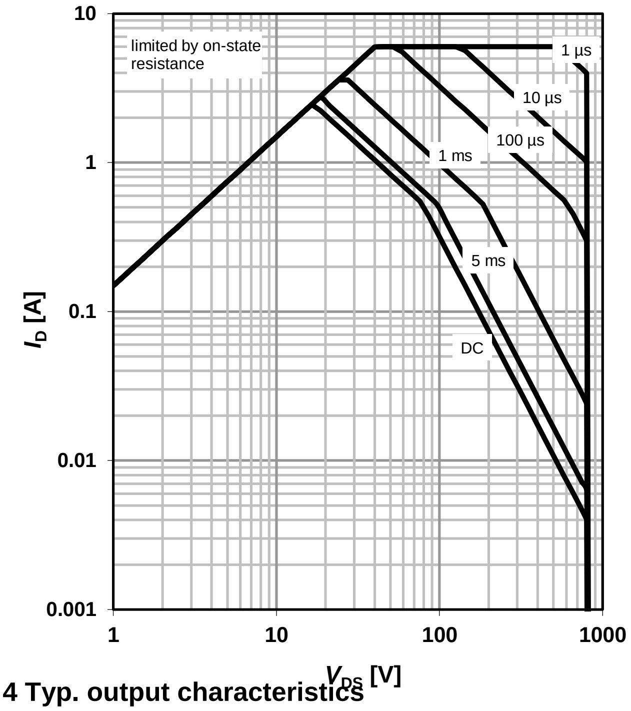
$P_{tot}$=f($T_C$)




## 2 Safe operating area [1)]

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0, Parameter: tp

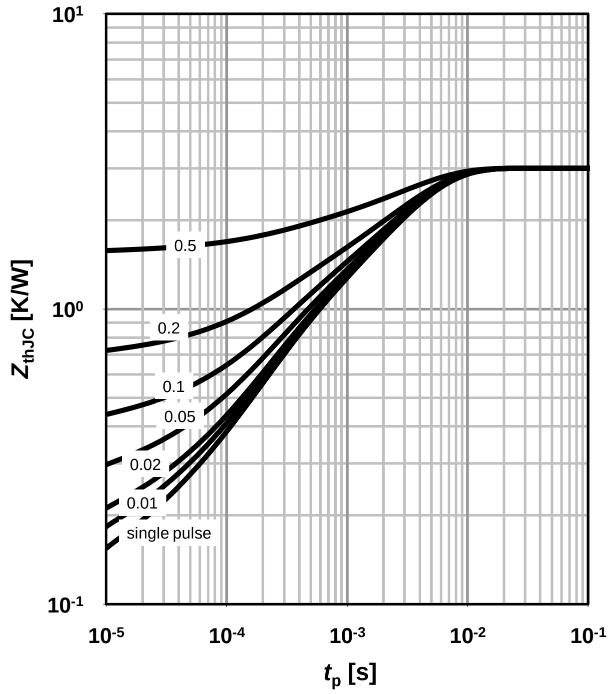
[1)] DC curve indicates operation at thermal equilibrated state, not guaranteed over lifetime.




## 3 Max. transient thermal impedance

$Z_{thJC}$=f($t_P$)

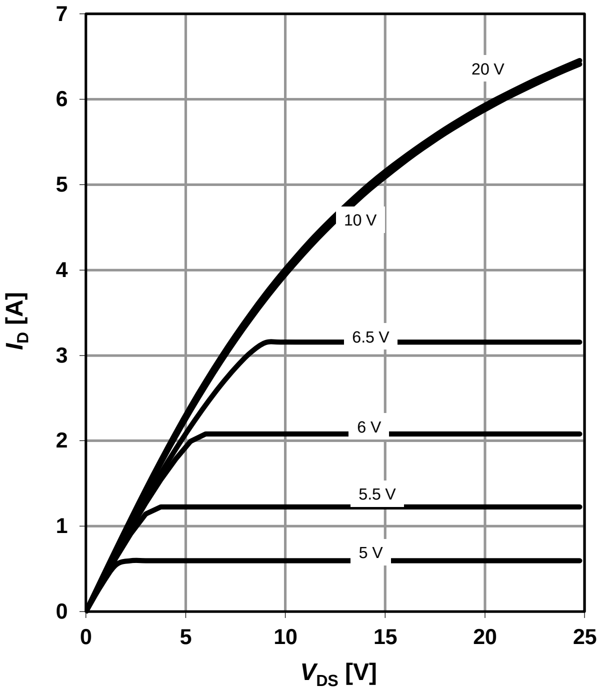
parameter: $D=t_p/T$




## 4 Typ. output characteristics

$I_D$=f($V_{DS}$); $T_j$=25 °C; $t_p$=10 µs

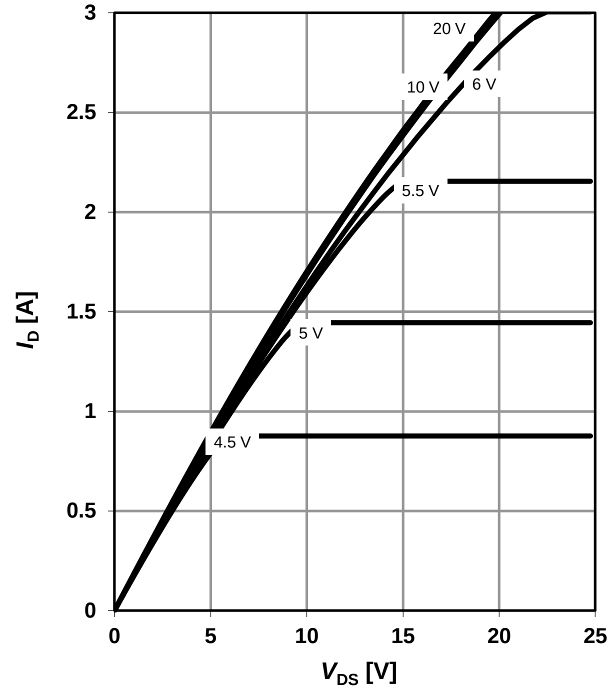
parameter: $V_{GS}$



### 5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 150$ °C; $t_p = 10$ µs

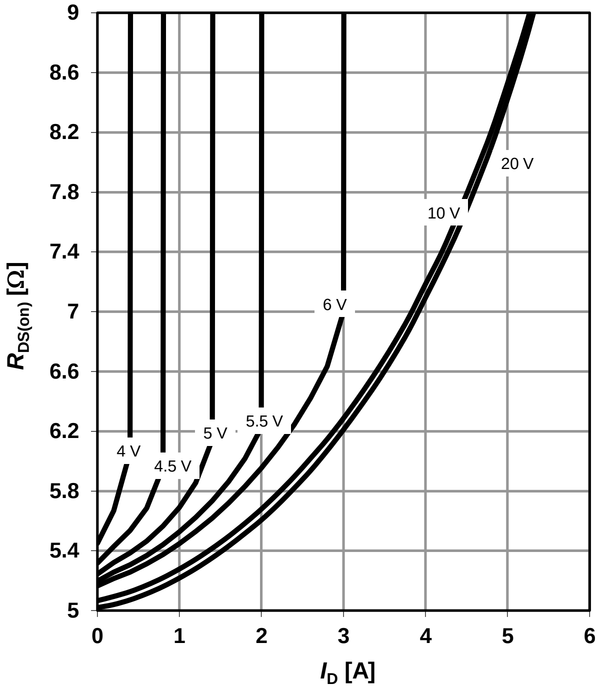
parameter: $V_{GS}$




### 6 Typ. drain-source on-state resistance

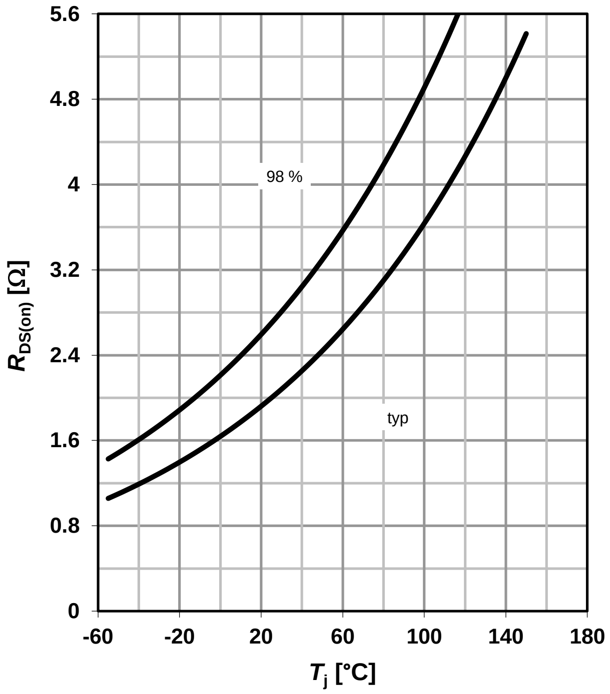
$R_{DS(on)} = f(I_D)$; $T_j = 150$ °C

parameter: $V_{GS}$




### 7 Drain-source on-state resistance

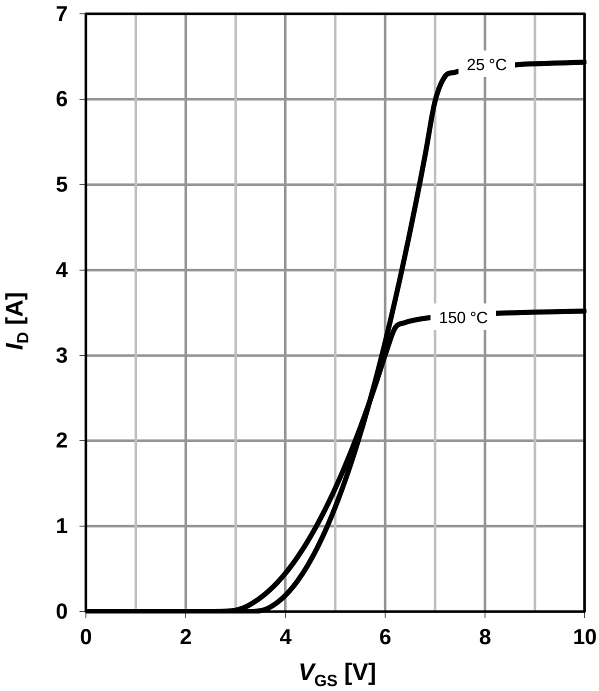
$R_{DS(on)} = f(T_j)$; $I_D = 1.2$ A; $V_{GS} = 10$ V




### 8 Typ. transfer characteristics

$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D| R_{DS(on)max}$; $t_p = 10$ µs

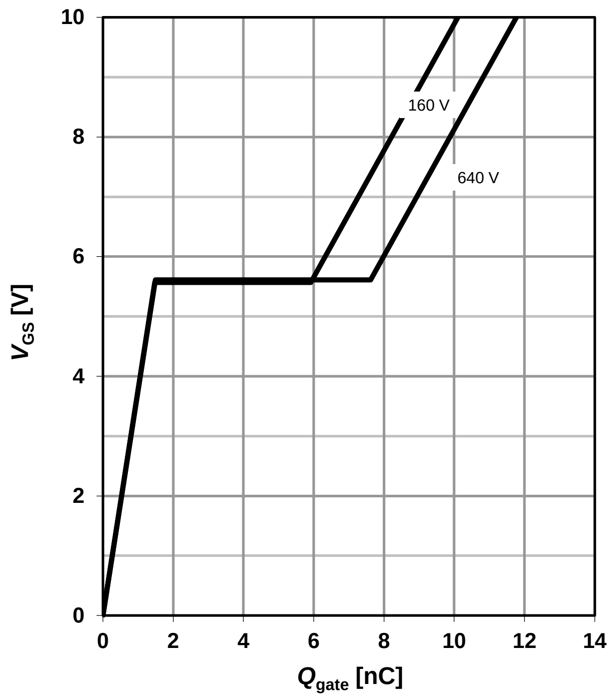
parameter: $T_j$



### 9 Typ. gate charge

$V_{GS}$=f($Q_{gate}$); $I_D$=2 A pulsed

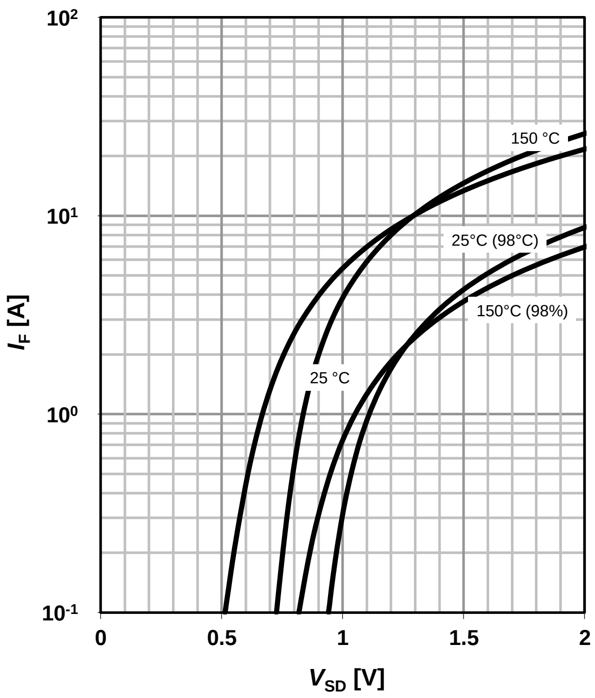
parameter: $V_{DD}$




### 10 Forward characteristics of reverse diode

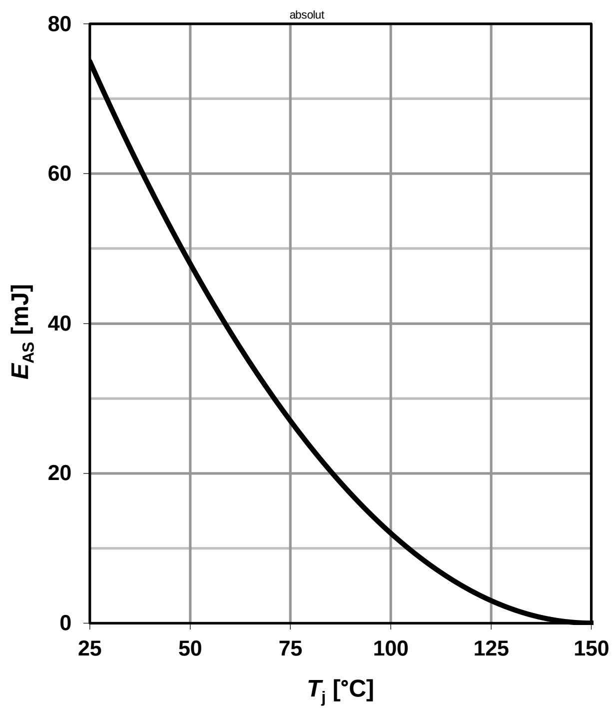
$I_F$=f($V_{SD}$); $t_p$=10 µs

parameter: $T_j$



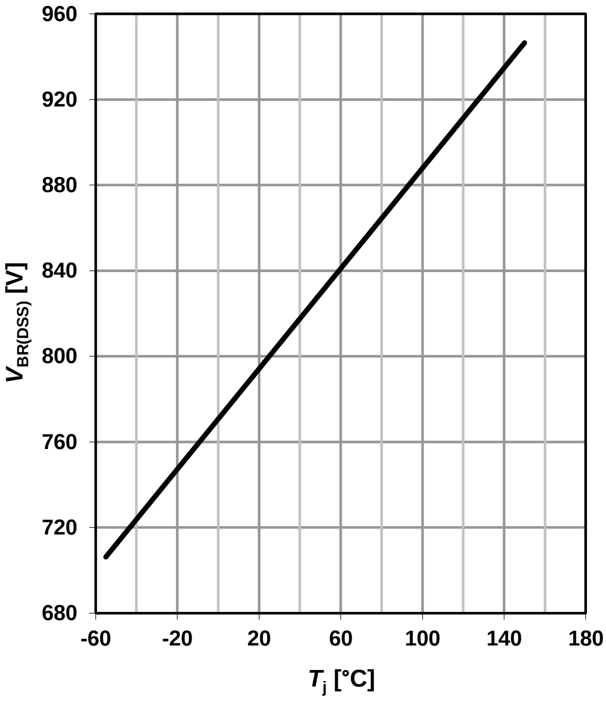

### 11 Avalanche energy

$E_{AS}$=f($T_j$); $I_D$=1 A; $V_{DD}$=50 V



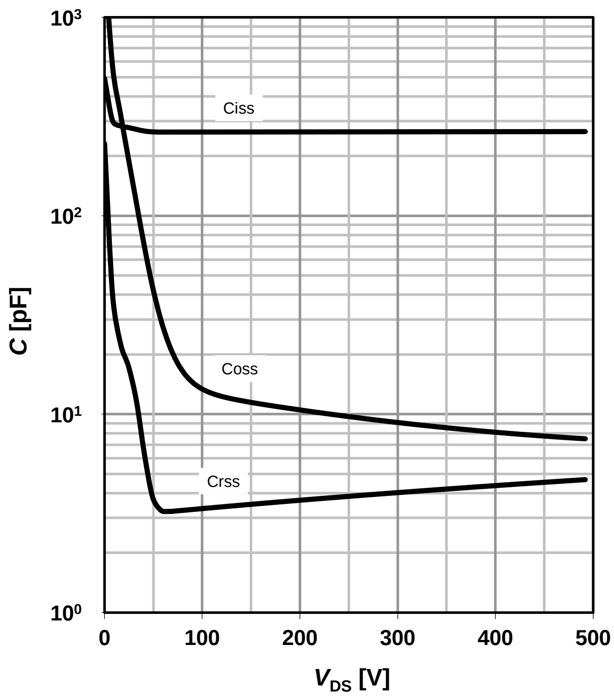

### 12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f($T_j$); $I_D$=0.25 mA



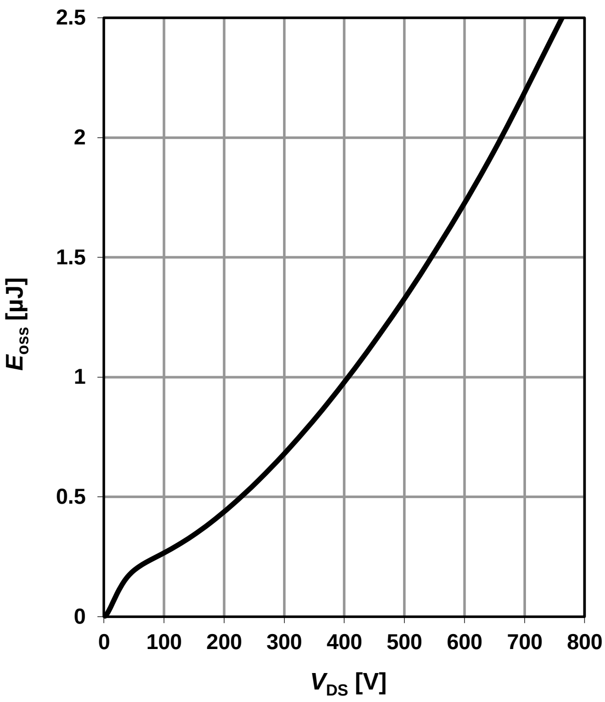
**13 Typ. capacitances**

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

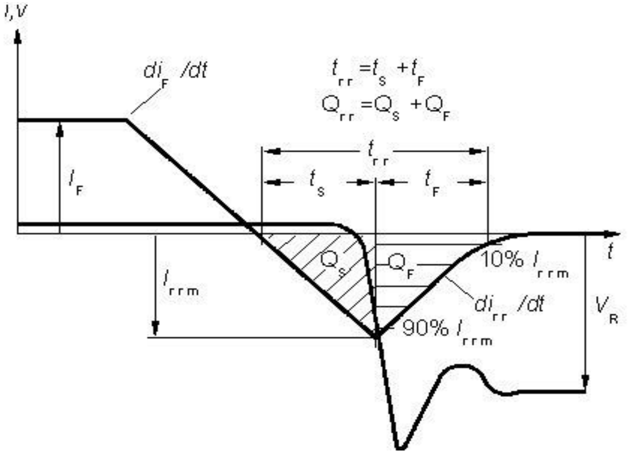



**14 Typ. Coss stored energy**

$E_{oss}$=f($V_{DS}$)

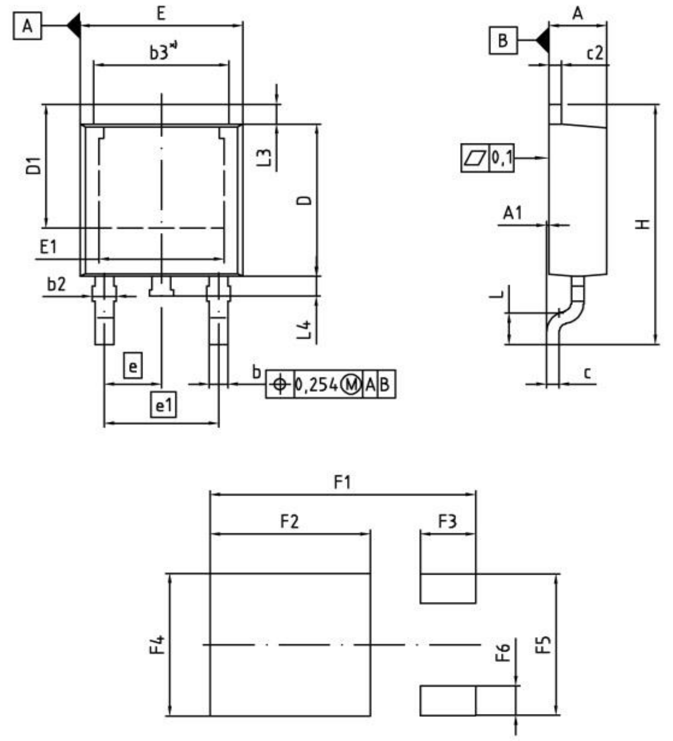


**Definition of diode switching characteristics**



**PG-TO252-3: Outline**

## TO252-3 (DPAK)




*) mold flash not included

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.16 | 2.41 | 0.085 | 0.095 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b2 | 0.65 | 1.15 | 0.026 | 0.045 |
| b3 | 5.00 | 5.50 | 0.197 | 0.217 |
| c | 0.46 | 0.60 | 0.018 | 0.024 |
| c2 | 0.46 | 0.98 | 0.018 | 0.039 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.02 | 5.84 | 0.198 | 0.230 |
| E | 6.40 | 6.73 | 0.252 | 0.265 |
| E1 | 4.70 | 5.21 | 0.185 | 0.205 |
| e | 2.29 (BSC) | | 0.090 (BSC) | |
| e1 | 4.57 | | 0.180 | |
| N | 3 | | 3 | |
| H | 9.40 | 10.48 | 0.370 | 0.413 |
| L | 1.18 | 1.70 | 0.046 | 0.067 |
| L3 | 0.90 | 1.25 | 0.035 | 0.049 |
| L4 | 0.51 | 1.00 | 0.020 | 0.039 |
| F1 | 10.60 | | 0.417 | |
| F2 | 6.40 | | 0.252 | |
| F3 | 2.20 | | 0.087 | |
| F4 | 5.80 | | 0.228 | |
| F5 | 5.76 | | 0.227 | |
| F6 | 1.20 | | 0.047 | |

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**SCALE** 0 2.0 0 2.0 4mm

**EUROPEAN PROJECTION**

**ISSUE DATE**
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**REVISION**
04

dimensions in mm/inches

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