

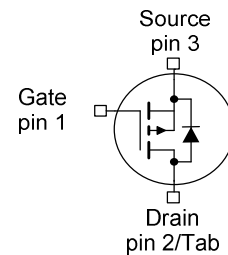
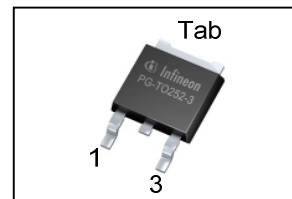
OptiMOS®-P2 Power-Transistor

Features

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

Product Summary

| | | |
|--------------|-----|----|
| V_{DS} | -40 | V |
| $R_{DS(on)}$ | 7.8 | mΩ |
| I_D | -70 | A |

PG-TO252-3-313


| Type | Package | Marking |
|----------------|----------------|---------|
| IPD70P04P4L-08 | PG-TO252-3-313 | 4P04L08 |

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|---------------|------|
| Continuous drain current | I_D | $T_C=25\text{ °C}$, $V_{GS}=-10\text{V}$ | -70 | A |
| | | $T_C=100\text{ °C}$, $V_{GS}=-10\text{V}^{1)}$ | -55 | |
| Pulsed drain current ¹⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | -280 | |
| Avalanche energy, single pulse ¹⁾ | E_{AS} | $I_D=-35\text{A}$ | 24 | mJ |
| Avalanche current, single pulse | I_{AS} | - | -70 | A |
| Gate source voltage | V_{GS} | - | $\pm 16^{2)}$ | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 75 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics¹⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | - | 2.0 | K/W |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ³⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|------|-------|------|------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=-1mA$ | -40 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=-120\mu A$ | -1.2 | -1.7 | -2.2 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ\text{C}$ | - | -0.05 | -1 | μA |
| | | $V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$ | - | -20 | -200 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=-16V, V_{DS}=0V$ | - | - | -100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=-4.5V, I_D=-40A$ | - | 9.0 | 12.9 | m Ω |
| | | $V_{GS}=-10V, I_D=-70A$ | - | 5.7 | 7.8 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics¹⁾

| | | | | | | |
|------------------------------|--------------|---|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$ | - | 4177 | 5430 | pF |
| Output capacitance | C_{oss} | | - | 1185 | 1778 | |
| Reverse transfer capacitance | C_{rss} | | - | 45 | 90 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-70A,$ $R_G=3.5\Omega$ | - | 12 | - | ns |
| Rise time | t_r | | - | 10 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 50 | - | |
| Fall time | t_f | | - | 41 | - | |

Gate Charge Characteristics¹⁾

| | | | | | | |
|-----------------------|---------------|--|---|------|----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=-32V, I_D=-70A,$ $V_{GS}=0$ to $-10V$ | - | 14 | 18 | nC |
| Gate to drain charge | Q_{gd} | | - | 10 | 20 | |
| Gate charge total | Q_g | | - | 71 | 92 | |
| Gate plateau voltage | $V_{plateau}$ | | - | -3.5 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|--|---|----|------|----|
| Diode continuous forward current ¹⁾ | I_S | $T_C=25^\circ C$ | - | - | -70 | A |
| Diode pulse current ¹⁾ | $I_{S,pulse}$ | | - | - | -280 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0V, I_F=-70A,$ $T_j=25^\circ C$ | - | -1 | -1.3 | V |
| Reverse recovery time ¹⁾ | t_{rr} | $V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$ | - | 46 | - | ns |
| Reverse recovery charge ¹⁾ | Q_{rr} | | - | 43 | - | nC |

¹⁾ Defined by design. Not subject to production test.

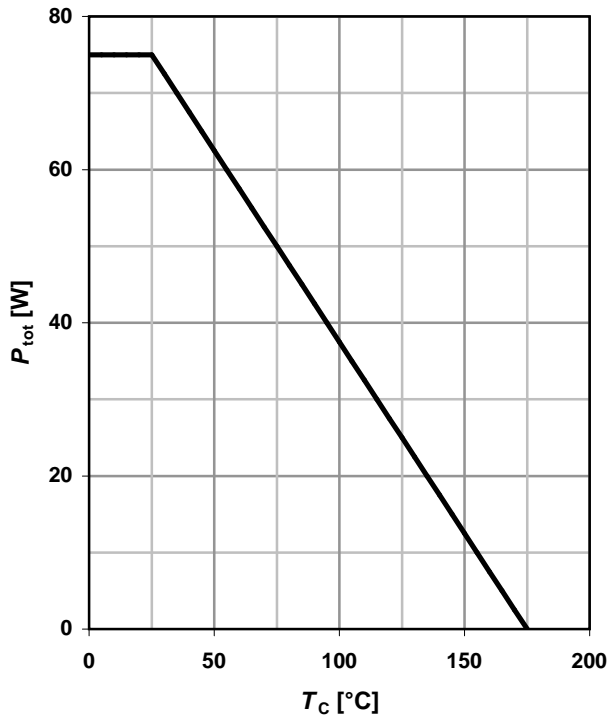
²⁾ $V_{GS}=+5V/-16V$ according AEC;

$V_{GS}=+16V$ for max 168h at $T_i=175^\circ C$

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

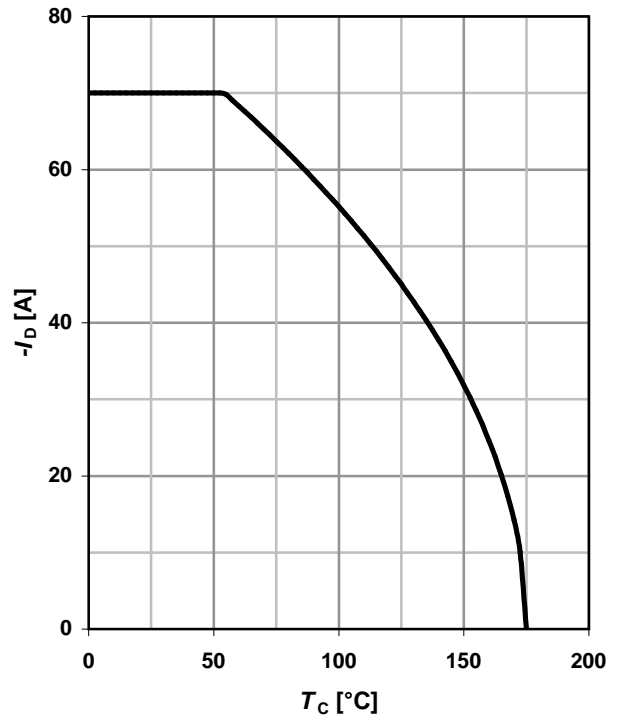
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \leq -6V$



2 Drain current

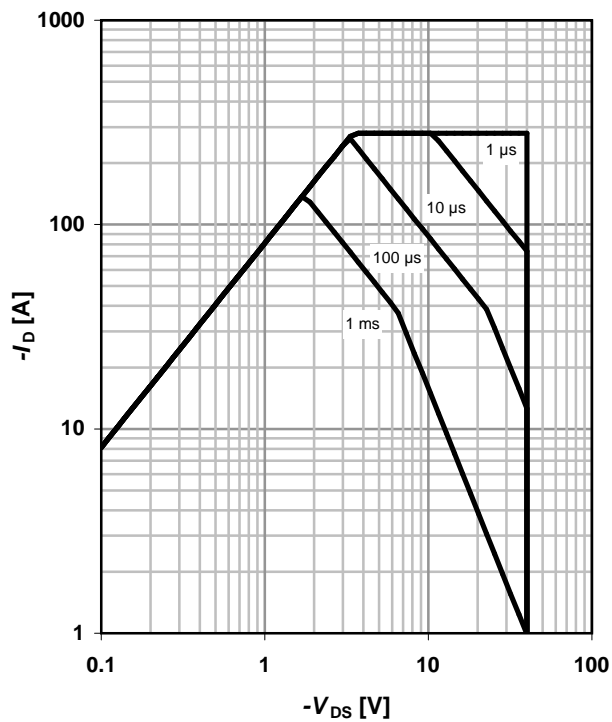
$I_D = f(T_C); V_{GS} = -10V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

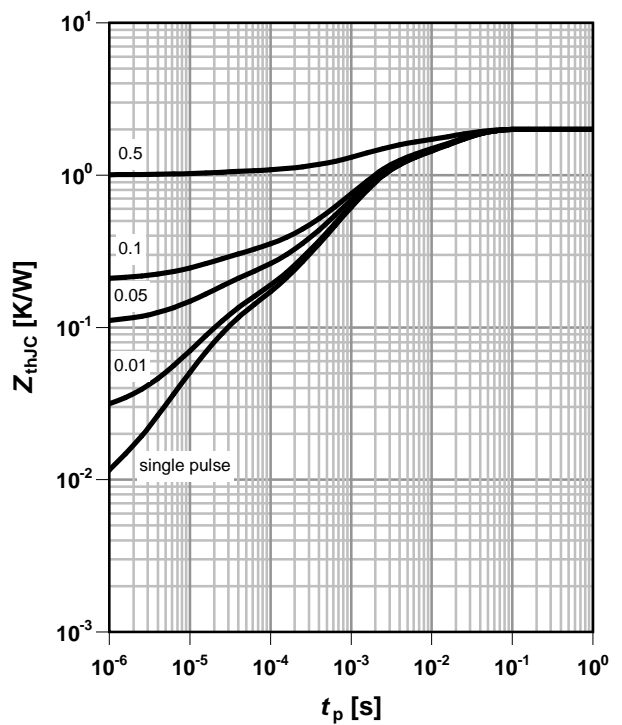
parameter: t_p



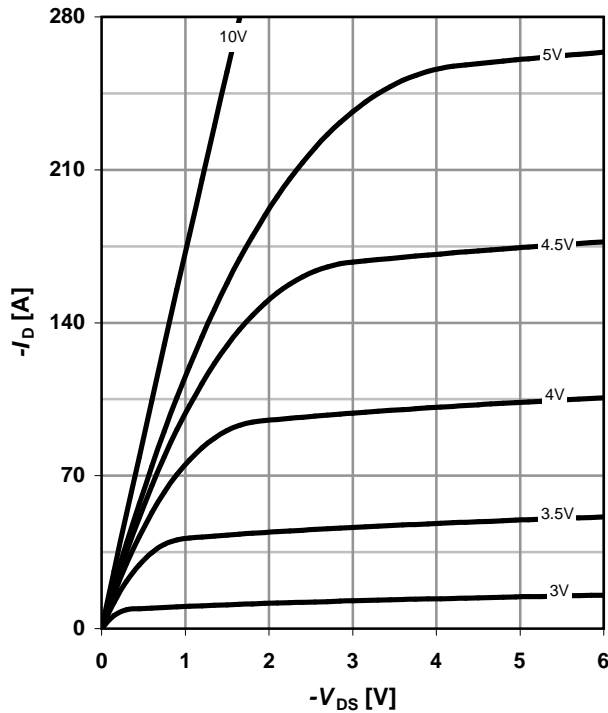
4 Max. transient thermal impedance

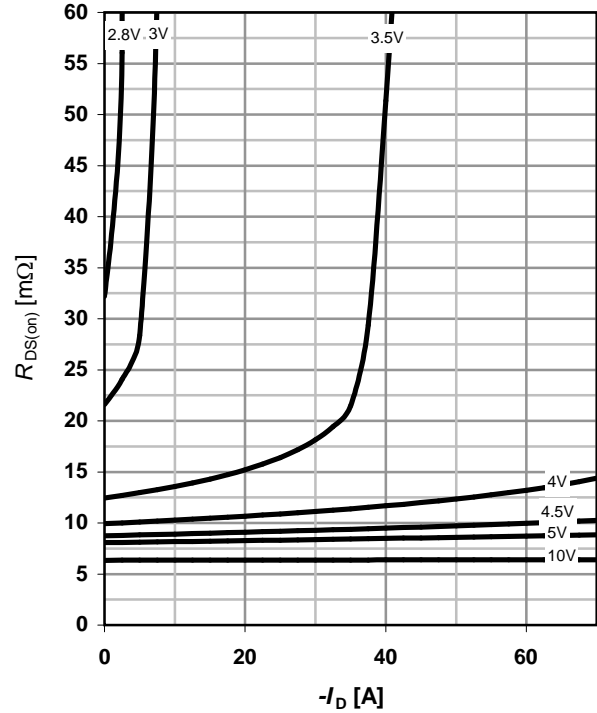
$Z_{thJC} = f(t_p)$

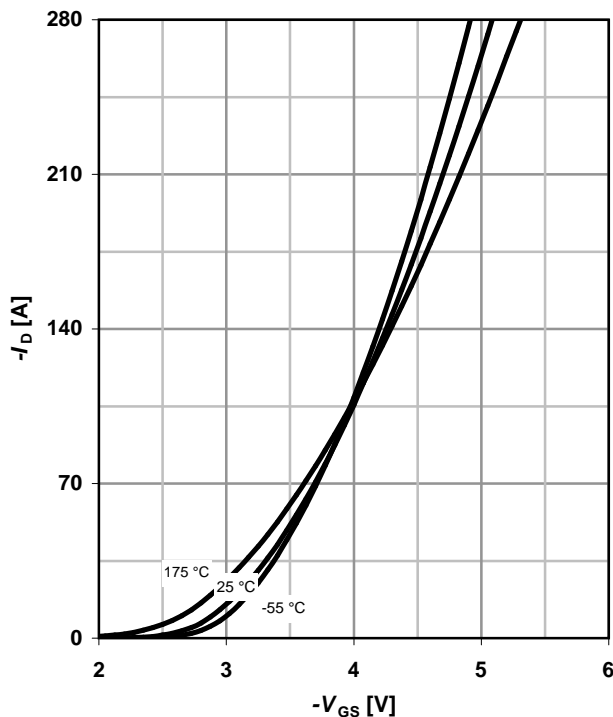
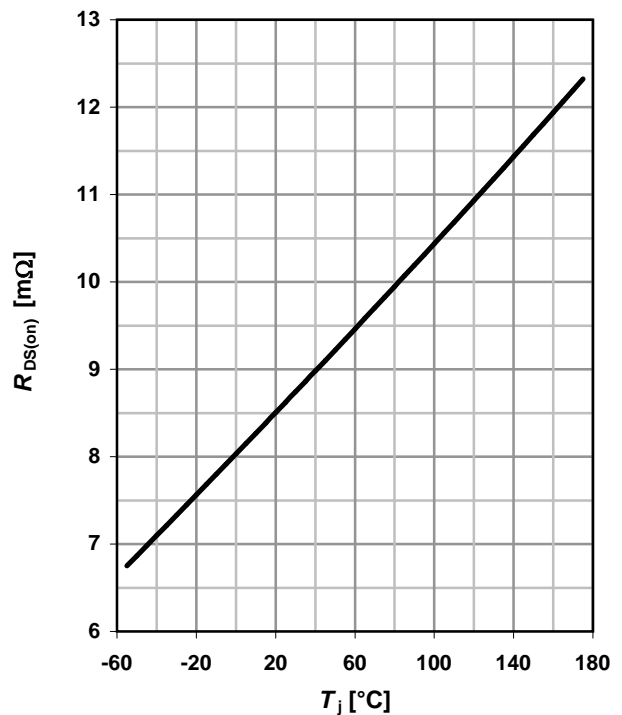
parameter: $D = t_p/T$



5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25\text{ °C}$

 parameter: $-V_{GS}$

6 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

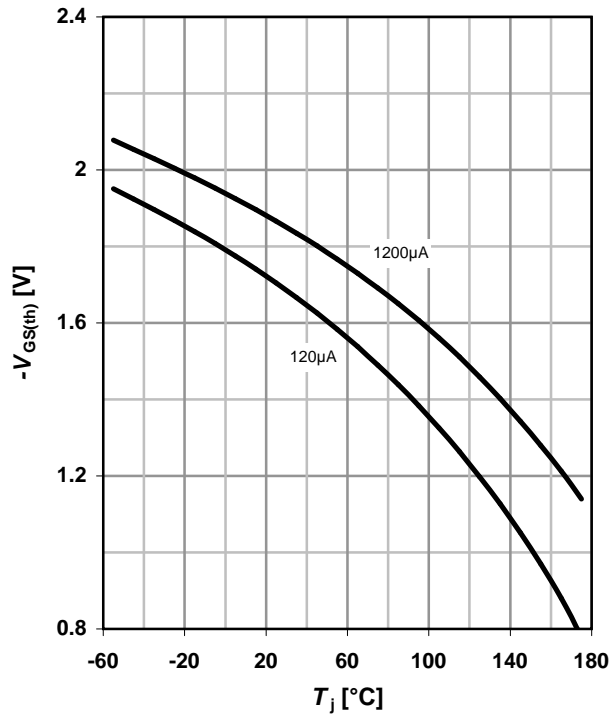
 parameter: $-V_{GS}$

7 Typ. transfer characteristics
 $I_D = f(V_{GS}); V_{DS} = -6V$

 parameter: T_j

8 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = -70\text{ A}; V_{GS} = -10\text{ V}$


9 Typ. gate threshold voltage

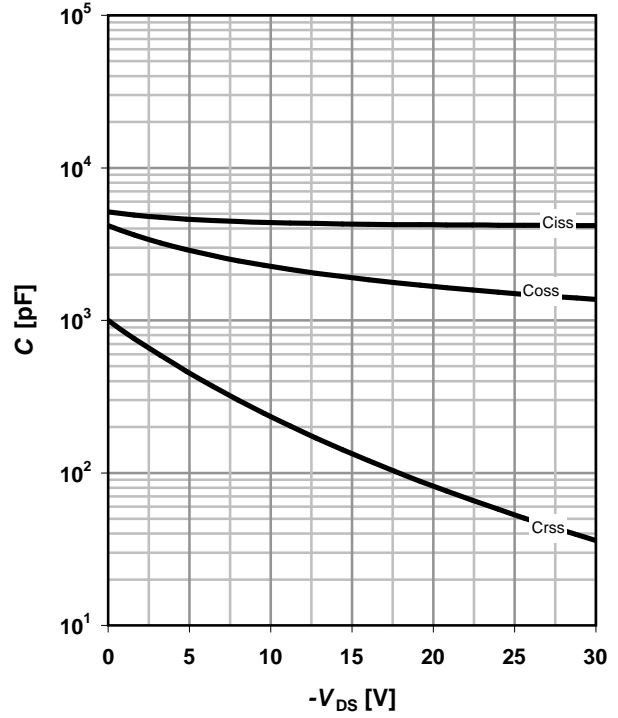
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: $-I_D$



10 Typ. capacitances

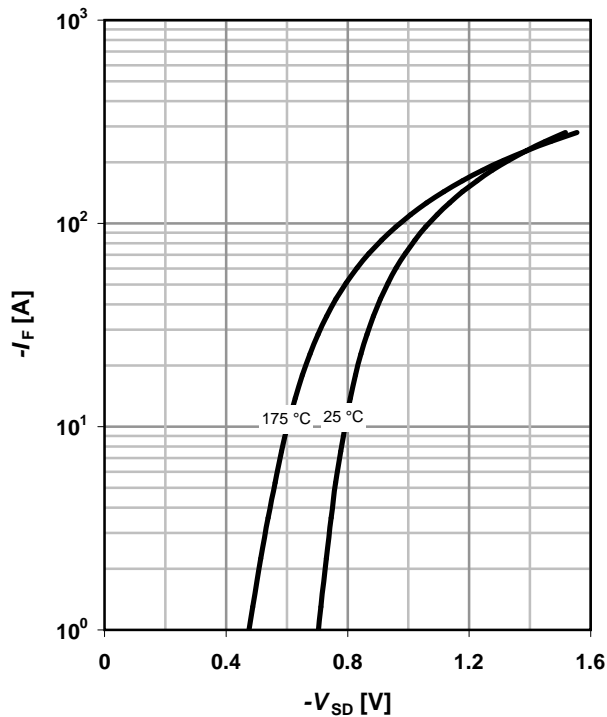
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

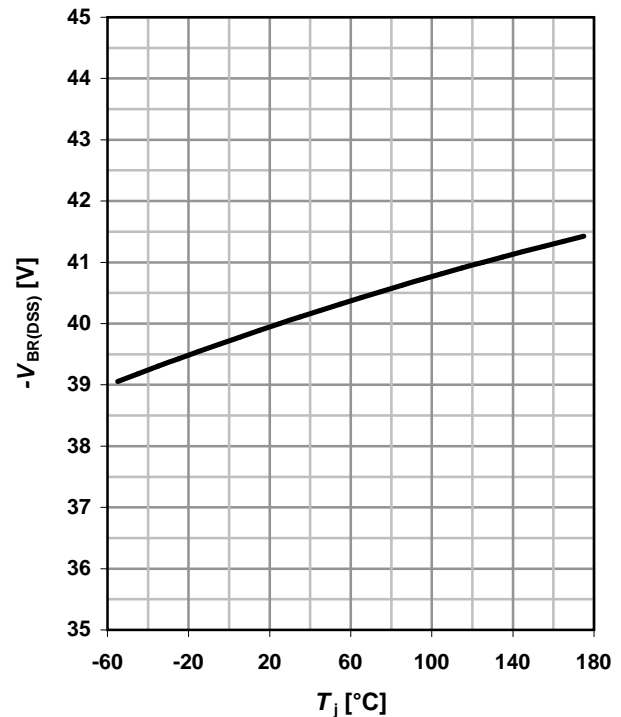
$I_F = f(V_{SD})$

parameter: T_j



12 Drain-source breakdown voltage

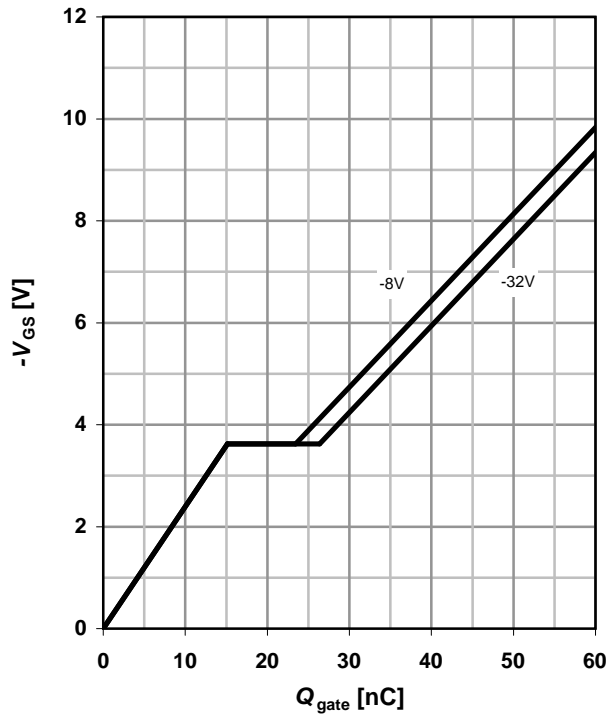
$V_{BR(DSS)} = f(T_j); I_D = -1 mA$



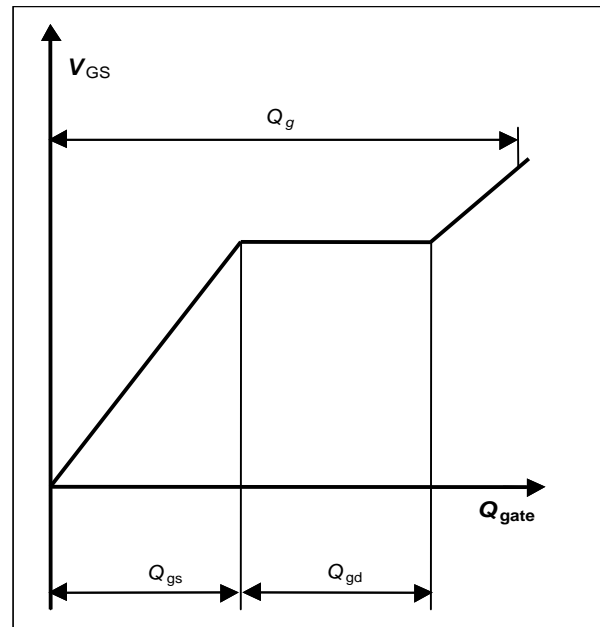
13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -70\text{ A pulsed}$

parameter: V_{DD}



14 Gate charge waveforms



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Revision History

| Version | Date | Changes |
|---------|------------|---------------------------|
| 0.1 | 08.03.2010 | Initial Target Data Sheet |
| 0.2 | 20.12.2010 | Preliminary Data Sheet |
| 1.0 | 14.03.2011 | Final Data Sheet |