

OptiMOS™ - 6 Power-Transistor

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	2.0	m Ω
I_D	100	A

Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TDSON-8


Type	Package	Marking
IAUC100N04S6L020	PG-TDSON-8	6N04L020

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{V}$	100	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{V}^{2)}$	100	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	400	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=20\text{A}$, $R_{G,min}=25\Omega$	147	mJ
Avalanche current, single pulse	I_{AS}	$R_{G,min}=25\Omega$	20	A
Gate source voltage	V_{GS}	-	± 16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	75	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.0	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ³⁾	-	-	50	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1\text{mA}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=32\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=50A$	-	2.26	2.70	m Ω
		$V_{GS}=10V, I_D=50A$	-	1.66	2.04	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	2111	2744	pF
Output capacitance	C_{oss}		-	587	763	
Reverse transfer capacitance	C_{rss}		-	35	53	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=100A, R_G=3.5\Omega$	-	4	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=100A,$ $V_{GS}=0$ to 10V	-	6.6	8.7	nC
Gate to drain charge	Q_{gd}		-	6.7	10.1	
Gate charge total	Q_g		-	34	46	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	100	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=50A,$ $T_j=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	28	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	15	-	nC

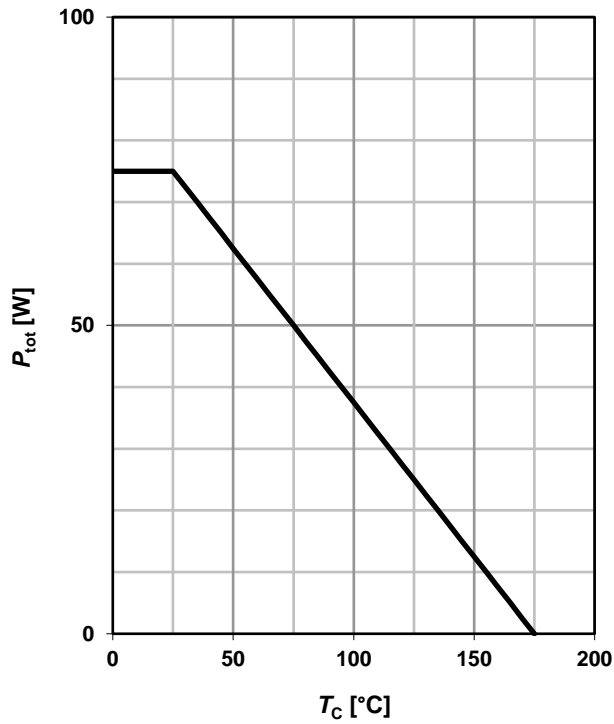
¹⁾ Current is limited by package; with an $R_{thJC} = 2.0$ K/W the chip is able to carry 144 A at 25°C.

²⁾ The parameter is not subject to production test- verified by design/characterization.

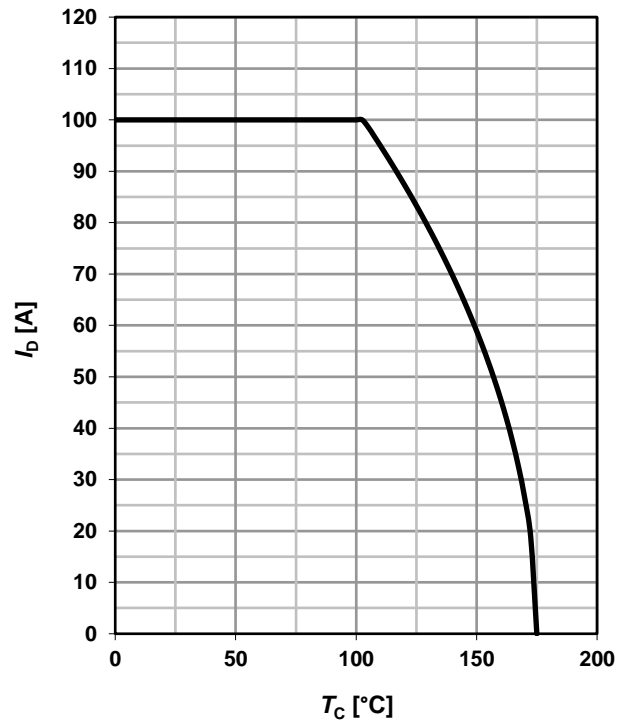
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

1 Power dissipation

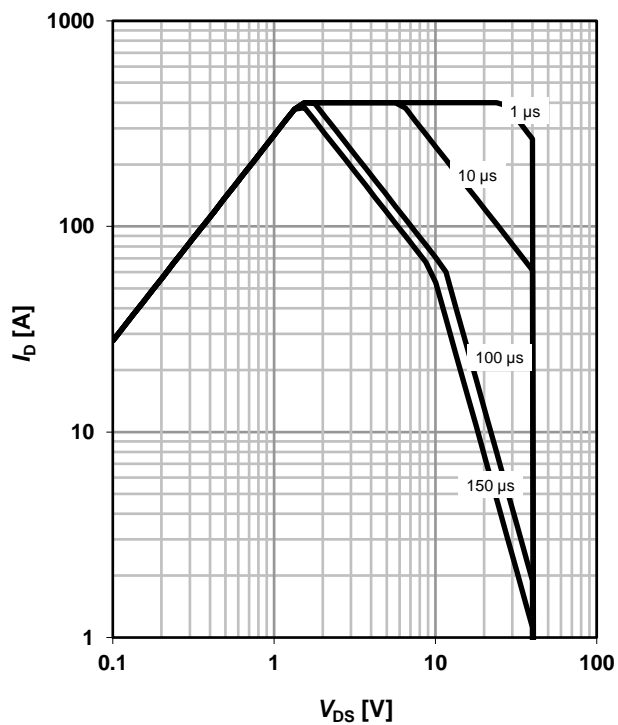
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


2 Drain current

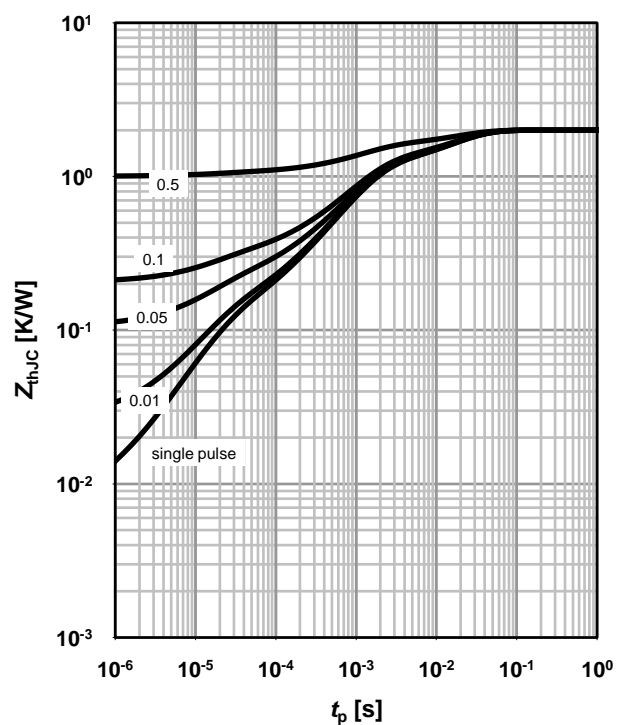
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

 parameter: t_p

4 Max. transient thermal impedance

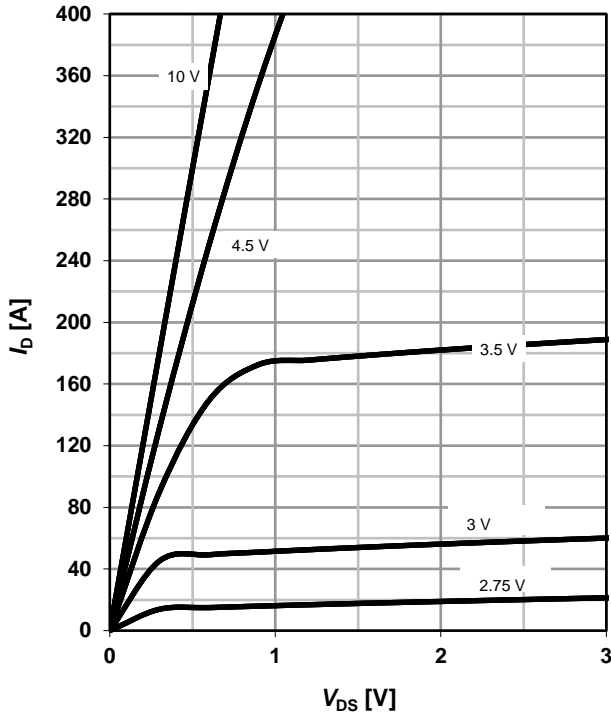
$$Z_{\text{thJC}} = f(t_p)$$

 parameter: $D = t_p/T$


5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

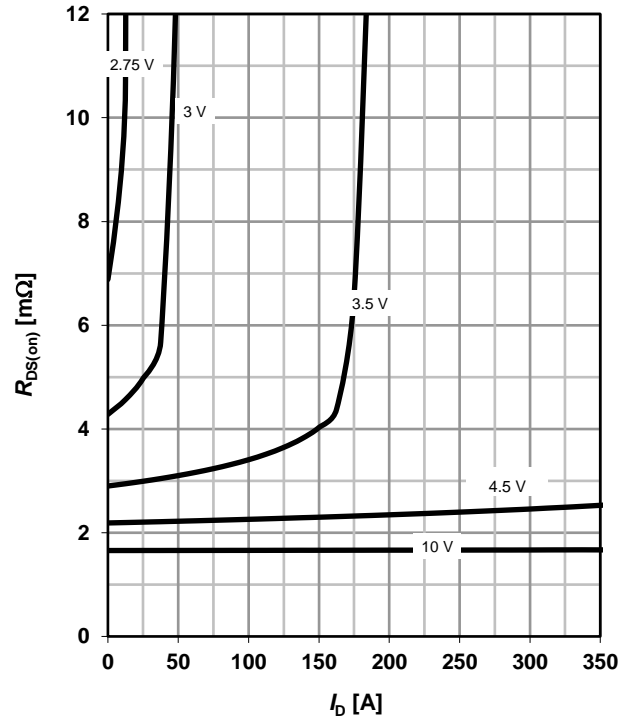
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

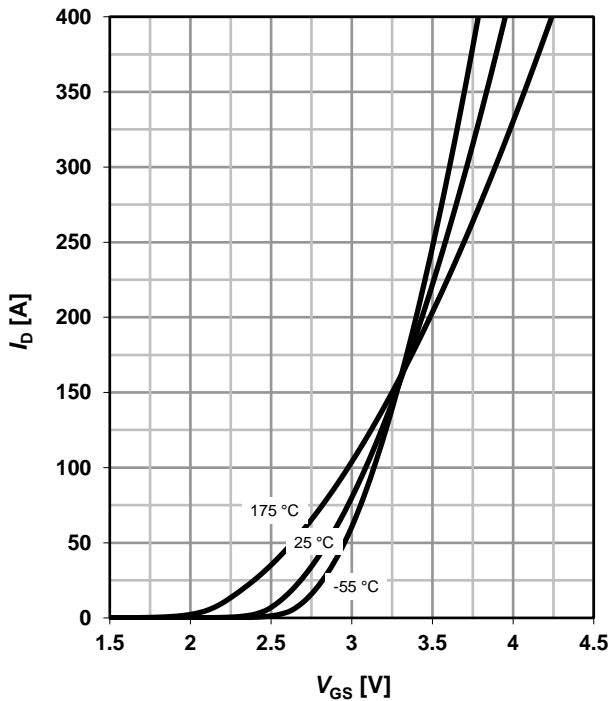
parameter: V_{GS}



7 Typ. transfer characteristics

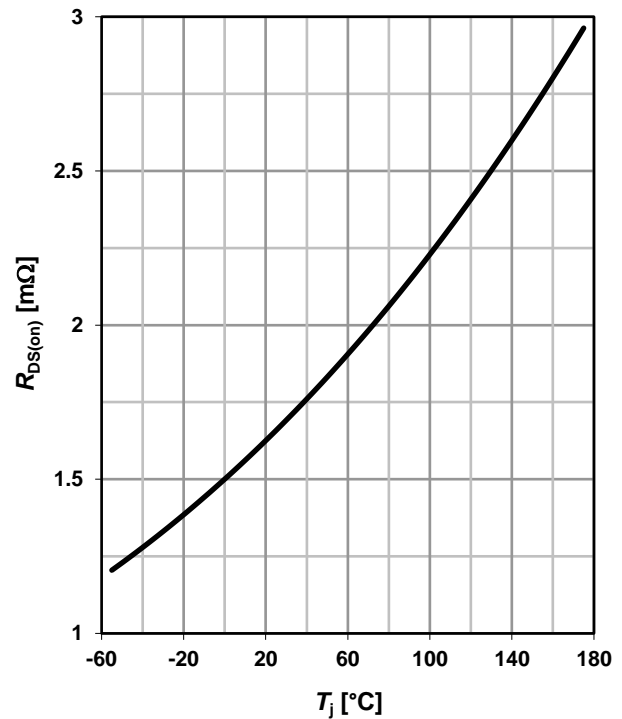
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

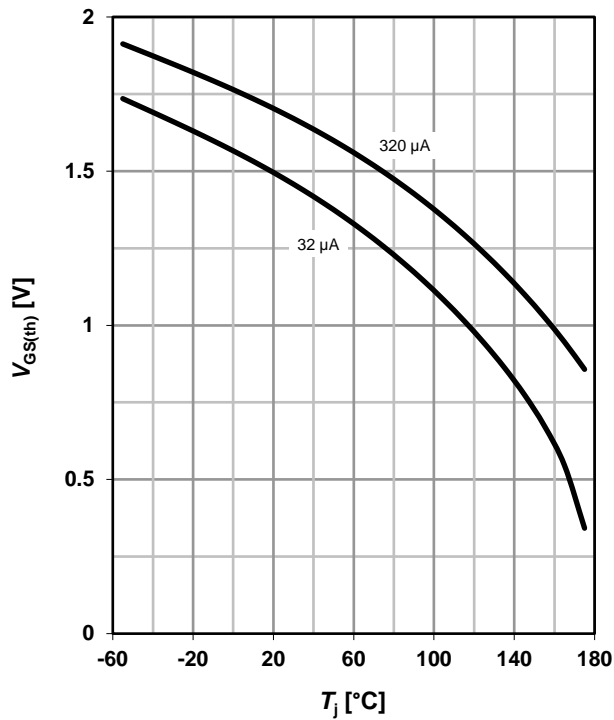
$R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

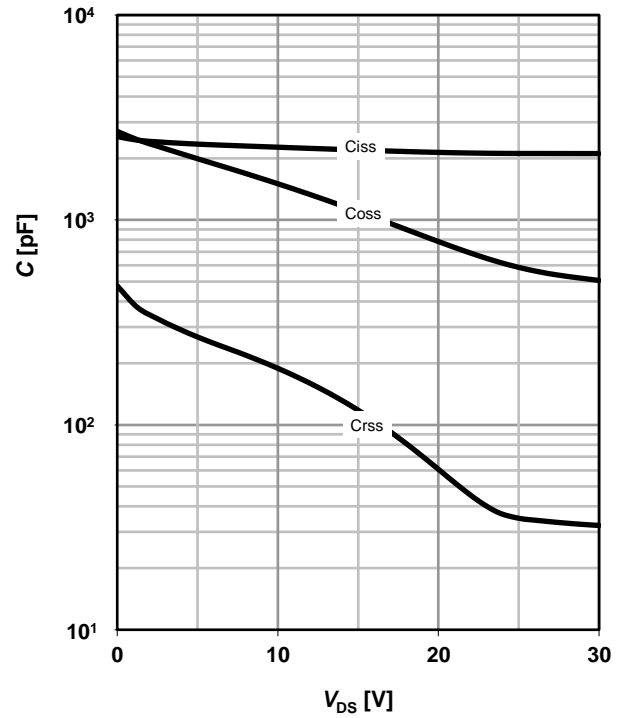
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

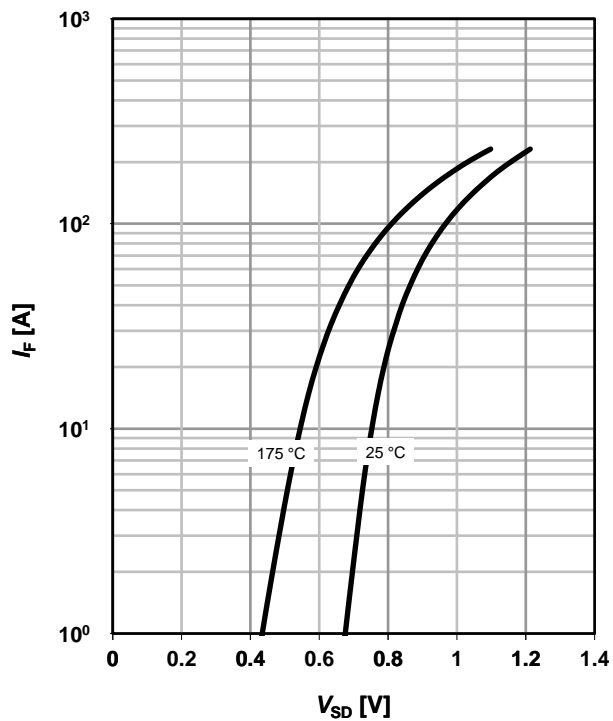
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

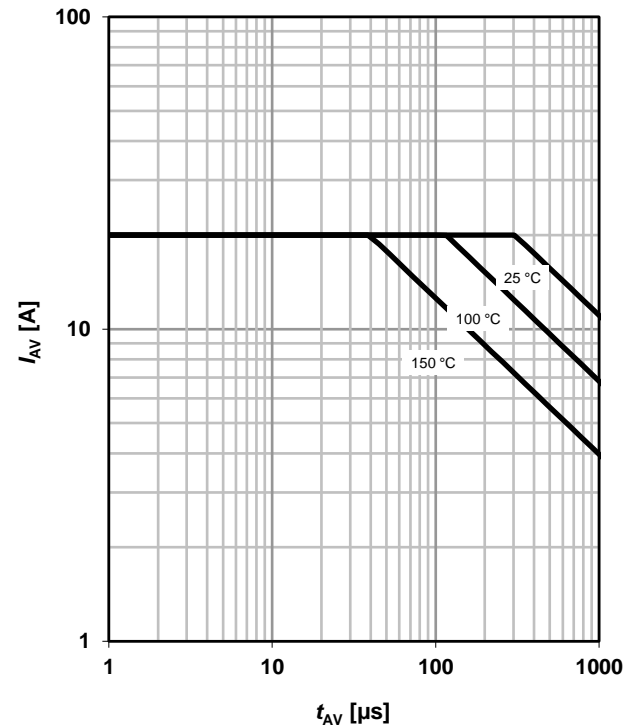
parameter: T_j



12 Avalanche characteristics

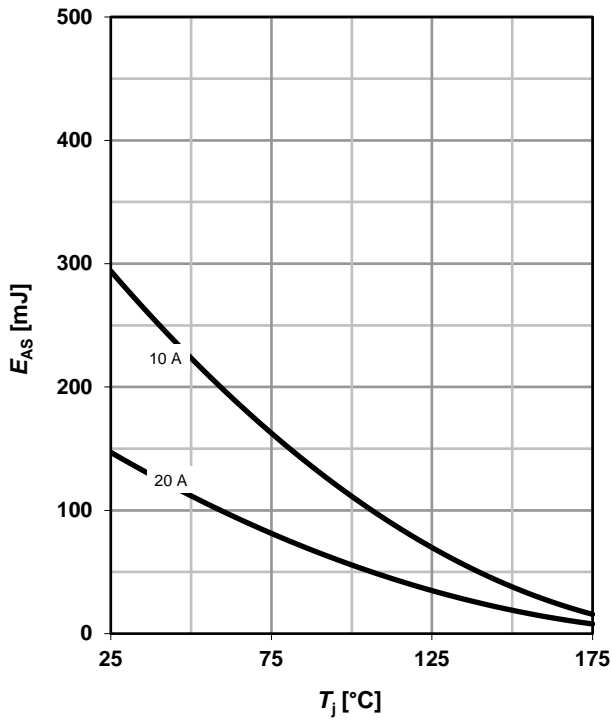
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$

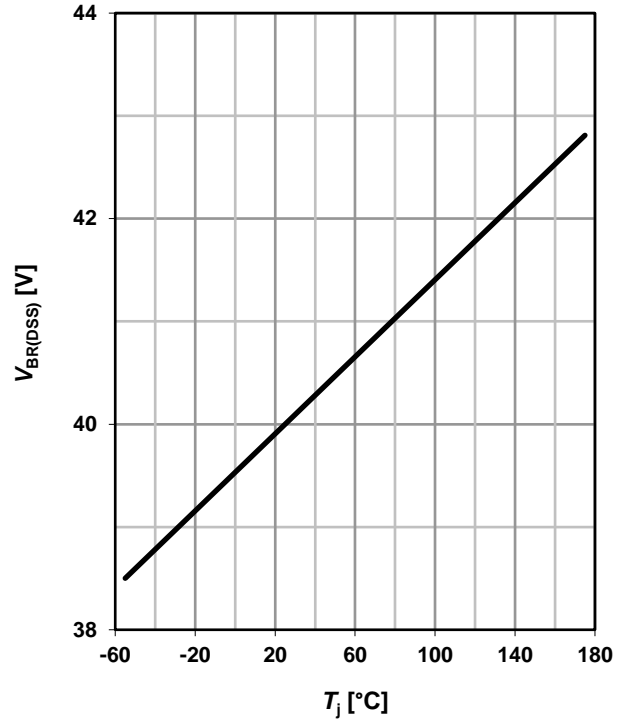


13 Avalanche energy

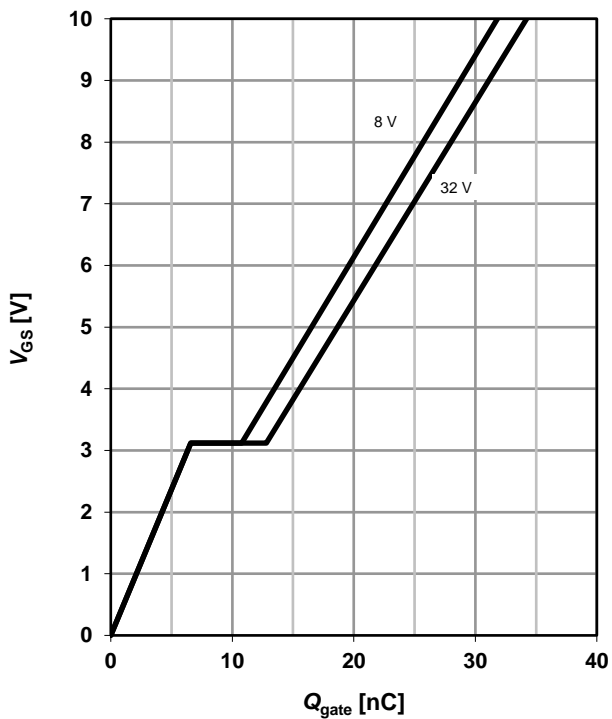
$$E_{AS} = f(T_j)$$


14 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$


15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

 parameter: V_{DD}

16 Gate charge waveforms


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Revision History

Version	Date	Changes