64-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

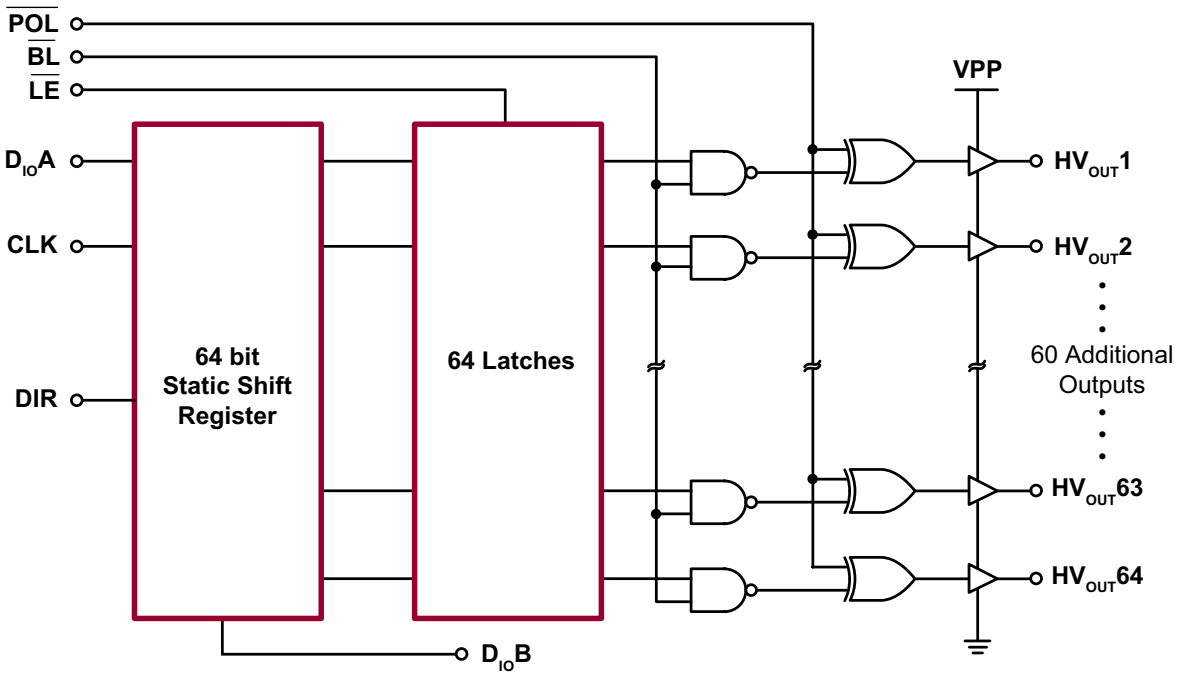
- Processed with HVCMOS® technology
- Output voltages to 180V
- Low power level shifting
- Shift register speed:
  - 6.0MHz @ V_{DD} = 5.0V
  - 12MHz @ V_{DD} = 12V
- Latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

General Description

The HV3418 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for inkjet applications. It can also be used in any application requiring multiple output, high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, $D_{IO}A$ is Data-In and $D_{IO}B$ is Data-Out; data is shifted from $HV_{OUT}64$ to $HV_{OUT}1$. When DIR is at logic high, $D_{IO}B$ is Data-In and $D_{IO}A$ is Data-Out: data is then shifted from $HV_{OUT}1$ to $HV_{OUT}64$. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL(polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) is high. The data in the latch is stored during LE transition from high to low.

Functional Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV3418PG-G	80-Lead PQFP	66/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

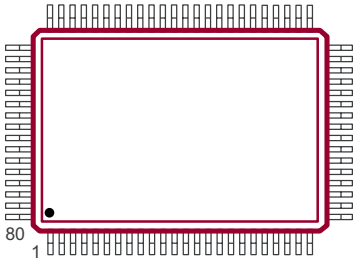
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +15V
Output voltage, V_{PP}	V_{DD} to +200V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current [1]	1.5A
High voltage supply current [1]	1.3A
Continuous total power dissipation [2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

Notes:

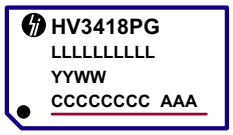
1. *Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambiant derate linearly to maximum operating temperature at 20mW/°C.*

Pin Configuration



80-Lead PQFP
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
____= "Green" Packaging

80-Lead PQFP

Package may or may not include the following marks: Si or

Typical Thermal Resistance

Package	θ_{ja}
80-Lead PQFP	37°C/W

Recommended Operating Conditions

Sym	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage	V_{DD} = 5.0V	4.5	5.0	5.5	V
		V_{DD} = 12V	10.8	12.0	13.2	
V_{PP}	High voltage supply		60	-	180	V
V_{IH}	High-level input voltage		V_{DD} - 0.9	-	V_{DD}	V
V_{IL}	Low-level input voltage		0	-	0.9	V
T_A	Operating free-air temperature		-40	-	+85	°C

Power-up sequence should be the following:

1. *Connect ground*
2. *Apply V_{DD}*
3. *Set all inputs (Data, CLK, Enable, etc.) to a known state*
4. *Apply V_{PP}*

The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	25	mA	f_{CLK} = 12MHz, f_{DATA} = 12MHz, $\overline{LE}$ = low
I_{DDQ}	Quiescent V_{DD} supply current		-	200	µA	All V_{IN} = 0 or V_{DD}
I_{PP}	High voltage supply current		-	0.50	mA	V_{PP} = 180V. All outputs high.
			-	0.50		V_{PP} = 180V. All outputs low.
I_{IH}	High-level logic input current		-	10	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	-10	µA	V_{IL} = 0V
V_{OH}	High level output	HV_{OUT}	155	-	V	V_{PP} = 180V, IHV_{OUT} = -5.0mA, ID_{OUT} = -100µA
		D_{OUT}	V_{DD} - 1.0V	-		
V_{OL}	Low level output	HV_{OUT}	-	25	V	V_{PP} = 180V, IHV_{OUT} = +5.0mA, ID_{OUT} = +100µA
		D_{OUT}	-	1.0		
V_{OC}	HV_{OUT} clamp voltage		-	V_{DD} + 1.5	V	I_{OL} = +5.0mA
			-	-1.5		I_{OL} = -5.0mA

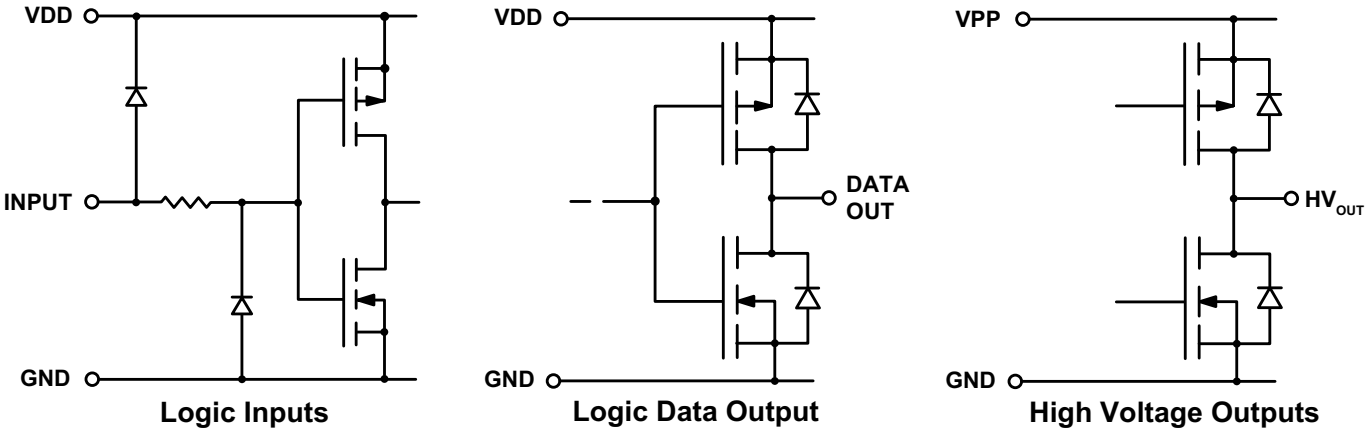
AC Electrical Characteristics *(For V_{DD} = 12V. Values in parentheses are for V_{DD} = 5.0V, V_{PP} = 180V, T_A = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	12 (6.0)	MHz	---
t_W	Clock width high or low	40 (83)	-	ns	---
t_{SU}	Data set-up time before clock rises	25 (35)	-	ns	---
t_H	Data hold time after clock rises	10 (30)	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	62 (80)	-	ns	---
t_{DLE}	Delay time clock to $\overline{LE}$ high to low	25 (35)	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	30 (40)	-	ns	---
t_{ON}, t_{OFF}	Time from $\overline{LE}$ to HV_{OUT}	-	1.0 (1.5)	µs	C_L = 20pF
t_{DHL}	Delay time clock to data high to low	-	50 (110)	ns	C_L = 20pF
t_{DLH}	Delay time clock to data low to high	-	75 (160)	ns	C_L = 20pF
t_R, t_F	All logic inputs	-	5.0	ns	---

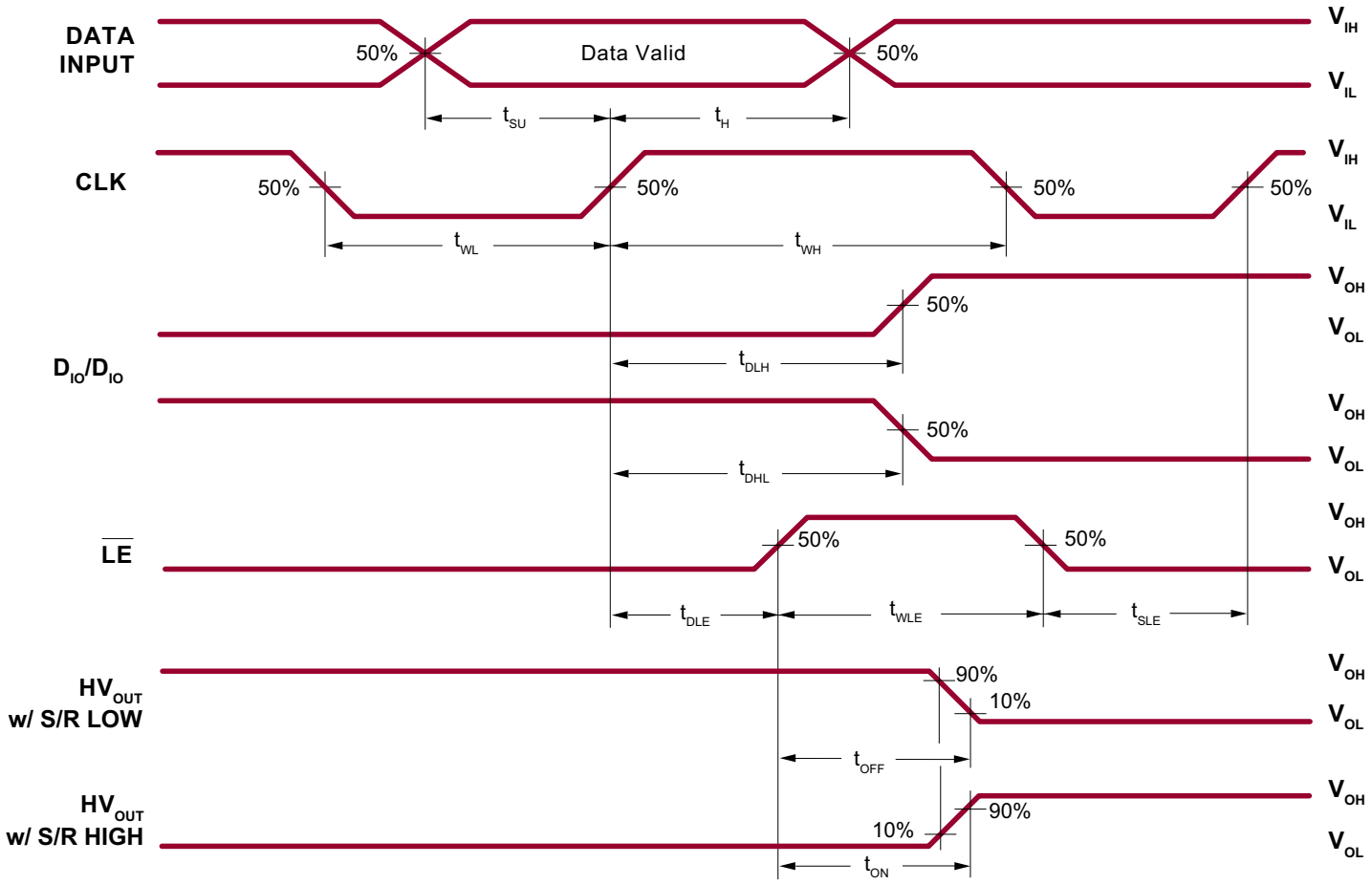
Notes:

1. *Shift register speed can be as low as DC as long as data set-up and hold time meet the spec.*
2. *AC characteristics are guaranteed only under V_{DD} = 12V and V_{DD} = 5.0V.*

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1	Shift Reg 2...64	HV Outputs 1	HV Outputs 2...64	Data Out *
All on	X	X	X	L	L	X	*	*...*	H	H...H	*
All off	X	X	X	L	H	X	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*...*	*	*...*	*
Load/store data in latches	X	X	↓	H	H	X	*	*...*	*	*...*	*
	X	X	↓	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	X	L	*...*	L	*...*	*
	H	↑	H	H	H	X	H	*...*	H	*...*	*
I/O relation	$D_{IO}A$	↑	X	X	X	L	Q_N→	Q_{N+1}	-		$D_{IO}B$
	$D_{IO}B$	↑	X	X	X	H	Q_N→	Q_{N+1}	-		$D_{IO}A$

Notes:

H = high level, L = low level = 0V, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.

* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Pin Description

Pin #	Function
1	HV_{OUT}41/24
2	HV_{OUT}42/23
3	HV_{OUT}43/22
4	HV_{OUT}44/21
5	HV_{OUT}45/20
6	HV_{OUT}46/19
7	HV_{OUT}47/18
8	HV_{OUT}48/17
9	HV_{OUT}49/16
10	HV_{OUT}50/15
11	HV_{OUT}51/14
12	HV_{OUT}52/13
13	HV_{OUT}53/12
14	HV_{OUT}54/11
15	HV_{OUT}55/10
16	HV_{OUT}56/9
17	HV_{OUT}57/8
18	HV_{OUT}58/7
19	HV_{OUT}59/6
20	HV_{OUT}60/5
21	HV_{OUT}61/4
22	HV_{OUT}62/3
23	HV_{OUT}63/2
24	HV_{OUT}64/1
25	VPP
26	D_{IO}A
27	N/C

Pin #	Function
28	N/C
29	$\overline{BL}$
30	$\overline{POL}$
31	VDD
32	DIR
33	LGND
34	OGND
35	N/C
36	N/C
37	CLK
38	$\overline{LE}$
39	D_{IO}B
40	VPP
41	HV_{OUT}1/64
42	HV_{OUT}2/63
43	HV_{OUT}3/62
44	HV_{OUT}4/61
45	HV_{OUT}5/60
46	HV_{OUT}6/59
47	HV_{OUT}7/58
48	HV_{OUT}8/57
49	HV_{OUT}9/56
50	HV_{OUT}10/55
51	HV_{OUT}11/54
52	HV_{OUT}12/53
53	HV_{OUT}13/52
54	HV_{OUT}14/51

Pin #	Function
55	HV_{OUT}15/50
56	HV_{OUT}16/49
57	HV_{OUT}17/48
58	HV_{OUT}18/47
59	HV_{OUT}19/46
60	HV_{OUT}20/45
61	HV_{OUT}21/44
62	HV_{OUT}22/43
63	HV_{OUT}23/42
64	HV_{OUT}24/41
65	HV_{OUT}25/40
66	HV_{OUT}26/39
67	HV_{OUT}27/38
68	HV_{OUT}28/37
69	HV_{OUT}29/36
70	HV_{OUT}30/35
71	HV_{OUT}31/34
72	HV_{OUT}32/33
73	HV_{OUT}33/32
74	HV_{OUT}34/31
75	HV_{OUT}35/30
76	HV_{OUT}36/29
77	HV_{OUT}37/28
78	HV_{OUT}38/27
79	HV_{OUT}39/26
80	HV_{OUT}40/25

Notes:

Pin designation for DIR = H/L

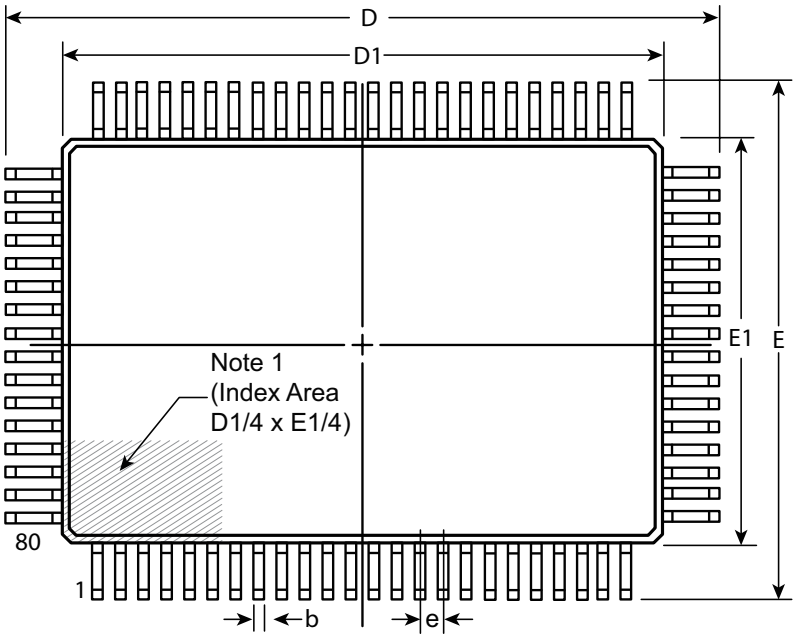
Example:

for DIR = H, Pin 1 is HV_{OUT}41

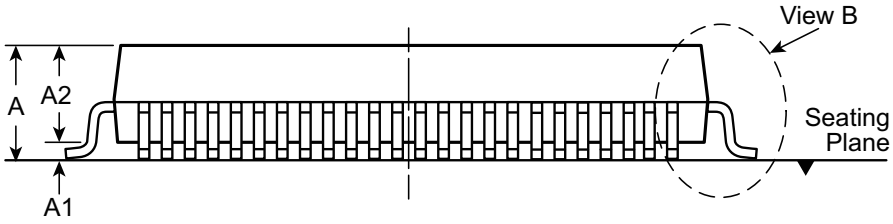
for DIR = L, Pin 1 is HV_{OUT}24

80-Lead PQFP Package Outline (PG)

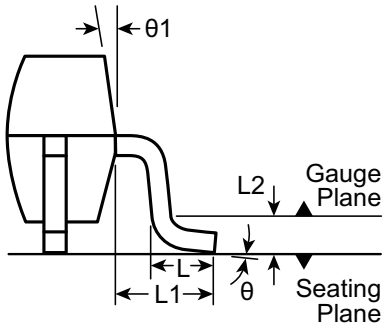
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimen-sion (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-80PQFPPG, Version C041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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