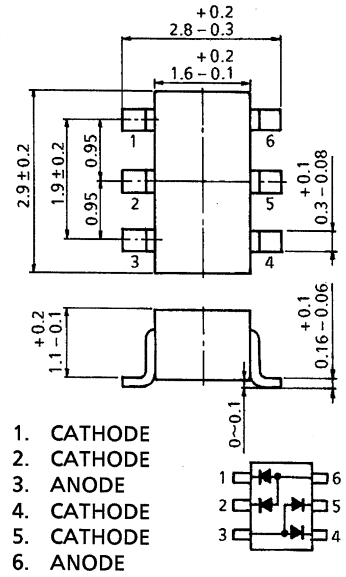
TOSHIBA Diode Silicon Epitaxial Planar Type

HN1D01F

Ultra-High-Speed Switching Applications

- Small package
- Low forward voltage : $V_{F\ (3)}$ = 0.92 V (typ.)
- Fast reverse recovery time : t_{rr} = 1.6 ns (typ.)
- Small total capacitance : C_T = 2.2 pF (typ.)

Unit: mm



JEDEC	—
JEITA	SC-74
TOSHIBA	1-3K1A

Weight: 0.015 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	300 (*)	mA
Average forward current	I_O	100 (*)	mA
Surge current (10 ms)	I_{FSM}	2 (*)	A
Power dissipation	P	300 (*)	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55~125	°C

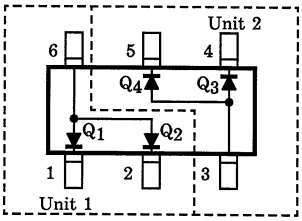
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(*) These are the Absolute Maximum Ratings for a single diode (Q1 or Q2 or Q3 or Q4). If Unit 1 and Unit 2 are used independently or simultaneously, the Absolute Maximum Ratings per diode are 75% of those of a single diode.

Electrical Characteristics (Q_1, Q_2, Q_3, Q_4 Common, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_{F\ (1)}$	—	I_F = 1 mA	—	0.61	—	V
	$V_{F\ (2)}$	—	I_F = 10 mA	—	0.74	—	
	$V_{F\ (3)}$	—	I_F = 100 mA	—	0.92	1.20	
Reverse current	$I_{R\ (1)}$	—	V_R = 30 V	—	—	0.1	μA
	$I_{R\ (2)}$	—	V_R = 80 V	—	—	0.5	
Total capacitance	C_T	—	V_R = 0, f = 1 MHz	—	2.2	4.0	pF
Reverse recovery time	t_{rr}	—	I_F = 10 mA (Fig. 1)	—	1.6	4.0	ns

Pin Assignment (Top View)



Marking

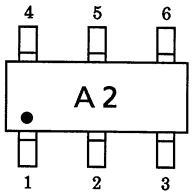
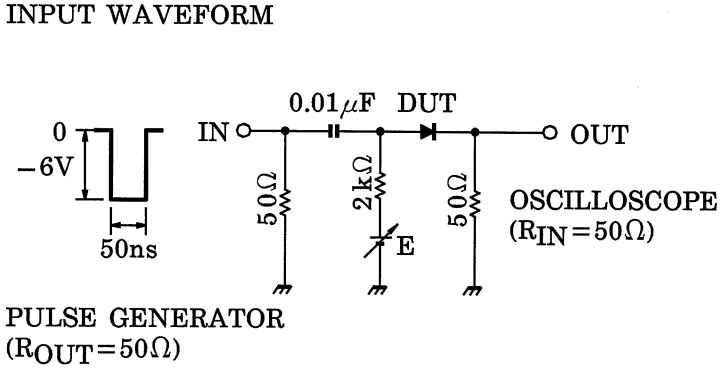
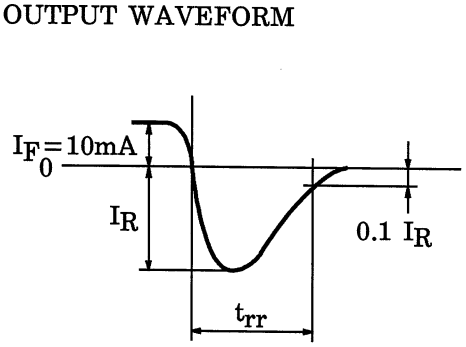
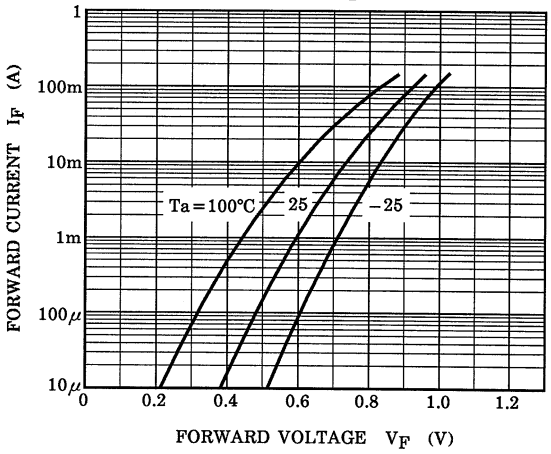


Fig. 1. Reverse Recovery Time (t_{rr}) Test Circuit

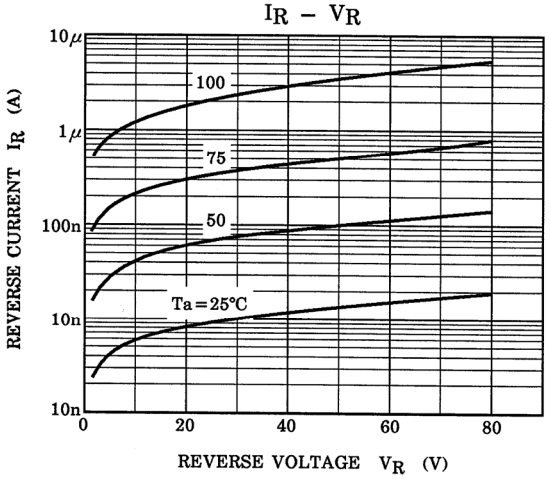




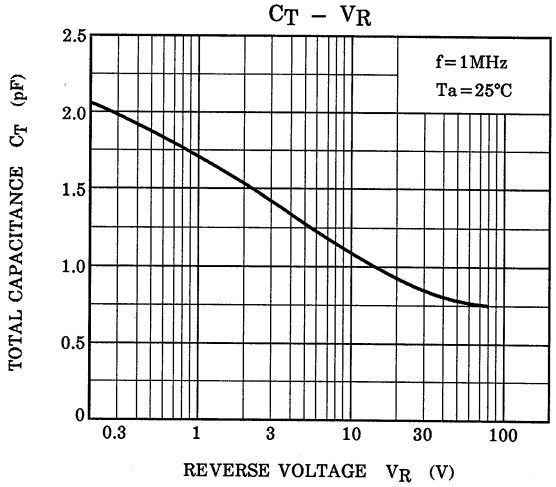
$I_F - V_F$



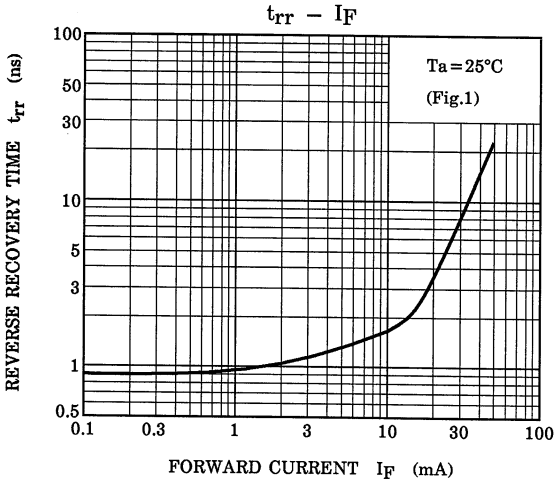
$I_R - V_R$



$C_T - V_R$



$t_{rr} - I_F$



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20070701-EN GENERAL

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