Low Noise, 2:8 Differential Fanout Buffer

Data Sheet

HMC6832

FEATURES

- Ultralow noise floor: −165.9 dBc/Hz or −165.2 dBc/Hz (LVPECL or LVDS) at 2000 MHz
- Configurable to LVPECL or pseudo LVDS outputs
- 2.5 V or 3.3 V LVPECL operation (LVDS 2.5 V only)
- Wideband: 10 MHz to 3500 MHz operating frequency range
- Flexible input interface
  - LVPECL, LVDS, CML, and CMOS compatible
  - AC or dc coupling
  - On-chip 50 kΩ pull-up/pull-down resistors to VDD and GND
- Multiple output drivers
  - Up to 8 differential or 16 single-ended LVPECL or LVDS outputs
- Low speed digital control via the IN_SEL and CONFIG pins
- 28-lead, 5 mm × 5 mm, LFCSP package, 25 mm²

APPLICATIONS

- SONET, Fibre Channel, GigE clock distribution
- ADC/DAC clock distribution
- Low skew and jitter clocks
- Wireless/wired communications
- Level translation
- High performance instrumentation
- Medical imaging
- Single-ended to differential conversions

GENERAL DESCRIPTION

The HMC6832 is an input selectable, 2:8 differential fanout buffer designed for low noise clock distribution. The IN_SEL control pin selects one of the two differential inputs. This input is then buffered to all eight differential outputs. The low jitter outputs of the HMC6832 lead to synchronized low noise switching of downstream circuits, such as mixers, analog-to-digital converters (ADCs)/digital-to-analog converters (DACs), or serializer/deserializer (SERDES) devices. The device is capable of low voltage, positive emitter-coupled logic (LVPECL) or low voltage differential signaling (LVDS) configurations by pulling the CONFIG pin low for LVPECL or high or open (internally pulled high) for pseudo LVDS.

PRODUCT HIGHLIGHTS

1. Multiple Output Configurations.
   The CONFIG pin allows the user to select LVPECL or LVDS output termination.
2. Multiple Supply Voltage Operation.
   The HMC6832 operates at 2.5 V or 3.3 V for LVPECL terminations (2.5 V only for LVDS).
3. Low Noise.
   The HMC6832 noise is low, typically from −168 dBc/Hz to −162 dBc/Hz up to 3000 MHz.
4. Low Propagation Delay.
   The HMC6832 displays a low delay, less than 207 ps, typical. Channel skew is also low, ±5 ps, typical.
5. Low Core Current.
   The HMC6832 has a low core current of 56 mA, typical.

Rev. C
Document Feedback

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1/2018—Rev. B to Rev. C

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3/2016—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

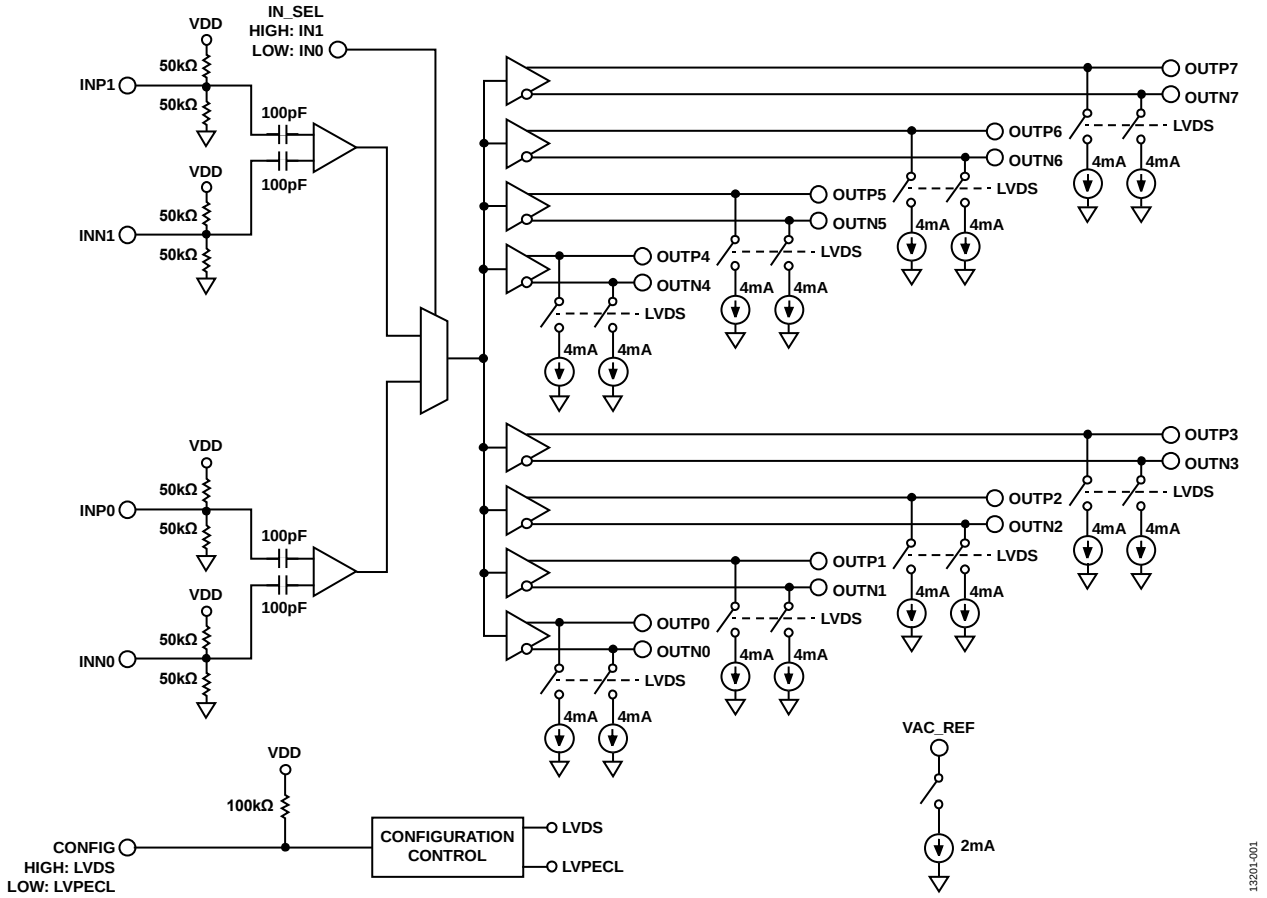


Figure 1.

SPECIFICATIONS

Typical is given as f_{INPUT} = 1.25 GHz (ac-coupled), differential input power = 7.5 dBm, $T_{NOMINAL}$ = 25°C, unless otherwise noted. All outputs captured using 50 Ω scope termination. 50 Ω board termination on inputs used to minimize reflections.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS					
VDD					
LVPECL	2.375	2.5	2.625	V	2.5 V operation
	3.0	3.3	3.6	V	3.3 V operation
LVDS	2.375	2.5	2.625	V	
Input Common-Mode Voltage	GND + 0.2	VDD/2	VDD − 0.2	V	Guaranteed by design
SELECTION PINS					
IN_SEL Pin					GND = IN0, VDD = IN1
Input Voltage Low (V_{IL})			VDD/2 − 0.4	V	
Input Voltage High (V_{IH})	VDD/2 + 0.4			V	
CONFIG Pin					GND = LVPECL, VDD = LVDS
Input Voltage Low (V_{IL})			2VDD/3 − 0.3	V	
Input Voltage High (V_{IH})	2VDD/3 + 0.3			V	
TEMPERATURE RANGE, T_A	−40	+25	+85	°C	
SUPPLY CURRENT					Outputs unterminated
Core Current		56		mA	VDD = 2.5 V
		56		mA	VDD = 3.3 V
Full Load Current					
LVPECL Termination		301		mA	R_{TERM}[1] = 86 Ω, VDD = 2.5 V
		283		mA	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		125		mA	R_{TERM} = 100 Ω
RF INPUT CHARACTERISTICS					
Operating Frequency Range	10		3500	MHz	
Input Swing (Single-Ended)	0.1		2	V	
Input Capacitance		3.6		pF	
Pull-Up/Pull-Down Resistance		50		kΩ	See Figure 1

[1] For LVPECL termination, R_{TERM} is the single-ended termination resistance to GND. For LVDS termination, R_{TERM} is the differential termination resistance.

AC OUTPUT CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OUTPUT VOLTAGE SWING					Differential inputs and outputs; adjusted for impedance mismatch and printed circuit board (PCB) losses; see Figure 41 and Figure 42 for ac measurement test circuits
LVPECL Termination		652		mV p-p	R_{TERM} = 86 Ω, VDD = 2.5 V
		721		mV p-p	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		462		mV p-p	R_{TERM} = 100 Ω, VDD = 2.5 V
OUTPUT VOLTAGE, HIGH LEVEL					Differential inputs and outputs
LVPECL Termination		1.63		V	R_{TERM} = 86 Ω, VDD = 2.5 V
		2.51		V	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		1.65		V	R_{TERM} = 100 Ω, VDD = 2.5 V
OUTPUT VOLTAGE, COMMON LEVEL					Differential inputs and outputs; see Figure 39 and Figure 40 for dc measurement test circuits
LVPECL Termination		1.30		V	R_{TERM} = 86 Ω, VDD = 2.5 V
		2.15		V	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		1.42		V	R_{TERM} = 100 Ω, VDD = 2.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE, LOW LEVEL					Differential inputs and outputs
LVPECL Termination		0.97		V	R_{TERM} = 86 Ω, VDD = 2.5 V
		1.79		V	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		1.19		V	R_{TERM} = 100 Ω, VDD = 2.5 V
AC PERFORMANCE					See Figure 41 and Figure 42 for ac measurement test circuits
3 dB Bandwidth					Adjusted for impedance mismatch and PCB losses; refer to Figure 19 and Figure 21
LVPECL Differential Input		1600		MHz	Differential input = 100 mV p-p; VDD = 2.5 V
		2500		MHz	Differential input = 200 mV p-p; VDD = 2.5 V
		3200		MHz	Differential input = 400 mV p-p; VDD = 2.5 V
LVDS Differential Input		1750		MHz	Differential input = 100 mV p-p; VDD = 2.5 V
		2550		MHz	Differential input = 200 mV p-p; VDD = 2.5 V
		4100		MHz	Differential input = 400 mV p-p; VDD = 2.5 V
Output Rise Time (20% to 80%)					Differential inputs and outputs
LVPECL Termination		56		ps	R_{TERM} = 86 Ω, VDD = 2.5 V
		57		ps	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		45		ps	R_{TERM} = 100 Ω, VDD = 2.5 V
Output Fall Time (20% to 80%)					Differential inputs and outputs
LVPECL Termination		59		ps	R_{TERM} = 86 Ω, VDD = 2.5 V
		59		ps	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		46		ps	R_{TERM} = 100 Ω, VDD = 2.5 V
Duty Cycle Variation					Differential inputs and outputs
LVPECL Termination		50		%	R_{TERM} = 86 Ω, VDD = 2.5 V
		50		%	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		50		%	R_{TERM} = 100 Ω, VDD = 2.5 V
Power Supply Rejection Ratio					50 kHz, 100 mV p-p sinusoidal signal modulated onto VDD; single-ended 1 GHz, 0 dBm input; outputs measured differentially
LVPECL Termination		−55		dBc	R_{TERM} = 86 Ω, VDD = 2.5 V
		−59		dBc	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		−52		dBc	R_{TERM} = 100 Ω, VDD = 2.5 V

OUTPUT GAIN AND POWER CHARACTERISTICS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL SMALL SIGNAL GAIN (S21)					Adjusted for impedance mismatch and printed circuit board (PCB) losses
LVPECL Termination					
		25		dB	R_{TERM} = 86 Ω, VDD = 2.5 V
		26		dB	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		22		dB	R_{TERM} = 100 Ω, VDD = 2.5 V
INPUT 1 dB COMPRESSION POINT (P1dB)					1250 MHz, adjusted for impedance mismatch and PCB losses
LVPECL Termination		−25		dBm	R_{TERM} = 86 Ω, VDD = 2.5 V
		−25		dBm	R_{TERM} = 150 Ω, VDD = 3.3 V
LVDS Termination		−26		dBm	R_{TERM} = 100 Ω, VDD = 2.5 V
SATURATED POWER IN FUNDAMENTAL TONE (SINGLE-ENDED)					VDD = 2.5 V, adjusted for impedance mismatch and PCB losses
LVPECL Termination					
1000 MHz		−4		dBm	−4 dBm = 399 mV p-p
2000 MHz		−2		dBm	−2 dBm = 502 mV p-p
3000 MHz		−5		dBm	−5 dBm = 356 mV p-p

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS Termination					
1000 MHz		−7		dBm	−7 dBm = 283 mV p-p
2000 MHz		−7		dBm	−7 dBm = 283 mV p-p
3000 MHz		−7		dBm	−7 dBm = 283 mV p-p
HARMONICS					VDD = 2.5 V, adjusted for impedance mismatch and PCB losses, f_{INPUT} = 2 GHz
LVPECL Termination					
f_{OUT}		−2		dBm	−2 dBm = 502 mV p-p
2 × f_{OUT}		−28		dBc	
3 × f_{OUT}		−17		dBc	
4 × f_{OUT}		−38		dBc	
5 × f_{OUT}		−24		dBc	
LVDS Termination					
f_{OUT}		−7		dBm	−7 dBm = 283 mV p-p
2 × f_{OUT}		−22		dBc	
3 × f_{OUT}		−16		dBc	
4 × f_{OUT}		−38		dBc	
5 × f_{OUT}		−29		dBc	
OUTPUT RETURN LOSS < 10 dB		<6		GHz	LVDS termination

Table 4. Jitter

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FLOOR DENSITY JITTER					Single-ended input; differential output; measured with saturated amplifier to remove amplitude modulation (AM) noise (only affects 100 MHz data); LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω; VDD = 2.5 V; see Figure 43 and Figure 44 for phase noise measurement test circuits
Input Carrier Frequency					
LVPECL Termination					
100 MHz		13.09		as/√Hz	
622 MHz		1.61		as/√Hz	
1000 MHz		1.26		as/√Hz	
1600 MHz		0.91		as/√Hz	
1750 MHz		0.81		as/√Hz	
2000 MHz		0.64		as/√Hz	
3000 MHz		0.51		as/√Hz	
LVDS Termination					
100 MHz		15.55		as/√Hz	
622 MHz		1.63		as/√Hz	
1000 MHz		1.21		as/√Hz	
1600 MHz		0.80		as/√Hz	
1750 MHz		0.72		as/√Hz	
2000 MHz		0.69		as/√Hz	
3000 MHz		0.64		as/√Hz	
INTEGRATED RMS JITTER					Single-ended input; differential output; measured with saturated amplifier to remove AM noise (only affects 100 MHz data); LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω; VDD = 2.5 V; see Figure 43 and Figure 44 for phase noise measurement test circuits
100 MHz Carrier Frequency					
LVPECL Termination					
60 kHz to 10 MHz		37		fs rms	
60 kHz to 20 MHz		52		fs rms	
60 kHz to 40 MHz		74		fs rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS Termination					
60 kHz to 10 MHz		44		fs rms	
60 kHz to 20 MHz		62		fs rms	
60 kHz to 40 MHz		88		fs rms	
622.06 MHz Carrier Frequency					
LVPECL Termination					
10 MHz to 80 MHz		12		fs rms	
10 MHz to 100 MHz		14		fs rms	
LVDS Termination					
10 MHz to 80 MHz		12		fs rms	
10 MHz to 100 MHz		14		fs rms	
1000 MHz Carrier Frequency					
LVPECL Termination					
10 MHz to 80 MHz		9		fs rms	
10 MHz to 100 MHz		11		fs rms	
LVDS Termination					
10 MHz to 80 MHz		10		fs rms	
10 MHz to 100 MHz		10		fs rms	
1600 MHz Carrier Frequency					
LVPECL Termination					
10 MHz to 80 MHz		7		fs rms	
10 MHz to 100 MHz		8		fs rms	
LVDS Termination					
10 MHz to 80 MHz		6		fs rms	
10 MHz to 100 MHz		7		fs rms	
2000 MHz Carrier Frequency					
LVPECL Termination					
10 MHz to 80 MHz		5		fs rms	
10 MHz to 100 MHz		6		fs rms	
LVDS Termination					
10 MHz to 80 MHz		5		fs rms	
10 MHz to 100 MHz		6		fs rms	
3000 MHz Carrier Frequency					
LVPECL Termination					
10 MHz to 80 MHz		3		fs rms	
10 MHz to 100 MHz		4		fs rms	
LVDS Termination					
10 MHz to 80 MHz		4		fs rms	
10 MHz to 100 MHz		5		fs rms	

Table 5. Phase Noise Floor

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SINGLE-SIDEBAND (SSB PHASE NOISE FLOOR)					Single-ended input; differential output; measured with saturated amplifier to remove AM noise (only affects 100 MHz data); LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω; VDD = 2.5 V; see Figure 43 and Figure 44 for phase noise measurement test circuits
Input Carrier Frequency					
LVPECL Termination					
100 MHz		−165.7		dBc/Hz	
622 MHz		−168.0		dBc/Hz	
1000 MHz		−166.0		dBc/Hz	
1600 MHz		−164.8		dBc/Hz	
1750 MHz		−165.0		dBc/Hz	
2000 MHz		−165.9		dBc/Hz	
3000 MHz		−164.4		dBc/Hz	
LVDS Termination					
100 MHz		−164.2		dBc/Hz	
622 MHz		−167.9		dBc/Hz	
1000 MHz		−166.4		dBc/Hz	
1600 MHz		−165.9		dBc/Hz	
1750 MHz		−166.0		dBc/Hz	
2000 MHz		−165.2		dBc/Hz	
3000 MHz		−162.4		dBc/Hz	

TIMING CHARACTERISTICS

T_A = 25°C, unless otherwise noted. Minimum/maximum values are guaranteed by design and characterization.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TYPICAL CHANNEL SKEW		±5		ps	Relative to OUTP5, VDD = 2.5 V or 3.3 V
TYPICAL PROPAGATION DELAY					
LVPECL Termination		201		ps	VDD = 2.375 V to 3.6 V
LVDS Termination		207		ps	VDD = 2.375 V to 2.625 V
TYPICAL DELAY VARIATION					
At T_A = 25°C					
LVPECL Termination		±5		ps	VDD = 2.375 V to 3.6 V, measurement uncertainty = ±2 ps
LVDS Termination		±5		ps	VDD = 2.375 V to 2.625 V, measurement uncertainty = ±2 ps
At T_A = −40°C to +85°C					
LVPECL Termination		±13		ps	VDD = 2.375 V to 3.6 V, measurement uncertainty = ±4 ps
LVDS Termination		±13		ps	VDD = 2.375 V to 2.625 V, measurement uncertainty = ±4 ps
PROCESS PROPAGATION DELAY VARIATION	−18		+18	ps	Process simulation, VDD = 2.5 V

TIMING SPECIFICATIONS

VDD = 2.5 V or 3.3 V, T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Typical	Unit	Description
t_{SKEW}	±5	ps	Output skew
t_R	57/45	ps	Output rise/fall time (LVPECL/LVDS)
t_F	59/46	ps	Output rise/fall time (LVPECL/LVDS)
t_D	201/207	ps	Propagation delay (LVPECL/LVDS)

Timing Diagram

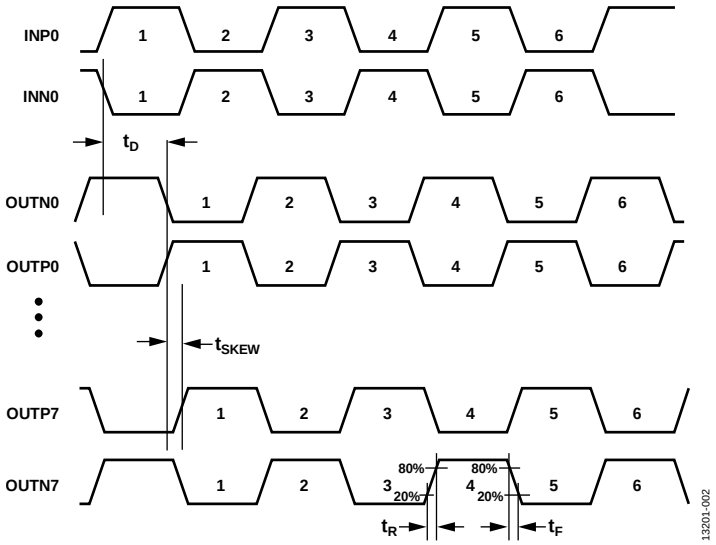


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Maximum Voltage Between VDD Pins and EPAD	−0.3 V to +4 V
Maximum RF Power to INPx and INNx	15 dBm, single-ended
INPx and INNx	−0.3 V to +3.6 V
Minimum Output Load Resistor	
LVPECL (VDD = 2.5 V)	75 Ω to GND
LVPECL (VDD = 3.3 V)	100 Ω to GND
LVPECL Output Load Current	40 mA/single-ended output channel
Input Select Voltage Range	−0.3 V to +3.6 V
Maximum VAC_REF Load Current	2 mA
Maximum Reflow Temperature (MSL3 Rating)	260°C
ESD Sensitivity	
Human Body Model (HBM)	Class 1C
Field Induced Charged Device Model (FICDM)	Class C4

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 9. Thermal Resistance

Package Type	θ_{JC}	Unit
28-Lead LFCSP	10.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

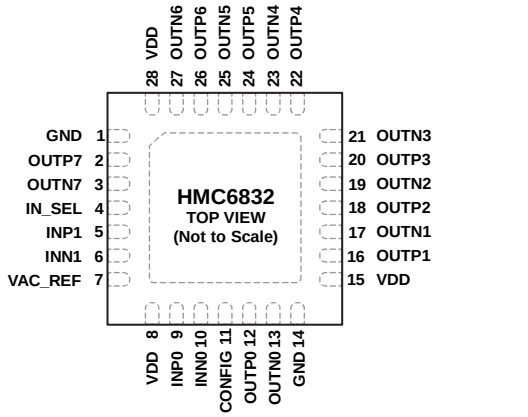


Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	OUTP7	Differential Signal Output 7, Positive.
3	OUTN7	Differential Signal Output 7, Negative.
4	IN_SEL	Input Select. Logic 0 = INP0/INN0 and Logic 1 = INP1/INN1.
5	INP1	Differential Signal Input 1, Positive.
6	INN1	Differential Signal Input 1, Negative.
7	VAC_REF	Output Reference Voltage.
8	VDD	Power Supply.
9	INP0	Differential Signal Input 0, Positive.
10	INN0	Differential Signal Input 0, Negative.
11	CONFIG	Output Termination Configuration Input. Logic 0 = LVPECL and Logic 1 = LVDS.
12	OUTP0	Differential Signal Output 0, Positive.
13	OUTN0	Differential Signal Output 0, Negative.
14	GND	Ground.
15	VDD	Power Supply.
16	OUTP1	Differential Signal Output 1, Positive.
17	OUTN1	Differential Signal Output 1, Negative.
18	OUTP2	Differential Signal Output 2, Positive.
19	OUTN2	Differential Signal Output 2, Negative.
20	OUTP3	Differential Signal Output 3, Positive.
21	OUTN3	Differential Signal Output 3, Negative.
22	OUTP4	Differential Signal Output 4, Positive.
23	OUTN4	Differential Signal Output 4, Negative.
24	OUTP5	Differential Signal Output 5, Positive.
25	OUTN5	Differential Signal Output 5, Negative.
26	OUTP6	Differential Signal Output 6, Positive.
27	OUTN6	Differential Signal Output 6, Negative.
28	VDD	Power Supply.
	EPAD	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical is given as f_{INPUT} = 1.25 GHz (ac-coupled), differential input power = 7.5 dBm, $T_{NOMINAL}$ = 25°C, unless otherwise noted. All outputs captured using 50 Ω scope termination. Used 50 Ω board termination on inputs to minimize reflections.

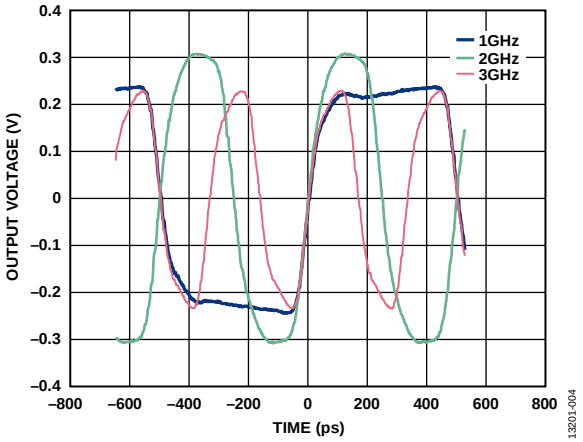


Figure 4. LVPECL Differential Output Voltage, 86 Ω, 2.5 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

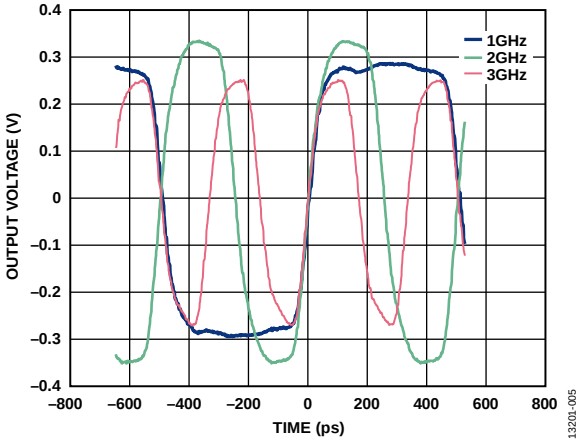


Figure 5. LVPECL Differential Output Voltage, 150 Ω, 3.3 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

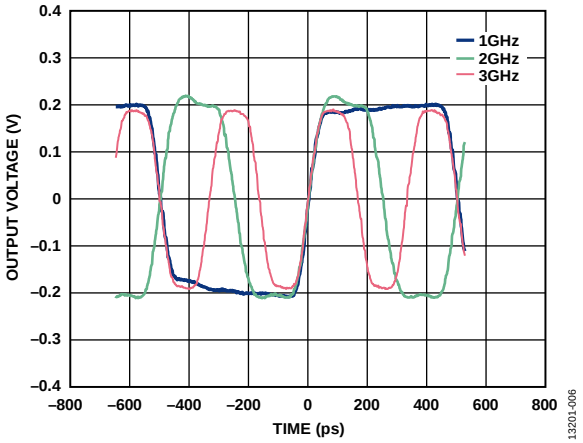


Figure 6. LVDS Differential Output Voltage, 100 Ω, 2.5 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

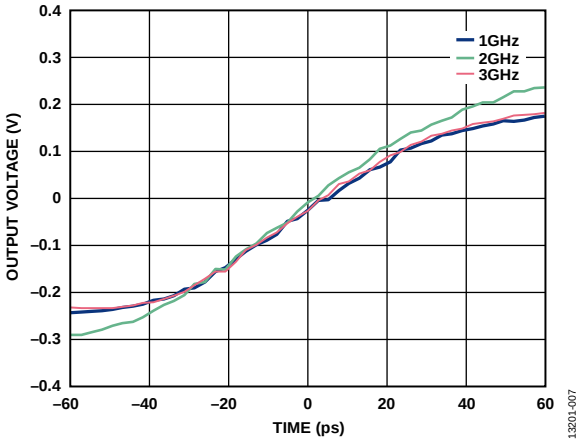


Figure 7. LVPECL Differential Output Voltage, 86 Ω, 2.5 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

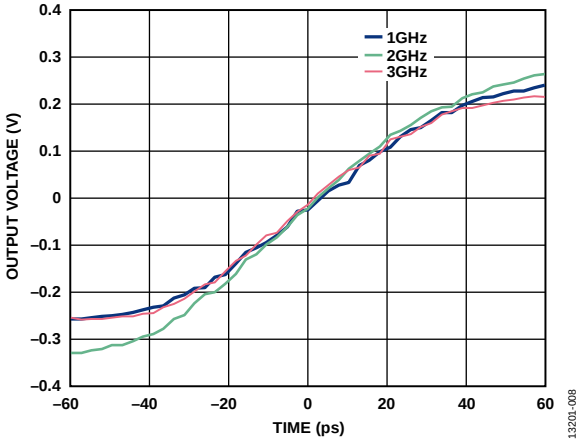


Figure 8. LVPECL Differential Output Voltage, 150 Ω, 3.3 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

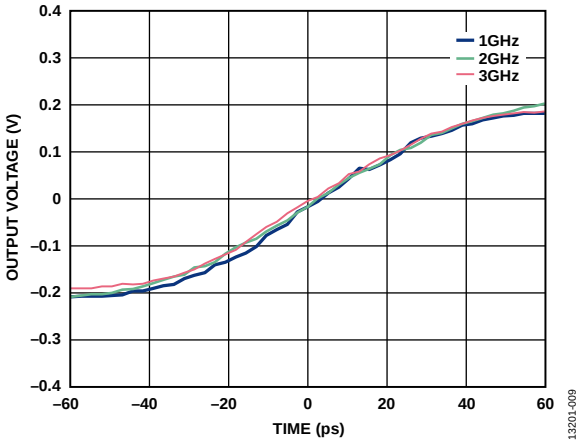


Figure 9. LVDS Differential Output Voltage, 100 Ω, 2.5 V vs. Carrier Frequency over Time, 2 dBm Input, Uncorrected for Board Loss, and Measurement Band Limited by the Trace Bandwidth

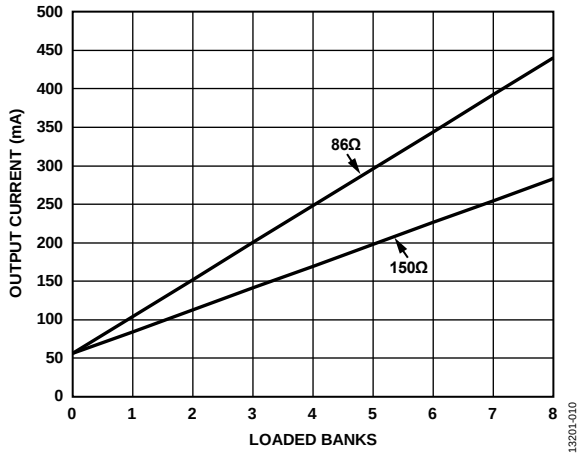


Figure 10. 3.3 V Current Consumption vs. Loaded Banks for Given LVPECL R_{TERM} Values

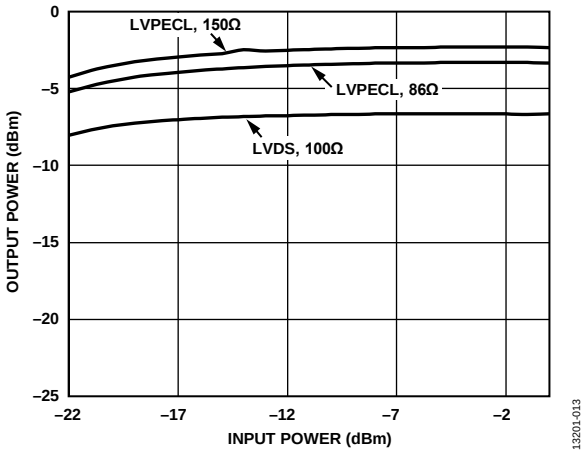


Figure 13. 1.25 GHz Fundamental Differential Output Power vs. Differential Input Power, Uncorrected for Impedance Mismatch

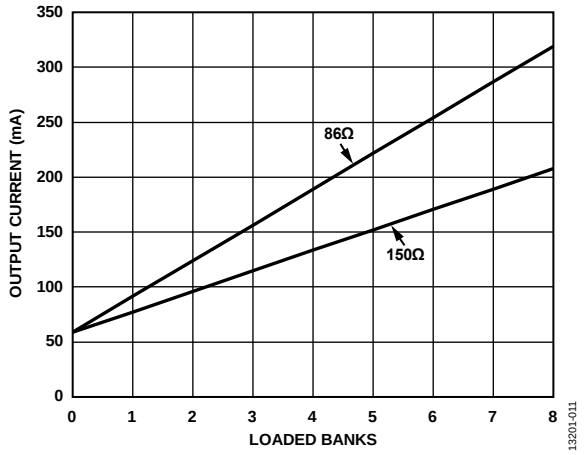


Figure 11. 2.5 V Current Consumption vs. Loaded Banks for Given LVPECL R_{TERM} Values

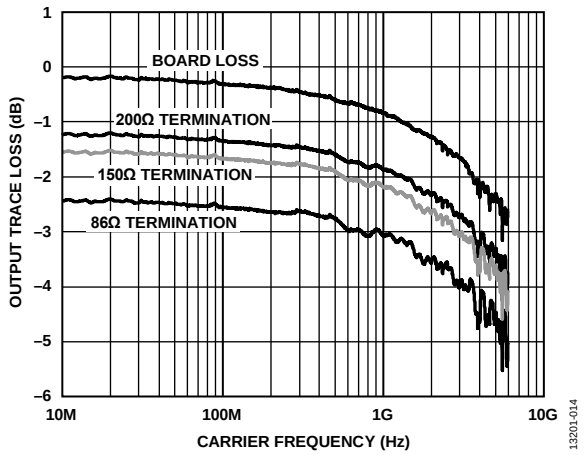


Figure 14. LVPECL Evaluation Board Output Trace Loss and Distortion from Impedance Mismatch vs. Carrier Frequency

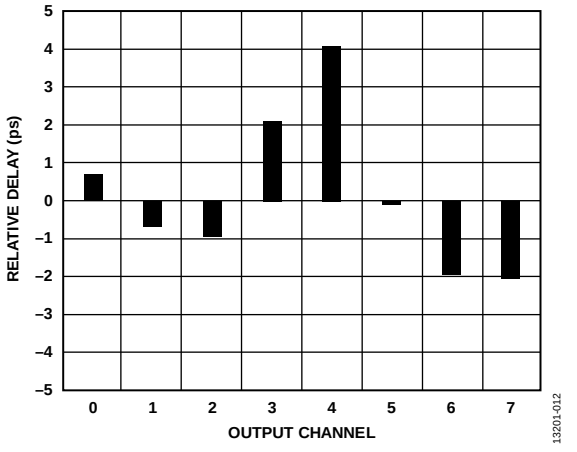


Figure 12. Skew of Outputs Relative to Average Delay, Characterized at 1.25 GHz; Effects of Customer Evaluation Board Skew and Loss Are De-Embedded

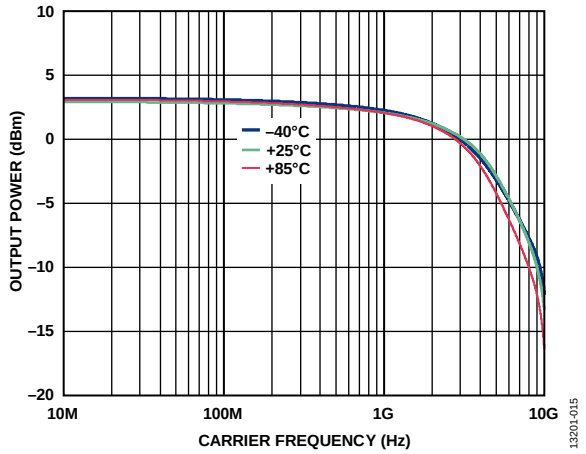


Figure 15. LVPECL 2.5 V Differential Output Power vs. Carrier Frequency for Various Temperatures, 0 dBm Input, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

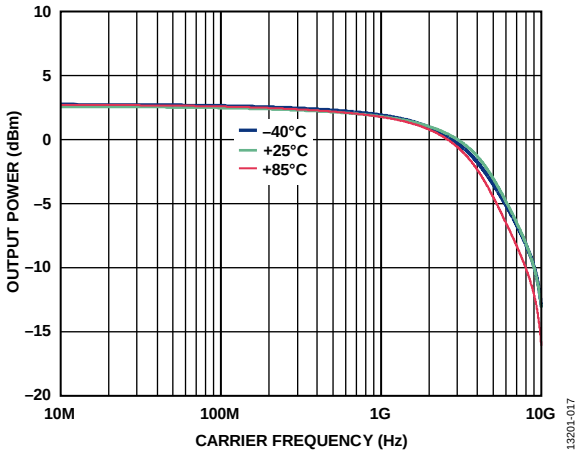


Figure 16. LVPECL 3.3 V Differential Output Power vs. Carrier Frequency for Various Temperatures, 0 dBm Input, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

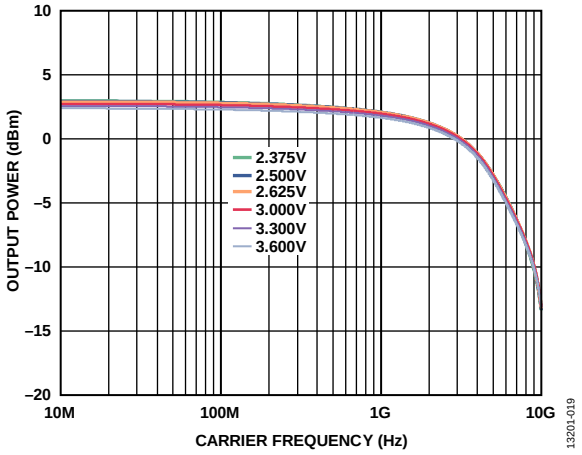


Figure 17. LVPECL Differential Output Power vs. Carrier Frequency for Various Supplies, 0 dBm Input, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

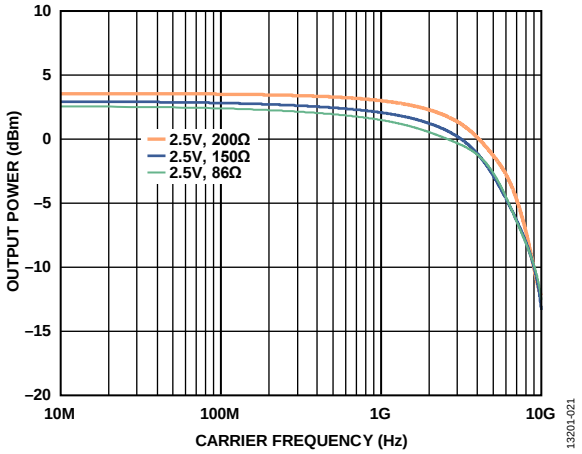


Figure 18. LVPECL Differential Output Power vs. Carrier Frequency for Various Terminations, 0 dBm Input, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

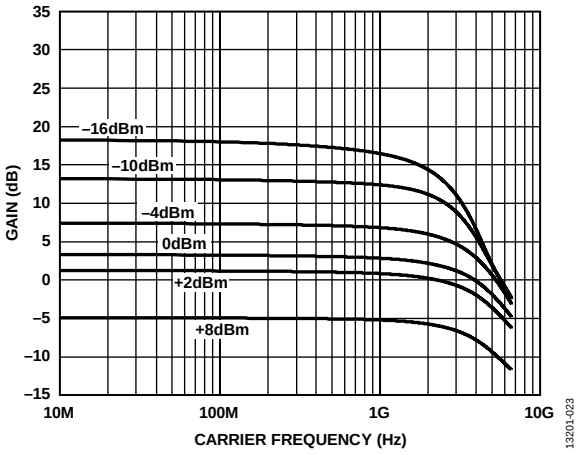


Figure 19. LVPECL 2.5 V, 150 Ω Differential Gain vs. Carrier Frequency for Various Input Powers, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

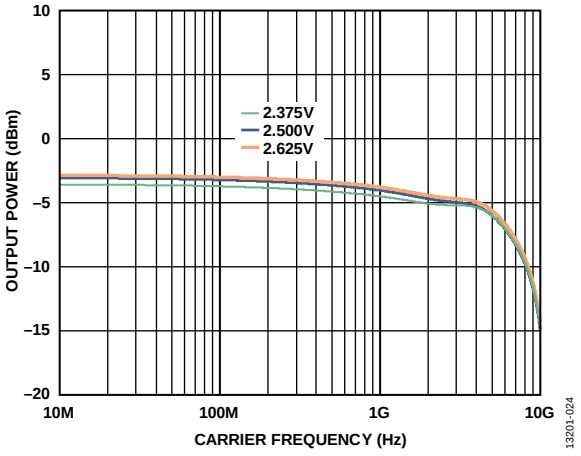


Figure 20. LVDS Differential Output Power vs. Carrier Frequency for Various Supplies, 0 dBm Input, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

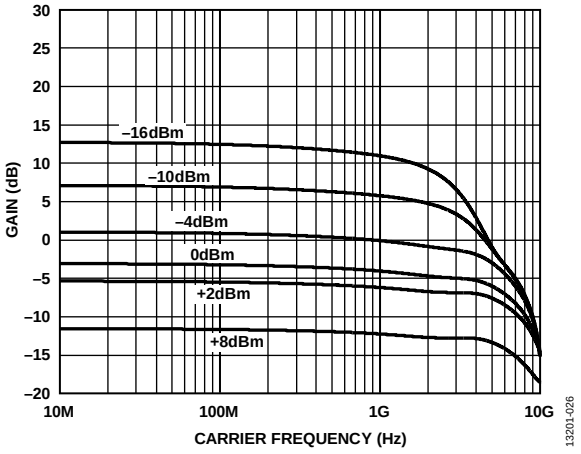


Figure 21. LVDS Differential Gain vs. Carrier Frequency for Various Input Powers with 100 Ω, Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

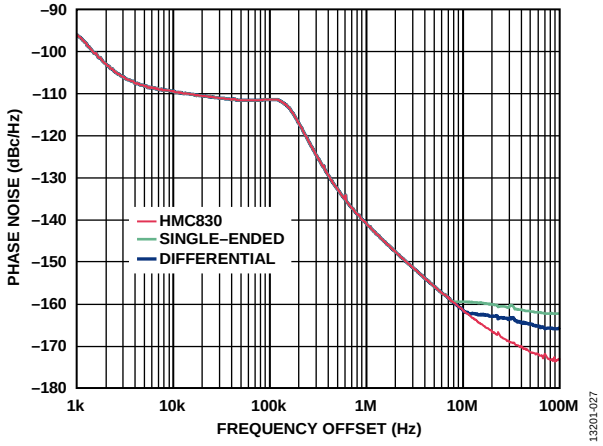


Figure 22. Phase Noise Performance at 2 GHz, 2.5 V Supply, HMC830 Used as Signal Source; Driving 9 dBm Single-Ended Through Balun

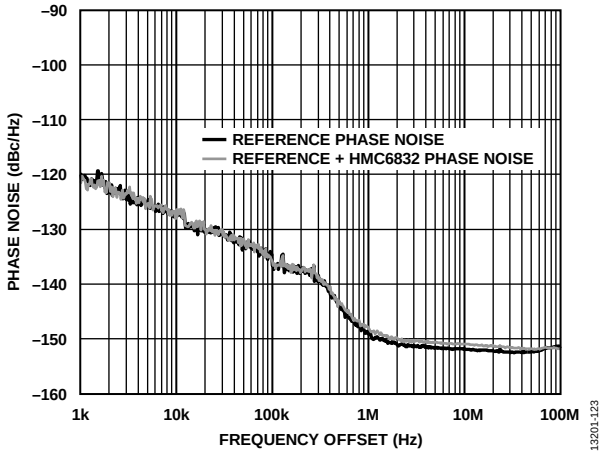


Figure 23. Phase Noise Performance at 2 GHz, Agilent E8257D (UNY Option) Used as Signal Source, 0 dBm Single-Ended Input Signal, Single-Ended Output, Depicts Residual Phase Noise Much Better than Reference Source

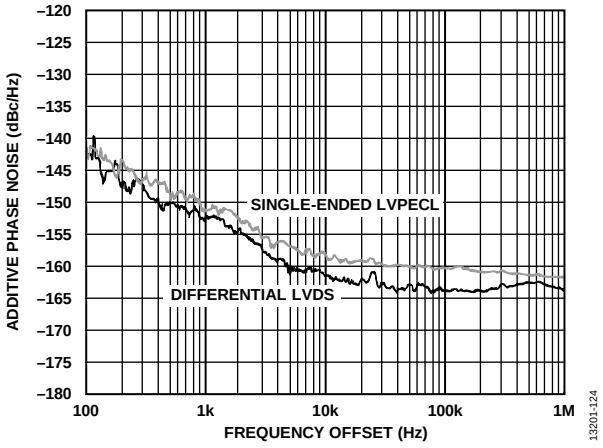


Figure 24. Additive Phase Noise at 2 GHz, 0 dBm Single-Ended Input Signal, Differential LVDS Output and Single-Ended LVPECL Output

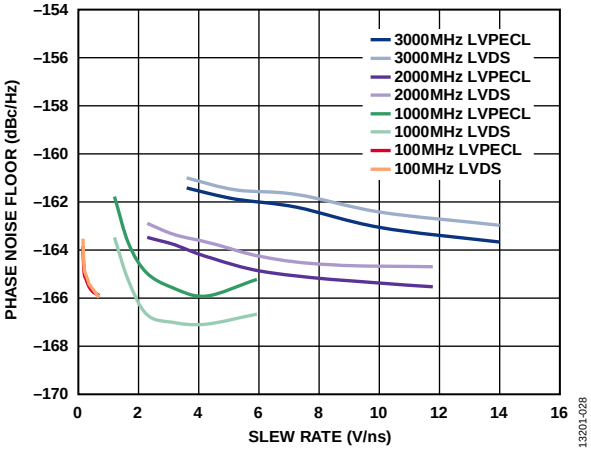


Figure 25. Phase Noise Floor vs. Slew Rate for Carrier Frequencies and Output Configurations, LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω

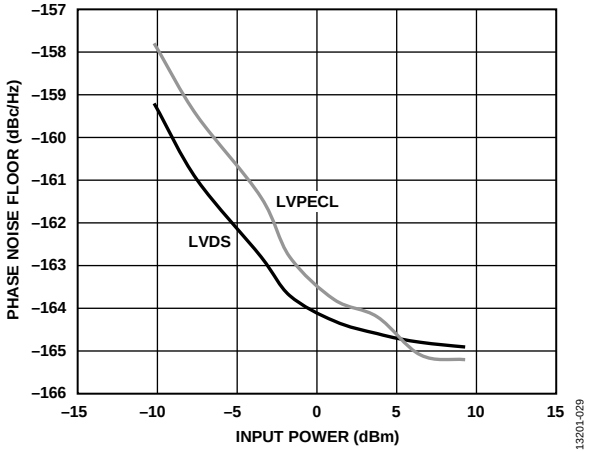


Figure 26. Phase Noise Floor at 1.6 GHz vs. Input Power, LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω

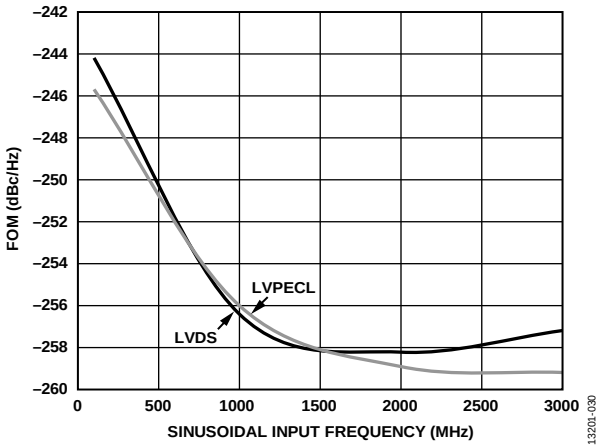


Figure 27. Phase Noise Performance with Low Frequency Sinusoidal Inputs, Input Power = 10 dBm Single-Ended, LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω, Phase Noise Floor (dBc/Hz) = Figure of Merit (FOM) (dBc/Hz)) + 10 log(f_{OUT} (Hz))

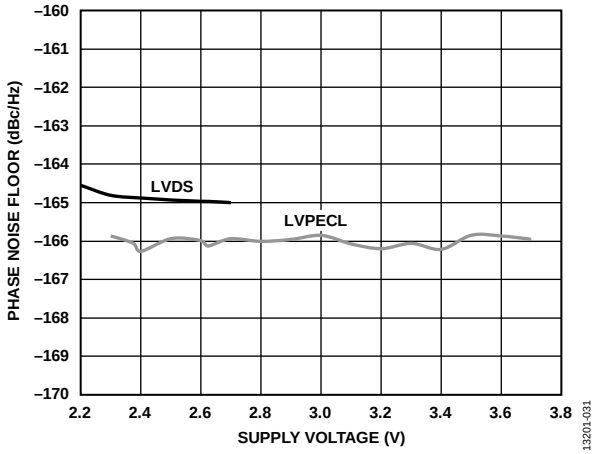


Figure 28. Phase Noise Floor vs. Supply Voltage for LVPECL and LVDS, LVPECL R_{TERM} = 150 Ω; LVDS R_{TERM} = 100 Ω

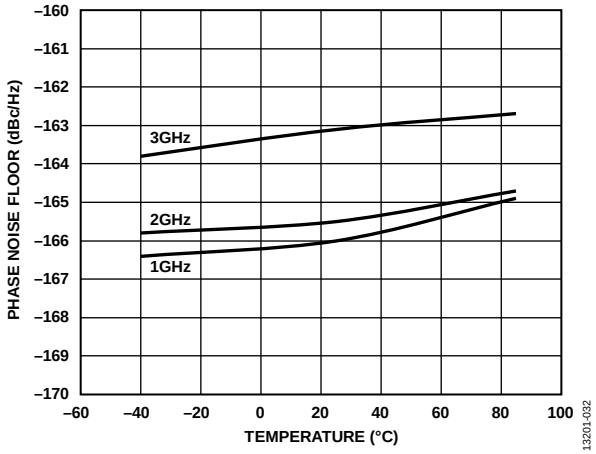


Figure 29. LVPECL 2.5 V, 150 Ω, Phase Noise Floor vs. Temperature for Various Carrier Frequencies

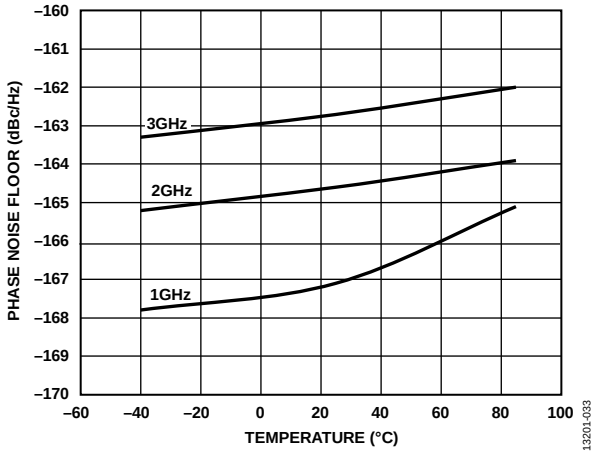


Figure 30. LVDS Phase Noise Floor vs. Temperature for Various Carrier Frequencies

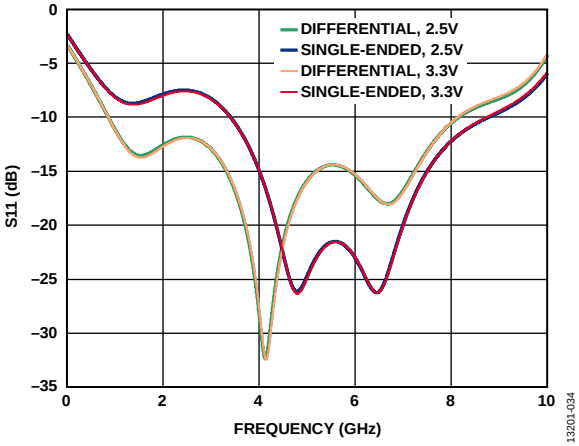


Figure 31. LVDS/LVPECL S Parameters (S11), Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

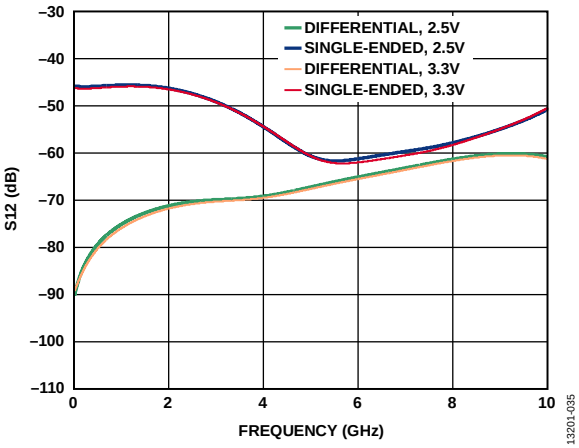


Figure 32. LVPECL S Parameters (S12), Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

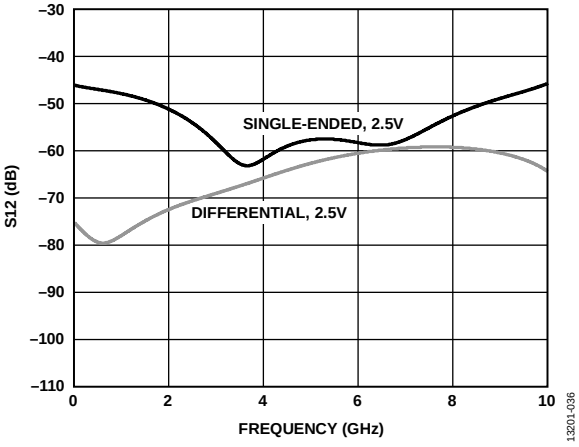


Figure 33. LVDS S Parameters (S12), Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

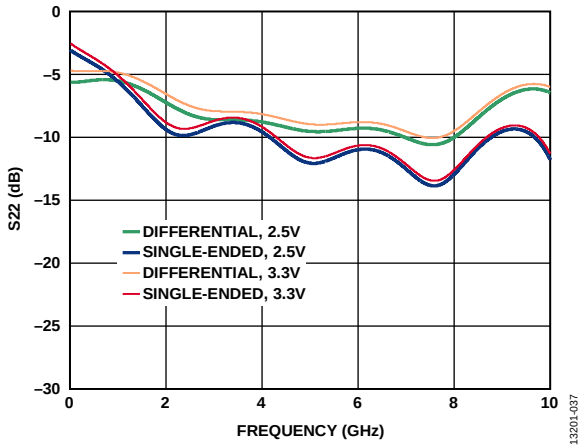


Figure 34. LVPECL S Parameters (S22), Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

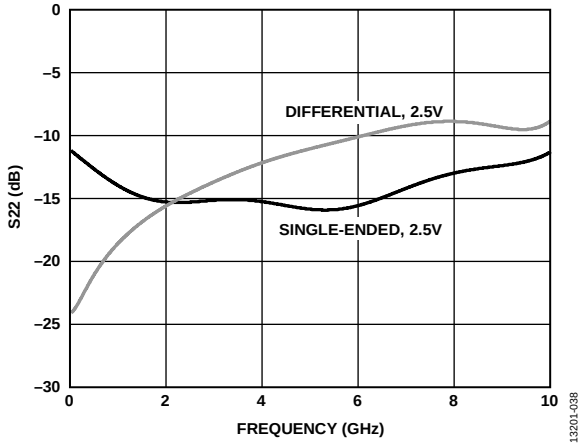


Figure 35. LVDS S Parameters (S22), Network Analyzer Gating Used to Remove Input and Output Impedance Mismatch and Board Loss

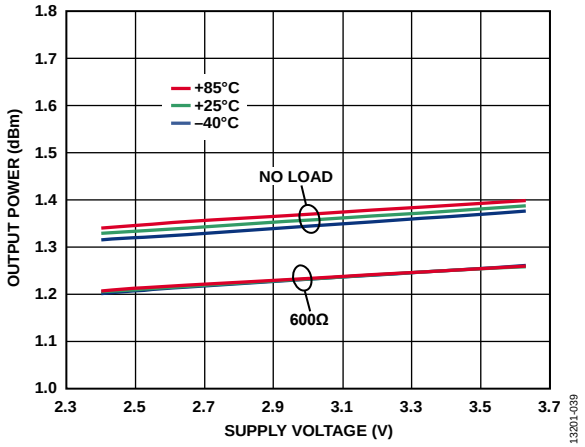


Figure 36. VAC_REF Output Power vs. Supply Voltage for Various Temperatures and Current Loads; 600 Ω Signifies 2 mA Output Load

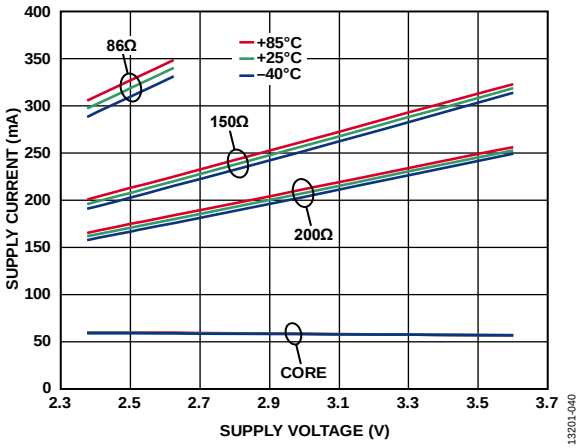


Figure 37. LVPECL Supply Current vs. Supply Voltage for Various Temperatures and R_{TERM} Values

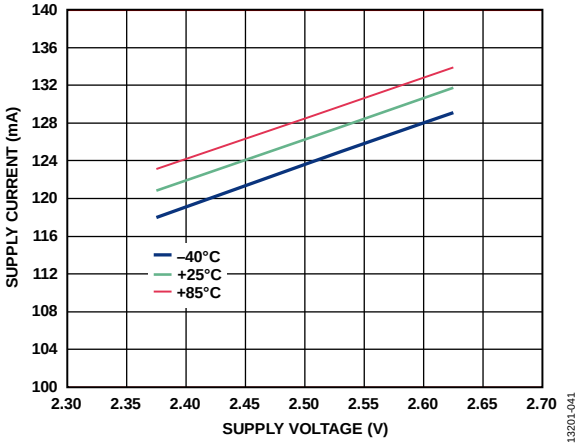


Figure 38. LVDS Supply Current vs. Supply Voltage for Various Temperatures

TEST CIRCUITS

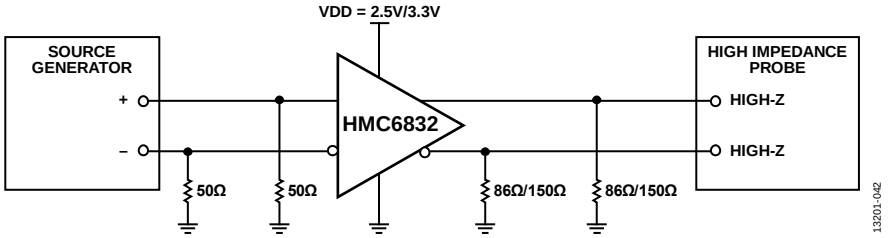


Figure 39. Test Circuit for DC LVPECL Measurements, 86 Ω Termination Used for VDD = 2.5 V; 150 Ω Termination Used for VDD = 3.3 V

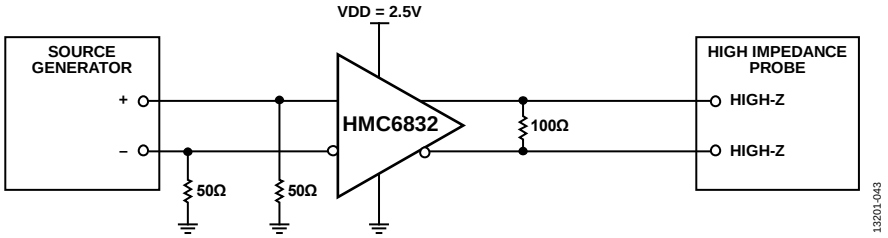


Figure 40. Test Circuit for DC LVDS Measurements

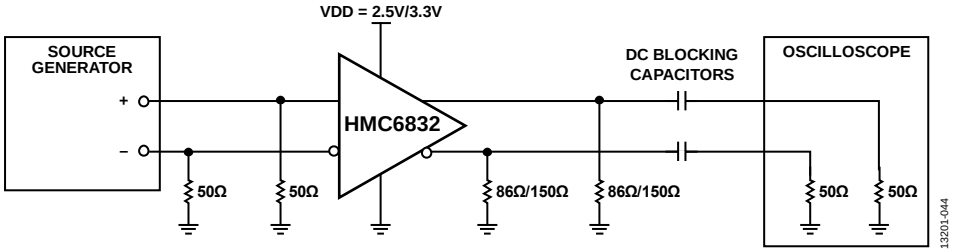


Figure 41. Test Circuit for Transient (AC) LVPECL Measurements, 86 Ω Termination Used for VDD = 2.5 V; 150 Ω Termination Used for VDD = 3.3 V

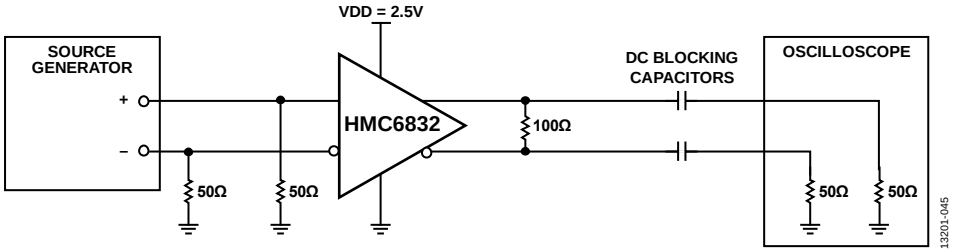


Figure 42. Test Circuit for Transient (AC) LVDS Measurements

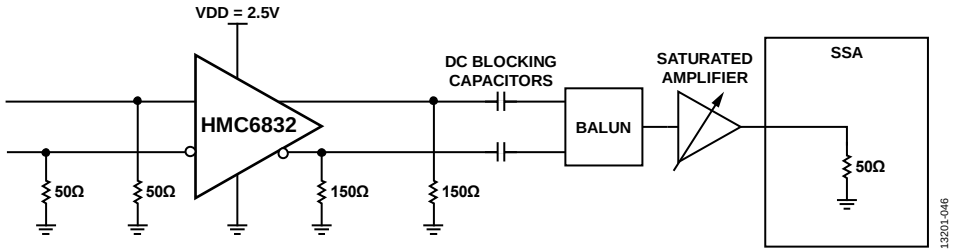


Figure 43. Test Circuit for Phase Noise LVPECL Measurements

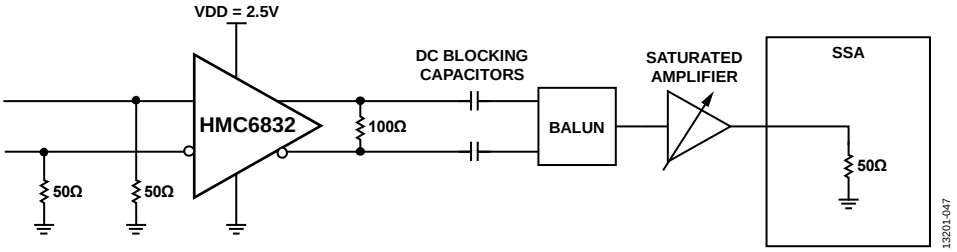


Figure 44. Test Circuit for Phase Noise LVDS Measurements

THEORY OF OPERATION

INPUT STAGE

The input stage shown in Figure 45 is flexible. It can be driven single-ended or differential with LVPECL, LVDS, or CML signals. If driven single-ended, place a large ac-coupled capacitor between the undriven input and a nearby GND pin. There are pull-up and pull-down resistors on each single-ended input to set the nominal dc voltage to VDD/2. The input is selectable by the input select pin (IN_SEL), a digital pin that can be set to either GND (INx0) or VDD (INx1). To select the output termination, use the configuration pin (CONFIG), a digital pin that can be set to either GND (LVPECL) or to VDD (LVDS). When left floating, the CONFIG pin is internally pulled to VDD (LVDS).

LVPECL OUTPUT STAGE

The LVPECL output driver produces up to 0.8 V p-p differential swing into 100 Ω differential loads. LVPECL drivers are terminated with off-chip resistors that provide the dc current through the emitter-follower output stage. If unused, LVPECL outputs can be left floating. VAC_REF is an output reference voltage capable of sourcing 2 mA at 1.25 V.

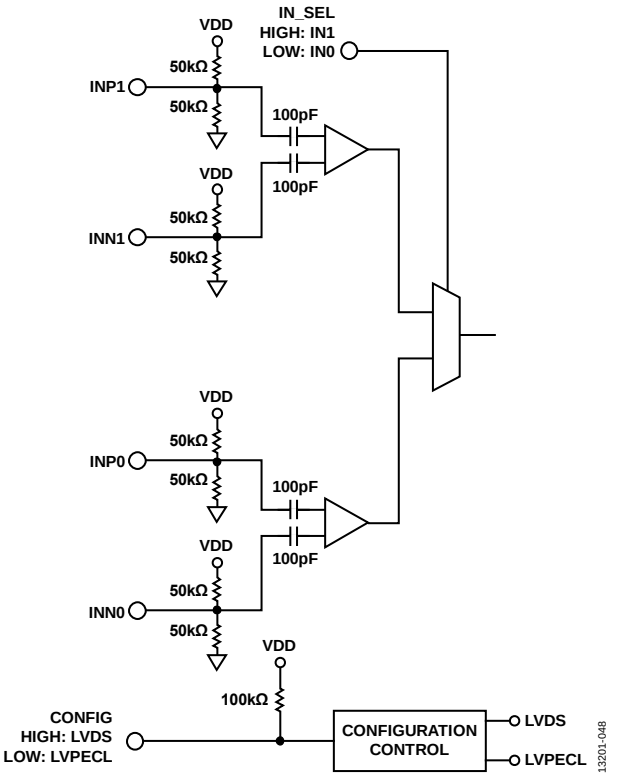


Figure 45. Input Stage Block Diagram

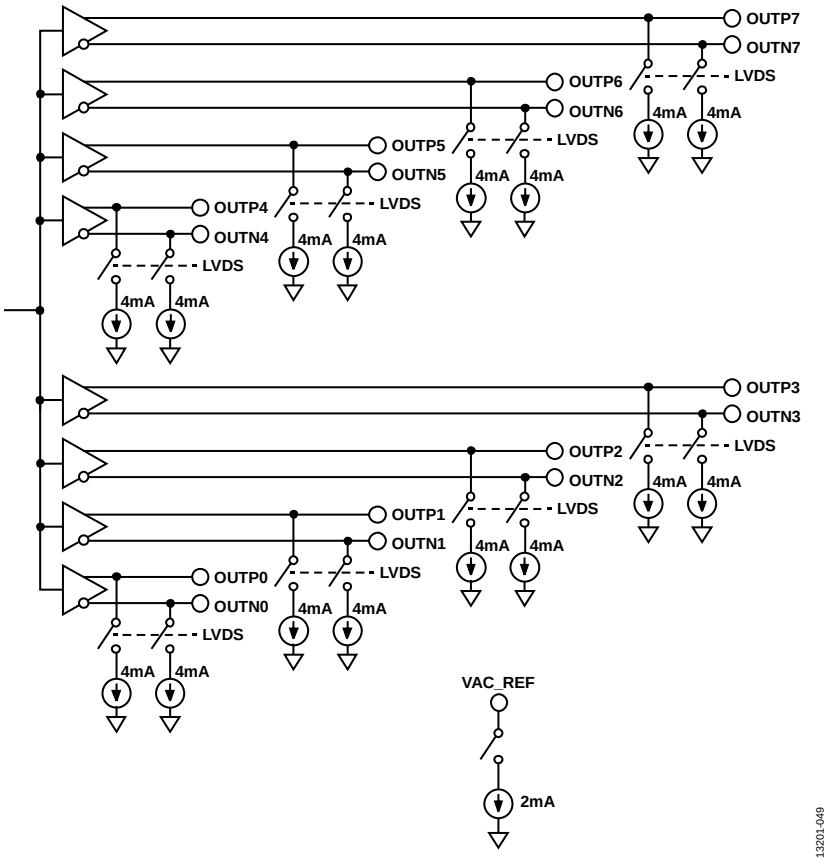


Figure 46. Output Stage Block Diagram

A number of choices are available for connecting the LVPECL drivers and receivers. There are compromises between matching performance, common-mode levels, and signal swing. For clocking applications, the user often has the option of using ac coupling, unlike in many datapath situations. Figure 47 shows a simplified interface schematic between an LVPECL output and an input stage, where various options and trade-offs for the termination components are provided (see Table 11). The Analog Devices, Inc., evaluation board has a great deal of flexibility in how the inputs/outputs are configured. Several configurations are shown in the Applications Information section.

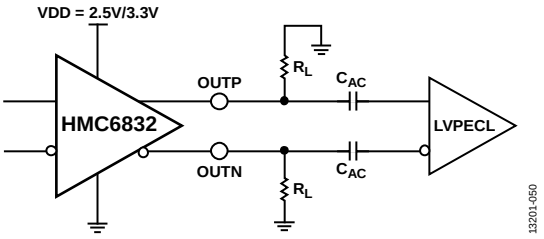


Figure 47. Recommended Interface Diagram

Table 11. Interface Values

Interface Value	Description
Load Resistor (R_L)	DC current termination for LVPECL output stage
150 Ω	Analog Devices evaluation board default, standard LVPECL termination voltages
200 Ω	Reduced current, no performance degradation
300 Ω	Further reduced current, lower output power but flatter frequency response
Open	If using internal dc termination network at the receiver
AC-Coupled Capacitor (C_{AC})	
Large Capacitor	Analog Devices evaluation board default, when ac coupling is used

APPLICATIONS INFORMATION

Figure 48 to Figure 50 illustrate the common input interface configurations. Figure 48 shows how to interface a LVCMOS input to the HMC6832. A capacitor is needed between the LVCMOS driver and the HMC6832 to ac couple the input. In addition, add a capacitor between the inverted input of the HMC6832 and a nearby GND pin to reduce noise in the system.

The series resistance (R_{SERIES}) provides impedance matching and signal attenuation. The R_{SERIES} value is the difference between the LVCMOS driver output impedance and the transmission line impedance. Position R_{SERIES} near the LVCMOS driver.

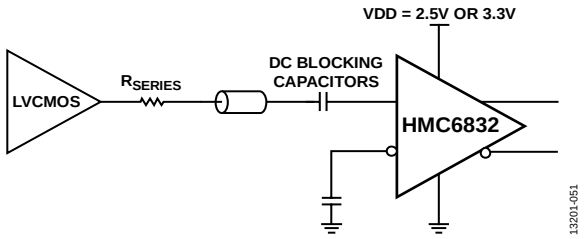


Figure 48. LVCMOS AC-Coupled Input Interface

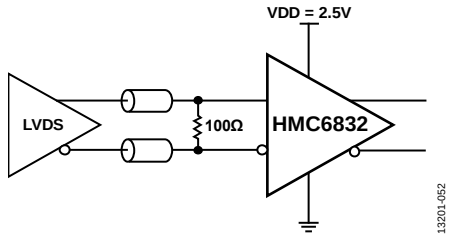


Figure 49. LVDS DC-Coupled Input Interface

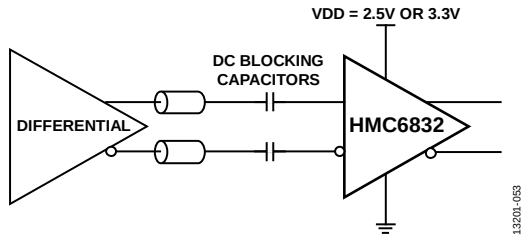


Figure 50. Differential Input AC-Coupled Interface

Figure 51 and Figure 52 illustrate the common output interface configurations.

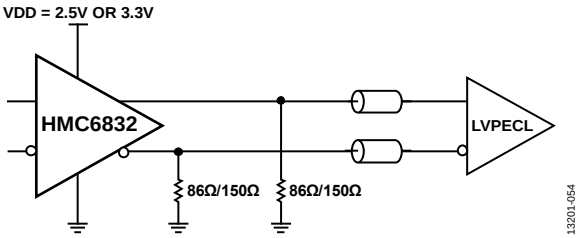


Figure 51. LVPECL Output DC Termination Interface (86 Ω Termination Can Be Used at 2.5 V Only)

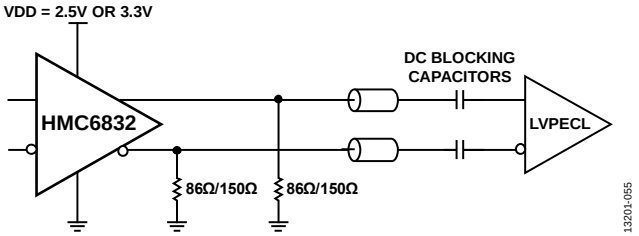


Figure 52. LVPECL Output AC Termination Interface (86 Ω Termination Can Be Used at 2.5 V Only)

RECOMMENDED SOLDER REFLOW PROFILE

The typical Pb-free reflow solder profile shown in Figure 53 is based on JEDEC J-STD-20C.

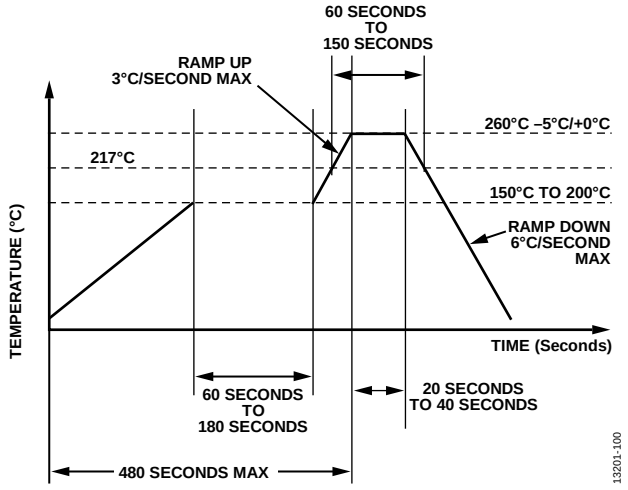


Figure 53. LFCSP Pb-Free Reflow Profile

EVALUATION PRINTED CIRCUIT BOARD (PCB)

An easy to use evaluation PCB is available from Analog Devices upon request. Top and bottom view layouts of the evaluation board are given in Figure 54 and Figure 55. For the circuit board in this application, use RF circuit design techniques. Ensure that signal lines have 50 Ω impedance. Connect the package ground leads and exposed paddle directly to the ground plane similarly to that shown in Figure 54 (top view) and Figure 55 (bottom view). Use a sufficient number of via holes to connect the top and bottom ground planes.

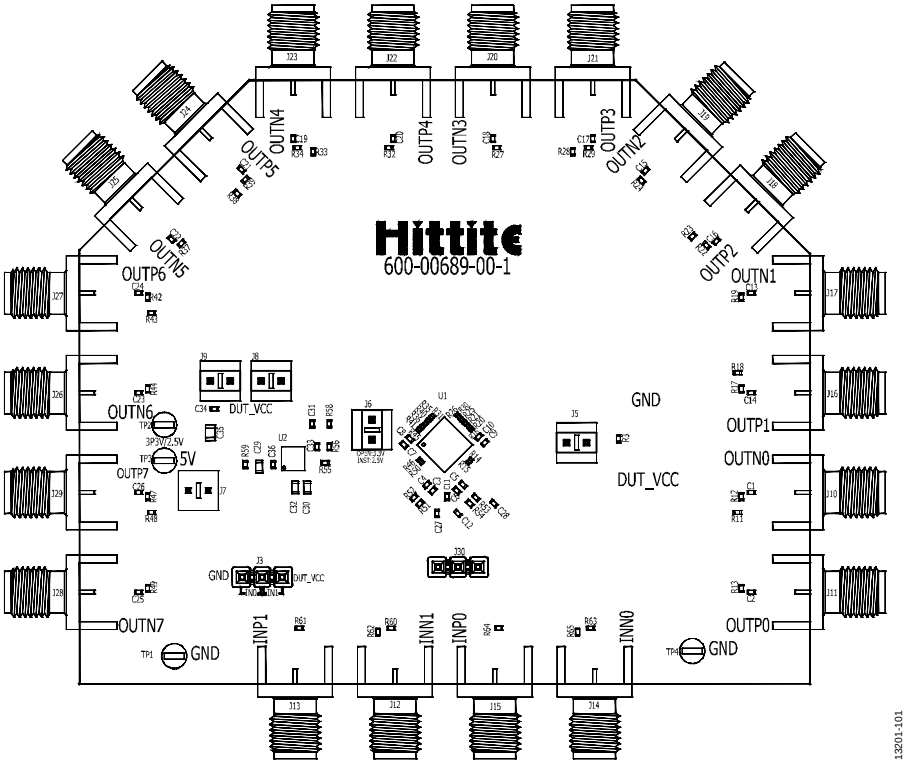


Figure 54. Evaluation PCB (Top View)

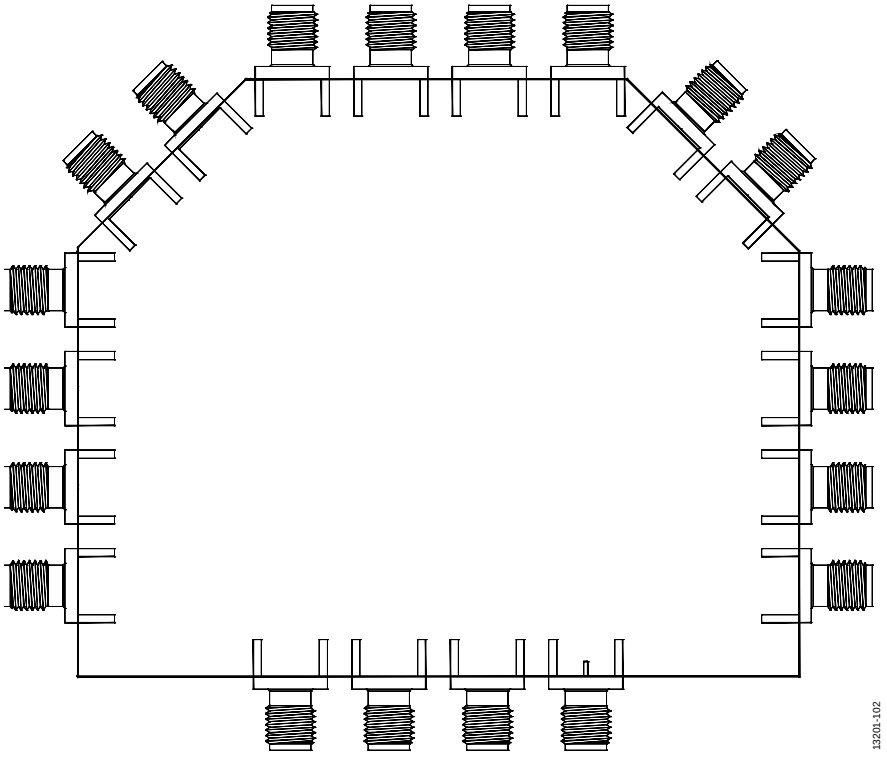
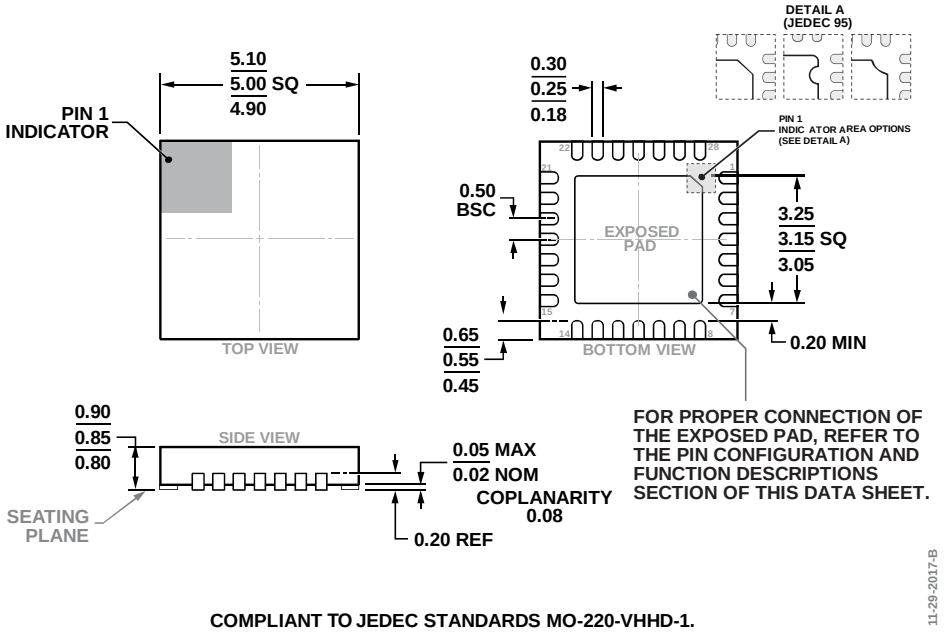


Figure 55. Evaluation PCB (Bottom View)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-1.

Figure 56. 28-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.85 mm Package Height
(HCP-28-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC6832ALP5LE	−40°C to +85°C	MSL3	28-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-28-1
HMC6832ALP5LETR	−40°C to +85°C	MSL3	28-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-28-1
EV1HMC6832ALP5L			Evaluation Board (LVPECL Configuration)	
EV2HMC6832ALP5L			Evaluation Board (LVDS Configuration)	

[1] All models are RoHS Compliant Parts.
[2] The maximum peak reflow temperature is 260°C for the HMC6832ALP5LE and HMC6832ALP5LETR. See the Absolute Maximum Ratings section, Table 8.