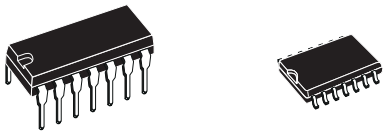
HCF4047B

LOW POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

- LOW POWER CONSUMPTION : SPECIAL CMOS OSCILLATOR CONFIGURATION
- MONOSTABLE (one - shot) OR ASTABLE (free-running) OPERATION
- TRUE AND COMPLEMENTED BUFFERED OUTPUTS
- ONLY ONE EXTERNAL R AND C REQUIRED
- BUFFERED INPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP SOP

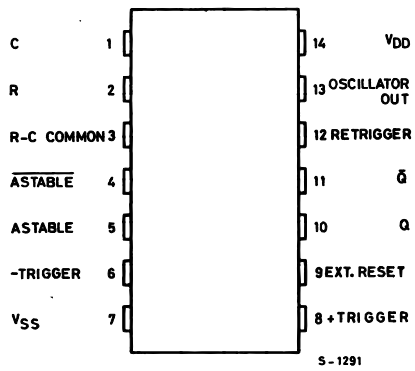
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4047BEY	
SOP	HCF4047BM1	HCF4047M013TR

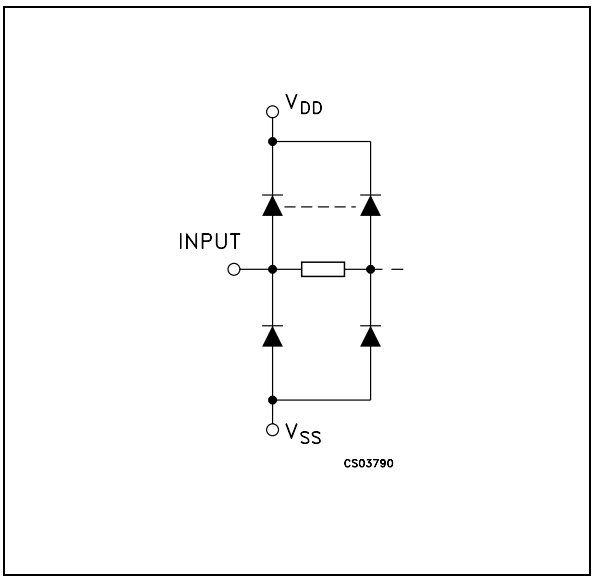
DESCRIPTION

The HCF4047B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4047B consist of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$ and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.
For operating modes see functional terminal connections and application notes.

PIN CONNECTION



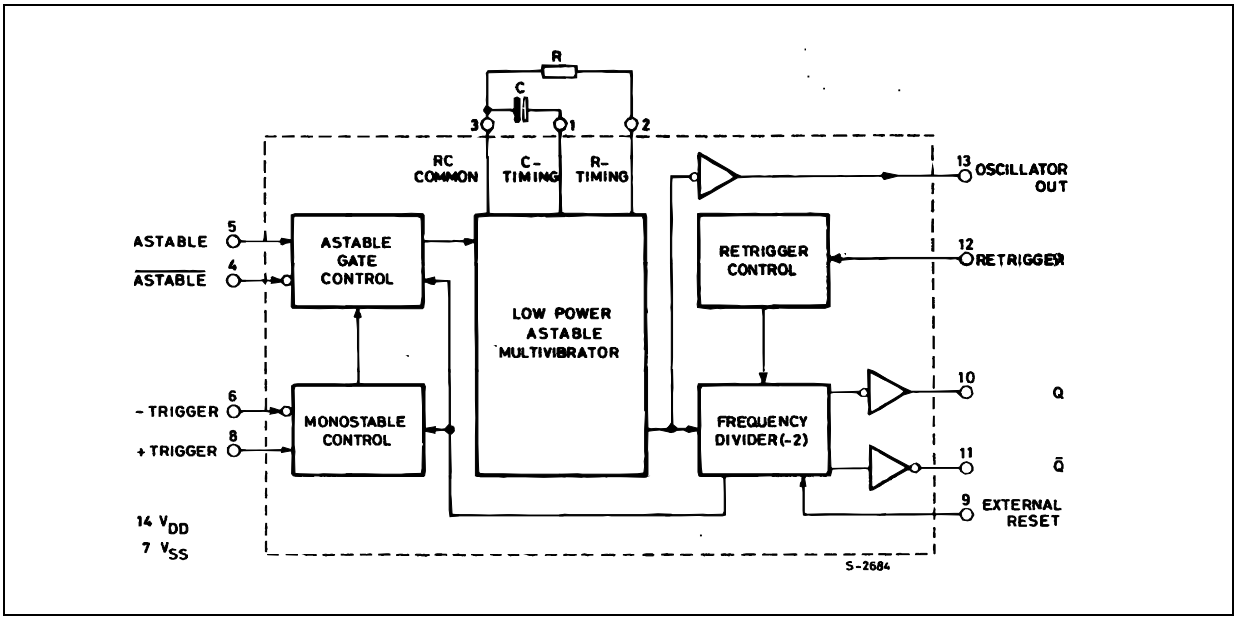
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	C	External Capacitor
2	R	External Resistor
3	RC COM-MON	External Connection to (1) and (2)
4	$\overline{\text{ASTABLE}}$	Complement Astable Pulse
5	ASTABLE	True Astable Pulse
6	-TRIGGER	Negative Trigger Pulse
8	+TRIGGER	Positive Trigger Pulse
9	EXT. RESET	External Reset
12	RETRIG-GER	Retrigger Mode Pulse
13	OSC. OUT	Oscillator Output
10,11	Q, $\overline{Q}$	Q Outputs
7	V_{SS}	Negative Supply Voltage
14	V_{DD}	Positive Supply Voltage

BLOCK DIAGRAM

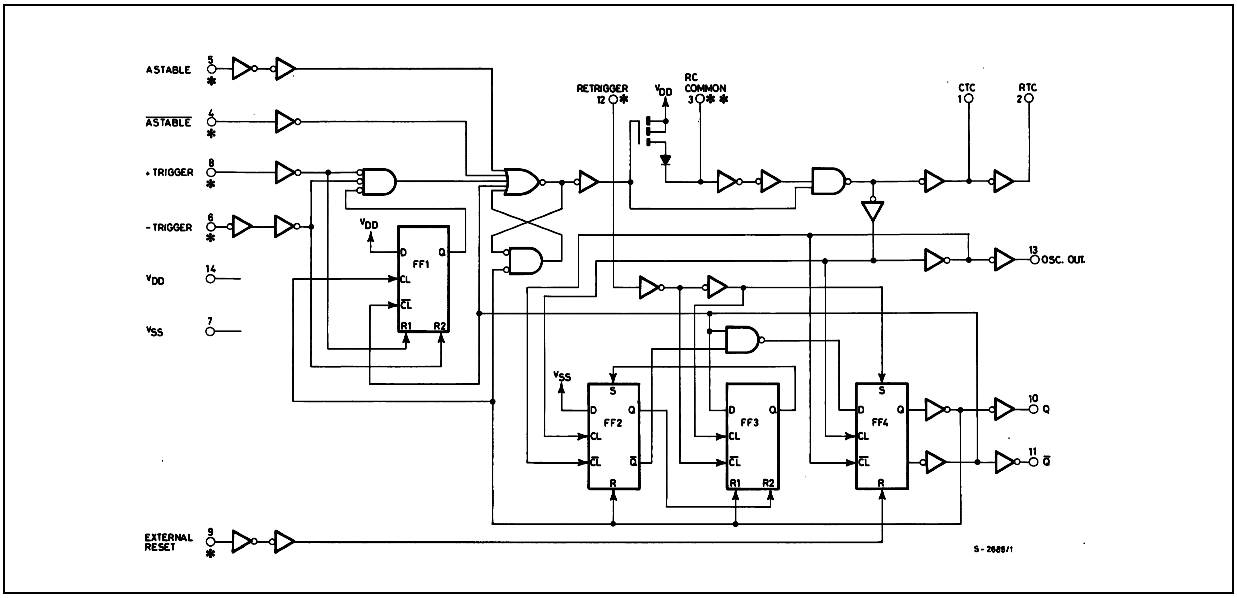


FUNCTIONAL TERMINAL CONNECTIONS

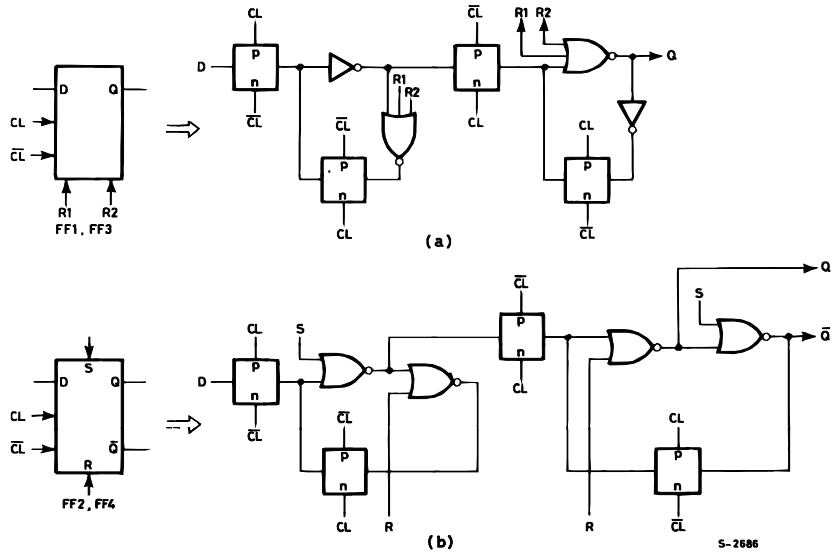
FUNCTION*	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	to V_{DD}	to V_{SS}	Input Pulse to		
Astable Multivibrator					
Free Running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	t_A (10,11) = 4.40RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	t_A (13) = 2.20RC
Monostable Multivibrator					
Positive - Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative - Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10,11) = 2.48RC
External Countdown**	14	5, 6, 7, 8, 9, 12	-	10, 11	

* In all cases external capacitor and resistor between pins, 1, 2 and 3 (see logic diagrams).
** Input pulse to Reset of External Counting Chip.
External Counting Chip Output to pin 4.

LOGIC DIAGRAM



DETAIL FOR FLIP-FLOPS FF1 AND FF3 (a) AND FOR FLIP-FLOPS FF2 AND FF4 (b)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.01	1		30		30	μA
		0/10			10		0.01	2		60		60	
		0/15			15		0.01	4		120		120	
		0/20			20		0.02	20		600		600	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter		Test Condition		Value (*)			Unit
			V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	Astable, $\overline{\text{Astable}}$ to Osc. Out	5			200	400	ns
			10			100	200	
			15			80	160	
		Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	5			350	700	
			10			175	350	
			15			125	250	
		+ or - Trigger to Q, $\overline{Q}$	5			500	1000	
			10			225	450	
			15			150	300	
		Retrigger to Q, $\overline{Q}$	5			300	600	
			10			150	300	
			15			100	200	
		External Reset to Q, $\overline{Q}$	5			250	500	
			10			100	200	
			15			70	140	
t_{THL} t_{TLH}	Transition Time Osc. Out Q, $\overline{Q}$		5			100	200	ns
			10			50	100	
			15			40	80	
t_W	Input Pulse Width	+ Trigger - Trigger	5			200	400	ns
			10			80	160	
			15			50	100	
		Reset	5			100	200	
			10			50	100	
			15			30	60	
		Retrigger	5			300	600	
			10			115	230	
			15			75	150	
t_r, t_f	Input Rise and Fall Time All Inputs		5		Unlimited			µs
			10					
			15					
	Q or $\overline{Q}$ Deviation from 50% Duty Factor		5			±0.5	±1	%
			10			±0.5	±1	
			15			±0.1	±0.5	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

APPLICATION INFORMATION

1 - CIRCUIT DESCRIPTION

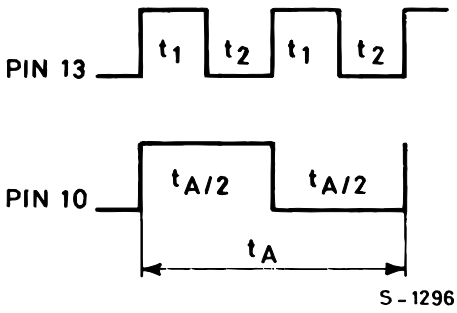
Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the ASTABLE input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by

coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the ASTABLE input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

2 - ASTABLE MODE

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (VTR) shift (33% - 67% V_{DD}) for free-running (astable) operation.

ASTABLE MODE WAVEFORMS



$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

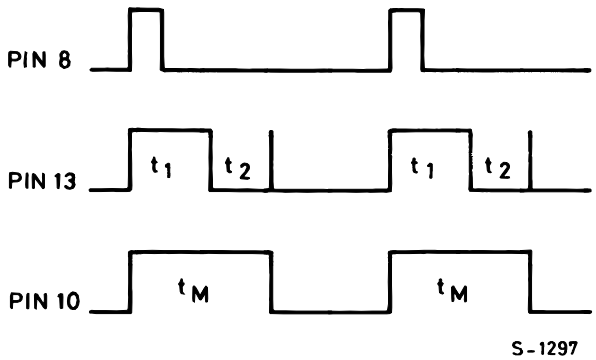
$$t_3 = 2(t_1+t_2) = -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min : $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max : $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$
thus if t_A = 4.40 RC is used, the maximum variation will be (+ 5.0%, -0.0%)
In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - MONOSTABLE MODE

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for one-shot (monostable) operation.

MONOSTABLE WAVEFORMS



$$t_1 = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

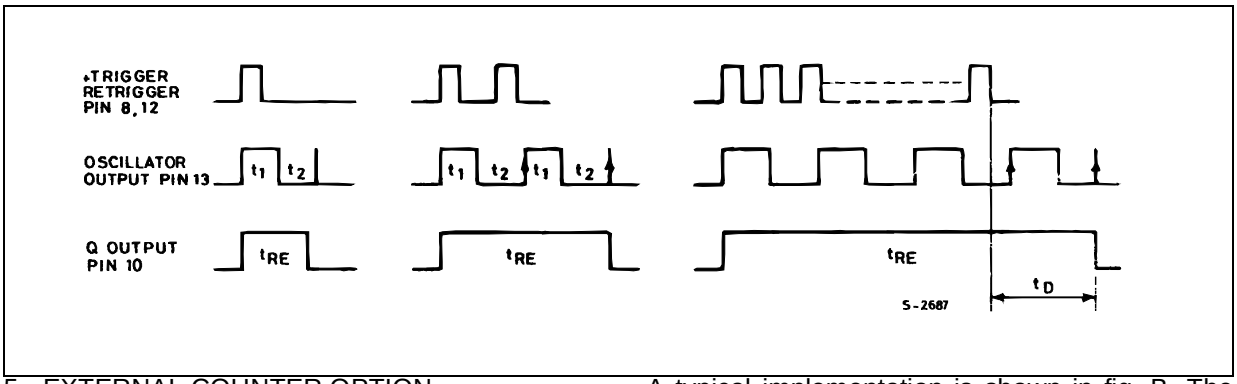
$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_M = (t_1+t_2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

Where tM = monostable mode pulse width. Values for tM are as follows :
Typ : $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48$ RC
Min : $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71$ RC
Max : $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48$ RC
Thus if t_M = 2.48 RC is used, the maximum variation will be (+ 9.3%, - 0.0%).
Note : In the astable mode, the first positive half cycle has a duration of T_M ; succeeding durations are $t_A/2$.
In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - RETRIGGER MODE
The HCF4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in fig.A normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

FIGURE A : Retrigger-mode waveforms

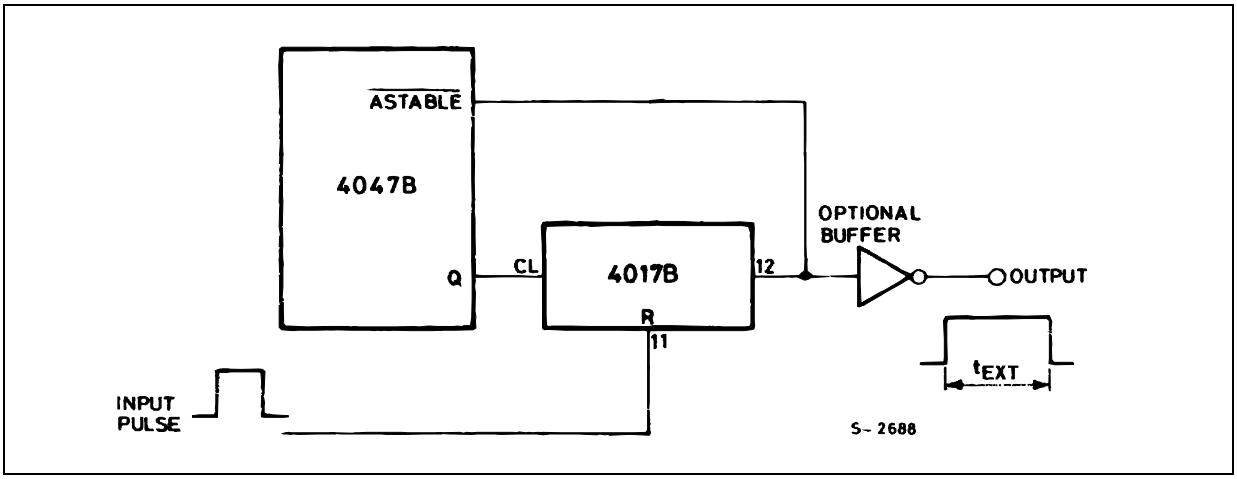


5 - EXTERNAL COUNTER OPTION

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time.

A typical implementation is shown in fig. B. The pulse duration at the output is
text = (N - 1) (t_A) + (t_M + $t_A/2$)
Where text = pulse duration of the circuitry, and N is the number of counts used.

FIGURE B : Implementation of external counter option



6 - POWER CONSUMPTION

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula :

Astable Mode :

$P = 2CV^2f$. (Output at Pin 13)

$P = 4CV^2f$. (Output at Pin 10 and 11)

Monostable Mode : $P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$

(Output at Pin 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - TIMING-COMPONENT LIMITATIONS

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). Three is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

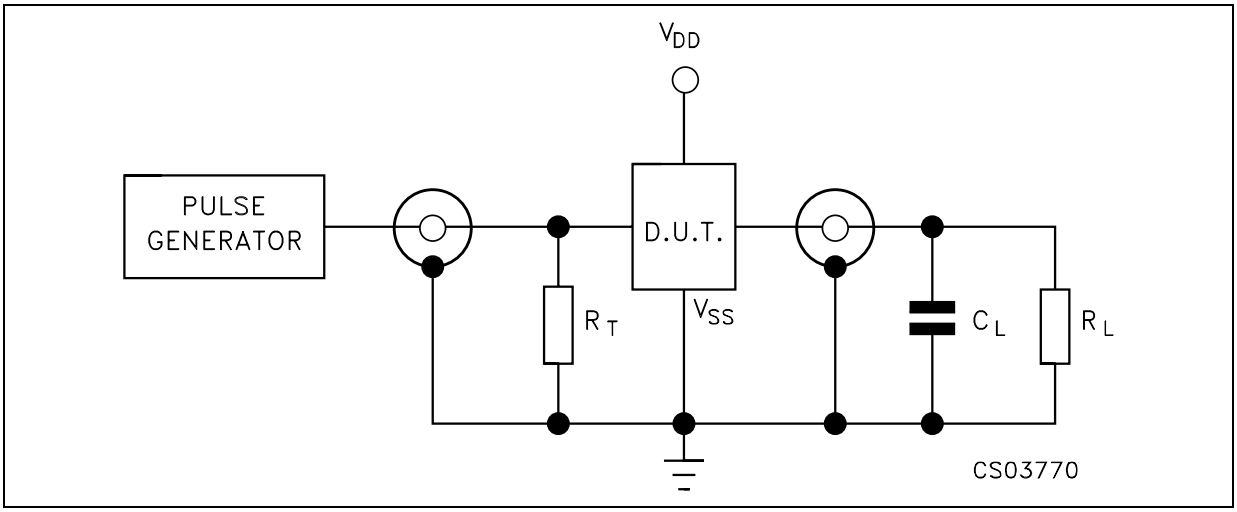
The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be :

$C \geq 100pF$, up to any practical value, for astable modes ;

$C \geq 1000pF$, up to any practical value, for monostable modes.

$10K\Omega \leq R \leq 1M\Omega$.

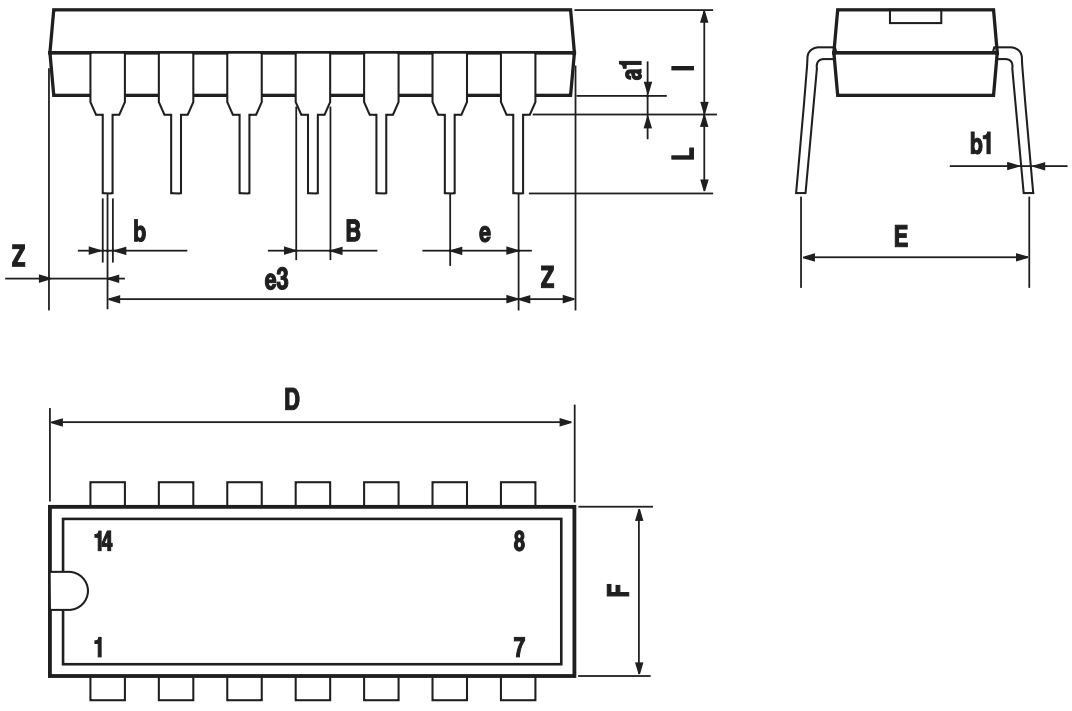
TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Plastic DIP-14 MECHANICAL DATA

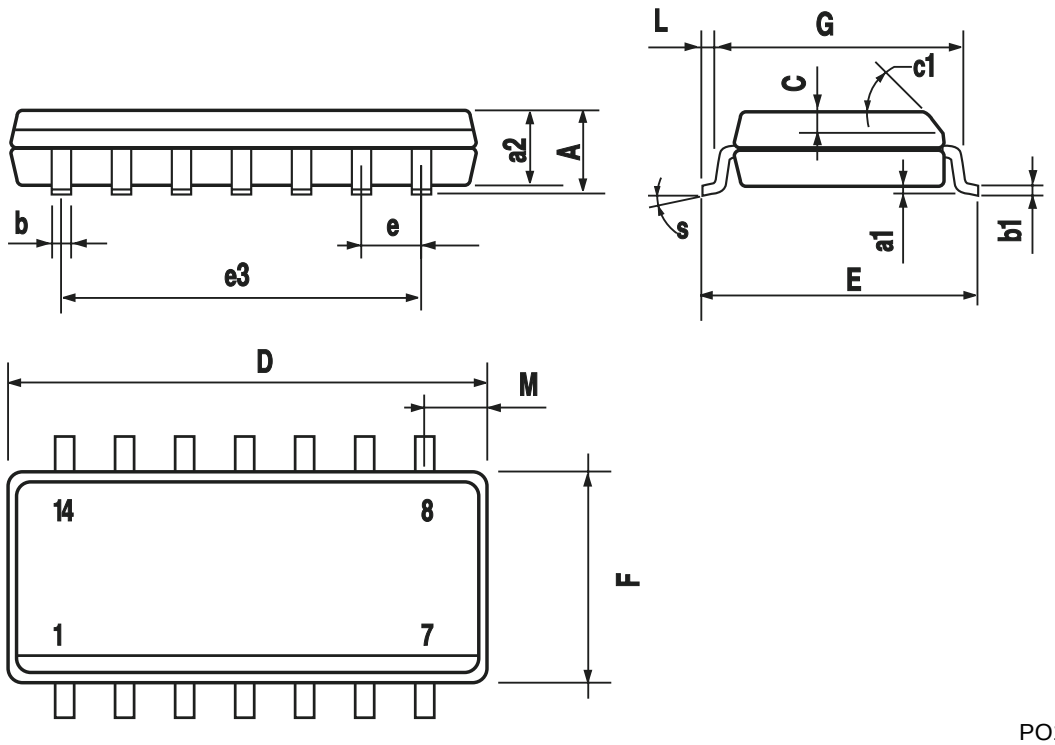
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G