GTL2014

4-bit LVTTL to GTL transceiver

Rev. 01 — 19 May 2005 Product data sheet

1. General description

The GTL2014 is a 4-bit translating transceiver designed for 3.3 V LVTTL system interface with a GTL–/GTL/GTL+ bus.

The direction pin allows the part to function as either a GTL to LVTTL sampling receiver or as a LVTTL to GTL interface.

The GTL2014 LVTTL inputs (only) are tolerant up to 5.5 V allowing direct access to TTL or 5 V CMOS inputs. The LVTTL outputs are not 5.5 V tolerant.

The GTL2014 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

2. Features

- Operates as a 4-bit GTL–/GTL/GTL+ sampling receiver or as a LVTTL to GTL–/GTL/GTL+ driver
- 3.0 V to 3.6 V operation with 5 V tolerant LVTTL input
- GTL input and output 3.6 V tolerant
- V_{ref} adjustable from 0.5 V to $V_{CC}/2$
- Partial power-down permitted
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-CC101
- Latch-up protection exceeds 500 mA per JESD78
- Package offered: TSSOP14

3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay; An-to-Bn	C_L = 50 pF; V_{CC} = 3.3 V	-	2.8	-	ns
t_{PHL}			-	3.4	-	ns
t_{PLH}	propagation delay; Bn-to-An	C_L = 50 pF; V_{CC} = 3.3 V	-	5.2	-	ns
t_{PHL}			-	4.9	-	ns
C_i	input capacitance on pin DIR; A-to-B or B-to-A	V_I = 0 V or V_{CC}	-	2	2.5	pF
C_{io}	input/output capacitance; A-to-B	outputs disabled; V_I and V_O = 0 V or 3.0 V	-	4.6	6.0	pF
	input/output capacitance; B-to-A		-	3.4	4.3	pF

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
GTL2014PW	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

Standard packing quantities and other packaging data are available at *www.standardics.philips.com/packaging*.

4.1 Ordering options

Table 3: Ordering options

Type number	Topside mark	Temperature range
GTL2014PW	GTL2014	T_{amb} = –40 °C to +85 °C

5. Functional diagram

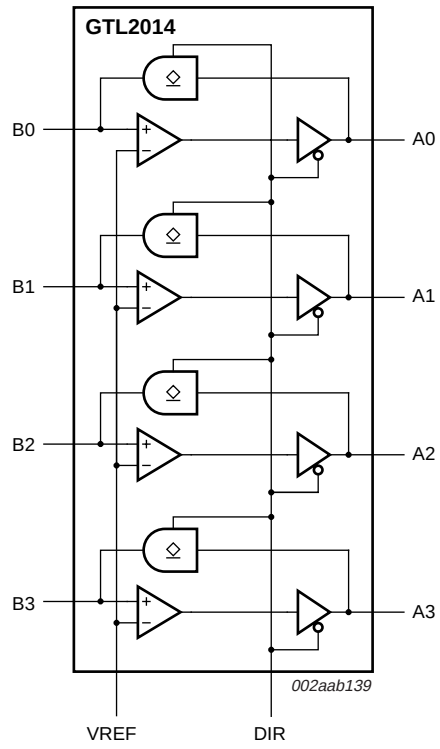


Fig 1. Logic diagram for GTL2014

6. Pinning information

6.1 Pinning

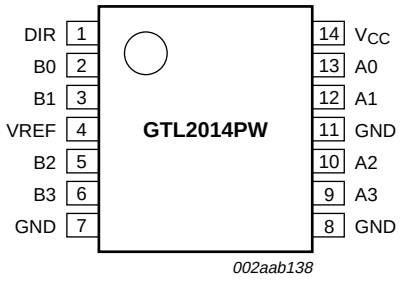


Fig 2. Pin configuration for TSSOP14

6.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
DIR	1	direction control input (LVTTL)
B0	2	data inputs/outputs (GTL)
B1	3	
B2	5	
B3	6	
A0	13	data inputs/outputs (LVTTL)
A1	12	
A2	10	
A3	9	
VREF	4	GTL reference voltage
GND	7, 8, 11	ground (0 V)
V_{CC}	14	positive supply voltage

7. Functional description

Refer to Figure 1 “Logic diagram for GTL2014” on page 2.

7.1 Function table

Table 5: Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Input/output	
DIR	**A (LVTTL)**	**B (GTL)**
H	input	Bn = An
L	An = Bn	input

8. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	input clamping diode current	$V_I < 0$ V	-	–50	mA
V_I	DC input voltage	A port	–0.5 [2]	+7.0	V
		B port	–0.5 [2]	+4.6	V
I_{OK}	output diode clamping current	A port; $V_O < 0$ V	-	–50	mA
V_O	DC output voltage	output in OFF or HIGH state; A port	–0.5 [2]	+7.0	V
		output in OFF or HIGH state; B port	–0.5 [2]	+4.6	V
I_{OL}	current into any output in the LOW state	A port	-	32	mA
		B port	-	80	mA
I_{OH}	current into any output in the HIGH state	A port	-	–32	mA
T_{stg}	storage temperature range	[3]	–60	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 9 “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[3] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 7: Operating conditions [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	-	3.6	V
V_{TT}	termination voltage [2]	GTL–	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	V
V_{ref}	reference voltage	overall	0.5	$^2/_3V_{TT}$	$V_{CC}/2$	V
		GTL–	0.5	0.6	0.63	V
		GTL	0.76	0.8	0.84	V
		GTL+	0.87	1.0	1.10	V
V_I	input voltage	B port	0	V_{TT}	3.6	V
		except B port	0	3.3	5.5 [3]	V
V_{IH}	HIGH-level input voltage	B port	V_{ref} + 0.050	-	-	V
		except B port	2	-	-	V
V_{IL}	LOW-level input voltage	B port	-	-	V_{ref} – 0.050	V
		except B port	-	-	0.8	V
I_{OH}	HIGH-level output current	A port	-	-	–16	mA
I_{OL}	LOW-level output current	B port	-	-	40	mA
		A port	-	-	16	mA
T_{amb}	operating ambient temperature	in free-air	–40	-	+85	°C

[1] Unused inputs must be held HIGH or LOW to prevent them from floating.

[2] V_{TT} maximum of 3.6 V with resistor sized so I_{OL} maximum is not exceeded.

[3] A0, A1, A2, A3 $V_{I(max)}$ is 3.6 V if configured as outputs (DIR = L).

10. Static characteristics

Table 8: Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{OH}	HIGH-level output voltage	A port; V_{CC} = 3.0 V to 3.6 V; I_{OH} = −100 µA	[2]	V_{CC} − 0.2	-	-	V
		A port; V_{CC} = 3.0 V; I_{OH} = −16 mA	[2]	2.0	-	-	V
V_{OL}	LOW-level output voltage	B port; V_{CC} = 3.0 V; I_{OL} = 40 mA	[2]	-	0.23	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 8 mA	[2]	-	0.28	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 12 mA	[2]	-	0.40	0.55	V
		A port; V_{CC} = 3.0 V; I_{OL} = 16 mA	[2]	-	0.55	0.8	V
I_I	input current	control inputs; V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	-	±1	µA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND		-	-	±1	µA
		A port; V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	-	10	µA
		A port; V_{CC} = 3.6 V; V_I = V_{CC}		-	-	±1	µA
		A port; V_{CC} = 3.6 V; V_I = 0 V		-	-	−5	µA
I_{OZ}	off-state output current	A port; V_{CC} = 0 V; V_I or V_O = 0 V to 3.6 V		-	-	±100	µA
I_{CC}	quiescent supply current	A port; V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 mA		-	4	10	mA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND; I_O = 0 mA		-	4	10	mA
ΔI_{CC} [3]	additional quiescent current (per input)	A port or control inputs; V_{CC} = 3.6 V; V_I = V_{CC} − 0.6 V		-	-	500	µA
C_i	input capacitance	control inputs; V_I = 3.0 V or 0 V		-	2	2.5	pF
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V		-	4.6	6	pF
		B port; V_O = V_{TT} or 0 V		-	3.4	4.3	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

11. Dynamic characteristics

Table 9: Dynamic characteristics

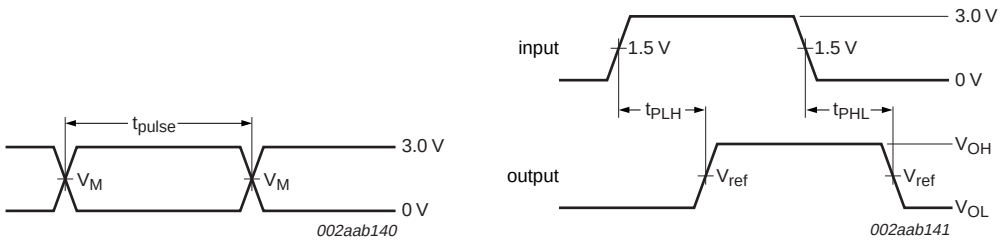
V_{CC} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
GTL−; V_{ref} = 0.6 V; V_{TT} = 0.9 V						
t_{PLH}	propagation delay, An to Bn	see Figure 3	-	2.8	5	ns
t_{PHL}			-	3.3	7	ns
t_{PLH}	propagation delay, Bn to An	see Figure 4	-	5.3	8	ns
t_{PHL}			-	5.2	8	ns
GTL; V_{ref} = 0.8 V; V_{TT} = 1.2 V						
t_{PLH}	propagation delay, An to Bn	see Figure 3	-	2.8	5	ns
t_{PHL}			-	3.4	7	ns
t_{PLH}	propagation delay, Bn to An	see Figure 4	-	5.2	8	ns
t_{PHL}			-	4.9	7	ns
GTL+; V_{ref} = 1.0 V; V_{TT} = 1.5 V						
t_{PLH}	propagation delay, An to Bn	see Figure 3	-	2.8	5	ns
t_{PHL}			-	3.4	7	ns
t_{PLH}	propagation delay, Bn to An	see Figure 4	-	5.1	8	ns
t_{PHL}			-	4.7	7	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11.1 Waveforms

V_M = 1.5 V at $V_{CC} \geq 3.0$ V; $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7$ V for A ports and control pins; $V_M = V_{ref}$ for B ports.



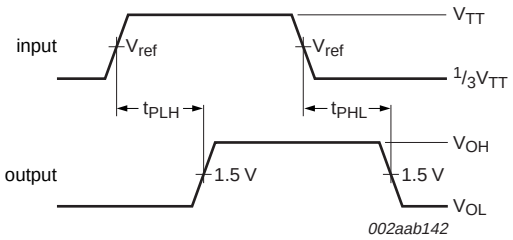
V_M = 1.5 V for A port and V_{ref} for B port

a. Pulse duration

B port to A port

b. Propagation delay times

Fig 3. Voltage waveforms



PRR ≤ 10 MHz; Z_0 = 50 Ω; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns

Fig 4. Propagation delay, Bn to An

12. Test information

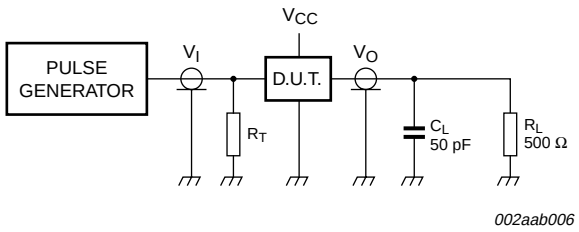


Fig 5. Load circuitry for switching times

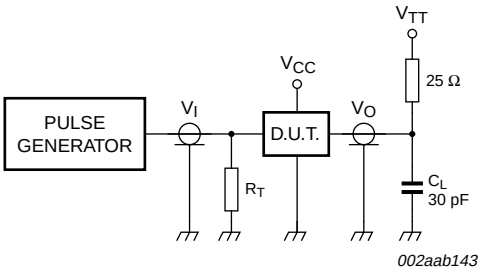


Fig 6. Load circuit for B outputs

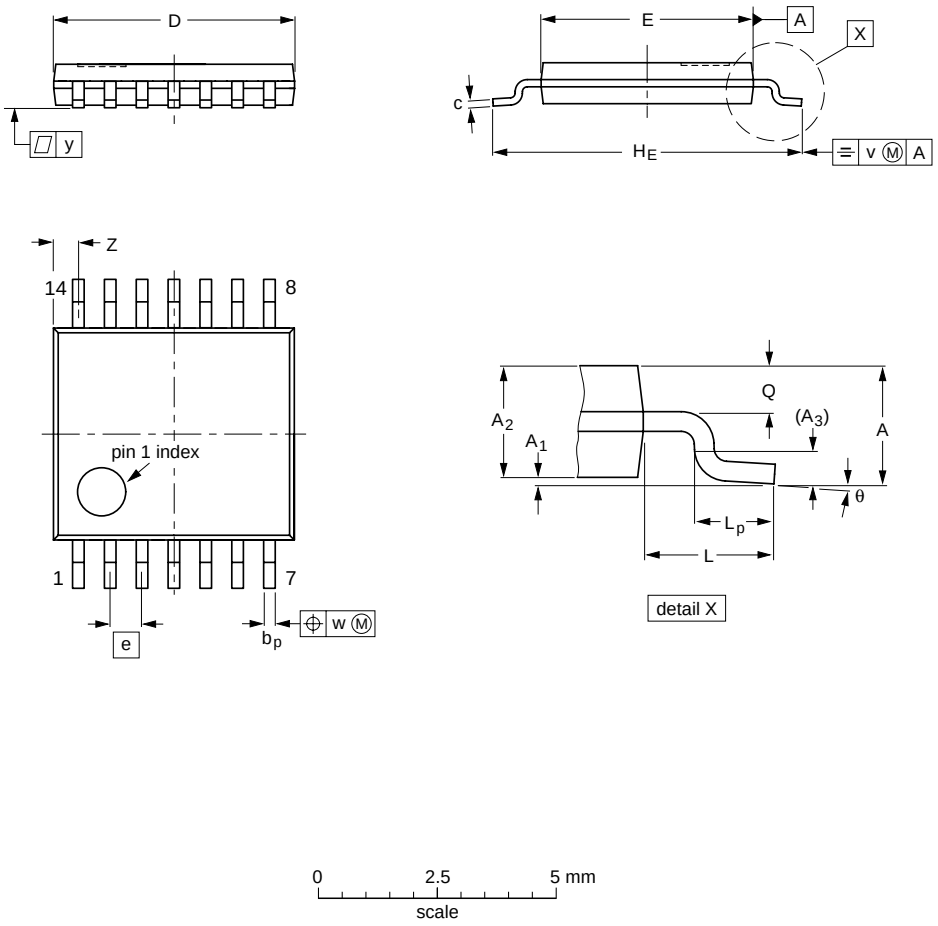
R_L — Load resistor

C_L — Load capacitance; includes jig and probe capacitance

R_T — Termination resistance; should be equal to output impedance of pulse generators.

13. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT402-1 (TSSOP14)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 11: Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Silicon
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

16. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
GTL2014_1	20050519	Product data sheet	-	9397 750 13534	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

19. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

20. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

21. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

22. Contents

1 General description 1
2 Features 1
3 Quick reference data 1
4 Ordering information 2
4.1 Ordering options 2
5 Functional diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 Functional description 3
7.1 Function table 3
8 Limiting values 4
9 Recommended operating conditions 5
10 Static characteristics 6
11 Dynamic characteristics 7
11.1 Waveforms 8
12 Test information 9
13 Package outline 10
14 Soldering 11
14.1 Introduction to soldering surface mount packages 11
14.2 Reflow soldering 11
14.3 Wave soldering 11
14.4 Manual soldering 12
14.5 Package related soldering information 12
15 Abbreviations 13
16 Revision history 13
17 Data sheet status 14
18 Definitions 14
19 Disclaimers 14
20 Trademarks 14
21 Contact information 14

Date of release: 19 May 2005
Document number: 9397 750 13534

Published in The Netherlands