ON Semiconductor®

September 2017

FUSB340
USB 3.1 SuperSpeed 10 Gbps Switch

Features

- 10 GHz Typical Bandwidth
- USB 3.1 SuperSpeed 5Gbps and10 Gbps Switch
- -1.0 dB Typical Insertion Loss at 2.5 GHz
- Low Active Power of 12 µA Typical
- Low Shutdown Power of < 1 µA Max.
- 2 kV HBM ESD Protection
- Small Packaging, 18 Lead TMLP
- Wide V_{DD} Operating Range, 1.5 V-5.0 V

Applications

- Smartphones
- Tablets
- Notebooks

Description

The FUSB340 is a 2:1 data switch for USB SuperSpeed Gen1 and Gen2, 5 Gbps and 10 Gbps data. It is targeted at the mobile device market and for use in Type-C applications where a reversible cable requires a switch.

The FUSB340 data switch offers superior performance various high speed data transmission protocols:

- USB 3.1 SuperSpeed (Gen 2), 10 Gbps
- PCI Express, Gen 3
- SATA
- Fibre Channel
- Display Port 1.3

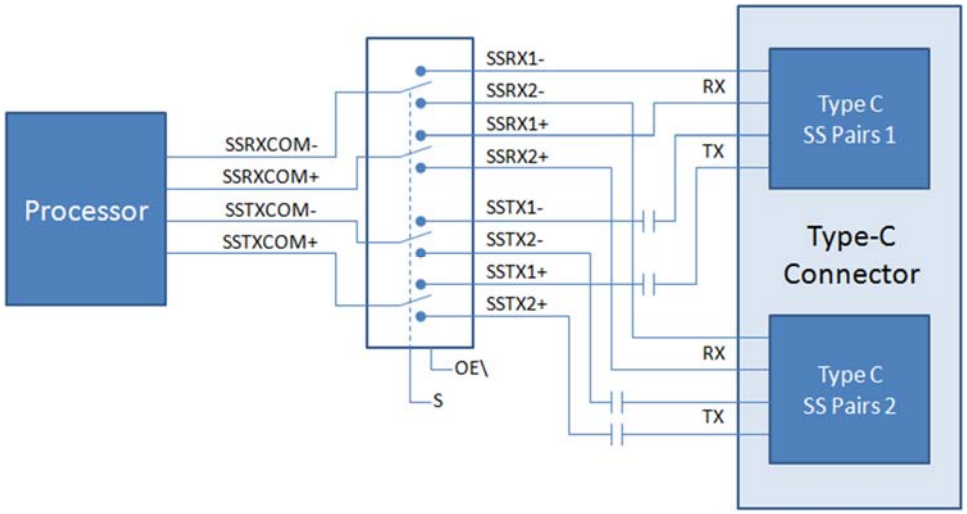

Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FUSB340TMX	-40 to 85°C	18-Lead, Quad, Ultra-ultrathin Molded Leadless Package (TMLP), 2.0 mm x 2.8 mm x 0.375 mm	Tape and Reel

Typical Application

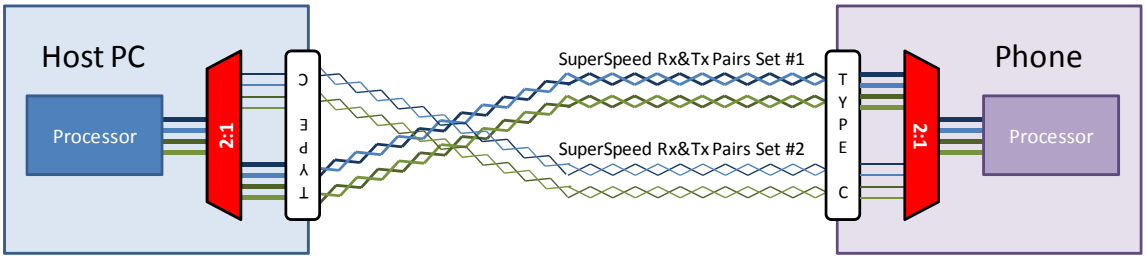

Figure 2. Typical Application

Pin Configuration

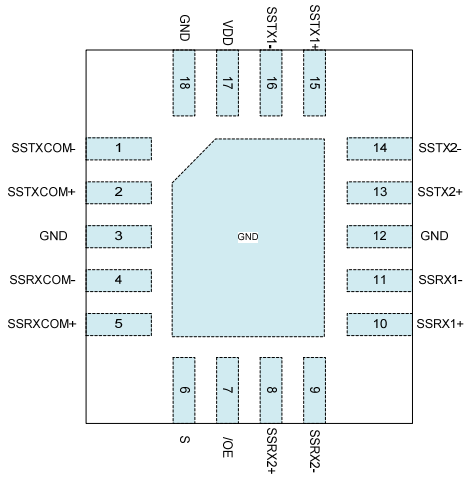

Figure 3. Pin Assignment (Top Through View)

Pin Descriptions

Pin #	Name	Type	Description
1	SSTXCOM-	SW	SuperSpeed TX- Common
2	SSTXCOM+	SW	SuperSpeed TX+ Common
3	GND	GND	Ground (connected to die attach pad)
4	SSRXCOM-	SW	SuperSpeed RX- Common
5	SSRXCOM+	SW	SuperSpeed RX+ Common
6	S	Input	Switch Select (0=SW1, 1=SW2)
7	/OE	Input	Output Enable (0=Switches Enabled, 1=Switches Disabled)
8	SSRX2+	SW	SuperSpeed RX2+
9	SSRX2-	SW	SuperSpeed RX2-
10	SSRX1+	SW	SuperSpeed RX1+
11	SSRX1-	SW	SuperSpeed RX1-
12	GND	GND	Ground (connected to die attach pad)
13	SSTX2+	SW	SuperSpeed TX2+
14	SSTX2-	SW	SuperSpeed TX2-
15	SSTX1+	SW	SuperSpeed TX1+
16	SSTX1-	SW	SuperSpeed TX1-
17	V_{DD}	VDD	Device Power
18	GND	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5	6.0	V
V_{CNTRL}	DC Input Voltage (S, /OE)(1)		-0.5	V_{DD}	V
V_{SW}	DC Switch I/O Voltage(1,2)		-0.3	2.1	V
I_{IK}	DC Input Diode Current		-50		mA
I_{sw}	DC Switch Current			25	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	2		kV
	IEC 61000-2-4, Level 4, for Switch Pins	Contact	8		
		Air	15		
	Charged Device Model, JESD22-C101		1		

Notes:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	1.5	5.0	V
$t_{RAMP(VDD)}$	Power Supply Slew Rate	100	1000	µs/V
V_{CNTRL}	Control Input Voltage (S, /OE)(3)	0	5.0	V
V_{SW}	Switch I/O Voltage (Both SSUSB Switch Paths)	0	2.0	V
T_A	Operating Temperature	-40	+85	°C

Note:

3. The control inputs must be held HIGH or LOW; they must not float.

DC and Transient Characteristics

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{DD} (V)	T_A= -40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage S, /OE	I_{IN}=-18 mA	1.5	-1.2		-0.6	V
I_{IK}	Clamp Diode Current (Switch Pins)	V_{IN}=-0.3 V	0			18	µA
V_{IH}	Control Input Voltage High	S, /OE	1.5	1.30			V
		S, /OE	3.6	1.4			V
		S, /OE	5.0	1.5			V
V_{IL}	Control Input Voltage Low	S, /OE	1.5			0.4	V
		S, /OE	3.6			0.4	V
		S, /OE	5.0			0.4	V
I_{IN}	Control Input Leakage	V_{SW}= -0.6 to 2.0 V V_{CNTRL}=0 to V_{DD}	5.0	-500		500	nA
I_{OZ}	Off-State Leakage for Open Data Paths	V_{SW}= 0.0 ≤ DATA ≤ 2.0 V	5.0	-0.5		0.5	µA
I_{CL}	On-State Leakage for Closed Data Paths(4)	V_{SW}= 0.0 ≤ DATA ≤ 2.0 V	5.0	-0.5		0.5	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}= 0 V or 2.0 V	0	-500		500	nA
R_{ON}	Switch On Resistance	V_{SW}= 0 V, I_{ON}=-8 mA	1.5		5.4	8.0	Ω
ΔR_{ON}	Difference in R_{ON} Between Positive-Negative	V_{SW}= 0 V, I_{ON}=-8 mA	1.5		0.1		Ω
R_{ONF}	Flatness for R_{ON}	V_{SW}= 0 ≤ DATA ≤ 2.0 V, I_{ON}=-8 mA	1.5		0.9		Ω
I_{CC}	Quiescent Supply Current	$V_{/OE}$=0, V_{SEL}=0 or V_{DD}, I_{OUT}=0	5.0		12	30	µA
I_{CCZ}	Quiescent Supply Current (High Impedance)	V_{SEL}=X, $V_{/OE}$=V_{DD}, I_{OUT}=0	5.0			1	µA
I_{CCT}	Increase in Quiescent Supply Current per V_{CNTRL}	V_{SEL} or $V_{/OE}$=1.5 V	5.0		5	15	µA

Note:

4. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical value are for V_{DD} =3.6 V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{DD} (V)	T_A= -40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time, S to Output	R_L=50 Ω, C_L=0 pF, V_{SW}=0 V, V_{SW}=0.6 V	1.5 to 5.0 V		350	600	ns
t_{OFF}	Turn-Off Time, S to Output	R_L=50 Ω, C_L=0 pF, V_{SW}=0 V, V_{SW}=3.3 V	1.5 to 5.0 V		125	300	ns
$t_{ZHM,ZL}$	Enable Time, /OE to Output	R_L=50 Ω, C_L=0pF, V_{SW}=0.6 V	1.5 to 5.0 V		60	150	µs
$t_{LZM,HZ}$	Disable Time, /OE to Output	R_L=50 Ω, C_L=0 pF, V_{SW}=0.6 V	1.5 to 5.0 V		35	240	ns
t_{PD}	Propagation Delay(5)	C_L=, C_L=0 pF, R_L=50 Ω,	1.5 to 5.0 V		60		ps
t_{BBM}	Break-Before-Make(5)	R_L=50 Ω, C_L=0 pF, V_{SW1}=0.6 V,V_{SW2}= -0.6 V,	1.5 to 5.0 V	100		350	ns
DO_{IRR}	Differential Off Isolation(5)	V_S=0dBm, R_L=50 Ω, f=2.5 GHz	3.6 V		-28		dB
		V_S=0dBm, R_L=50 Ω, f=5.0 GHz			-25		
SDDNEXT	Differential Channel Crosstalk(5)	V_S=0dBm, R=50 Ω, f=2.5 GHz	3.6 V		-44		dB
		V_S=0dBm, R=50 Ω, f=5.0 GHz			-40		
DIL	Differential Insertion Loss(5) (All Data Paths)	V_{IN}=0dBm, f=2.5 GHz, R_L=50 Ω, C_L=0 pF	3.6 V		-1.0		dB
		V_{IN}=0dBm, f=5.0 GHz, R_L=50 Ω, C_L=0 pF			-1.8		
BW	Differential -3 dB Bandwidth(5)	V_{IN}=1 V_{pk-pk}, R_L=50 Ω, C_L=0 pF, (Both Data Paths)	3.6 V		10		GHz
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(5)	R_{PU}=50 Ω to V_{DD}, C_L=0 pF	3.6 V		6		ps
C_{IN}	Control Pin Input Capacitance (5)	V_{DD}=0 V, f=1 MHz			2.7		pF
C_{ON}	On Capacitance (5)	V_{DD}=3.3 V, f=2.5 GHz			0.5		pF
C_{OFF}	Off Capacitance (5)	V_{DD}=3.3 V, f=2.5 GHz			0.4		pF

Note:

5. Guaranteed by characterization.

Eye Diagrams

All plots below are for V_{DD}=3.6 V and T_A=25°C with 0 dBm differential data.

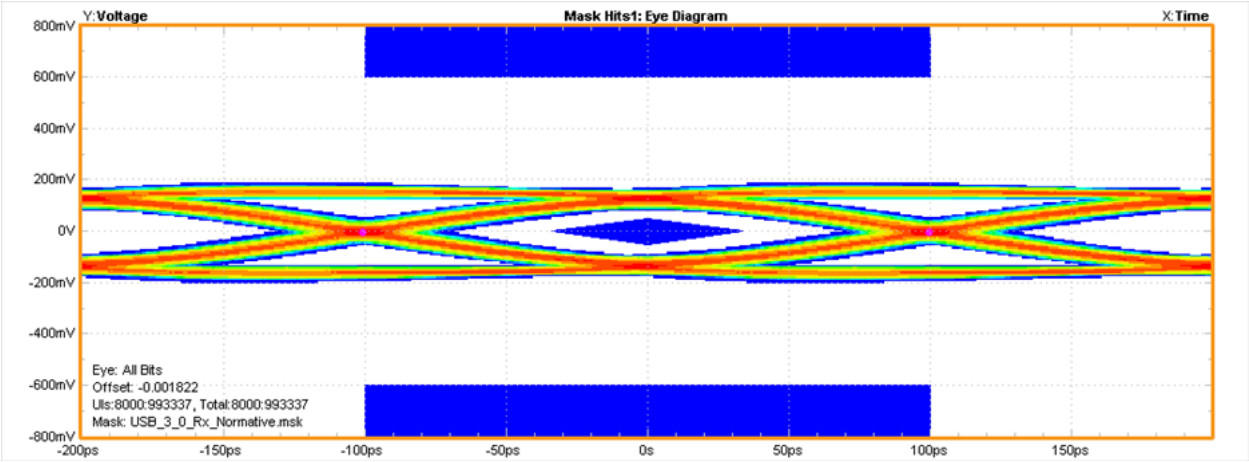

Figure 4. 5 Gbps Eye Diagram with Eye Mask

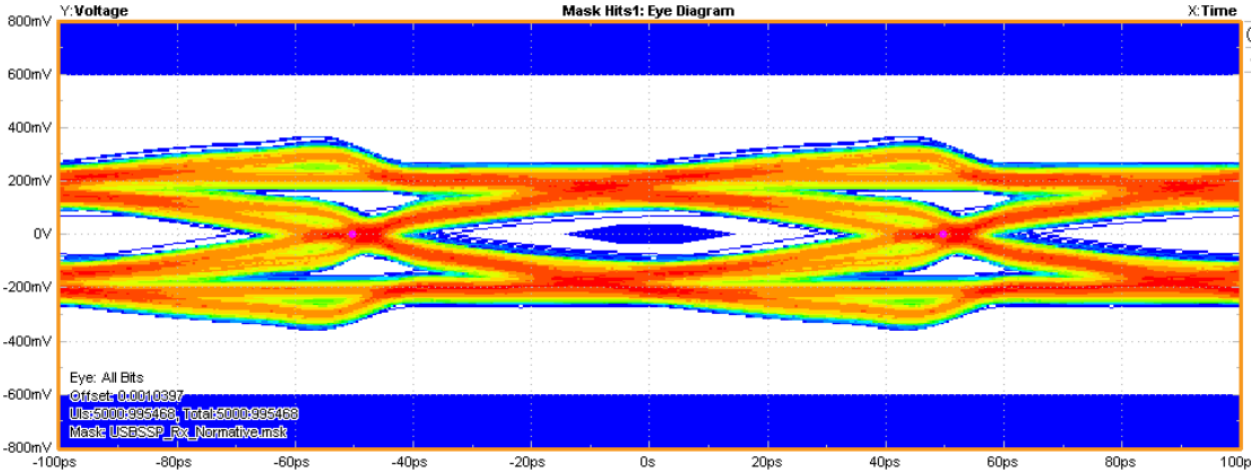

Figure 5. 10 Gbps Eye Diagram with Eye Mask

The table below pertains to the UMLP Package drawing on the following page.

Product-Specific Dimensions

Product	A	B
FUSB340TMX	2.00 mm	2.80 mm

Physical Dimensions

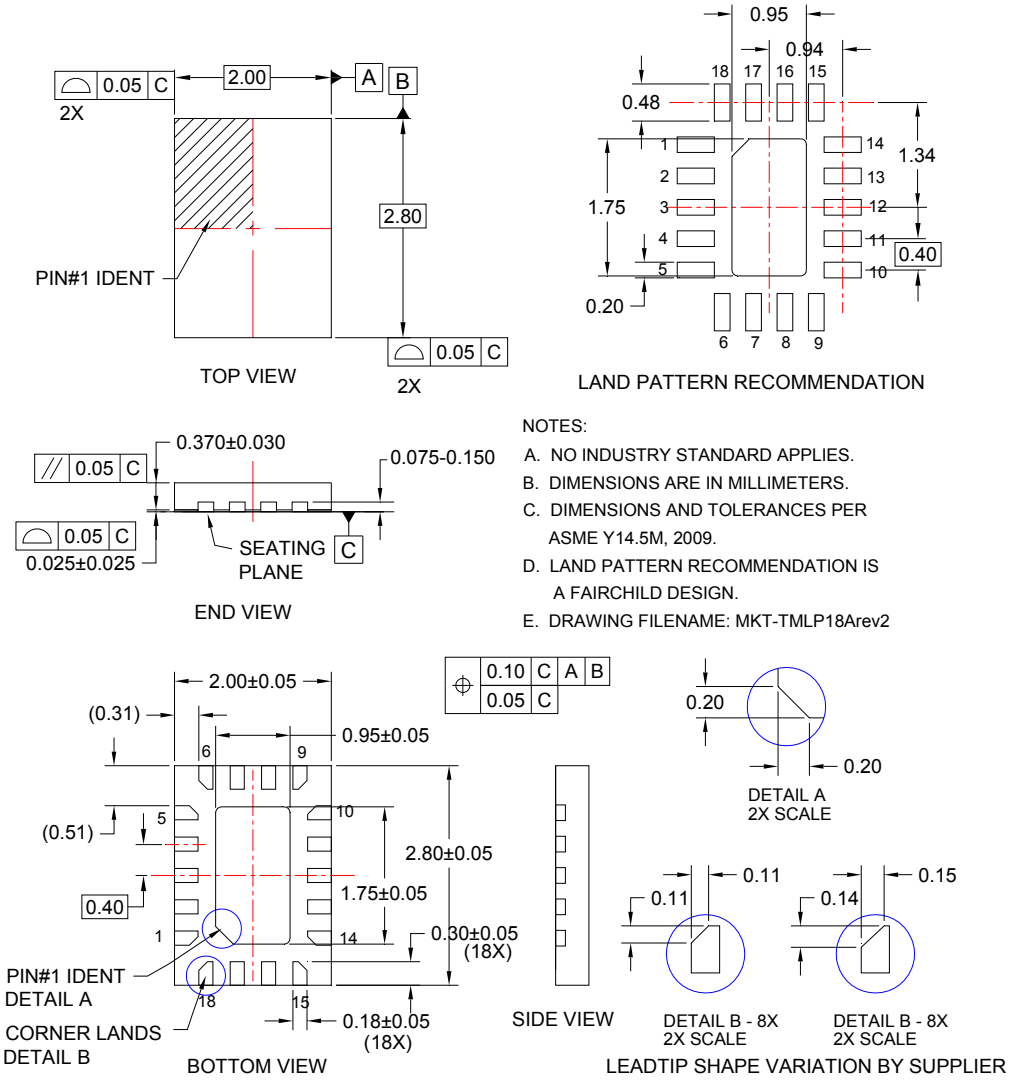

Figure 6. 18 Lead, UMLP, Quad, Ultra-Thin MLP, 1.8 x 2.6 mm

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
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