



ON Semiconductor®

FPF2280 Over-Voltage Protection Load Switch

Features

- Surge Protection
 - IEC 61000-4-5: > 100 V
- Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- ESD Protection
 - Human Body Model (HBM): > 3.5 kV
 - Charged Device Model (CDM): > 2 kV
 - IEC 61000-4-2 Air Discharge: > 15 kV
 - IEC 61000-4-2 Contact Discharge: > 8 kV

Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players

Description

The FPF2280 features a low- R_{ON} internal FET and an operating range of $2.5 V_{DC}$ to $5.5 V_{DC}$ (absolute maximum of $29 V_{DC}$). An internal clamp is capable of shunting surge voltages >100 V, protecting downstream components and enhancing system robustness. The FPF2280 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors. Over-temperature protection also powers down the device at $130^{\circ}C$ (typical). Exceptionally low off-state current (<1 μA maximum) facilitates compliance with standby power requirements.

The FPF2280 is available in a fully “green” compliant $1.3 \text{ mm} \times 1.8 \text{ mm}$ Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

Related Resources

- <http://www.onsemi.com/>

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2280BUCX-F130	-40°C – 105°C	HC	12-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

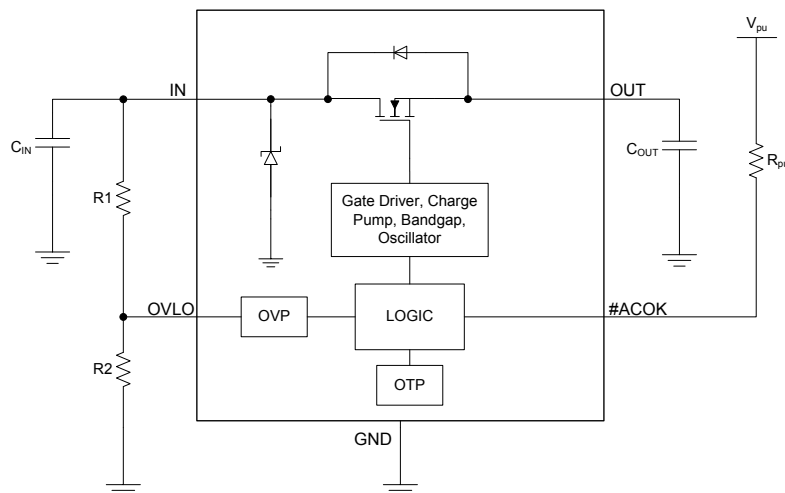


Figure 1. Functional Block Diagram

Pin Configuration

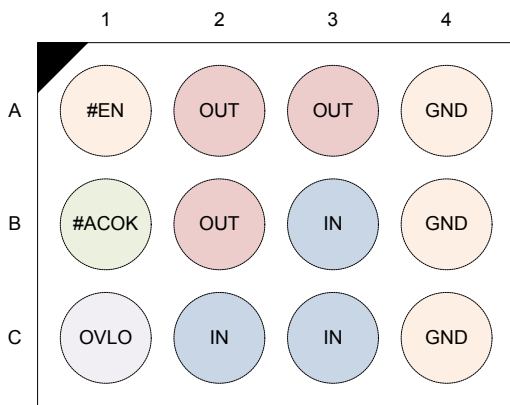
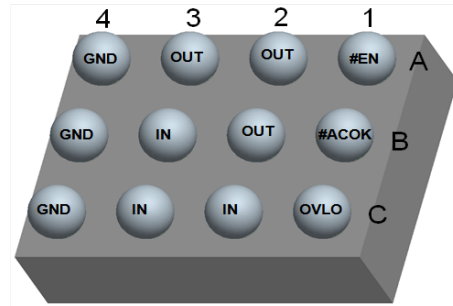
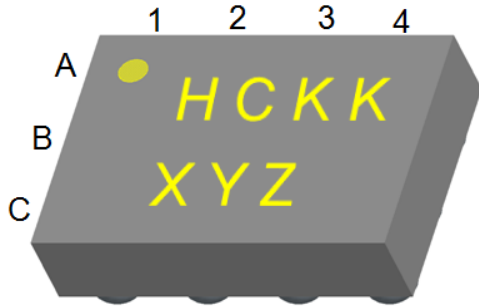


Figure 2. Pin Configuration (Top View)

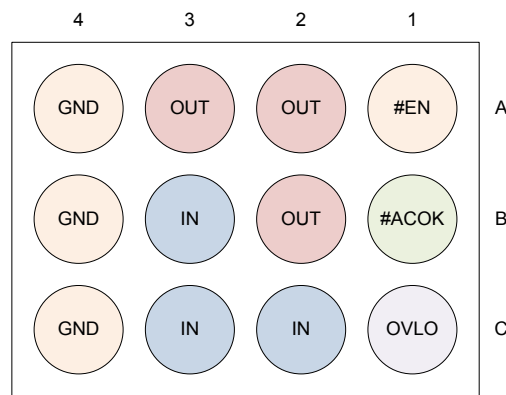


Figure 3. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description	
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply	
OUT	A2, A3, B2	Output	Switch Output to Load	
#ACOK	B1	Output (Open Drain)	1	$V_{IN} < V_{IN_min}$ or $V_{IN} \geq V_{OVLO}$
			0	Voltage Stable
#EN	A1	Input	Device Enable (Active LOW)	
OVLO	C1	Input	Over-Voltage Lockout Adjustment Pin	
GND	A4, B4, C4	Supply	Device Ground	

Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVP. By connecting an external resistor-driver to the OVLO pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{IN_OLVO} = V_{OVLO_TH} \times [1 + R1/R2] \quad (1)$$

Recommended minimum R1 = 1 MΩ.

On-The-Go (OTG) Functionality

During OTG operation, the FPF2280 is initially disabled and the power FET's bulk diode is forward biased. The bulk diode represents ~0.7 V drop across the device, which remains until the V_{IN} voltage increases past 2.5 V, when the device is fully enabled. While the device is disabled and the body diode is forward biased, the max DC current through the diode is 1.8 A. This current is limited by the thermal performance of the device

(0.7 V × 1.8 A = 1.36 W). This current should be transient; the #EN pin must be pulled LOW to ensure the device fully enables. The transient should not exceed the RC time constant of the C_{IN} and C_{OUT} capacitors. At the system level, over-voltage and current protection should be provided outside the FPF2280.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	V _{IN} to GND & V _{IN} to V _{OUT} = GND or Float	-0.3	29.0	V
V _{OUT}	V _{OUT} to GND	-0.3	V _{IN} + 0.3	V
V _{OVLO}	OVLO to GND	-0.3	24.0	V
V _{#EN_ACOK}	Maximum DC Voltage Allowed on #EN or ACOK Pin		6	V
I _{IN}	Switch I/O Current (Continuous)		4.5	A
t _{PD}	Total Power Dissipation at T _A = 25°C		1.48	W
T _{STG}	Storage Temperature Range	-65	+150	°C
T _J	Maximum Junction Temperature		+150	°C
T _L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
θ _{JA}	Thermal Resistance, Junction-to-Ambient ⁽¹⁾ (1-in. ² Pad of 2-oz. Copper)		84.1	°C/W
ESD	IEC 61000-4-2 System ESD	Air Gap	15.0	kV
		Contact	8.0	
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	3.5	
	Charged Device Model, JESD22-C101	All Pins	2.0	
Surge	IEC 61000-4-5, Surge Protection	V _{IN}	100	V

Note:

1. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Supply Voltage	2.5	20.0	V
T _A	Operating Temperature	-40	+105	°C

Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 105°C unless otherwise indicated. Typical values are $V_{IN} = 5.0\text{ V}$, $I_{IN} \leq 3\text{ A}$, $C_{IN} = 0.1\text{ }\mu\text{F}$ and $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN_CLAMP}	Input Clamping Voltage	$I_{IN} = 10\text{ mA}$		35		V
I_Q	Input Quiescent Current	$V_{IN} = 5\text{ V}$, $\#EN = 0\text{ V}$		58	100	μA
I_{IN_Q}	OVLO Supply Current	$V_{OVLO} = 3\text{ V}$, $V_{IN} = 5\text{ V}$, $V_{OUT} = 0\text{ V}$		63	100	μA
V_{IN_OVLO}	Internal Over-Voltage Trip Level	V_{IN} Rising, $OVLO = \text{GND}$	6.6	6.8	7.0	V
		V_{IN} Falling	6.2			V
V_{OVLO_TH}	OVLO Set Threshold	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	1.12	1.20	1.24	V
V_{OVLO_RNG}	Adjustable OVLO Threshold Range	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	4		20	V
V_{OVLO_SELECT}	External OVLO Select Threshold			0.30	0.28	V
R_{ON}	Resistance from V_{IN} to V_{OUT}	$V_{IN} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$, $T_A = 25^{\circ}\text{C}$		30	39	$\text{m}\Omega$
C_{OUT}	OUT Load Capacitance ⁽²⁾	$V_{IN} = 5\text{ V}$			1000	μF
I_{OLVO}	OVLO Input Leakage Current	$V_{OVLO} = V_{OVLO_TH}$	-100		100	nA
T_{SDN}	Thermal Shutdown ⁽²⁾			130		$^{\circ}\text{C}$
T_{SDN_HYS}	Thermal Shutdown Hysteresis ⁽²⁾			20		$^{\circ}\text{C}$
Digital Signals						
V_{OL}	#ACOK Output Low Voltage	$V_{IO} = 3.3\text{ V}$, $I_{SINK} = 1\text{ mA}$			0.4	V
$V_{IH_}\#EN$	Enable HIGH Voltage	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	1.2			V
$V_{IL_}\#EN$	Enable LOW Voltage	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}			0.5	V
I_{ACOK_LEAK}	#ACOK Leakage Current	$V_{IO} = 3.3\text{ V}$, #ACOK Deasserted, #EN = 0 V	-0.5		0.5	μA
$\#EN_Leak$	#EN Leakage Current	$V_{IN} = 5.0\text{ V}$, $V_{OUT} = \text{Float}$	-1.0		1.0	μA
Timing Characteristics						
t_{DEB}	Debounce Time	Time from $2.5\text{ V} < V_{IN} < V_{IN_OVLO}$ to $V_{OUT} = 0.1 \times V_{IN}$		15		ms
t_{START}	Soft-Start Time	Time from $V_{IN} = V_{IN_min}$ to $0.2 \times \#ACOK$, $V_{IO} = 1.8\text{ V}$ with $10\text{ k}\Omega$ Pull-up Resistor		30		ms
t_{ON}	Switch Turn-On Time	$V_{IN} = 5\text{ V}$, $R_L = 100\text{ }\Omega$, V_{OUT} from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$, $C_{LOAD} = 100\text{ }\mu\text{F}$		2		ms
t_{OFF}	Switch Turn-Off Time ⁽²⁾	$R_L = 100\text{ }\Omega$, $C_L = 0\text{ }\mu\text{F}$, $V_{IN} > V_{OVLO}$ to $V_{OUT} = 0.8 \times V_{IN}$		125		ns

Note:

- Guaranteed by characterization and design.

Timing Diagrams

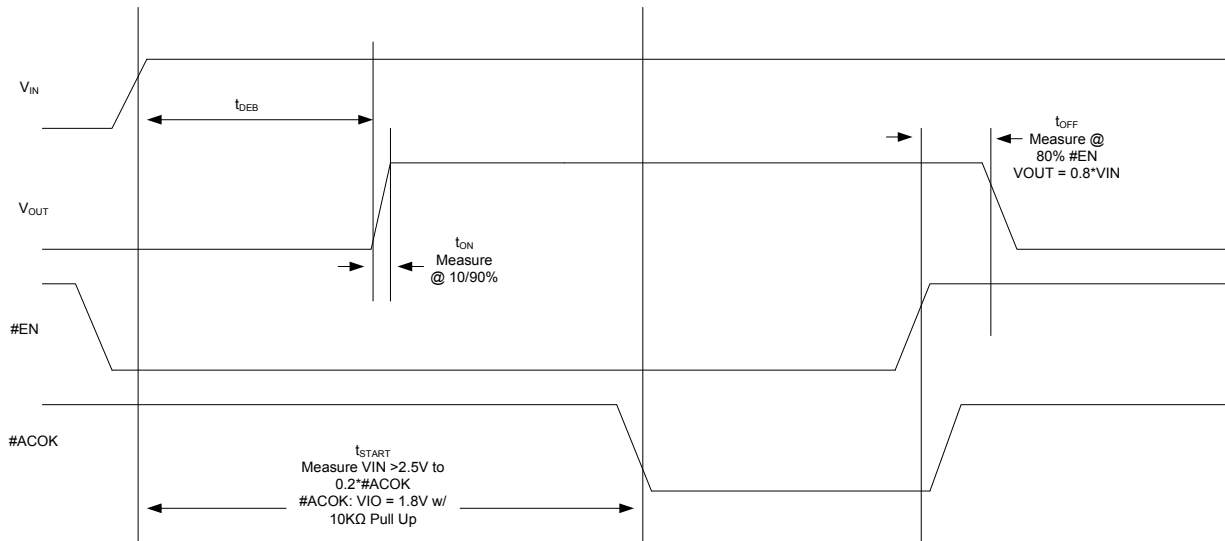


Figure 4. Timing for Power Up and Normal Operation

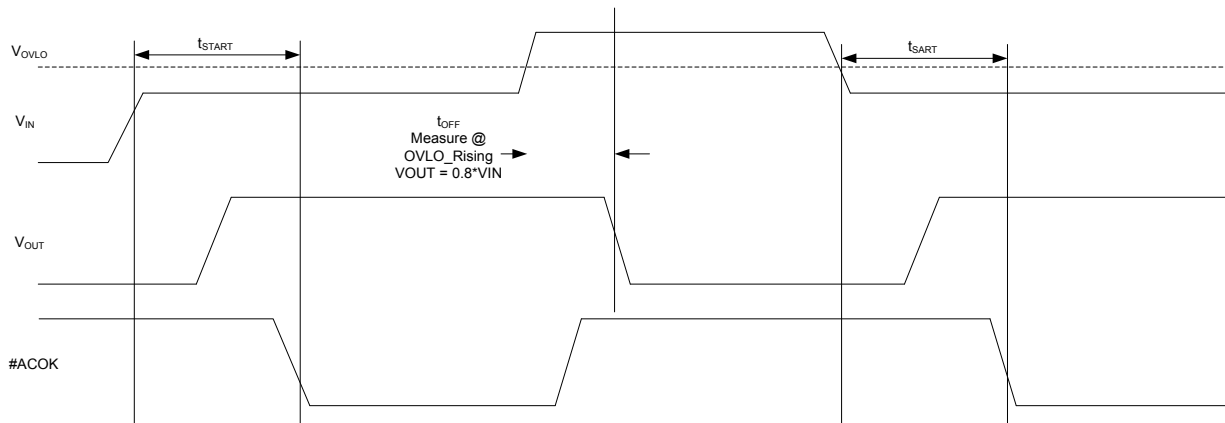
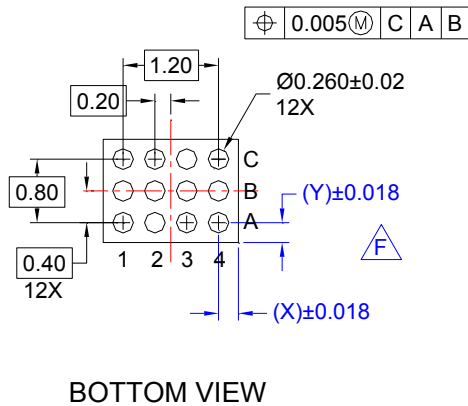
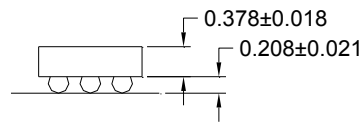
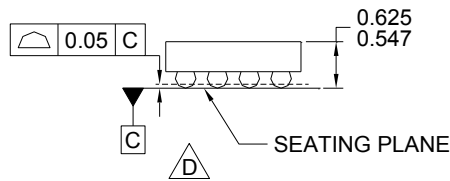
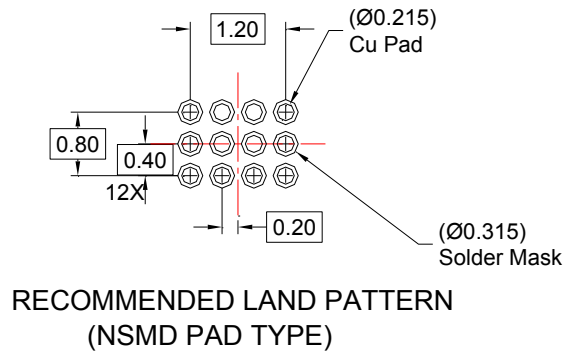
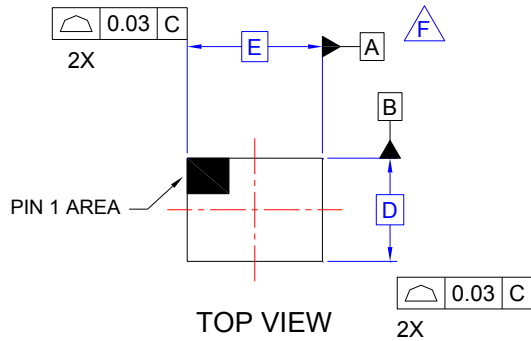


Figure 5. Timing for OVLO Trip

Product-Specific Package Dimensions

D	E	X	Y
1288 $\mu\text{m} \pm 30 \mu\text{m}$	1828 $\mu\text{m} \pm 30 \mu\text{m}$	314 $\mu\text{m} \pm 18 \mu\text{m}$	244 $\mu\text{m} \pm 18 \mu\text{m}$

Physical Dimensions



NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC012ZCrev2..
- H. ON SEMICONDUCTOR RECOMMENDS THAT LANDS IN THE LANDPATTERN ARE AT LEAST .215MM DIAMETER AS MEASURED AT THE BOTTOM OF THE LAND, NOT THE TOP EDGE

Figure 6. 12-Ball, 3x4 Array, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

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