DATA SHEET
www.onsemi.com

MOSFET – N-Channel, POWERTRENCH®

80 V, 80 A, 4.5 mΩ

FDWS86368-F085

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
80 V	4.5 mΩ @ 10 V	80 A

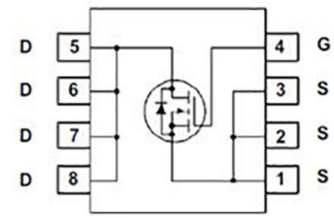
Features

- Typical $R_{DS(on)}$ = 3.7 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 57 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC−Q101 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

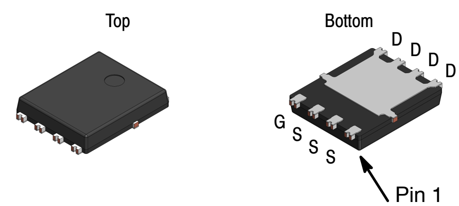
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

ELECTRICAL CONNECTION



N−Channel MOSFET



DFNW8
CASE 507AU

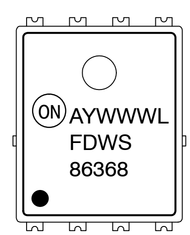
MOSFET MAXIMUM RATINGS (T_J = 25°C, Unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain−to−Source Voltage	80	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current (T_C = 25°C) Continuous (V_{GS} = 10 V) (Note 1) Pulsed	80 (See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	82	mJ
P_D	Power Dissipation	214	W
	Derate Above 25°C	1.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.7	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 40 μH, I_{AS} = 64 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
WL	= Assembly Lot
FDWS	= Device Code
86368	= Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDWS86368−F085	DFNW8 (Power56) (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications,

October, 2021 − Rev. 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS						
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25°C			1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 175°C (Note 4)			1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80 A, V_{GS} = 10 V, T_J = 25°C		3.7	4.5	mΩ
		I_D = 80 A, V_{GS} = 10 V, T_J = 175°C (Note 4)		7.4	9.0	
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		4350		pF
C_{oss}	Output Capacitance			636		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
R_g	Gate Resistance	f = 1 MHz		2.5		Ω
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 64 V, I_D = 80 A		57	75	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V		8		nC
Q_{gs}	Gate−to−Source Gate Charge			23		nC
Q_{gd}	Gate−to−Drain “Miller” Charge			11		nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10V, R_{GEN} = 6 Ω			60	ns
$t_{d(on)}$	Turn−On Delay			23		ns
t_r	Rise Time			22		ns
$t_{d(off)}$	Turn−Off Delay			32		ns
t_f	Fall Time			13		ns
t_{off}	Turn−Off Time				59	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Voltage	V_{GS} = 0 V, I_{SD} = 80 A V_{GS} = 0 V, I_{SD} = 40 A			1.25 1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 80 A, $\Delta I_{SD}/\Delta t$ = 100 A/μs, V_{DD} = 64 V		58	75	ns
Q_{rr}	Reverse−Recovery Charge			49	67	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

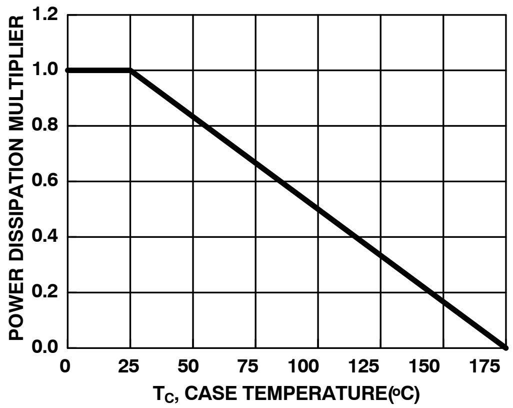


Figure 1. Normalized Power Dissipation vs. Case Temperature

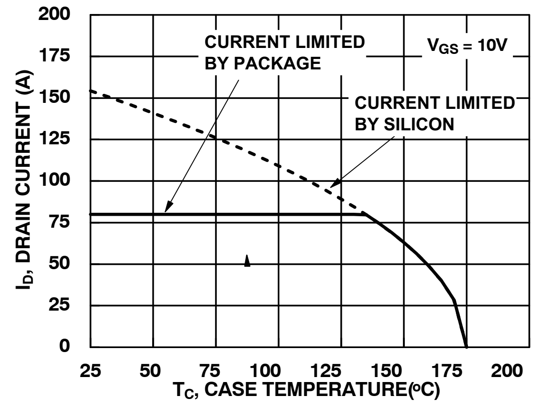


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

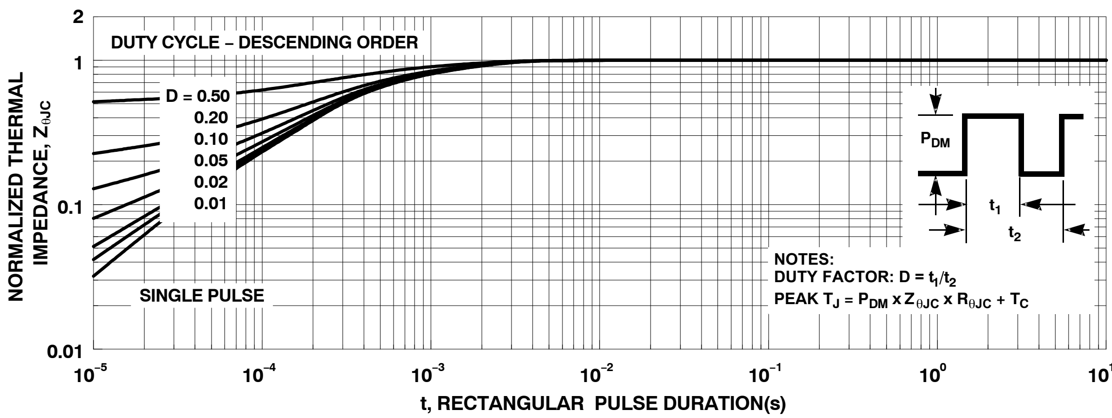


Figure 3. Normalized Maximum Transient Thermal Impedance

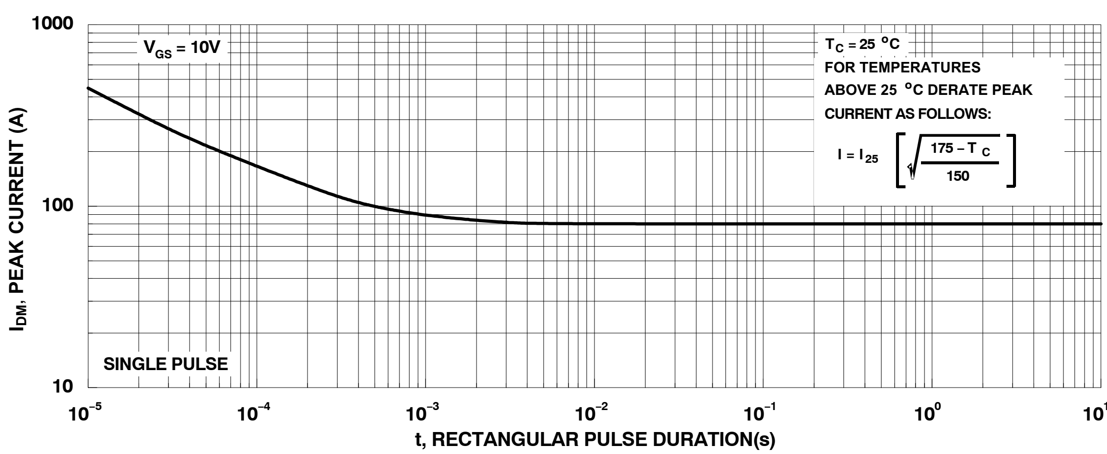


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

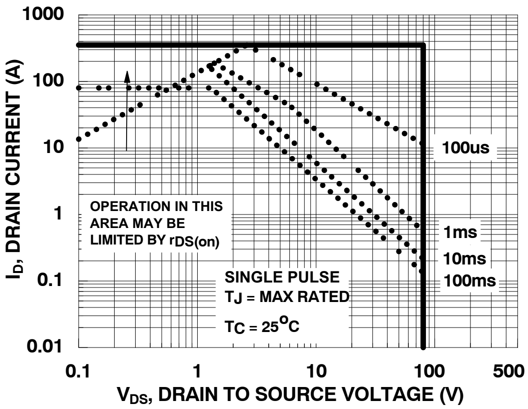
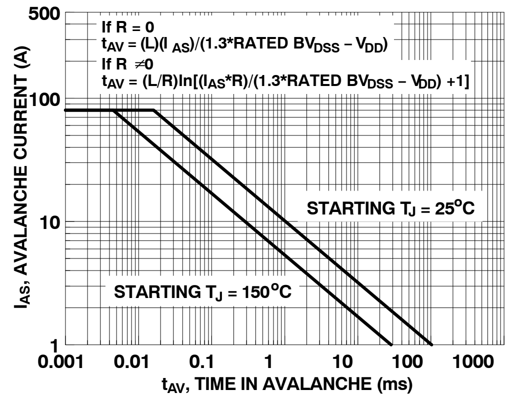


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

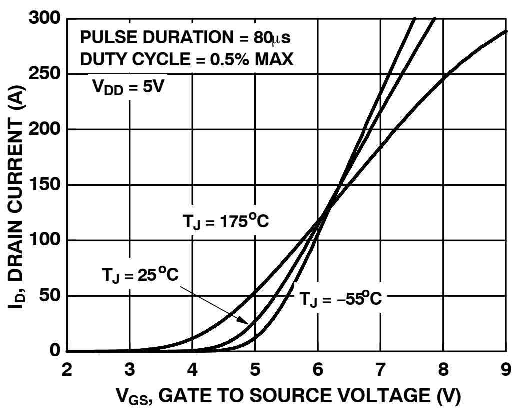


Figure 7. Transfer Characteristics

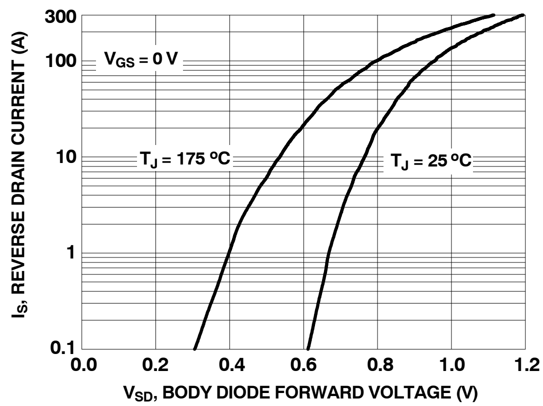


Figure 8. Forward Diode Characteristics

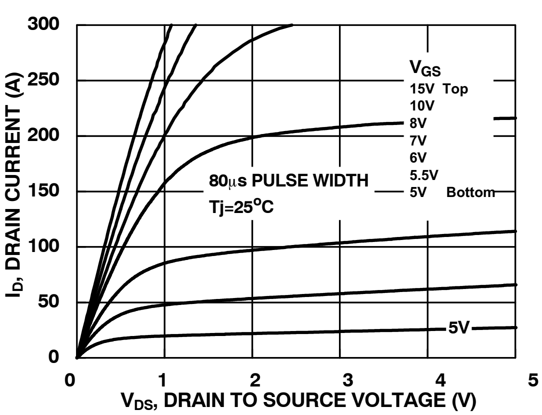


Figure 9. Saturation Characteristics

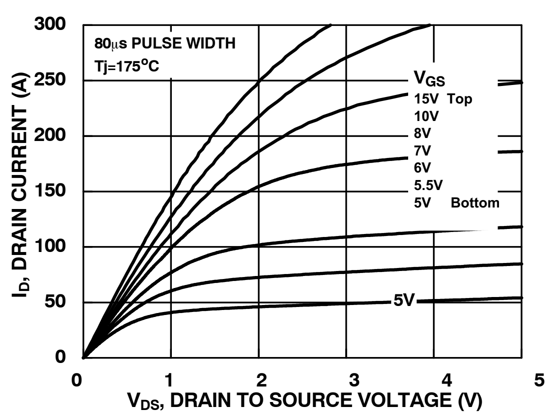


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

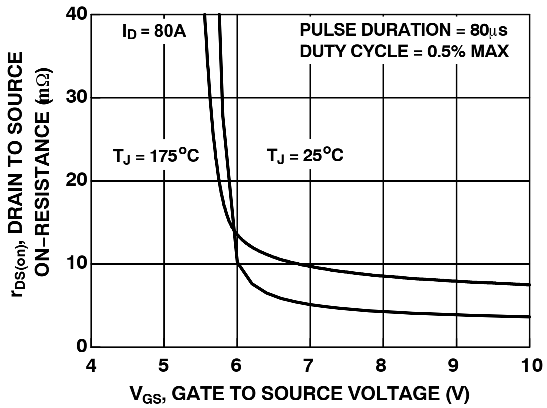


Figure 11. R_{DSON} vs. Gate Voltage

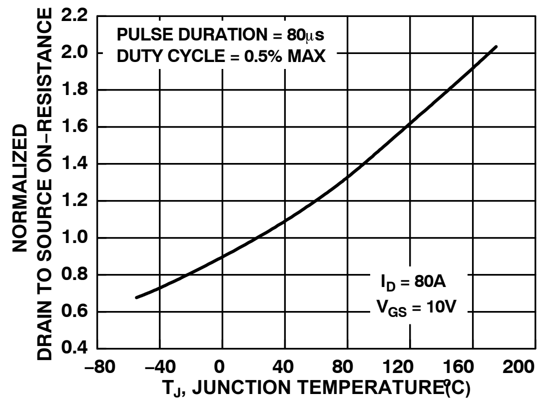


Figure 12. Normalized R_{DSON} vs. Junction Temperature

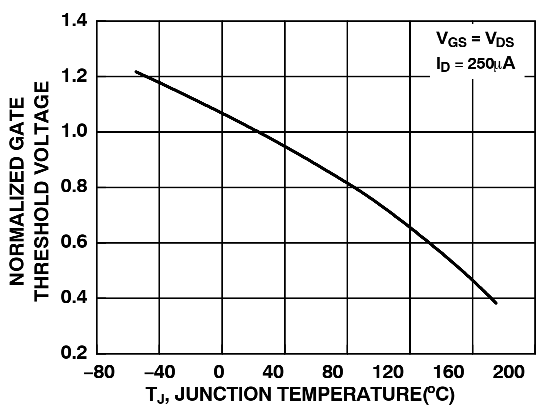


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

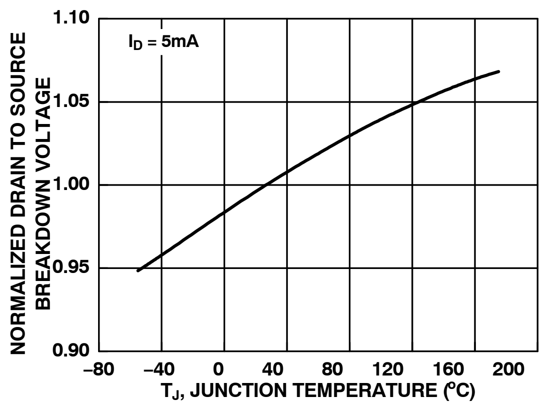


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

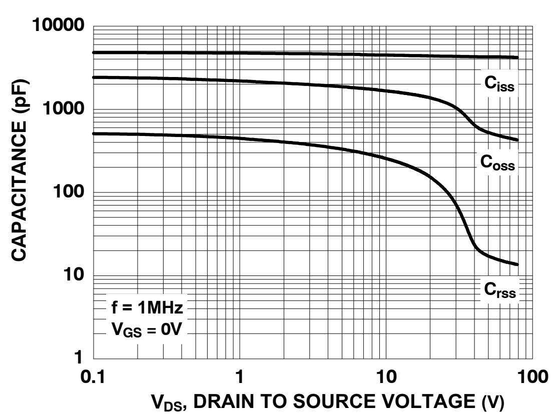


Figure 15. Capacitance vs. Drain to Source Voltage

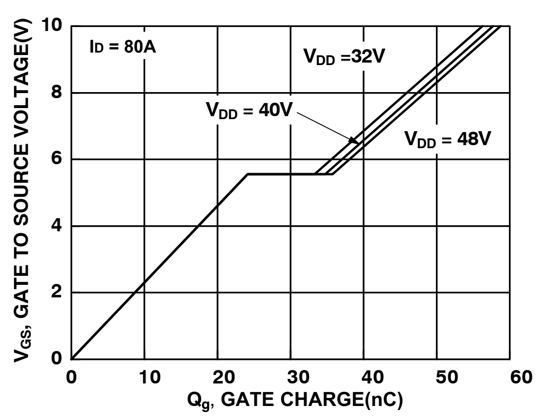
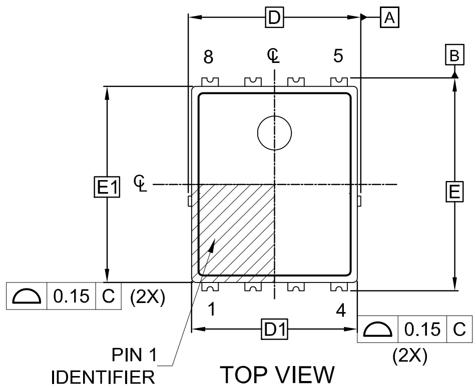


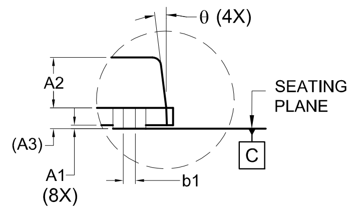
Figure 16. Single Pulse Maximum Power Dissipation

PACKAGE DIMENSIONS

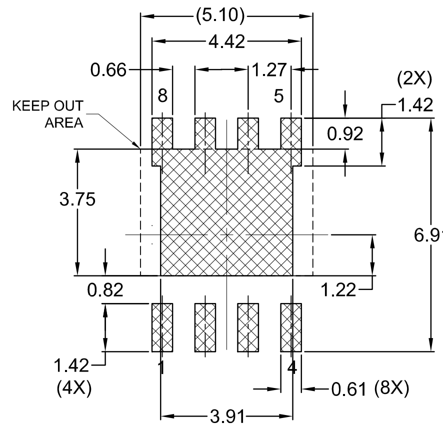
DFNW8 5.2x6.3, 1.27P
CASE 507AU
ISSUE A



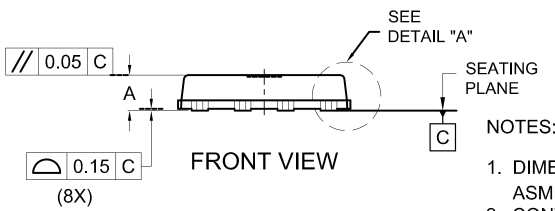
TOP VIEW



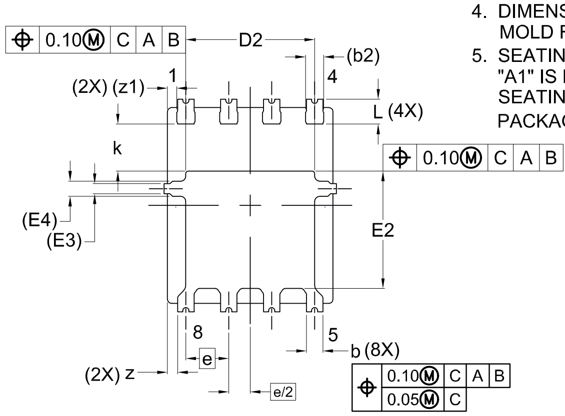
DETAIL "A"
SCALE: 2:1



LAND PATTERN
RECOMMENDATION



FRONT VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	-	-	0.05
A2	0.65	0.75	0.85
A3	0.30 REF		
b	0.47	0.52	0.57
b1	0.13	0.18	0.23
b2	(0.54)		
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30 REF		
E4	0.45 REF		
e	1.27 BSC		
e/2	0.635BSC		
k	1.30	1.40	1.50
L	0.64	0.74	0.84
z	0.24	0.29	0.34
z1	(0.28)		
ϴ	0°	---	12°

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