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July 2016

FAN6240
Secondary-Side Synchronous Rectifier Controller for Flyback Converters

Features

- Works in Discontinuous Conduction Mode (DCM).
- Adaptive Turn-off Trigger Blanking Time for easier use
- Turn-on Trigger Blanking Time (Minimum-OFF Time) for Improved Noise Immunity
- Supports High-Frequency Applications up to 200 kHz
- Minimum Turn-on Delay (20 ns)
- Adaptive Turn-off Threshold Control for Minimized SR MOSFET Body Diode Conduction (Dead-Time is independent of SR MOSFET)
- Wide Voltage Range for LDO Input up to 30 V
- Small Footprint: SOT-23 6 Pin Package

Description

The FAN6240M6X is a secondary-side synchronous rectifier (SR) controller for an isolated flyback converter operating in Discontinuous Conduction Mode (DCM). The adaptive dead-time control algorithm minimizes the body diode conduction of SR MOSFET while guaranteeing stable and robust SR operation against noise and disturbance caused by the circuit parasitic. 30 V rated input voltage LDO and Low VDD Under-Voltage Lockout (UVLO) voltage allow FAN6240M6X to be used for wide ranges of switched mode power supply output voltage without additional circuit.

Applications

- Battery Chargers for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices that Require CV/CC Control

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6240M6X	-40°C to +125°C	6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide	Tape & Reel

Application Diagram

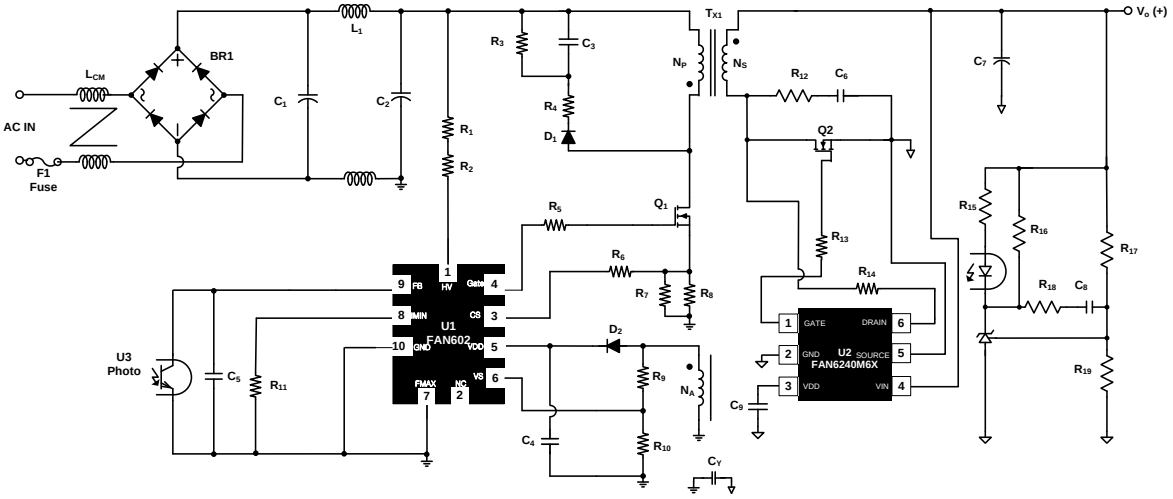


Figure 1. Typical Application

Internal Block Diagram

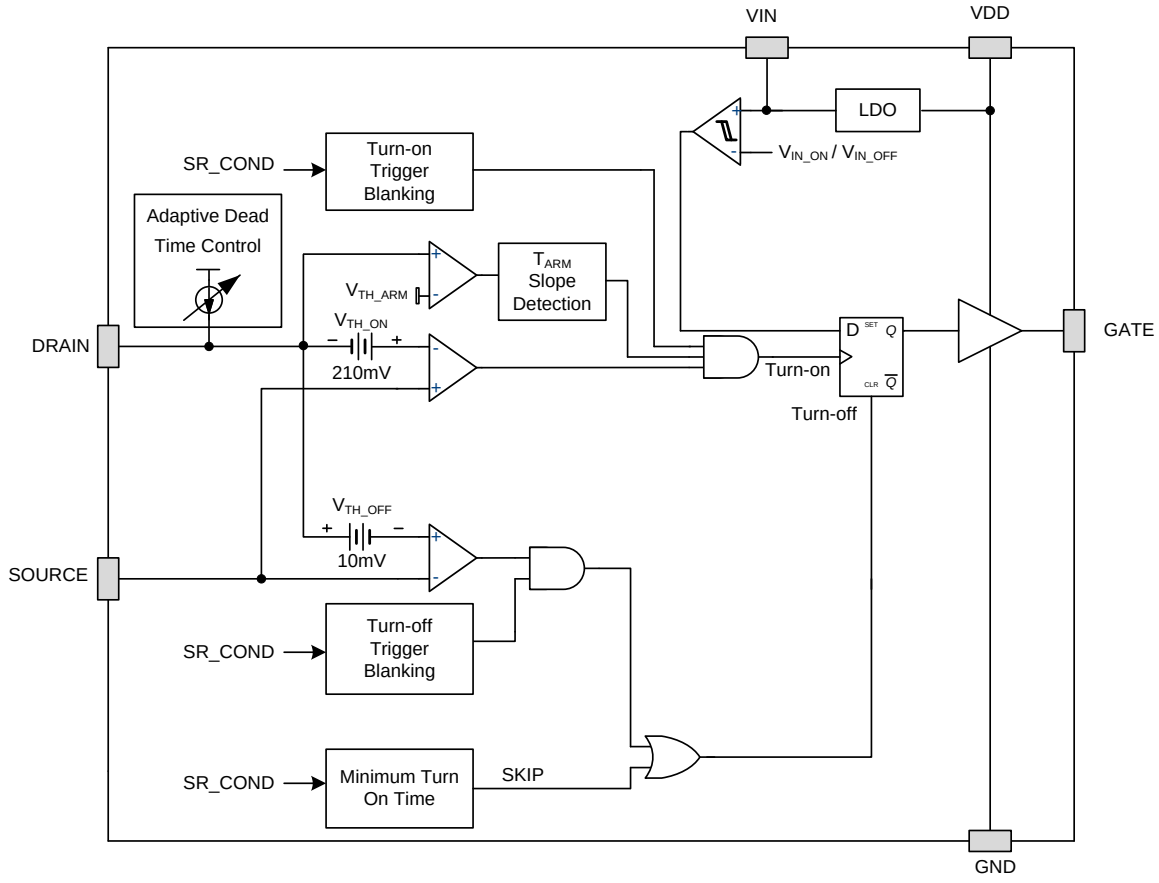
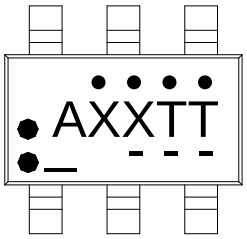


Figure 2. Function Block Diagram

Marking Information



Axx: ACD: FAN6240M6X
TT: Wafer Lot Code
●●●●: Year Code
_ _ _: Week Code

Figure 3. Top Mark

Pin Configuration

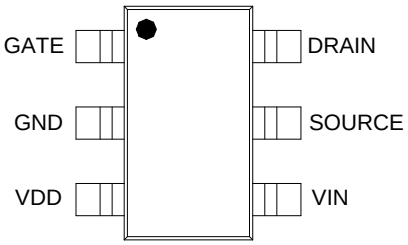


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GATE	Gate drive output
2	GND	Ground
3	VDD	Internal regulator 5 V output and gate drive power supply rail. Bypass with 1uF capacitor to GND.
4	VIN	LDO input, supports up to 30 V operation. An integrated 5 V LDO generates the internal VDD power supply rail for the low-voltage control circuitry.
5	SOURCE	Synchronous rectifier source sense input.
6	DRAIN	Synchronous rectifier drain sense input.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Power Supply Input Pin Voltage		-0.3	30	V
V_{DD}	Internal Regulator Output Pin Voltage		-0.3	6.5	V
V_{DRAIN}	Drain Sense Input Pin Voltage		-1	100	V
V_{GATE}	Gate Drive Output Pin Voltage		-0.3	6.5	V
V_{SOURCE}	Source Sense Input Pin Voltage		-1	1	V
P_D	Power Dissipation (T_A=25°C)			23	mW
Θ_{JA}	Thermal Resistance (Junction-to-Ambient Thermal)			235	°C/W
T_J	Operating Junction Temperature		-40	150	°C
T_{STG}	Storage Temperature Range		-60	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012		2.5	kV
		Charged Device Model, JESD22-C101		1.5	

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values are with respect to the GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply Input Pin Voltage	2.8		20	V
V_{DD}	Internal Regulator Output Pin Voltage	2.8		6	V
V_{DRAIN}	Drain Sense Input Pin Voltage	-0.3		100	V
V_{GATE}	Gate Drive Output Pin Voltage	-0.3		6	V
V_{SOURCE}	Source Sense Input Pin Voltage	-0.3		1	V

Electrical Characteristics

V_{IN} = 12 V and T_J = -40°C to 125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage						
V_{IN_ON}	Turn-On Threshold	V_{IN} Rising	3.1	3.4	3.7	V
V_{IN_OFF}	Turn-Off Threshold	V_{IN} Falling	2.8	2.9	3.0	V
I_{IN_OP}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 3.3 nF, V_{IN} = 5 V		2	3.5	mA
Power Supply Section						
V_{DD}	Internal LDO Output Voltage	V_{IN} = 20 V	5.00	5.25	5.50	V
Drain Voltage Sensing Section						
I_{OFFSET}		Maximum of adaptive offset current (15 steps, 6 µA resolution)	75	90	105	µA
V_{TH_ON}	Turn-On Threshold	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)	-235	-210	-185	mV
$T_{ON.DLY}$[3]	Turn-On Delay			20		ns
V_{TH_OFF}[3]	Turn-Off Threshold			10		mV
$T_{OFF.DLY}$[3]	Turn-Off Delay			20		ns
V_{TH_ARM}	Gate Re-arming Threshold	V_{IN} = 5 V, (Typically 0.7*V_{DD})	3.3	3.5	3.7	V
T_{ARM}[3]	Gate Re-arming Time for Slope Detection			85		ns
V_{TH_HGH}[3]	SR OFF Detection Threshold			0.5		V
Minimum On-Time and Minimum Off-Time						
K_{TON}[3]	Adaptive Minimum On-Time Ratio	Ratio between minimum on time and SR conduction of previous switching cycle		50		%
$t_{ON\_MIN.LL}$	Minimum On-Time Lower Limit		300	400	500	ns
$t_{ON\_MIN.UL}$[3]	Minimum On-Time Upper Limit			2		µs
t_{OFF_MIN}	Minimum Off-Time	Default Option for Medium Frequency	1.0	1.2	1.4	µs
Output Driver Section						
V_{OL}	Output Voltage Low	V_{IN} = 6 V			0.25	V
V_{OH}	Output Voltage High	V_{IN} = 6 V	5.0			V
t_R	Rise Time	V_{IN} = 6 V, C_L=3300 pF, GATE = 1 V~4 V			10	ns
t_F	Fall Time	V_{IN}=6 V, C_L = 3300 pF, GATE = 4 V~1 V			10	ns
Adaptive Dead-Time Control						
t_{DEAD}[3]	Dead-Time Self-Tuning Target	From GATE OFF to V_{DRAIN} rising above V_{TH_HGH}		290		ns

Note:

3. Not tested and guaranteed by design.

Functional Description

Theory of SR Control Operation

For an ideal circuit operation, the SR control algorithm of FAN6240 is very straightforward. FAN6240 controls the SR MOSFET based on the instantaneous drain-to-source voltage as illustrated in Figure 5. When the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold (V_{TH_ON}) which triggers the turn-on of the gate. Then the drain-to-source voltage is determined by the product of R_{DSON} and instantaneous SR current. When the drain-to-source voltage reaches the turn-off threshold (V_{TH_OFF}) as SR MOSFET current decreases to near zero, FAN6240 turns off the gate. If the turn off threshold (V_{TH_OFF}) is very close to zero, the turn off dead time can be minimized.

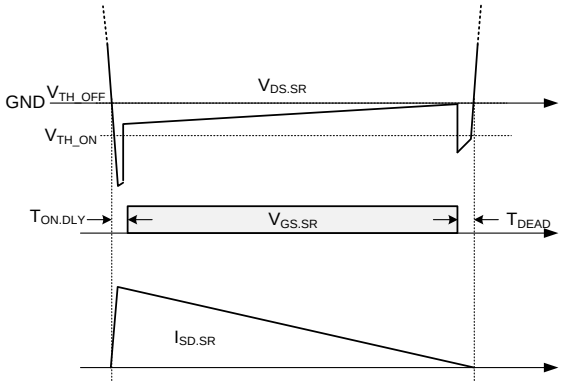


Figure 5. SR MOSFET Operation Waveforms (Ideal Case)

SR Turn-On Algorithm

As the diagram shown in Figure 6, the turn-on of SR GATE is triggered by the three input signals of AND gate. The first input signal is TURN_ON_ALLOW signal, which is given after t_{OFF_MIN} from the falling edge of $V_{GS.SR}$ signal. The second input is the TURN_ON_TRG signal, which is enabled after DRAIN pin voltage drops below V_{TH_ON}. The third signal is T_{ARM} which allows turn-on trigger only when SR drain voltage drops fast with a large slope, preventing SR from triggering by the drain resonance voltage in DCM operation.

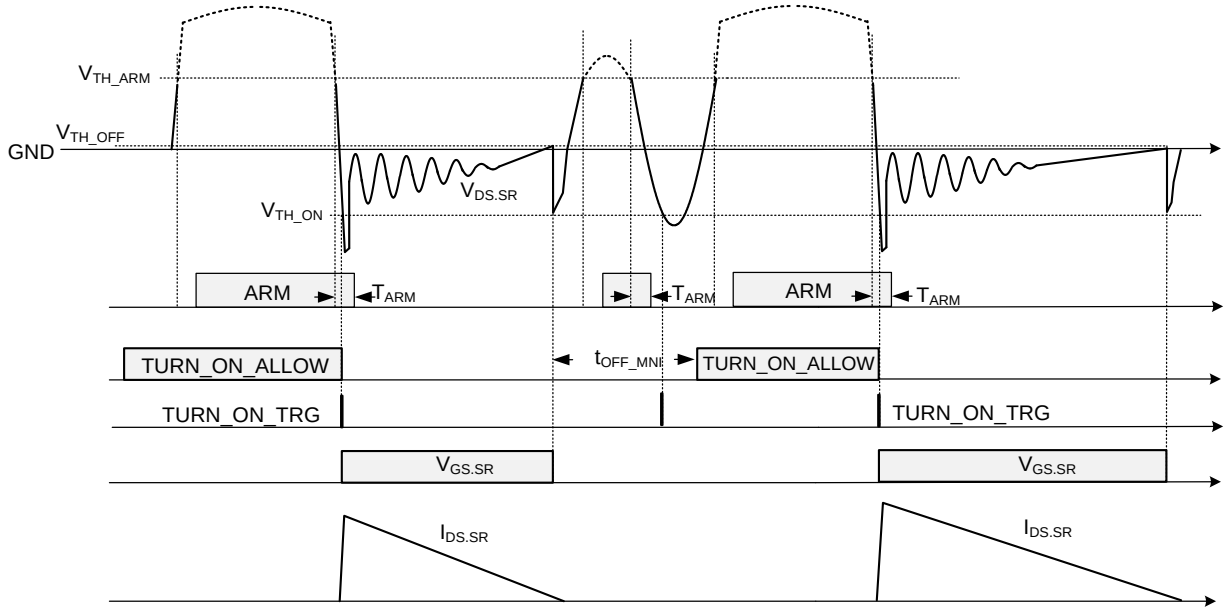


Figure 6. SR Turn-On Algorithm

SR Turn-Off Algorithm

As diagram shown in Figure 7, the turn-off of SR GATE is triggered by the two input signals of AND gate. The first input signal is turn off signal, which is enabled when $V_{DS.SR}$>V_{TH_OFF} .The second input is TURN_OFF_ALLOW signal given from the adaptive turn-off blanking. The blanking time is adaptively determined as half of SR conduction time (SR_COND) of the previous switching cycle for better noise immunity.

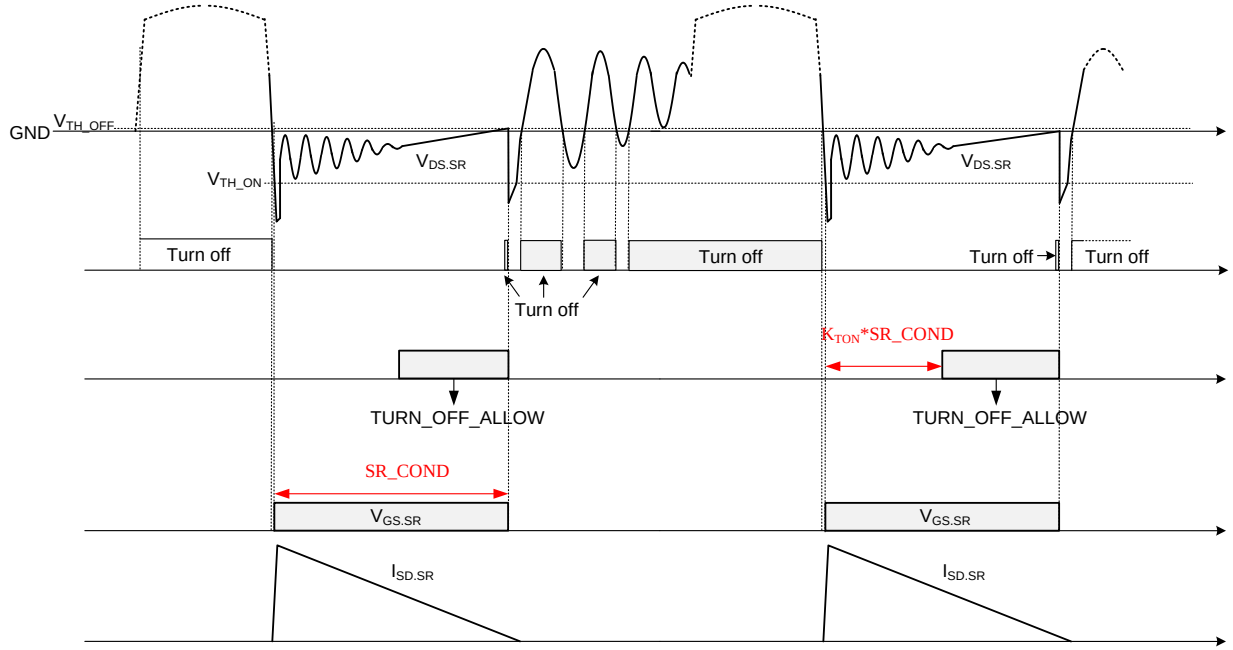


Figure 7. SR Turn-Off Algorithm

SR Skipping Mode Algorithm

As diagram shown in Figure 8, FAN6240 disables SR gate signal (SR skipping) at next cycle when previous cycle SR conduction time $V_{GS.SR}$ signal is smaller than the minimum ON time $t_{ON\_MIN.LL}$ in order reduce power consumption. This operation occurs only when the burst mode entry level of the primary side PWM controller is extremely low.

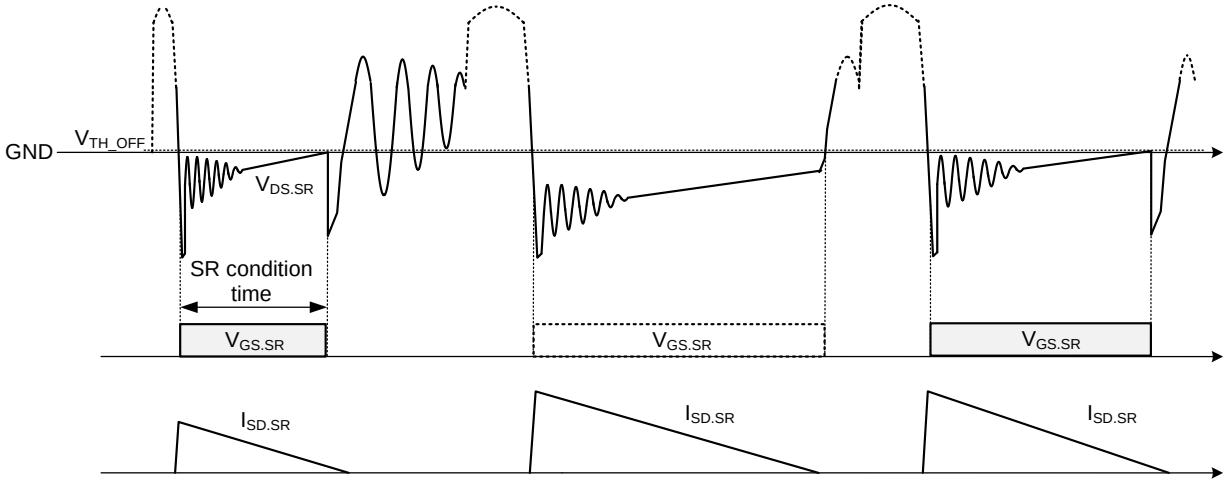
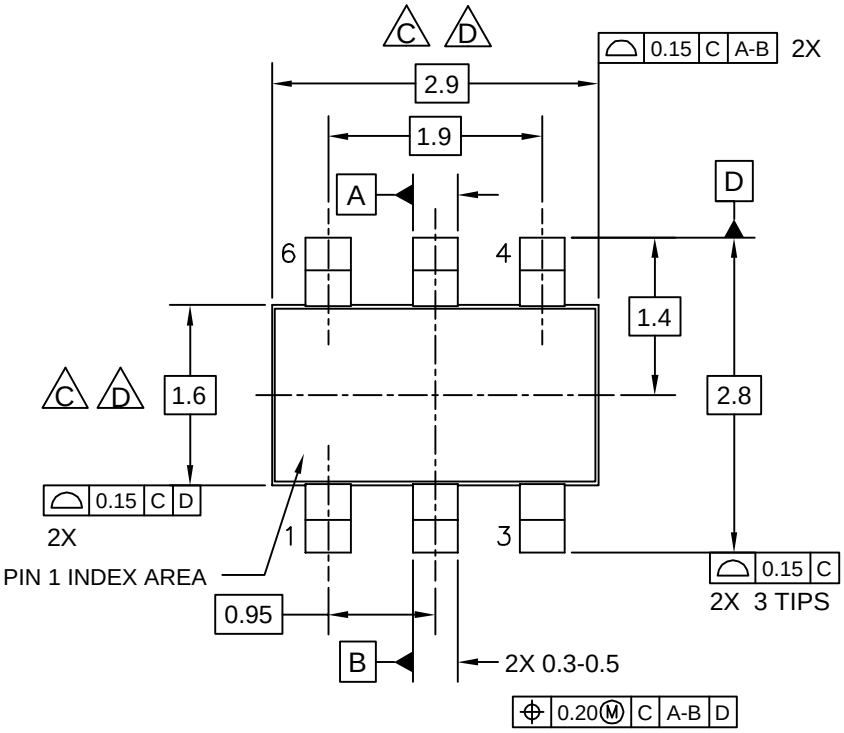
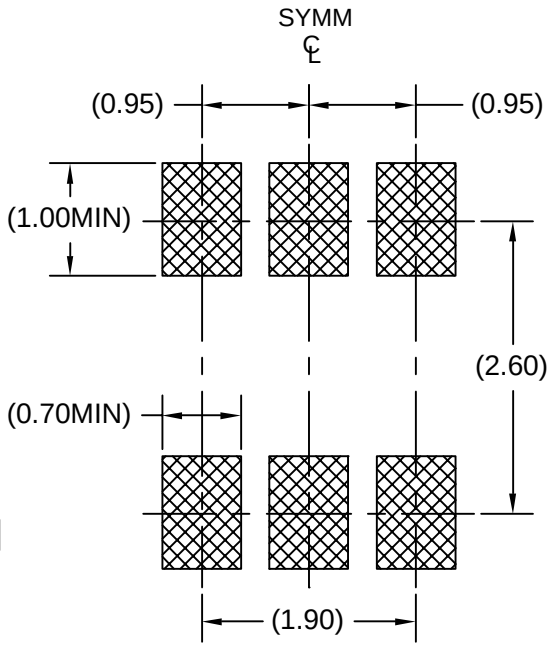


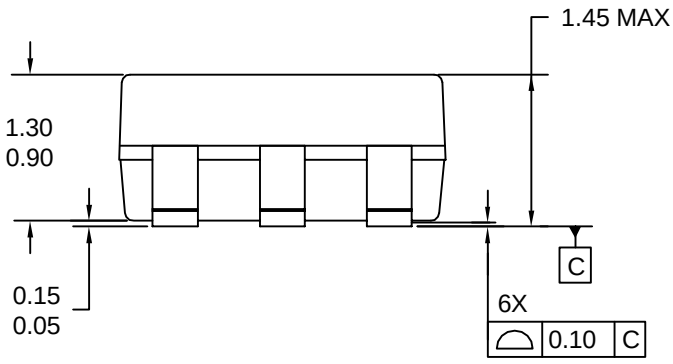
Figure 8. SR Skipping Diagram

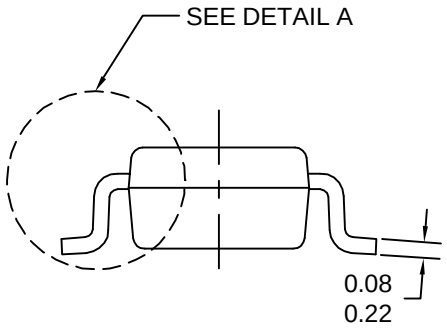
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	ECN-MKT-MA06E	11/4/2006	H.ALLEN
2	DWG UPDATED TO CONFORM TO MO178		5 JULY 07	L.HUEBENER

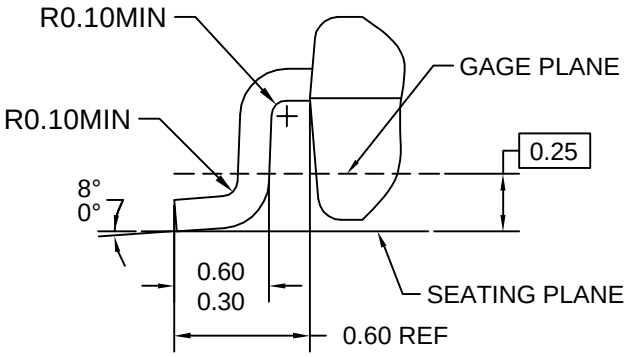




LAND PATTERN RECOMMENDATION







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