FAN53200

5 A, 2.4 MHz, Digitally Programmable TinyBuck® Regulator

ON Semiconductor®

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WLCSP−20
CASE 567SH

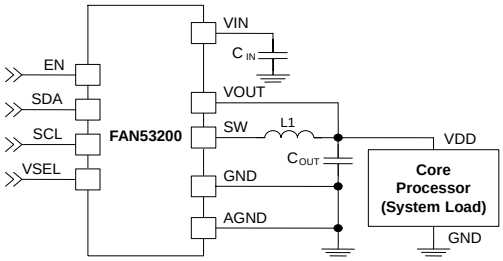


Figure 1. Typical Application

Descriptions

The FAN53200 is a step−down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5 V to 5.5 V. The output voltage is programmed through an I^2C interface capable of operating up to 3.4 Mbps.

Using a proprietary architecture with synchronous rectification, the FAN53200 is capable of delivering 5 A continuously at over 80% efficiency, while maintaining over 80% efficiency at load currents as low as 10 mA. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability. Inductance up to 1.2 μH may be used with additional output capacitance.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power−Save Mode with a typical quiescent current of 60 μA. At higher loads, the system automatically switches to fixed−frequency control, operating at 2.4 MHz. In Shutdown Mode, the supply current drops to 0.1 μA, reducing power consumption. PFM Mode can be disabled if constant frequency is desired. The FAN53200 is available in a 20−bump, 1.6 x 2.0 mm, WLCSP.

Features

- Quiescent Current in PFM Mode: 60 μA (Typical)
- Digitally Programmable Output Voltage:
  - 0.6 −1.3875 V in 12.5 mV Steps
- Best−in−Class Load Transient
- Continuous Output Current Capability: 5 A
- 2.5 V to 5.5 V Input Voltage Range
- Programmable Slew Rate for Voltage Transitions
- Fixed−Frequency Operation: 2.4 MHz
- I^2C−Compatible Interface Up to 3.4 Mbps
- Internal Soft−Start
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 20−Bump Wafer−Level Chip Scale Package (WLCSP)

Applications

- Graphic, and DSP Processors
  ARM™, Krait™, OMAP™, NovaThor™, ARMADA™
- Hard Disk Drives
- Tablets, Netbooks, Ultra−Mobile PCs
- Smart Phones
- Gaming Devices

ORDERING INFORMATION

Part Number	Power−Up Defaults		I^2C Slave Address	Device ID	Device Marketing	Package
	VSEL0	VSEL1				
FAN53200UC35X	OFF	1.15 V	C0	0000	B9	WLCSP−20
FAN53200UC44X	1.15V	0.85 V	C0	0000	CD	WLCSP−20

Pin Configuration

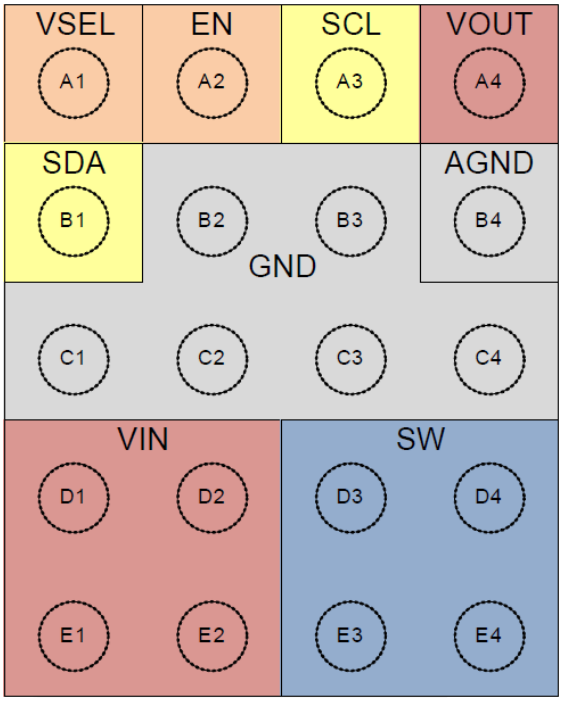


Figure 2. Pin Assignment (Top View)

Table 1. PIN DESCRIPTIONS

Pin #	Name	Description
A1	VSEL	Voltage Select. When this pin is LOW, V_{OUT} is set by the VSEL0 register. When this pin is HIGH, V_{OUT} is set by the VSEL1 register.
A2	EN	Enable. The device is in Shutdown Mode when this pin is LOW. All registers go to default values when EN pin is LOW.
A3	SCL	I^2C Serial Clock
A4	VOUT	VOUT. Sense pin for VOUT. Connect to C_{OUT}.
B1	SDA	I^2C Serial Data
B2, B3, C1 – C4	GND	Ground. Low−side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
B4	AGND	Analog Ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
D1, D2, E1, E2	VIN	Power Input Voltage. Connect to the input power source. Connect to C_{IN} with minimal path.
D3, D4, E3, E4	SW	Switching Node. Connect to the inductor.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	Voltage on SW, VIN Pins	IC Not Switching	−0.3	7.0	V
		IC Switching	−0.3	6.5	
	Voltage on All Other Pins	IC Not Switching	−0.3	V_{IN} (Note 1)	V
V_{OUT}	Voltage on VOUT Pin		−0.3	3.0	V
V_{INOV_SLEW}	Maximum Slew Rate of V_{IN} > 6.5 V, PWM Switching			100	V/ms
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114	2000		V
		Charged Device Model per JESD22−C101	1000		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 7.0 V or V_{IN} + 0.3 V

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current	0		5	A
L	Inductor		0.33		μH
C_{IN}	Input Capacitor		10		μF
C_{OUT}	Output Capacitor		44		μF
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. THERMAL PROPERTIES

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 2)		38		°C/W

2. See Thermal Considerations in the Application Information section.

Table 5. ELECTRICAL CHARACTERISTICS Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 5 V, and EN = HIGH.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES						
I_Q	Quiescent Current	I_{LOAD} = 0		60		μA
I_{SD}	H/W Shutdown Supply Current	EN = GND		0.1	5.0	μA
	S/W Shutdown Supply Current	EN = V_{IN}, BUCK_ENx = 0		41	75	μA
V_{UVLO}	Under−Voltage Lockout Threshold	V_{IN} Rising		2.35	2.45	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			350		mV
EN, VSEL, SDA, SCL						
V_{IH}	high−Level Input Voltage		1.1			V
V_{IL}	low−Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			160		mV
I_{IN}	Input Bias Current	Input Tied to GND or VIN		0.01	1.00	μA
PGOOD						
I_{OUTL}	PGOOD Pull−Down Current				1	mA
I_{OUTH}	PGOOD HIGH Leakage Current			0.01	1.00	μA
V_{OUT} REGULATION						
V_{REG}	V_{OUT} DC Accuracy	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = VSEL1 Default Value, 2.5 V ≤ V_{IN} ≤ 5.5 V	−1.5		1.5	%
		$I_{OUT(DC)}$ = 0 to 5 A, V_{OUT} = VSEL1, Default Value, Auto PFM/PWM, 2.5 V ≤ V_{IN} ≤ 4.5 V	−2.0		4.0	%
		$I_{OUT(DC)}$ = 0 to 5 A, V_{OUT} = VSEL1, Default Value, Auto PFM/PWM, 2.5 V ≤ V_{IN} ≤ 5.5 V	−3.0		5.0	%
POWER SWITCH AND PROTECTION						
I_{LIMPK}	P−MOS Peak Current Limit	Open Loop	6.3	7.4	8.5	A
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.15		V
		Falling Threshold	5.50	5.85		V
FREQUENCY CONTROL						
f_{SW}	Oscillator Frequency		2.05	2.40	2.75	MHz
R_{OFF}	VOUT Pull−Down Resistance	EN = 0 or V_{IN} < V_{UVLO}		160		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. SYSTEM CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
ΔV_{OUT_LOAD}	Load Regulation	I_{OUT} = 1 A to 5 A		0.2		mV/A
ΔV_{OUT_LINE}	Line Regulation	3.6 V ≤ V_{IN} ≤ 4.0 V, I_{OUT} = 3 A		−0.5		mV/V
V_{OUT_RIPPLE}	Ripple Voltage	I_{OUT} = 100 mA, PFM Mode		16		mV
		I_{OUT} = 2000 mA, PWM Mode		3		
η	Efficiency	V_{OUT} = 1.15 V, I_{OUT} = 100 mA		87		%
		V_{OUT} = 1.15 V, I_{OUT} = 500 mA		88		
		V_{OUT} = 1.15 V, I_{OUT} = 2 A		88		
T_{SS}	Soft−Start	EN High to 95% of V_{OUT} Target (1.15 V) R_{LOAD} = 50 Ω		340		μs
$\Delta V_{OUT\_LOAD\_TRAN}$	Load Transient	I_{OUT} = 0.1 A ⇔ 1.2 A, T_R = T_F = 100 ns		±20		mV
$\Delta V_{OUT\_LINE\_TRAN}$	Line Transient	V_{IN} = 3.0 V ⇔ 3.6 V, T_R = T_F = 10 μs, I_{OUT} = 500 mA		±20		mV

NOTE: The table above is verified by design and bench test while using the following external components: L = 0.33 μH, DFE252012F−R33M (TOKO), C_{IN} = 10 μF, C2012X5R1A106M (TDK), C_{OUT} = 2 x 22 μF, C2012X5R0J226M (TDK).
These parameters are not tested in production. Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, V_{EN} = 1.8 V, T_A = −40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, Auto PFM Mode.

Typical Characteristics

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, Auto PFM Mode, T_A = 25°C; circuit and components according to Figure 1.

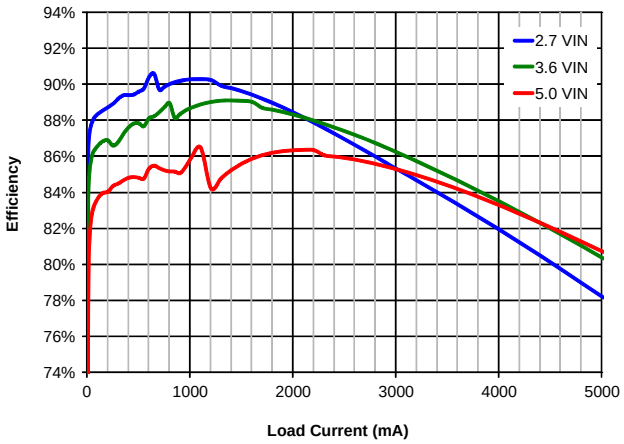


Figure 3. Efficiency vs. Load Current and Input Voltage

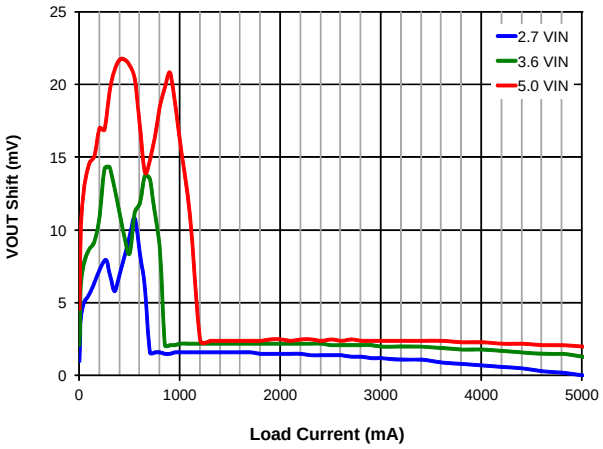


Figure 4. Output Regulation vs. Load Current and Input Voltage

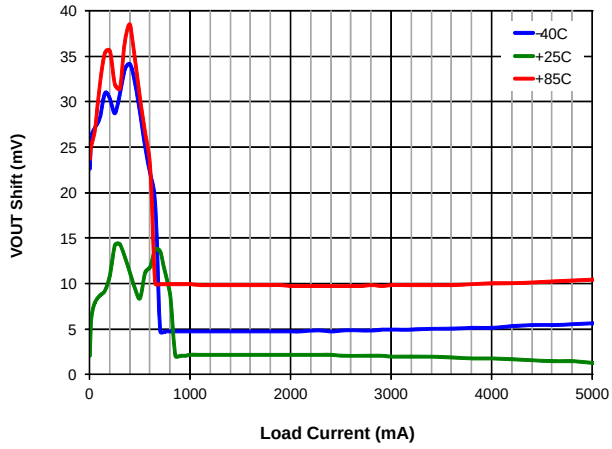


Figure 5. Output Regulation vs. Load Current, Over−Temperature

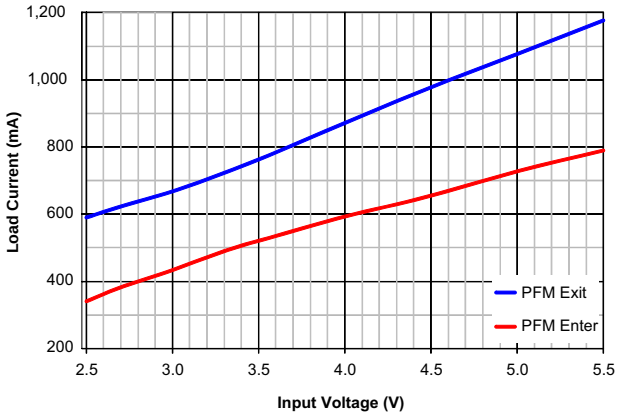


Figure 6. PFM Entry / Exit Level vs. Input Voltage

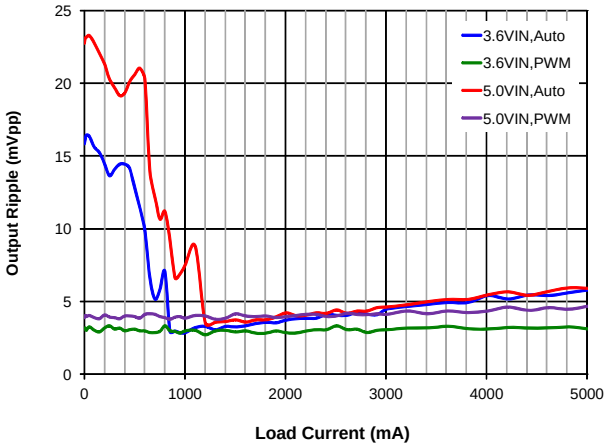


Figure 7. Output Ripple vs. Load Current

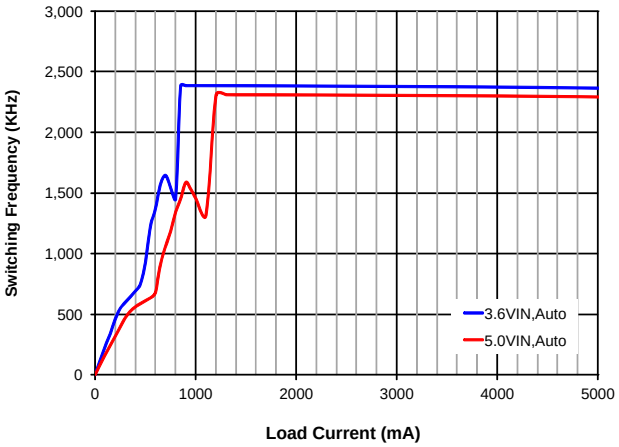


Figure 8. Frequency vs. Load Current

Typical Characteristics

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, Auto PFM Mode, T_A = 25°C; circuit and components according to Figure 1.

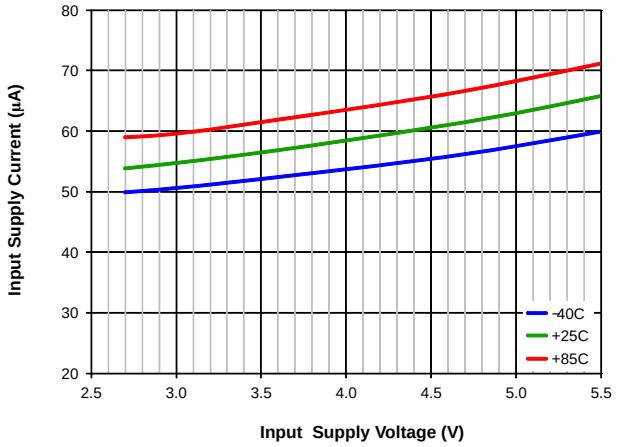


Figure 9. Quiescent Current vs. Input Voltage, Over−Temperature

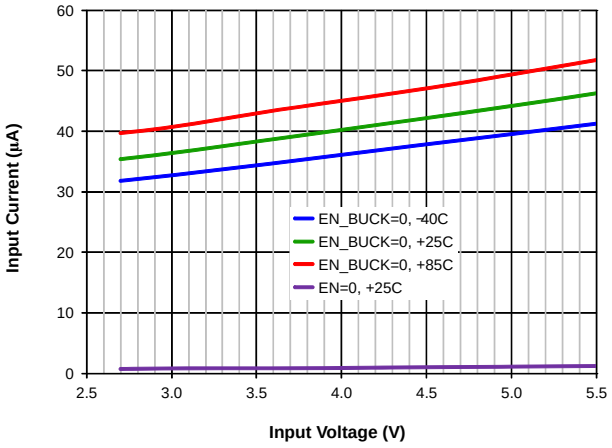


Figure 10. Shutdown Current vs. Input Voltage, Over−Temperature

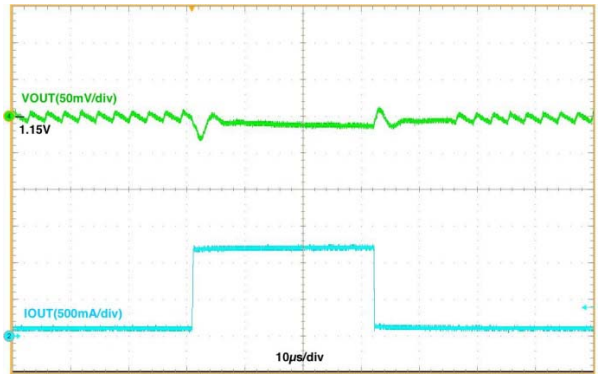


Figure 11. Load Transient, I_{OUT} = 0.1 A ⇔ 1.2 A, Auto PFM Mode, T_R = T_F = 100 ns

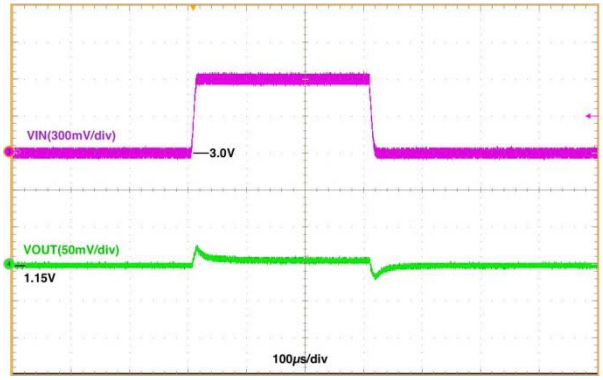


Figure 12. Line Transient, V_{IN} = 3.0 V ⇔ 3.6 V, T_R = T_F = 10 μs, I_{OUT} = 500 mA

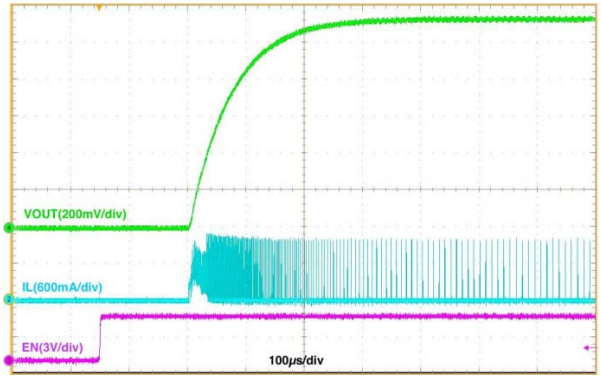


Figure 13. Startup, R_{load} = 50 Ω

Operation Description

The FAN53200 is a step−down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53200 is capable of delivering 5 A at over 80% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH for the output inductor and 44 μF for the output capacitor. High efficiency is maintained at light load with single−pulse PFM.

The FAN53200 integrates an I^2C−compatible interface, allowing transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically re−program the output voltage in 12.5 mV steps;
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable / disable the regulator.

Control Scheme

The FAN53200 uses a proprietary non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53200 operates in Discontinuous Conduction Mode (DCM) single−pulse PFM, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and Continuous Conduction Mode (CCM).

PFM can be disabled by programming the MODE bit HIGH in the VSEL registers.

Enable and Soft−Start

When the EN pin is LOW; the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I^2C cannot be written to or read from. All registers are reset to default values when EN pin is LOW.

When the OUTPUT_DISCHARGE bit in the CONTROL register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, a load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft−start cycle. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited during soft−start, allowing the IC to start into a pre−charged capacitive load.

If large output capacitance values are used, the regulator may fail to start. Maximum C_{OUT} capacitance for successfully starting with a heavy constant−current load is approximately:

$$C_{OUTMAX} \approx \left(I_{LIMPK} - I_{LOAD}\right) \cdot \frac{320\ \mu}{V_{OUT}} \qquad \text{(eq. 1)}$$

where C_{OUTMAX} is expressed in μF and I_{LOAD} is the load current during soft−start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters tri−state before reattempting soft−start 1700 μs later. This limits the duty cycle of full output current during soft−start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. Only BUCK_EN1 is initialized HIGH.

Table 7. HARDWARE AND SOFTWARE ENABLE

Pins		Bits		Output Voltage	
EN	VSEL	BUCK_EN0	BUCK_EN1	35X	44X
0	X	X	X	OFF	OFF
1	0	0	X	0 V	0 V
1	0	1	X	1.1 V	1.15 V
1	1	X	0	0 V	0 V
1	1	X	1	1.15 V	0.85 V

VSEL Pin and I^2C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output voltage is given as:

$$V_{OUT} = 0.60\ V + NSELx \cdot 12.5\ mV \qquad \text{(eq. 2)}$$

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages, shown in Table 11.

Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the CONTROL register (Table 12).

Table 8. TRANSITION SLEW RATE

Decimal	Bin	Slew Rate	
0	000	80	mV / μs
1	001	40	mV / μs
2	010	20	mV / μs
3	011	10	mV / μs
4	100	5	mV / μs
5	101	2.5	mV / μs
6	110	1.25	mV / μs
7	111	0.625	mV / μs

Transitions from high to low voltage rely on the output load to discharge V_{OUT} to the new set point. Once the high−to−low transition begins, the IC stops switching until V_{OUT} has reached the new set point.

Under−Voltage Lockout (UVLO)

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage raises high enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over−Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (about 6.2 V) the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. Sixteen consecutive current limit cycles in current limit cause the regulator to shut down and stay off for about 1700 μs before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresis.

I²C Interface

The FAN53200's serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C−Bus® specifications. The FAN53200's SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is C0.

Table 9. I²C SLAVE ADDRESS

Hex	Bits							
	7	6	5	4	3	2	1	0
C0	1	1	0	0	0	0	0	R/$\overline{W}$

Other slave addresses can be assigned. Contact an ON Semiconductor representative.

Bus Timing

As shown in Figure 14, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

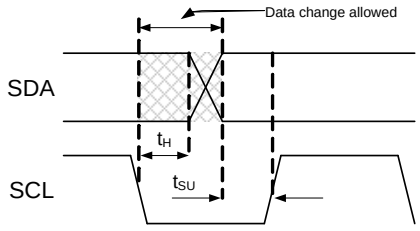


Figure 14. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL high, as shown in Figure 15.

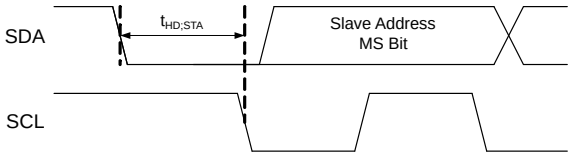


Figure 15. START Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 16.

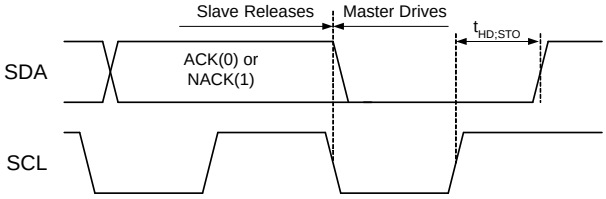


Figure 16. STOP Bit

During a read from the FAN53200, the master issues a REPEATED START after sending the register address, and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 17.

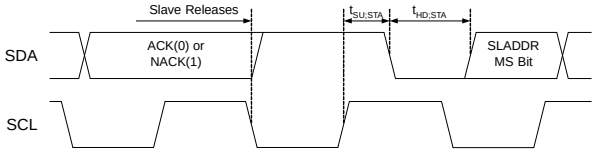


Figure 17. REPEATED START Timing

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical, except the bus speed for HS mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 16) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 17).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as

Master Drives Bus

and

Slave Drives Bus

All addresses and data are MSB first.

Table 10. I²C BIT DEFINITIONS for Figure 18 & Figure 19

Symbol	Definition
S	START, see Figure 15
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 17
P	STOP, see Figure 16

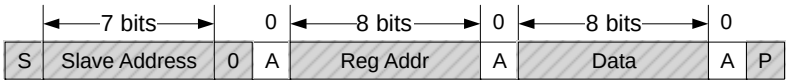


Figure 18. Write Transaction

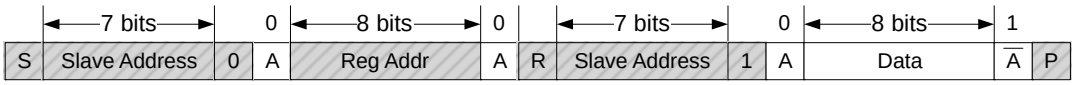


Figure 19. Read Transaction

Register Description

Table 11. REGISTER MAP

Hex Address	Name	Function
00	VSEL0	Controls V_{OUT} settings when VSEL pin = 0
01	VSEL1	Controls V_{OUT} settings when VSEL pin = 1
02	CONTROL	Determines whether V_{OUT} output discharge is enabled and also the slew rate of positive transitions
03	ID1	Read−only register identifies vendor and chip type
04	ID2	Read−only register identifies die revision
05	MONITOR	Indicates device status

The following table defines the operation of each register bit.

Table 12. BIT DEFINITIONS

Bit	Name	35X	44X	Description
VSEL0		**R/W**		**Register Address: 00**
7	BUCK_EN0	0	1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6	MODE0	0	0	0: Allow Auto PFM Mode during light load. 1: Forced PWM Mode.
5:0	NSEL0	101000	101100	Sets V_{OUT} value from 0.6V to 1.3875 V in 12.5 mV steps (see Equation 2).
VSEL1		**R/W**		**Register Address: 01**
7	BUCK_EN1	1	1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6	MODE1	0	0	0: Allow Auto PFM Mode during light load. 1: Forced PWM Mode.
5:0	NSEL1	101100	010100	Sets V_{OUT} value from 0.6V to 1.3875 V in 12.5 mV steps (see Equation 2).
CONTROL		**R/W**		**Register Address: 02**
7	OUTPUT_DISCHARGE	**1**	**0**	0: When the regulator is turned off, V_{OUT} is not discharged. 1: When the regulator is turned off, V_{OUT} discharges through an internal pull−down.
6:4	SLEW	000	000	Sets the slew rate for positive voltage transitions (see Table 8).
3	Reserved	0	0	Always reads back 0
2	RESET Reserved	0	0	1: Reset all registers to default values. 0: Always reads back 0
1:0	Reserved	00	00	Always reads back 00
ID1		**R**		**Register Address: 03**
7:5	VENDOR	100		Signifies ON Semiconductor as the IC vendor
4	Reserved	0		Always reads back 0
3:0	DIE_ID	0000		Refer to ordering information
ID2		**R**		**Register Address: 04**
7:4	Reserved	0000		Always reads back 0000
3:0	DIE_REV	0001		IC mask revision
MONITOR		**R**		**Register Address: 05**
7	PGOOD	1		1: buck is enabled and soft−start is completed
6:0	Not used	0000000		Always reads back 000 0000

Application Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \right) \qquad \text{(eq. 3)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \qquad \text{(eq. 4)}$$

The FAN53200 is optimized for operation with L = 330 nH, but is stable with inductances up to 1.0 μH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin−effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{2} + \frac{\Delta I^2}{12}} \qquad \text{(eq. 5)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 13. EFFECTS OF INDUCTOR VALUE (from 330 nH Recommended) on Regulator Performance

$I_{MAX(LOAD)}$	ΔV_{OUT} (Equation 7)	Transient Response
Increase	Decrease	Degraded

Inductor Current Rating

The current limit circuit can allow substantial peak currents to flow through L1 under worst−case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space−constrained applications, a lower current rating for L1 can be used. The FAN53200 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor and V_{OUT} Ripple

Table 14 suggests 0805 capacitors, but 0603 capacitors may be used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in−circuit capacitance than the 0805 package, which can degrade transient response and output ripple.

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \qquad \text{(eq. 6)}$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}. Equation 6 is only valid for Continuous Current Mode (CCM) operation, which occurs when the regulator is in PWM Mode.

For large C_{OUT} values, the regulator may fail to start under a load. If an inductor value greater than 1.0 μH is used, at least 30 μF of C_{OUT} should be used to ensure stability.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square−wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square−wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \cdot \frac{ESL_{COUT}}{L1} \qquad \text{(eq. 7)}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT} = 20 μF, a single 22 μF 0805 would produce twice the square wave ripple as two x 10 μF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 or 0612 capacitors with ultra−low ESL. Placing additional small−value capacitors near the load also reduces the high−frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under−damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction−to−ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53200UC, θ_{JA} is 38°C/W when mounted on its four−layer evaluation board in still air with two−ounce outer layer copper weight and one−ounce inner layers. Halving the copper thickness results in an increased θ_{JA} of 48°C/W.

For long−term reliable operation, the IC's junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature ($\leq$125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \times I_{LOAD} \times \left(\frac{1}{\eta} - 1\right) \quad \text{(eq. 8)}$$

where η is efficiency.

Estimate inductor copper losses using:

$$P_L = I_{LOAD}{}^2 \times DCR_L \quad \text{(eq. 9)}$$

3. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \quad \text{(eq. 10)}$$

4. Determine device operating temperature:

$$\Delta T = P_{IC} \times \Theta_{JA} \quad \text{(eq. 11)}$$

and

$$T_{IC} = T_A + \Delta T$$

It is important to note that the $R_{DS(ON)}$ of the IC's power MOSFETs increases linearly with temperature at about 0.21%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

Recommended External Components

Table 14. RECOMMENDED CAPACITORS

Component	Quantity	Vendor	Vendor	C (μF)	Size	Rated
C_{OUT}	2 Pieces	C2012X5R0J226M	TDK	22	0805	6.3 V
C_{IN}	1 Piece	C2012X5R1A106M	TDK	10	0805	10 V

Table 15. RECOMMENDED INDUCTORS

Manufacturer	Part#	L (nH)	DCR (mΩ)	I_{SAT}	L	W	H
TOKO	DFE201612E−R47M	470	20	6.1	2.0	1.6	1.2
TOKO	DFE252012F−R33M	330	14	8.5	2.5	2.0	1.2

Layout Recommendation

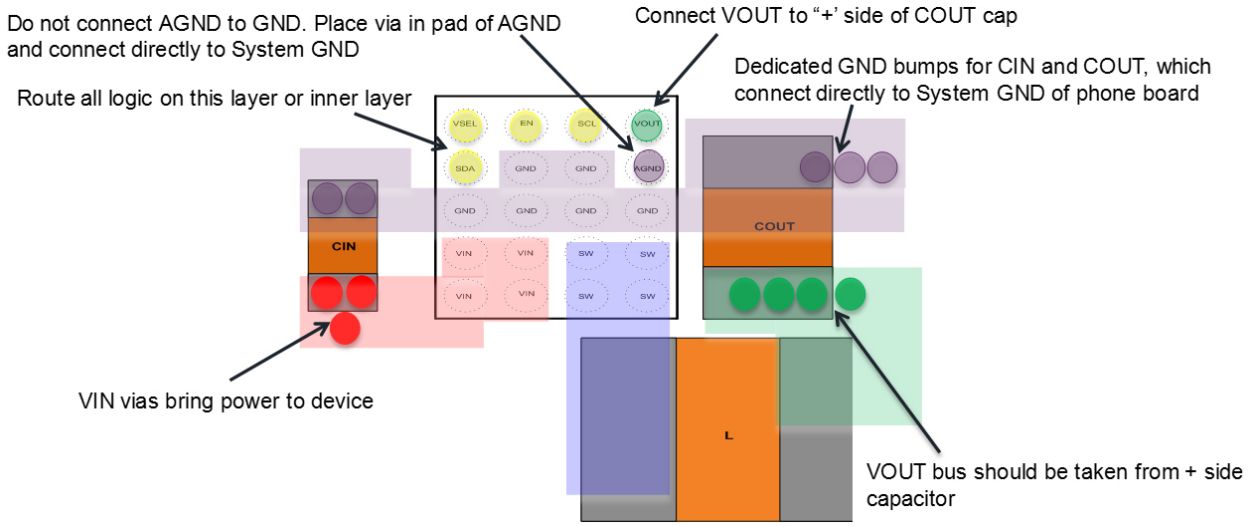


Figure 20. Guidance for Layer 1

Figure 21. Guidance for Layer 2

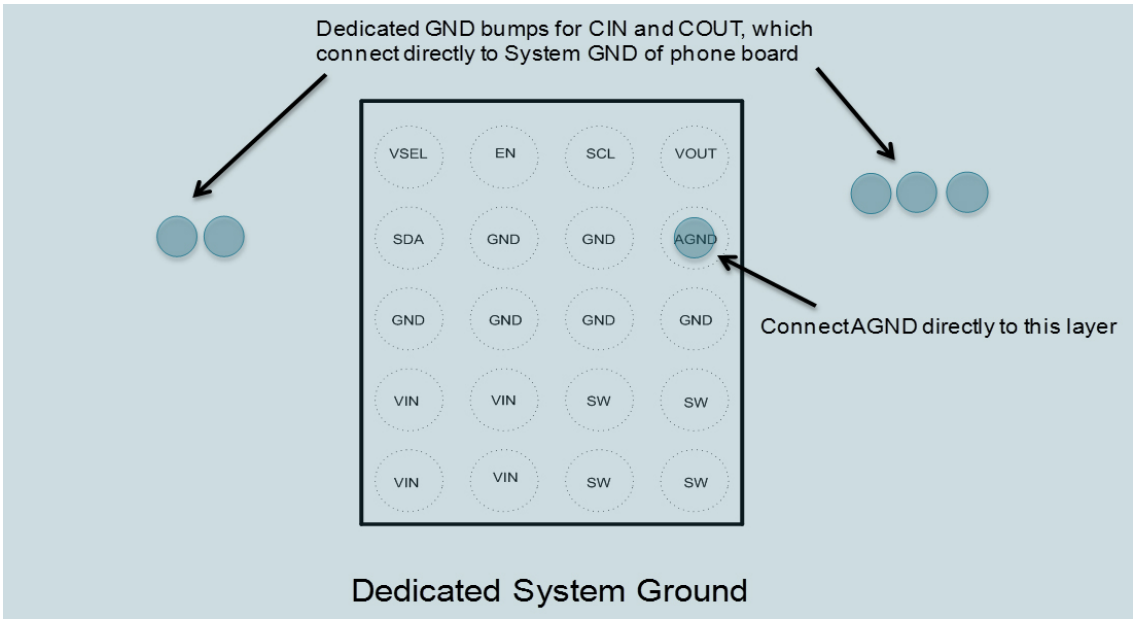
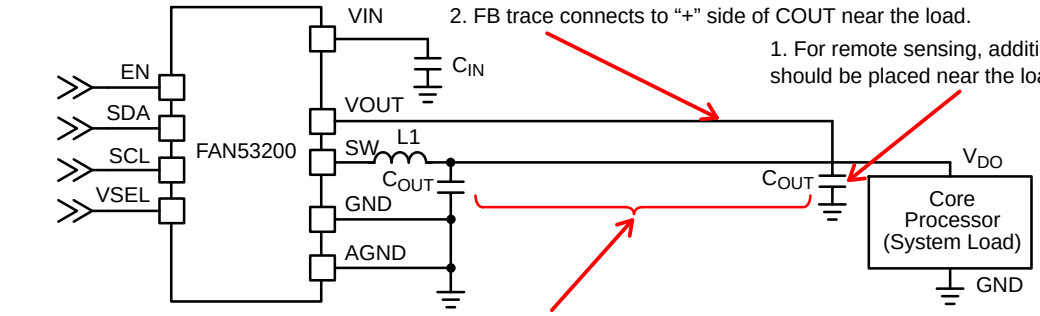


Figure 22. Guidance for Layer 3



3. The trace resistance between FAN53200 and CPU should not exceed 30 mΩ.

This table provides resistance values for given Copper Oz

Width (mils)	Length (mils)	Copper (Oz)	Resistance (mΩ)
25	500	2	4.9
25	500	1.5	6.5
25	500	1	9.7
25	500	0.5	19.4

Figure 23. Remote Sensing Schematic

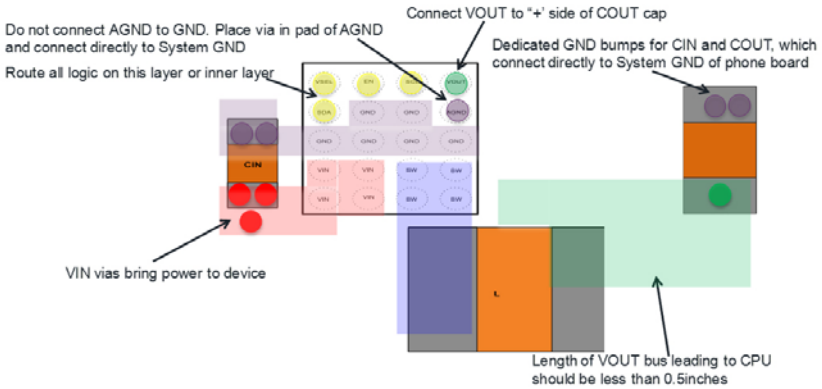
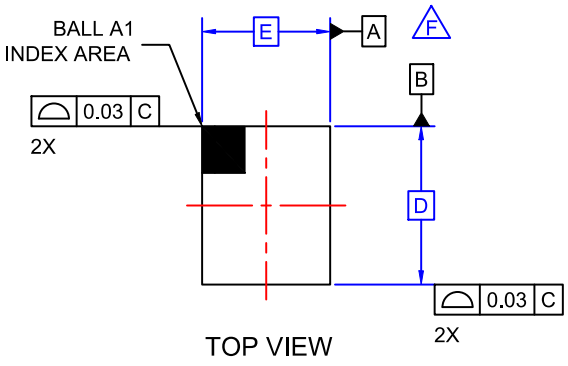


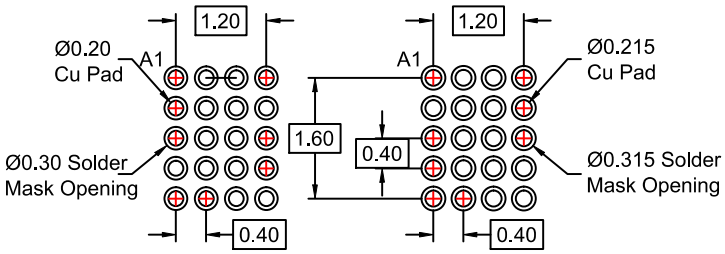
Figure 24. Remote Sensing Guidance, Top Layer

PACKAGE DIMENSIONS

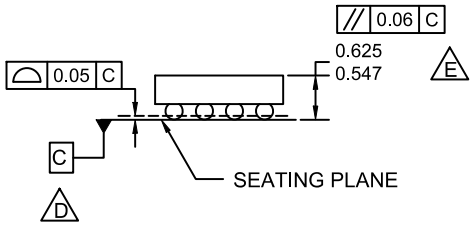
WLCSP20 2.015x1.615x0.586
CASE 567SH
ISSUE O

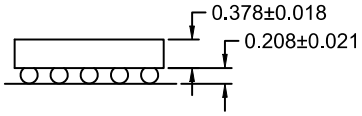


TOP VIEW

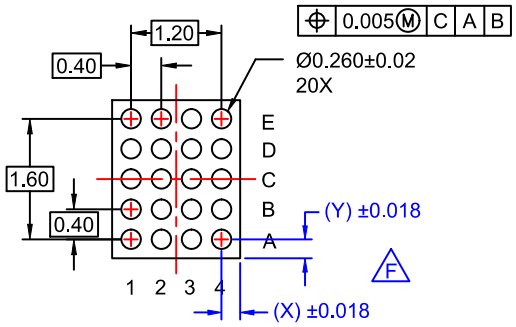


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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