ESD5B5.0S, SZESD5B5.0S

Transient Voltage Suppressor

Micro−Packaged Diode for ESD Protection

The ESD5B Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size and bi−directional design, it is ideal for use in cellular phones, MP3 players, and portable applications that require audio line protection.

Specification Features

- Low Capacitance 32 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: nom 0.063″ x 0.032″ (1.6x0.8 mm)
- Low Body Height: nom 0.024″ (0.6 mm)
- Reverse Working (Stand−off) Voltage: 5.0 V
- Peak Power up to 50 W @ 8 x 20 μs Pulse
- Low Leakage
- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000−4−2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free Device

Mechanical Characteristics

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V−0
LEAD FINISH: 100% Matte Sn (Tin)
MOUNTING POSITION: Any
QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±30 ±30	kV
ESD Voltage	Per Human Body Model Per Machine Model		16 400	kV V
Peak Power (Figure 1) Per 8 x 20 μs Waveform Peak Power (Figure 2)Per 10 x 1000 μs Waveform		P_{PK}	50 10	W
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C		P_D	200	mW
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.

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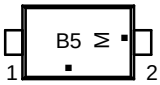
SOD−523
CASE 502

MARKING DIAGRAM



B5 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
ESD5B5.0ST1G	SOD−523 (Pb−Free)	3000 / Tape & Reel
ESD5B5.0ST5G	SOD−523 (Pb−Free)	8000 / Tape & Reel
SZESD5B5.0ST1G	SOD−523 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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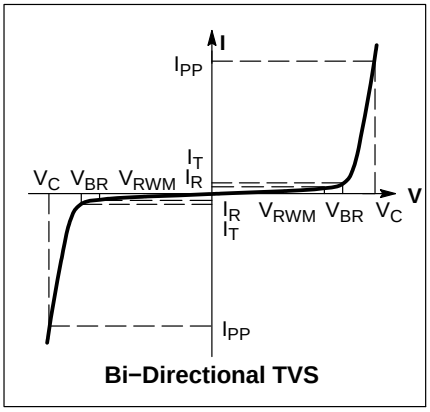
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 0.9 V Max. @ I_F = 10 mA for all types)

Device*	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)		I_T	C (pF) @ V_R = 0 V, f = 1 MHz	V_C
	Max	Max	Min	Max	mA	Typ	Per IEC61000−4−2 (Note 3)
ESD5B5.0ST1G/T5G, SZESD5B5.0ST1G	5.0	1.0	5.8	7.8	1.0	32	Figures 1 and 2 See Below

*Other voltages available upon request.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

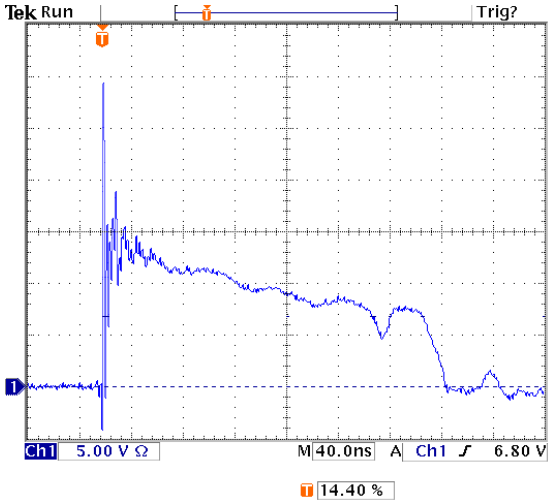


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC 61000−4−2

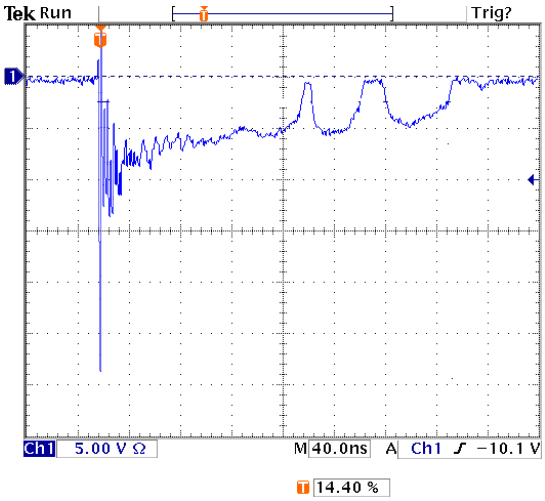


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC 61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

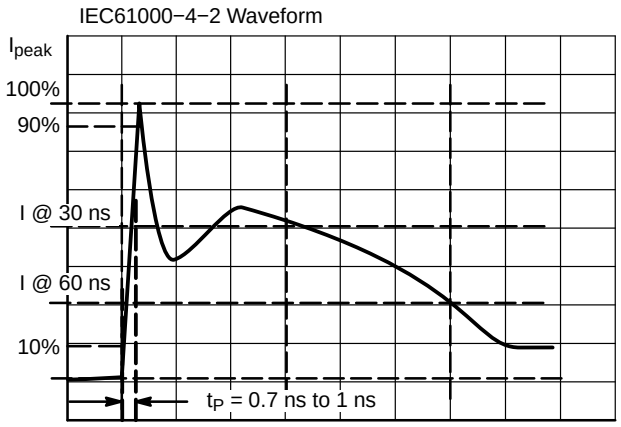


Figure 3. IEC61000−4−2 Spec

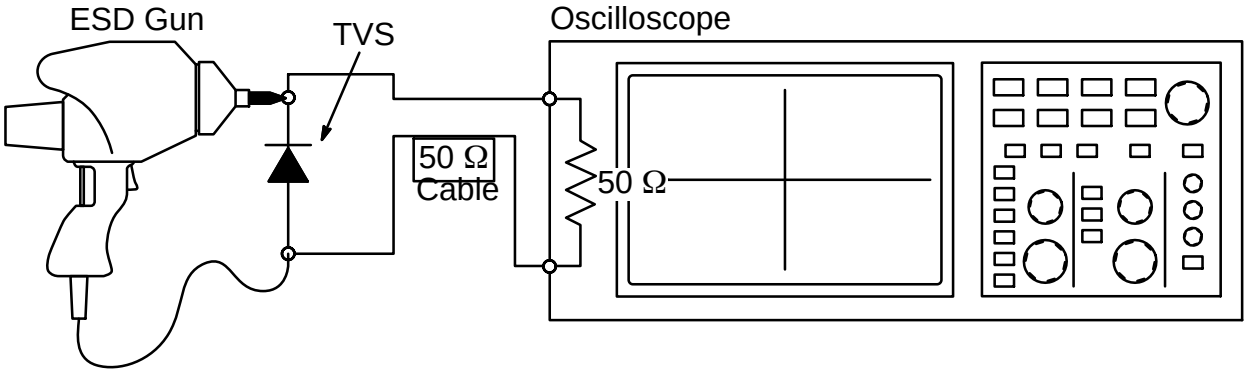


Figure 4. Diagram of ESD Test Setup

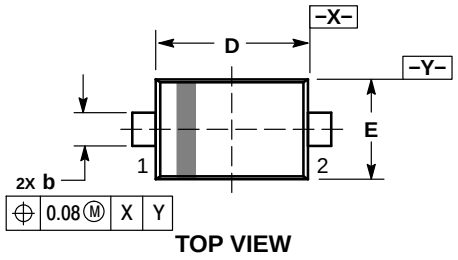
The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

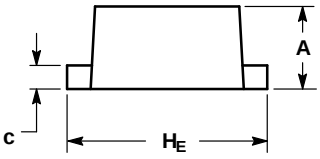
For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

PACKAGE DIMENSIONS

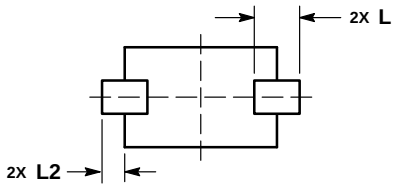
SOD−523
CASE 502
ISSUE E



TOP VIEW



SIDE VIEW

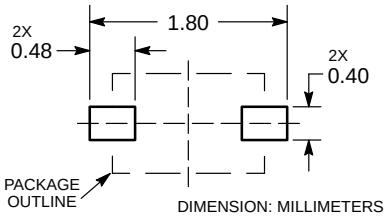


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.07	0.14	0.20
D	1.10	1.20	1.30
E	0.70	0.80	0.90
H_E	1.50	1.60	1.70
L	0.30 REF		
L2	0.15	0.20	0.25

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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