EPM5016 to EPM5192 EPLDs

High-Speed, High-Density MAX 5000 Devices

September 1991, ver. 2

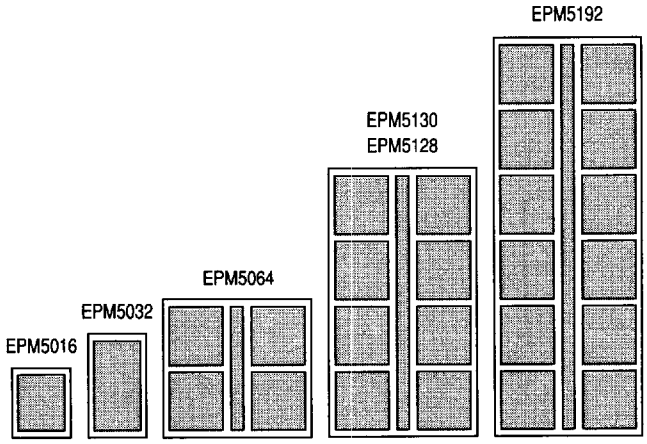
Data Sheet

Features

- Complete family of CMOS EPLDs solves design tasks ranging from fast 20-pin address decoders to 100-pin LSI custom peripherals.
- The advanced MAX 5000 architecture combines the speed, ease of use, and familiarity of PAL devices with the density of programmable gate arrays.
- MAX 5000 EPLDs provide 15-ns combinatorial delays, counter frequencies up to 100 MHz, pipelined data rates of 100 MHz, and high-complexity designs with true system clock rates up to 66 MHz.
- Available in a wide variety of packages, including DIP, SOIC, J-lead, PGA, and QFP formats in windowed ceramic and plastic one-time-programmable versions.
- MAX+PLUS and MAX+PLUS II PC- and workstation-based development tools compile large designs in minutes.
- An industry-standard EDIF interface to workstation and third-party CAE tools is available.

Figure 1 shows the MAX 5000 modular architecture.

Figure 1. MAX 5000 Modular Architecture



	EPM5016	EPM5032	EPM5064	EPM5130 / EPM5128	EPM5192
Macrocells	16	32	64	128	192
Maximum Flip-Flops	21	42	84	168	252
Maximum Latches	32	64	128	256	384
Pins	20	28	44	100/84/68	100/84

Family Highlights

- **Multiple Array MatriX (MAX) 5000 architecture solves speed, density, and design flexibility problems**
  - Advanced macrocell array provides registered, combinatorial, or flow-through latch operation.
  - Expander product-term array automatically provides additional combinatorial or registered logic.
  - Decoupled I/O block with dual feedback on I/O pins allows flexible pin utilization.
  - Programmable Interconnect Array (PIA) provides automatic 100% routing in devices with multiple LABs.
  - Each macrocell supports combinatorial and registered operation, using single or multiple clocks within a single EPLD.
- **MAX 5000 Performance**
  - Pipelined data rates up to 100 MHz
  - Counters as fast as 100 MHz
  - t_{PD} performance from 15 ns to 25 ns
  - Advanced 0.8-micron CMOS EPROM technology
- **MAX 5000 Logic Density**
  - 16- to 192-macrocell devices
  - 20- to 100-pin packages
  - 32 to 384 flip-flops and latches
  - More than 32 product terms on a single macrocell
  - Product-term expansion on any data or control path
- **MAX+PLUS & MAX+PLUS II Design Tools**
  - Design entry via unified, hierarchical schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry (waveform entry in MAX+PLUS II only)
  - Fast, automatic design processing with logic synthesis
  - Automatic design partitioning into multiple EPLDs (MAX+PLUS II only)
  - Automatic device fitting, no hand-editing needed
  - Hardware and software design verification tools
- **EDIF interface to MAX+PLUS & MAX+PLUS II provides paths to Viewlogic Systems, Valid Logic Systems, Mentor Graphics, and other workstation-based CAE tools.**

General Description

MAX 5000 Erasable Programmable Logic Devices (EPLDs) represent a revolutionary step in programmable logic: they combine innovative architecture and state-of-the-art process to offer optimum performance, logic density, flexibility, and the highest speeds and densities available in general-purpose reprogrammable logic. These EPLDs are high-speed, high-density replacements for SSI and MSI TTL and CMOS packages and conventional PLDs. For example, an EPM5192 replaces over 100 7400-series SSI and MSI TTL and CMOS packages, integrating complete subsystems into a single package, saving board area, and reducing power consumption.

The MAX 5000 EPLDs range in density from 16 to 192 macrocells. They are divided into two groups: higher-speed EPLDs (EPM5016 and EPM5032) and higher-density EPLDs (EPM5064, EPM5128, EPM5130, and EPM5192). The higher-speed devices achieve system clock frequencies of 66 MHz, and are capable of counter frequencies of 100 MHz.

Logic Array Blocks The EPM5016 and EPM5032 EPLDs have a single Logic Array Block (LAB). The EPM5064, EPM5128, EPM5130, and EPM5192 EPLDs contain multiple LABs. Each LAB contains a macrocell array, an expander product-term array, and a decoupled I/O block. Expander product terms (expanders) are unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. Thus, expressions requiring up to 66 product terms can be implemented in a single macrocell. Signals in the higher-density devices are routed between multiple LABs by a Programmable Interconnect Array (PIA) that ensures 100% routability. This multiple array architecture enables MAX 5000 EPLDs to offer the speed of smaller arrays with the integration density of larger arrays.

Modular Architecture The modular architecture of MAX 5000 EPLDs provides integration solutions over a wide range of logic densities. Migration from one type of device to another is easy. For example, the EPM5128 and EPM5130 EPLDs have the same logic capacity, but have packages optimized to handle different I/O requirements. Over the entire family, a wide range of packaging options for both through-hole and surface-mount applications is available. Plastic one-time-programmable (OTP) packages are available for economical volume production.

Logic Design Entry Logic designs are created and programmed into MAX 5000 EPLDs with the MAX+PLUS and MAX+PLUS II development systems. These complete CAE systems offer hierarchical design entry tools, automatic design compilation and fitting, timing simulation, and device programming. The MAX+PLUS and MAX+PLUS II Compilers feature advanced logic synthesis algorithms, allowing designs to be entered in a variety of high-level formats while ensuring the most efficient use of EPLD resources. The combination of a flexible architecture and advanced CAE tools ensures rapid design cycles so that a design may go from conception to completion in single day. Interfaces to third-party tools are also available to allow design entry and logic simulation on a variety of workstation platforms.

Functional Description

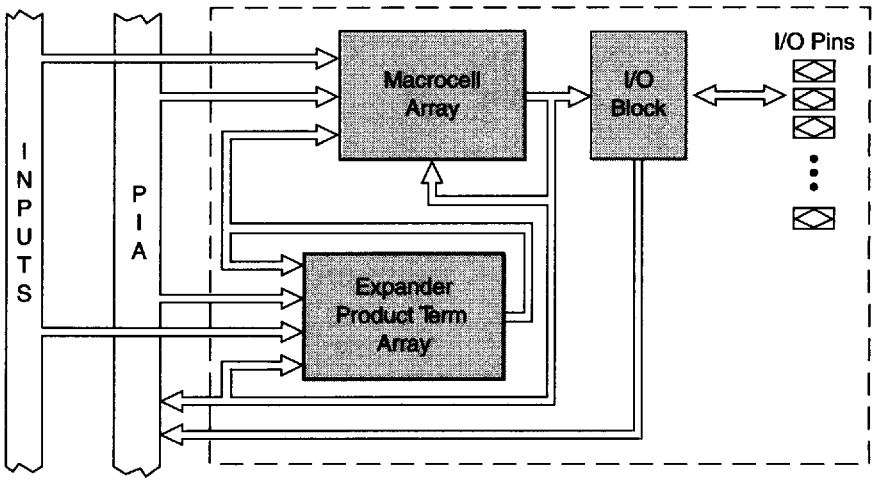
MAX 5000 EPLDs use CMOS EPROM cells to configure logic functions within the devices. The device architecture is user-configurable to accommodate a variety of independent logic functions, and the EPLDs can be erased for quick and efficient iterations during design development and debug cycles.

Logic Array Block

MAX 5000 EPLDs contain from 1 to 12 Logic Array Blocks (LABs). Each LAB, shown in Figure 2, consists of a macrocell array, an expander product-term array, and an I/O control block. (The number of macrocells and expanders in the arrays varies with each device.) Macrocells are the primary resource for logic implementation, but if needed, expanders can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms. Flexible macrocells and allocable expanders facilitate variable product-term designs without the waste associated with fixed product-term architectures. Thus, PAL or PLA devices are easily integrated into MAX 5000 EPLDs. The outputs of the macrocells feed the decoupled I/O block, which consists of a group of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192 EPLDs, multiple LABs are connected by a Programmable Interconnect Array (PIA).

Figure 2. Logic Array Block

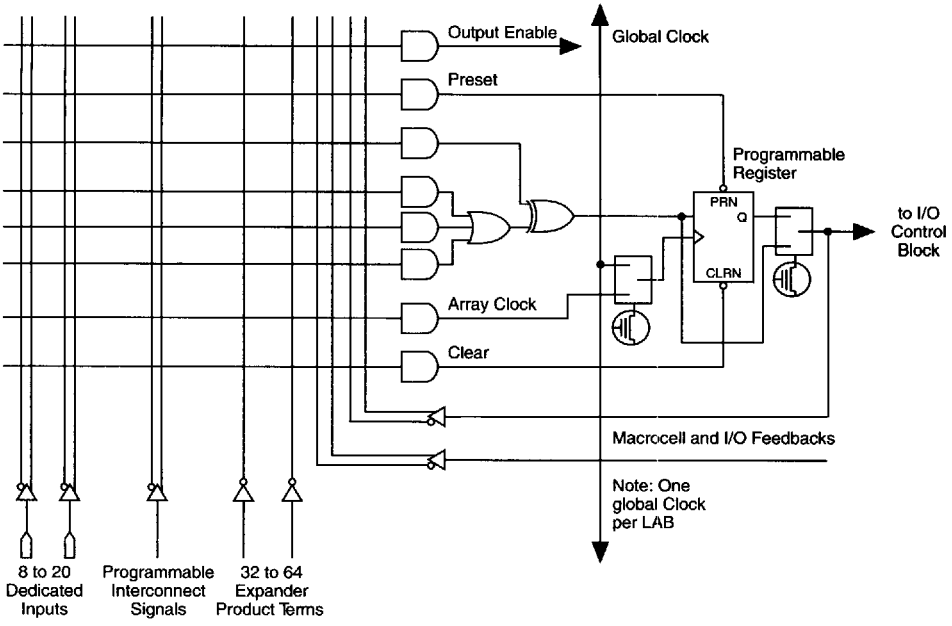
The LAB consists of a macrocell array, an expander product-term array, and a decoupled I/O block. The flexibility of the LAB ensures high speeds and efficient device utilization.



Macrocells

The MAX 5000 macrocell, shown in Figure 3, consists of a programmable logic array and an independently configurable register. This register may be programmed for D, T, JK, or SR operation, as a flow-through latch, or bypassed for purely combinatorial operation. Combinatorial logic is implemented in the programmable logic array, which consists of three product terms ORed together that feed one input of an XOR gate. The second input to the XOR gate is also controlled by a product term that makes it possible to implement active-high or active-low logic. The XOR gate is also used for complex XOR arithmetic logic functions and for De Morgan's inversion to reduce the number of product terms. The output of the XOR gate feeds the programmable register, or bypasses it for purely combinatorial operation. The logic array ensures high speed while

Figure 3. MAX 5000 Macrocell



eliminating inefficient, unused product terms. Also, expanders can be allocated to enhance the capability of the logic array.

Additional product terms, called secondary product terms, are used for Output Enable, Preset, Clear, and Clock logic. Preset and Clear product terms drive the active-low asynchronous Preset and asynchronous Clear inputs to the configurable flip-flop. The Clock product term allows each register to have an independent Clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin may use the Output Enable product term to control the active-high tri-state buffer in the I/O control block. These secondary product terms allow 7400-series TTL functions to be emulated exactly.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device. All macrocell outputs are globally routed within a LAB and also feed the PIA to provide efficient routing of signal-intensive designs.

Clock Options

Each LAB has two clocking modes: array (asynchronous) and global (synchronous). During array clocking, each flip-flop is clocked by a product term. Thus, any input or internal logic may be used as a clock. Systems that require multiple clocks are easily integrated into MAX 5000 EPLDs. Array

clocking also allows each flip-flop to be configured for positive- or negative-edge-triggered operation, giving the macrocell a high degree of flexibility.

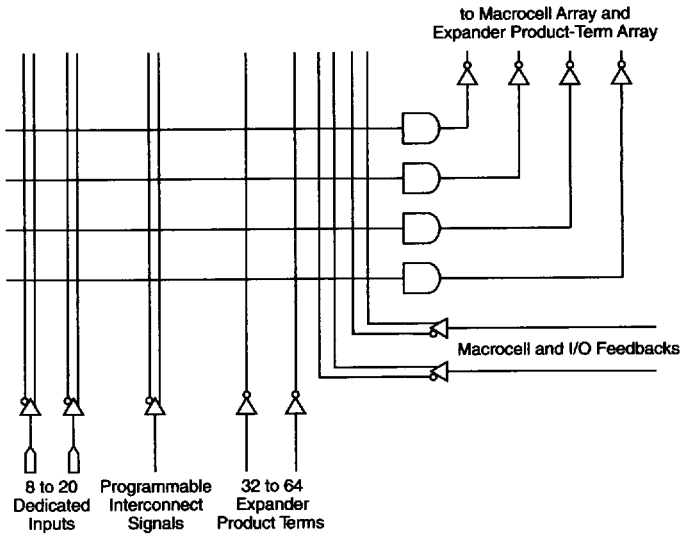
Global clocking is provided by a dedicated Clock signal (CLK). This direct connection provides enhanced clock-to-output delay times. Since each LAB has one global clock, all flip-flop clocks within it are positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global clock, it may be used as a dedicated input.

Expander Product Terms

The expander product-term array (Figure 4) contains unallocated, inverted product terms that enhance the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs for MAX 5000 EPLDs.

Figure 4. Expander Product Terms

Expander product terms are unallocated logic that can be used and shared by all macrocells in an LAB. Sharing allows efficient integration of complex combinatorial functions.



Expanders are fed by all signals in the LAB. One expander may feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flip-flops or latches.

I/O Control Block

Each LAB has an I/O control block (Figure 5) that consists of a user-configurable I/O control function for each I/O pin. The I/O control block is fed by the macrocell array. The tri-state buffer is controlled by a dedicated macrocell product term, and drives the I/O pad.

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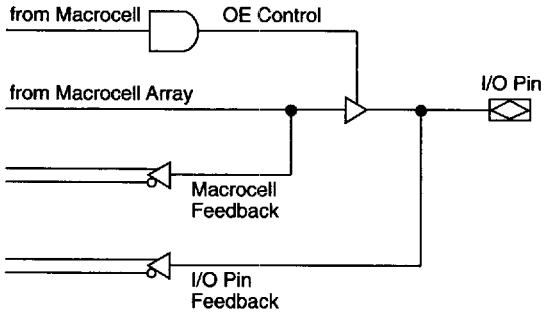
Figure 5. I/O Control Block

The decoupled I/O control block features dual feedback to maximize use of device pins.



Each MAX 5000 EPLD has dual feedback—a feedback path both before and after the tri-state buffer—for every I/O pin. The tri-state buffer decouples the I/O pins from the macrocells so that all registers within the LAB can be "buried." Thus, I/O pins can be configured as dedicated input, output, or bidirectional pins. In multi-LAB devices, I/O pins feed the PIA.

Programmable Interconnect Array

The higher-density MAX 5000 devices (EPM5064, EPM5128, EPM5130, and EPM5192) use a Programmable Interconnect Array (PIA) to route signals between the various LABs. The PIA routes only the signals required for implementing logic in an LAB, and is fed by all macrocell feedbacks and all I/O pin feedbacks. Unlike channel routing in masked or programmable gate arrays—where routing delays are variable and path-dependent—the PIA has a fixed delay. Because the PIA eliminates skew between signals, timing performance is easy to predict.

Timing Model

Timing within MAX 5000 EPLDs is easily determined with MAX+PLUS and MAX+PLUS II software or with the models shown in Figure 6. MAX 5000 EPLDs have fixed internal delays, which allow the user to determine the worst-case timing for any design. For complete timing information, both MAX+PLUS and MAX+PLUS II software provide point-to-point delay prediction, full timing simulation, and detailed timing analysis.

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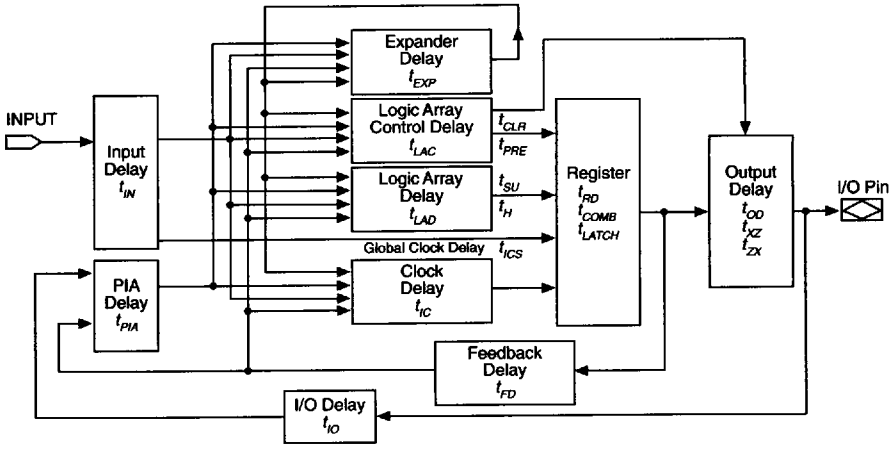
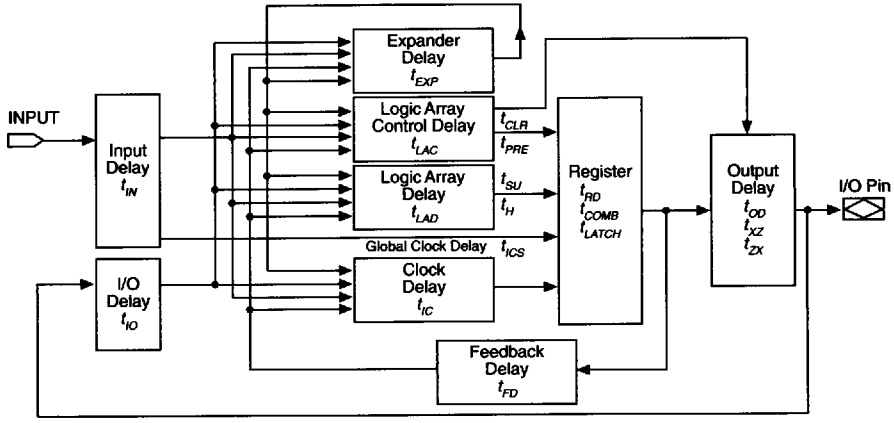
Figure 6. Timing Models

Design performance can be predicted with these timing models and the device performance specifications.

Multi-LAB EPLDs



Single-LAB EPLDs



The timing models shown in Figure 6 can be used together with the internal timing parameters for a particular EPLD to derive timing information. External timing parameters are derived from a sum of internal parameters and represent pin-to-pin timing delays. Figure 7 shows the internal timing waveforms for these devices. Refer to *Application Brief 75* for further information on MAX 5000 EPLD timing.

Design Security

MAX 5000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset by erasing the EPLD.

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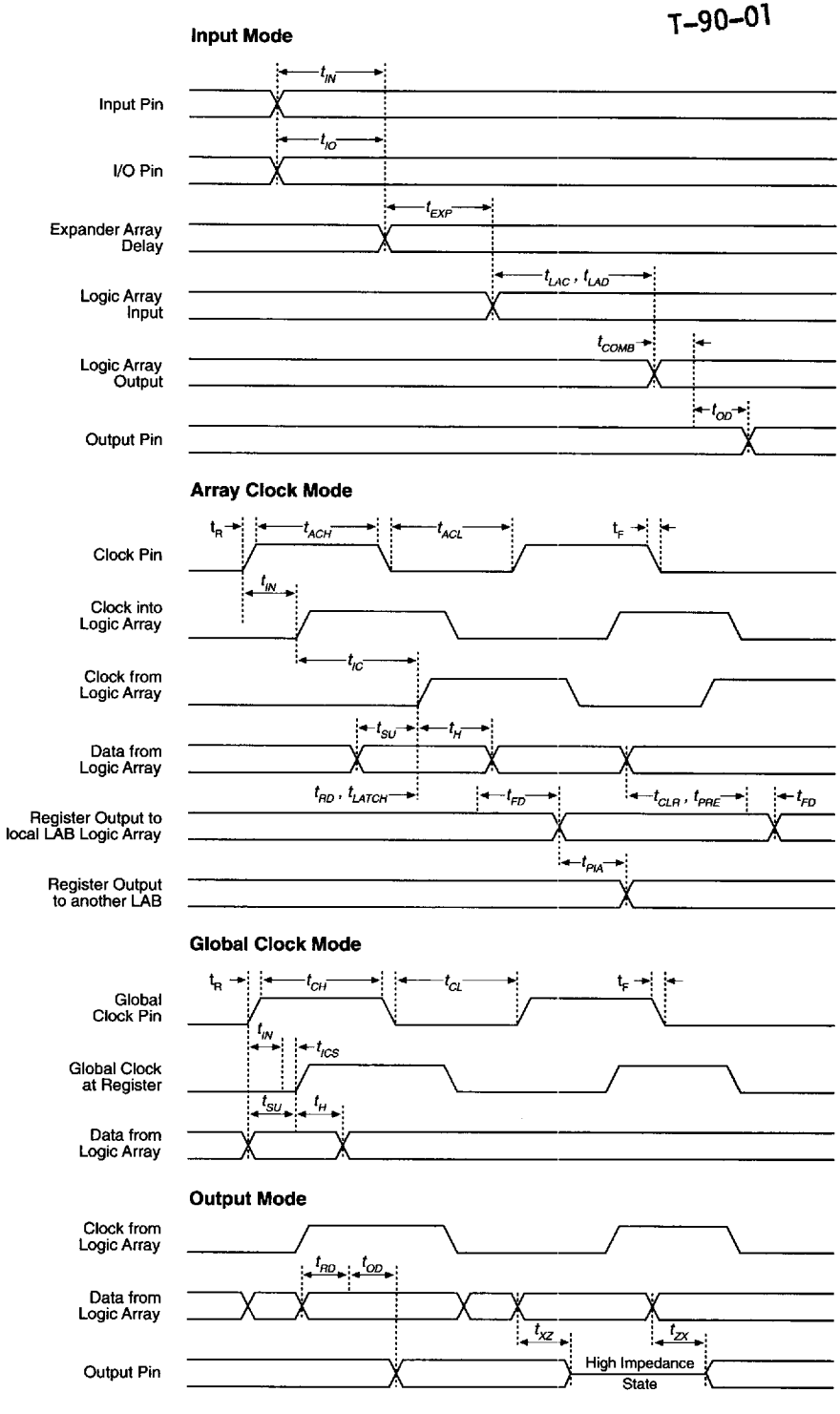
Figure 7. Switching Waveforms

In multi-LAB EPLDs, I/O pins used as inputs can traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Functional Testing

MAX 5000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are performed under the conditions shown in Figure 8.

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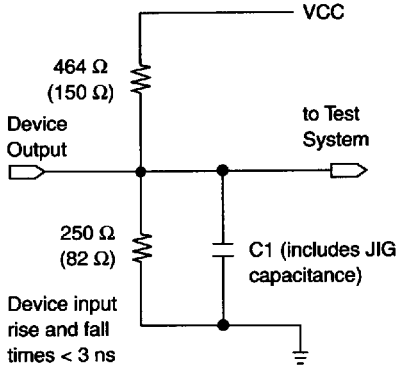
Figure 8. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable input noise immunity.

Note: Numbers in parentheses are for the EPM5016 EPLD.



Test programs can be used and then erased during early stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices. EPLDs also contain on-board logic test circuitry to allow verification of function and AC specifications of devices in windowless packages.

MAX+PLUS & MAX+PLUS II Development Systems

The MAX+PLUS and MAX+PLUS II development systems are unified CAE systems for integrating designs into MAX 5000 EPLDs. Table 1 summarizes the features available in each MAX+PLUS and MAX+PLUS II package.

Designs can be entered as logic schematics with the Graphic Editor or as state machines, truth tables, and Boolean equations with the Altera Hardware Description Language (AHDL); waveform design entry is also available with MAX+PLUS II software. Logic synthesis and minimization optimize the logic of a design. Automatic design partitioning into multiple EPLDs is also available with MAX+PLUS II software. Errors in a design are automatically located and highlighted in the original design file. Design verification and timing analysis are performed with built-in timing simulators, timing analyzers, and delay prediction.

Table 1. MAX 5000 EPLD Development Systems & Software Packages

	Design Entry					Design Compilation & Verification							
MAX+PLUS II:	Schematic Capture	AHDL	Waveform Entry	State Machine Entry	Boolean Equation Entry	Functional Simulation	Timing Simulation	Timing Analysis	Waveform Editing	Design Partitioning	Multi-EPLD Simulation	EDIF Interface	Programming Hardware
PLDS-HPS	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
PLS-HPS	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	
PLS-OS		✔		✔	✔					✔		✔	
PLS-ES		✔		✔	✔								
PLS-WS/HP		✔		✔	✔					✔		✔	
PLS-WS/SN		✔		✔	✔					✔		✔	
MAX+PLUS:													
PLDS-MAX	✔	✔		✔	✔		✔	✔	✔				✔
PLS-MAX	✔	✔		✔	✔		✔	✔	✔				

Hosted on IBM PS/2, PC-AT, or compatible machines, and workstations (e.g., HP/Apollo and Sun), MAX+PLUS and MAX+PLUS II give designers the tools to quickly and efficiently create complex logic designs. Further details about the MAX+PLUS and MAX+PLUS II development systems are available in the *PLDS-MAX & PLS-MAX*, *PLS-WS/HP*, *PLS-WS/SN*, and *PLDS-HPS*, *PLS-HPS*, *PLS-OS & PLS-ES* data sheets in this data book.

Device Programming

MAX 5000 EPLDs can be programmed on an IBM PS/2, PC-AT, or compatible computer with an Altera Logic Programmer card, the Master Programming Unit (MPU), and an appropriate device adapter. These items are included in the complete PLDS-MAX and PLDS-HPS Development Systems or may be purchased separately. MAX 5000 EPLDs can also be programmed with third-party hardware (see the *Third-Party Development & Programming Support Data Sheet* in this data book). Contact Altera or your programming equipment manufacturer for more information.

Notes:

EPM5016 EPLD

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Features

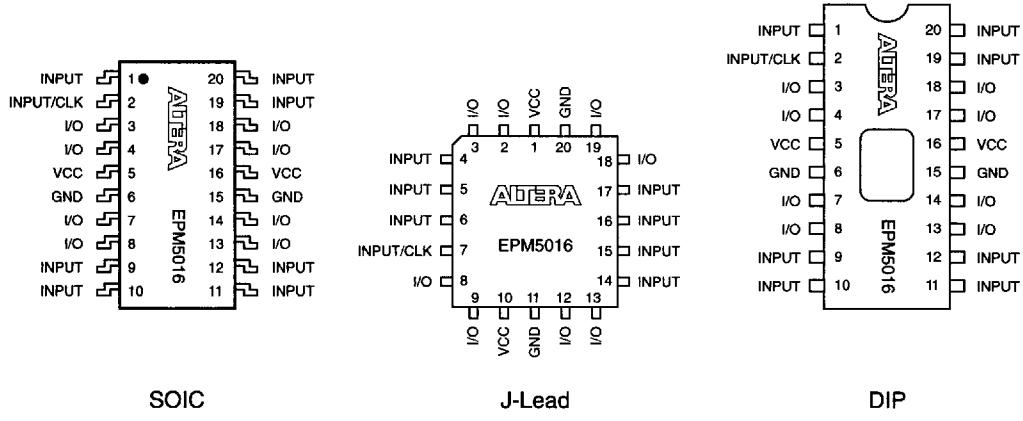
- High-speed 20-pin DIP, J-lead, or SOIC single-LAB MAX 5000 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- 16 individually configurable macrocells
- 32 expander product terms (expanders) that allow 34 product terms in a single macrocell
- Up to 21 flip-flops or 32 latches
- Up to 10 input latches that can be constructed with cross-coupled expanders
- 24-mA output drivers to allow direct interfacing to system buses
- Programmable I/O architecture allowing up to 16 inputs and 8 outputs
- Available in 20-pin windowed ceramic DIP package, or plastic one-time-programmable (OTP) DIP, J-lead (PLCC), and 300-mil SOIC packages

General Description

The Altera EPM5016 EPLD is a Multiple Array MatriX (MAX) 5000-family CMOS EPLD that is optimized for speed. It can integrate multiple SSI and MSI TTL and 74HC devices. In addition, it can replace any 20-pin PAL or PLA device with logic left over for further integration. See Figure 9.

Figure 9. EPM5016 Package Pin-Out Diagrams

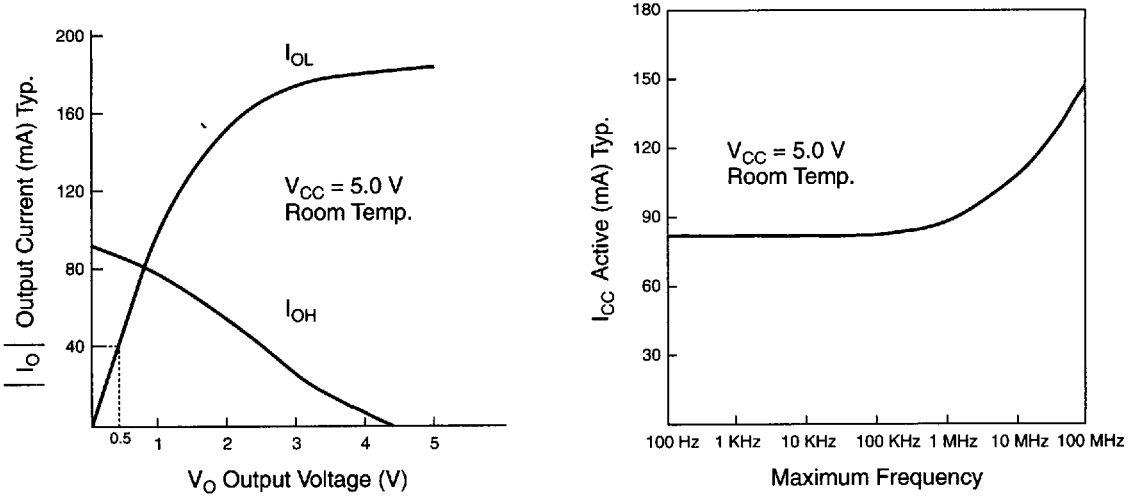
Package outlines not drawn to scale.



SOIC J-Lead DIP

Figure 10 shows output drive characteristics of EPM5016 I/O pins and typical supply current versus frequency for the EPM5016 EPLD.

Figure 10. EPM5016 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5016 EPLD contains 16 macrocells (see Figure 11). The expander product-term array for the EPM5016 EPLD contains 32 expanders. The I/O control block contains 8 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility.

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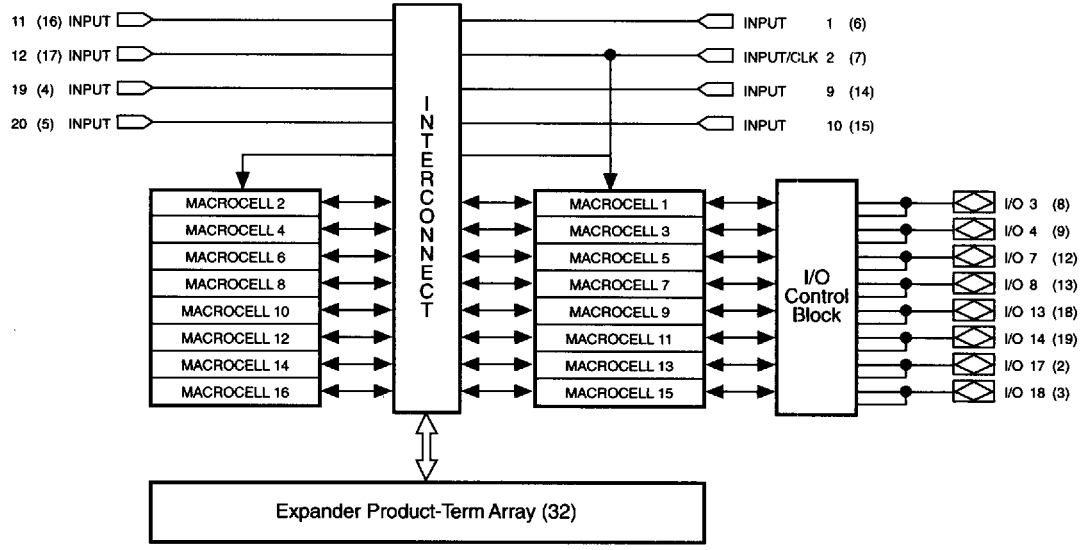
Figure 11. EPM5016 Block Diagram

The EPM5016 has 16 macrocells and 32 expanders. Numbers in parentheses are for the PLCC package.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			200	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		80	110 (150)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		85	115 (175)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20	ns
t_{PD2}	I/O input to non-registered output			15		17		20	ns
t_{SU}	Global clock setup time		6		8		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		9		11		13	ns
t_{CH}	Global clock high time		5		6		8		ns
t_{CL}	Global clock low time		5		6		8		ns
t_{ASU}	Array clock setup time		5		7		9		ns
t_{AH}	Array clock hold time		5		7		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		17		20	ns
t_{ACH}	Array clock high time	*See Note (6)*	4		5		7		ns
t_{ACL}	Array clock low time		6		7		9		ns
t_{CNT}	Minimum global clock period			10		12		16	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	100		83.3		62.5		MHz
t_{ACNT}	Minimum array clock period			10		12		16	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	100		83.3		62.5		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	100		83.3		62.5		MHz

Internal Timing Parameters *See Note (8)*			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		5		5	ns
t_{IO}	I/O input pad and buffer delay			4		5		5	ns
t_{EXP}	Expander array delay			5		8		10	ns
t_{LAD}	Logic array delay			6		7		9	ns
t_{LAC}	Logic control array delay			4		5		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5	ns
t_{ZX}	Output buffer enable delay			7		7		8	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8	ns
t_{SU}	Register setup time		2		5		8		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		6		8		9		ns
t_{IC}	Array clock delay			6		6		8	ns
t_{ICS}	Global clock delay			0		1		2	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			3		6		6	ns
t_{CLR}	Register clear time			3		6		6	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as a 16-bit counter.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5016-15, EPM5016-17, EPM5016-20
Industrial	(–40° C to 85° C)	EPM5016-20
Military	(–55° C to 125° C)	Consult factory

EPM5032 EPLD

T-46-19-07

Features

- High-speed 28-pin DIP, J-lead, or SOIC single-LAB MAX 5000 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 76 MHz
  - Pipelined data rates up to 83 MHz
- 32 individually configurable macrocells
- 64 expander product terms (expanders) that allow 66 product terms on a single macrocell
- Up to 42 flip-flops or 64 latches
- Up to 21 input latches that can be constructed with cross-coupled expanders
- Programmable I/O architecture allowing up to 24 inputs and 16 outputs
- Available in 28-pin windowed ceramic or plastic one-time-programmable (OTP) DIP and J-lead packages, as well as plastic OTP 300-mil SOIC packages

General Description

The Altera EPM5032 EPLD is a Multiple Array MatriX (MAX) 5000-family CMOS EPLD optimized for speed. It can integrate multiple SSI and MSI TTL and 74HC devices. In addition, it can replace multiple 20-pin PAL or PLA devices with logic left over for further integration. See Figure 12.

Figure 12. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale.

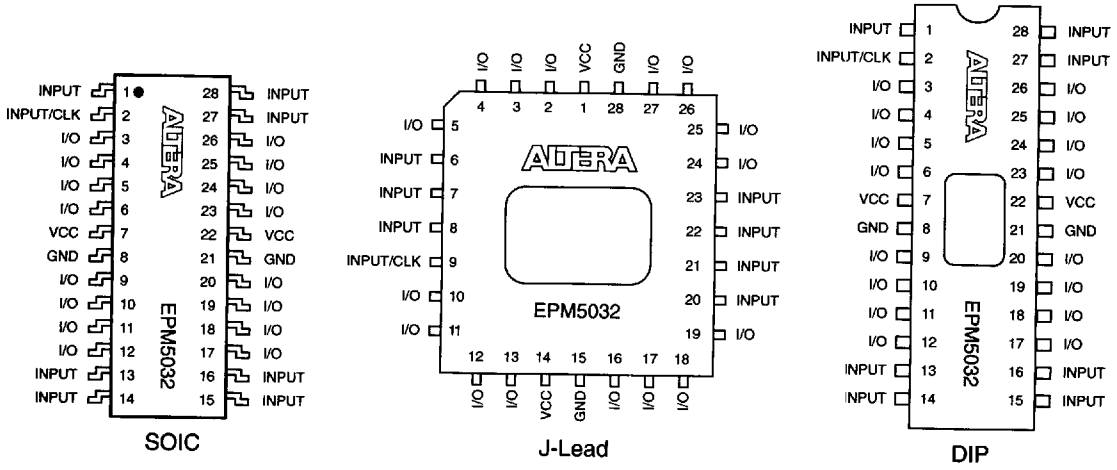
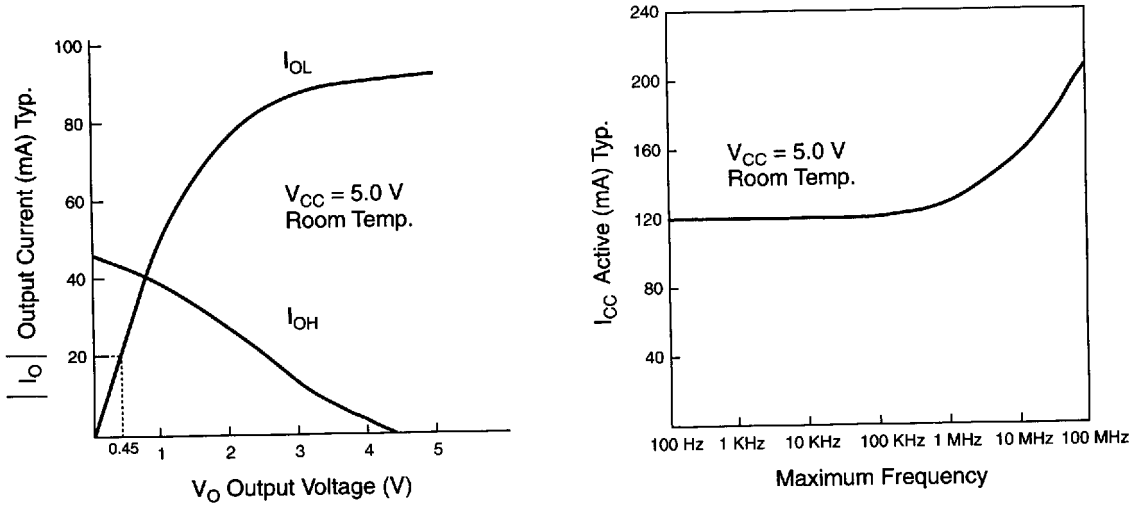


Figure 13 shows output drive characteristics of EPM5032 I/O pins and typical supply current versus frequency for the EPM5032 EPLD.

Figure 13. EPM5032 Output Drive Characteristics and I_{CC} vs. Frequency

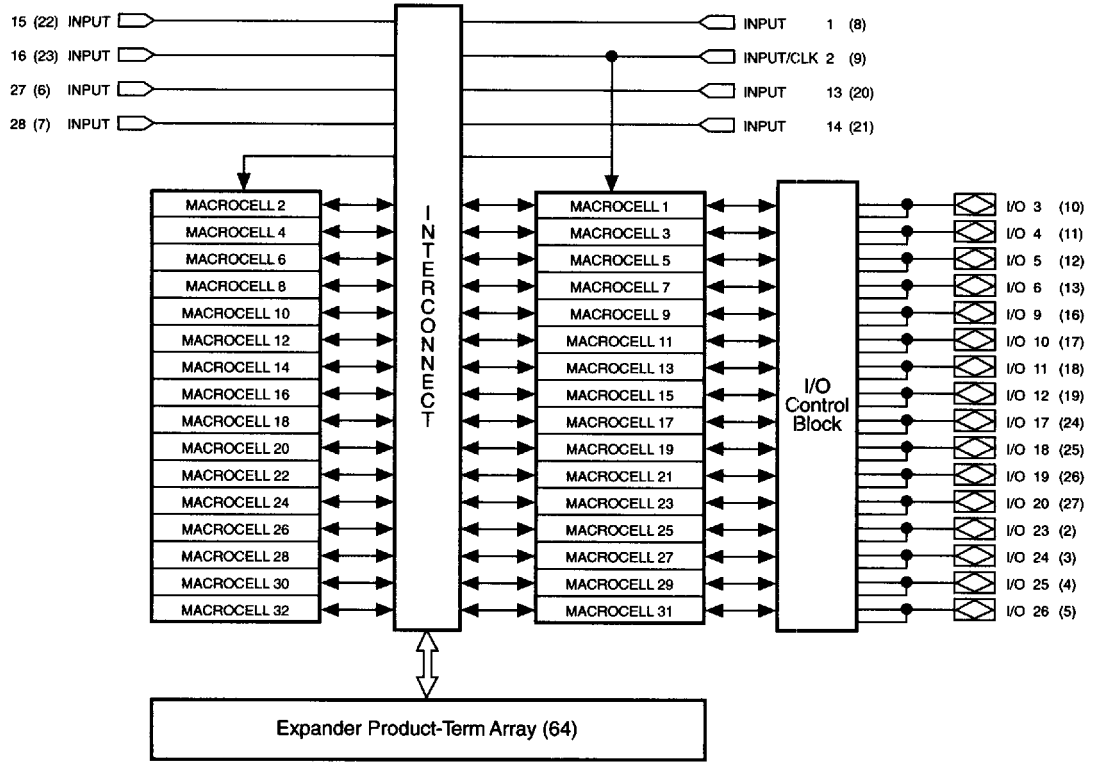


The EPM5032 EPLD contains 32 macrocells (see Figure 14). The EPM5032 expander product-term array contains 64 expanders. The I/O control block contains 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility.

T-46-19-09

Figure 14. EPM5032 Block Diagram

The EPM5032 has 32 macrocells and 64 expanders. Numbers in parentheses are for J-lead packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
T_C	Case temperature	For military use	–55	125	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND		120	150 (200)	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (5)*		125	155 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{PD2}	I/O input to non-registered output			15		17		20		25	ns
t_{SU}	Global clock setup time		9		10		12		15		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		10		12		15	ns
t_{CH}	Global clock high time		6		6		7		8		ns
t_{CL}	Global clock low time		6		6		7		8		ns
t_{ASU}	Array clock setup time		7		8		9		12		ns
t_{AH}	Array clock hold time		7		8		9		12		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		20		25	ns
t_{ACH}	Array clock high time	*See Note (6)*	6		6		7		9		ns
t_{ACL}	Array clock low time		7		8		9		11		ns
t_{CNT}	Minimum global clock period			13		14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	76.9		71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			13		14		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	76.9		71.4		62.5		50		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	83.3		83.3		71.4		62.5		MHz

Internal Timing Parameters *See Note (8)*			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		5		5		7	ns
t_{IO}	I/O input pad and buffer delay			4		5		5		7	ns
t_{EXP}	Expander array delay			8		8		10		15	ns
t_{LAD}	Logic array delay			6		7		9		10	ns
t_{LAC}	Logic control array delay			4		5		7		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5		5	ns
t_{ZX}	Output buffer enable delay			7		7		8		11	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8		11	ns
t_{SU}	Register setup time		5		5		5		8		ns
t_{LATCH}	Flow-through latch delay			1		1		1		3	ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		3	ns
t_{H}	Register hold time		6		6		9		12		ns
t_{IC}	Array clock delay			6		8		8		10	ns
t_{ICS}	Global clock delay			1		1		2		3	ns
t_{FD}	Feedback delay			1		1		1		1	ns
t_{PRE}	Register preset time			5		5		6		9	ns
t_{CLR}	Register clear time			5		5		6		9	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 32-bit counter.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5032-15, EPM5032-17, EPM5032-20, EPM5032-25
Industrial	(–40° C to 85° C)	EPM5032-25
Military	(–55° C to 125° C)	EPM5032-25

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

EPM5064 EPLD

T-46-19-09

Features

- High-density 64-macrocell general-purpose MAX 5000 EPLD
- 128 shareable expander product terms providing flexible logic expansion
  - Over 32 product terms in a single macrocell
  - 64 additional latches provided by cross-coupled expanders
- Multi-LAB MAX architecture with t_{PD} = 25 ns, counter frequencies up to 50 MHz, and pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 36 inputs and 28 outputs
- 44-pin J-lead package that easily integrates 10 standard PALs in 1/2 square inch of board space; windowed ceramic or plastic one-time-programmable packages for volume production

General Description

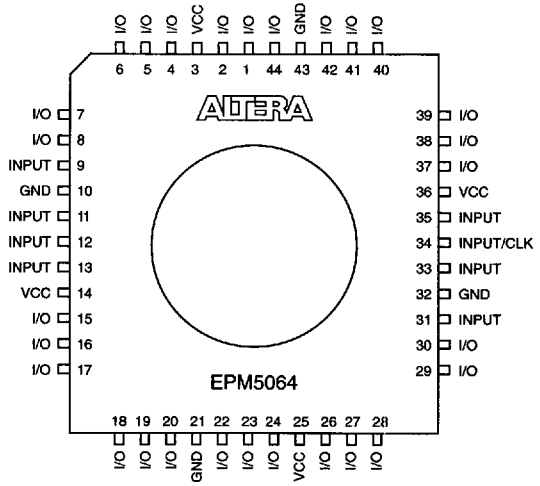
The Altera EPM5064 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that serves as a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. In addition, it can integrate multiple 20- and 24-pin low-density PLDs. For example, the EPM5064 EPLD can integrate the logic contained in over 10 standard 20-pin PALs.

Figure 15 shows the package pin-out for the EPM5064 J-lead package. This package occupies only 1/2 square inch of board space.

3 MAX 5000 EPLDs

Figure 15. EPM5064 Package Pin-Out Diagram

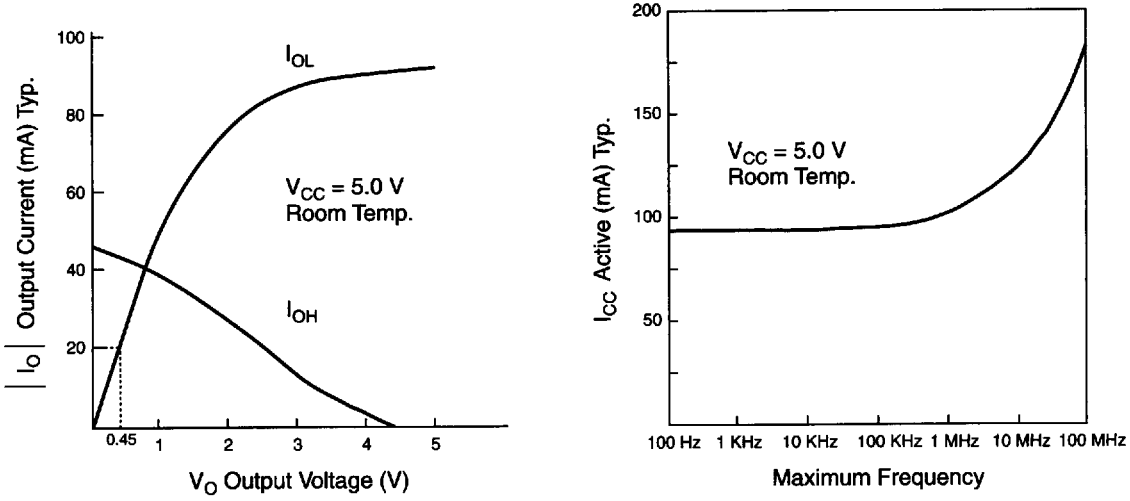
Package outline not drawn to scale.



J-Lead

Figure 16 shows output drive characteristics of EPM5064 I/O pins and typical supply current versus frequency for the EPM5064 EPLD. The high integration density of the EPM5064 EPLD often greatly reduces system power requirements.

Figure 16. EPM5064 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5064 consists of 64 macrocells equally divided into 4 Logic Array Blocks (LABs) that each contain 16 macrocells (see Figure 17). Each LAB also contains 32 expander product terms. The flexibility of the LABs allows easy integration of any common PLD.

The EPM5064 EPLD has 8 dedicated input pins, one of which can be used as a global system clock that provides enhanced clock-to-output delays. The device has 28 I/O pins that can be configured for input, output, or bidirectional data flow. The I/O pins feature dual-feedback to allow any macrocell to be buried. Two of the LABs have 8 I/O pins (ensuring high speed for 8-bit bus functions) and the other two LABs have 6 I/O pins.

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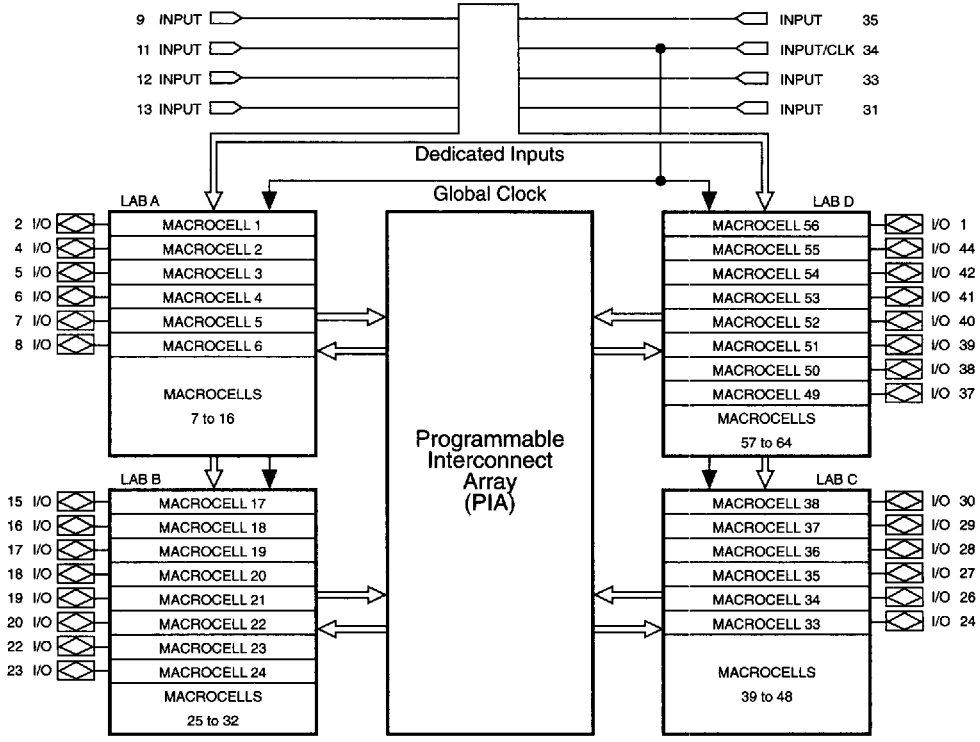
Figure 17. EPM5064 Block Diagram

The EPM5064 EPLD has 64 macrocells divided into 4 Logic Array Blocks.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		90	125 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		95	135 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		12		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5064-1, EPM5064-2, EPM5064
Industrial	(–40° C to 85° C)	EPM5064
Military	(–55° C to 125° C)	EPM5064

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

EPM5128 EPLD

T-46-19-09

Features

- High-density 128-macrocell general-purpose MAX 5000 EPLD
- 256 shareable expander product terms that allow over 32 product terms in a single macrocell
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in 68-pin windowed ceramic or plastic one-time-programmable (OTP) J-lead packages and in 68-pin windowed ceramic PGA packages

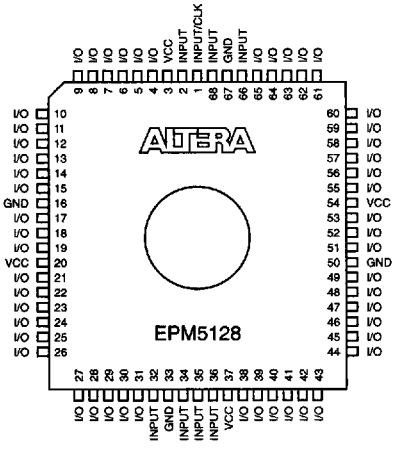
General Description

The Altera EPM5128 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. For example, a 74161 counter uses only 3% of the EPM5128 EPLD. The EPM5128 EPLD can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs. Figure 18 shows the J-lead and PGA package diagrams for the EPM5128 EPLD.

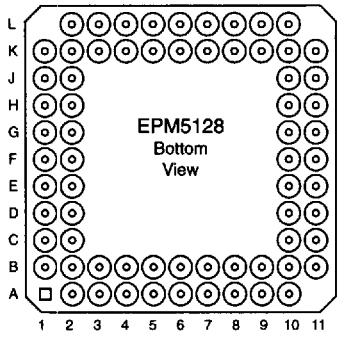
3 MAX 5000 EPLDs

Figure 18. EPM5128 Package Pin-Out Diagrams

See Table 2 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.



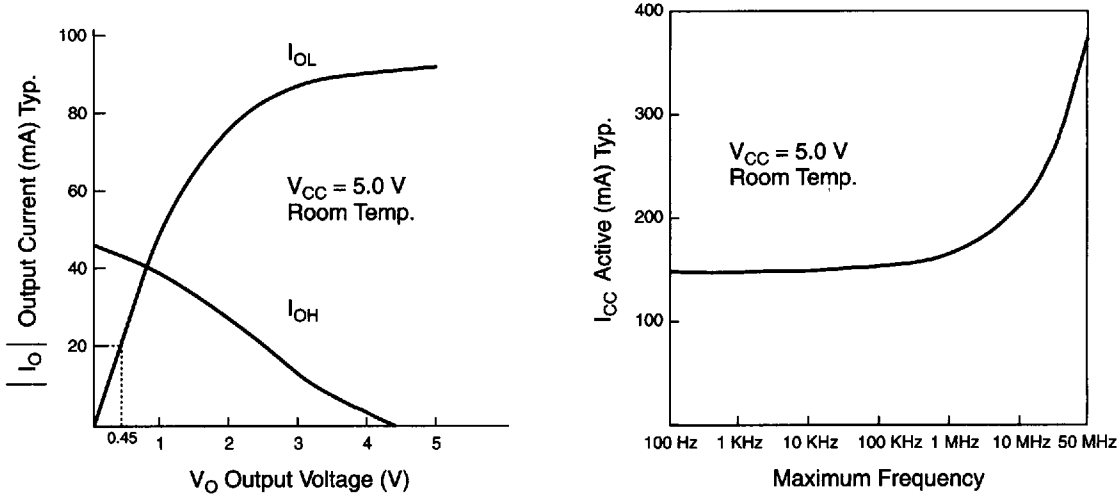
J-Lead



PGA

Figure 19 shows output drive characteristics of EPM5128 I/O pins and typical supply current versus frequency for the EPM5128 EPLD.

Figure 19. EPM5128 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5128 EPLD consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) that each contain 16 macrocells (see Figure 20). Each LAB also contains 32 expander product terms. The EPM5128 EPLD has 8 dedicated input pins, one of which may be used as a global (synchronous) system clock. The EPM5128 device contains 52 I/O pins that can be configured for input, output, or bidirectional data flow. Four of the LABs have 8 I/O pins, and the other 4 have 5 I/O pins.

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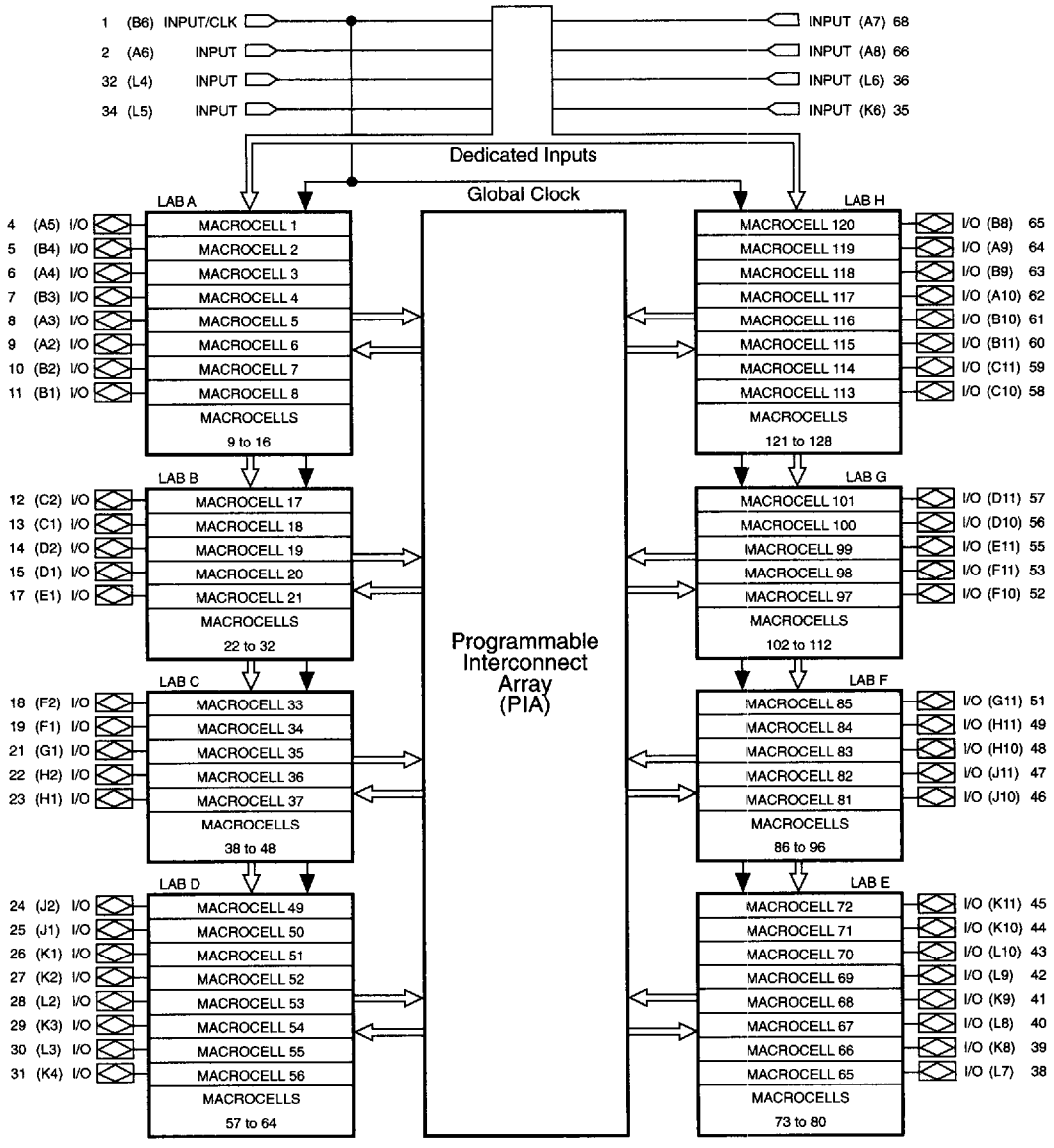
Figure 20. EPM5128 Block Diagram

Numbers in parentheses are for PGA packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

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Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the maximum frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5128-1, EPM5128-2, EPM5128
Industrial	(–40° C to 85° C)	EPM5128
Military	(–55° C to 125° C)	EPM5128

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Table 2 shows the pin-outs for the EPM5128 PGA package.

Table 2. EPM5128 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	I/O	K4	I/O
A3	I/O	B10	I/O	F11	I/O	K5	GND
A4	I/O	B11	I/O	G1	I/O	K6	INPUT
A5	I/O	C1	I/O	G2	VCC	K7	VCC
A6	INPUT	C2	I/O	G10	GND	K8	I/O
A7	INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	INPUT
B4	I/O	E2	GND	J10	I/O	L6	INPUT
B5	VCC	E10	VCC	J11	I/O	L7	I/O
B6	INPUT/CLK	E11	I/O	K1	I/O	L8	I/O
B7	GND	F1	I/O	K2	I/O	L9	I/O
B8	I/O	F2	I/O	K3	I/O	L10	I/O

EPM5130 EPLD

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Features

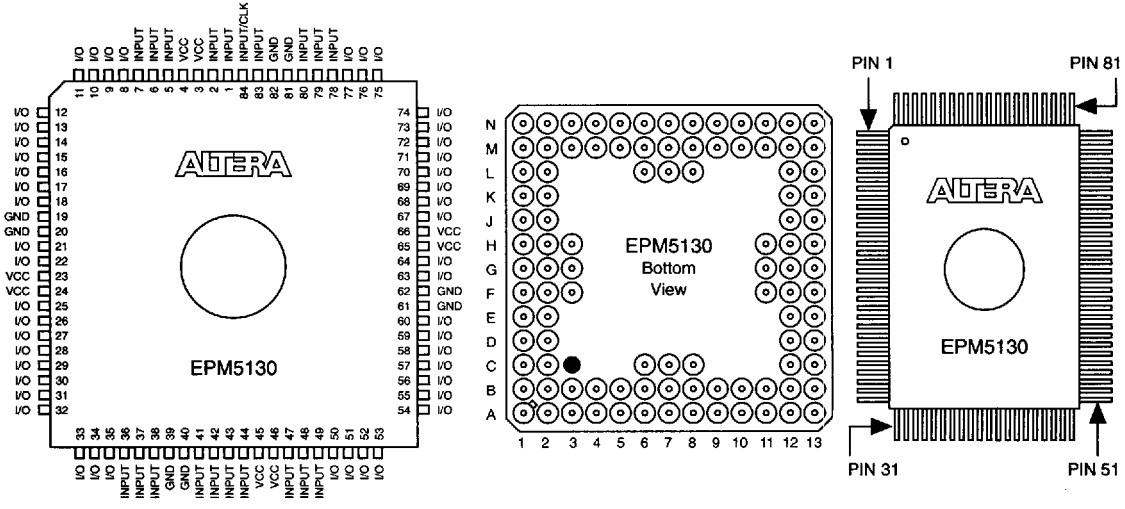
- High-density 128-macrocell general-purpose MAX 5000 EPLD
- 128 macrocells optimized for pin-intensive applications, easily integrating over 60 TTL MSI and SSI components
- High pin count for 16- or 32-bit data paths
- 256 shareable expander product terms
  - More than 32 product terms in a single macrocell
  - 128 additional latches provided by cross-coupling expanders
  - All inputs can be latched without using macrocells
- 20 high-speed dedicated inputs for fast latching of 16-bit functions
- Multi-LAB architecture ensuring high speeds
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Fast clock-to-output delays for bus-oriented functions
- Programmable I/O architecture that allows up to 84 inputs or 64 outputs in windowed ceramic PGA, and windowed ceramic and one-time-programmable (OTP) plastic QFP packages
- Programmable I/O architecture that allows up to 68 inputs or 48 outputs in windowed ceramic and plastic OTP J-lead packages

General Description

The EPM5130 EPLD (see Figure 21) is a user-configurable, high-performance Multiple Array Matrix (MAX) 5000-family EPLD that is optimized for pin-intensive designs. It provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic.

Figure 21. EPM5130 Package Pin-Out Diagrams

See Table 3 in this data sheet for QFP pin-outs and Table 4 for PGA pin-outs. Package outlines not drawn to scale.

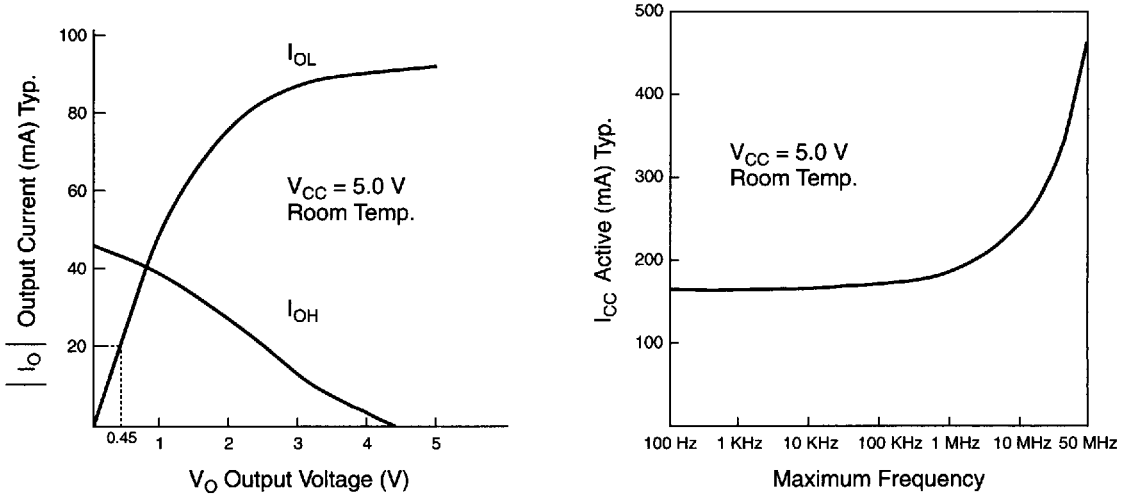


The EPM5130 EPLD is available in windowed ceramic 84-pin J-lead chip carrier (JLCC), 100-pin pin-grid array (PGA), and 100-pin quad flat pack (WQFP) packages, as well as OTP plastic J-lead (PLCC) and QFP packages.

A single EPM5130 EPLD can quickly integrate multiple 20- and 24-pin low-density PLDs and high-pin-count subsystems, such as custom DMA controllers. In addition, it can handle a 32-bit data path application with enough I/O to allow the required control signals to be implemented.

Figure 22 shows output drive characteristics of EPM5130 I/O pins and typical supply current versus frequency for the EPM5130 EPLD.

Figure 22. EPM5130 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5130 EPLD consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs), each containing 16 macrocells and 32 expander product terms (see Figure 23). Expander product terms can be used and shared by all macrocells in the device to ensure efficient use of device resources. Because the LAB is very compact, the high speeds required by most I/O subsystems are maintained.

The EPM5130 EPLD has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a global (synchronous) clock to provide enhanced clock-to-output delays for bus-oriented functions. The EPM5130 EPLD also has 64 I/O pins, 8 in each LAB, that can be configured for input, output, or bidirectional data flow. Dual feedback on the I/O pins provides the most efficient use of device pin resources.

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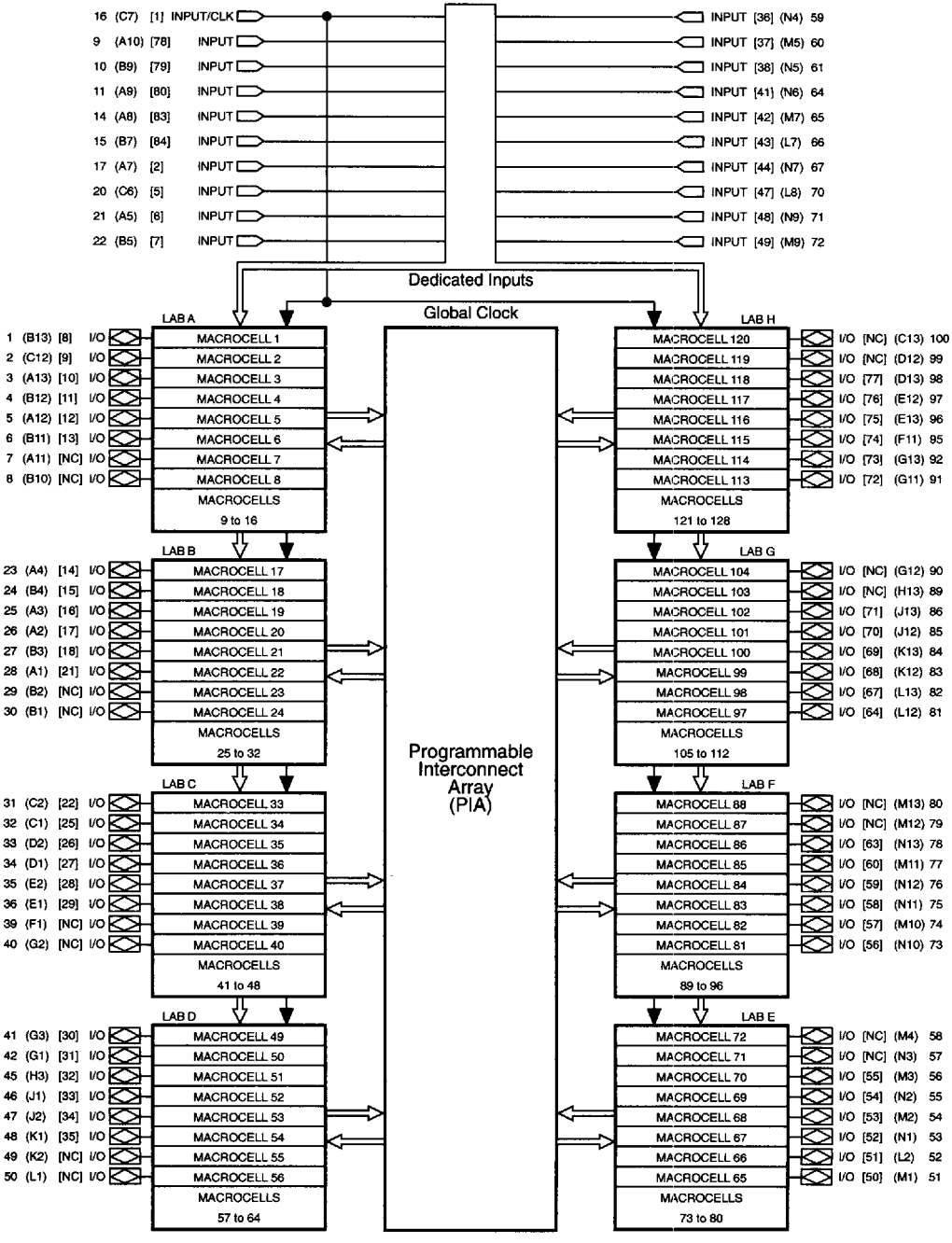
Figure 23. EPM5130 Block Diagram

Numbers in parentheses are for PGA packages; numbers in brackets are for J-lead packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		175	250 (325)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		180	275 (375)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5130-1, EPM5130-2, EPM5130
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Table 3 shows the pin-outs for the EPM5130 QFP package. T-46-19-09

Table 3. EPM5130 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	26	I/O	51	I/O	76	I/O
2	I/O	27	I/O	52	I/O	77	I/O
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	INPUT	34	I/O	59	INPUT	84	I/O
10	INPUT	35	I/O	60	INPUT	85	I/O
11	INPUT	36	I/O	61	INPUT	86	I/O
12	GND	37	GND	62	GND	87	GND
13	GND	38	GND	63	GND	88	GND
14	INPUT	39	I/O	64	INPUT	89	I/O
15	INPUT	40	I/O	65	INPUT	90	I/O
16	INPUT/CLK	41	I/O	66	INPUT	91	I/O
17	INPUT	42	I/O	67	INPUT	92	I/O
18	VCC	43	VCC	68	VCC	93	VCC
19	VCC	44	VCC	69	VCC	94	VCC
20	INPUT	45	I/O	70	INPUT	95	I/O
21	INPUT	46	I/O	71	INPUT	96	I/O
22	INPUT	47	I/O	72	INPUT	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	I/O	74	I/O	99	I/O
25	I/O	50	I/O	75	I/O	100	I/O

Table 4 shows the pin-outs for the EPM5130 PGA package.

Table 4. EPM5130 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	I/O	B13	I/O	G11	I/O	M2	I/O
A2	I/O	C1	I/O	G12	I/O	M3	I/O
A3	I/O	C2	I/O	G13	I/O	M4	I/O
A4	I/O	C6	INPUT	H1	VCC	M5	INPUT
A5	INPUT	C7	INPUT/CLK	H2	VCC	M6	GND
A6	VCC	C8	GND	H3	I/O	M7	INPUT
A7	INPUT	C12	I/O	H11	GND	M8	VCC
A8	INPUT	C13	I/O	H12	GND	M9	INPUT
A9	INPUT	D1	I/O	H13	I/O	M10	I/O
A10	INPUT	D2	I/O	J1	I/O	M11	I/O
A11	I/O	D12	I/O	J2	I/O	M12	I/O
A12	I/O	D13	I/O	J12	I/O	M13	I/O
A13	I/O	E1	I/O	J13	I/O	N1	I/O
B1	I/O	E2	I/O	K1	I/O	N2	I/O
B2	I/O	E12	I/O	K2	I/O	N3	I/O
B3	I/O	E13	I/O	K12	I/O	N4	INPUT
B4	I/O	F1	I/O	K13	I/O	N5	INPUT
B5	INPUT	F2	GND	L1	I/O	N6	INPUT
B6	VCC	F3	GND	L2	I/O	N7	INPUT
B7	INPUT	F11	I/O	L6	GND	N8	VCC
B8	GND	F12	VCC	L7	INPUT	N9	INPUT
B9	INPUT	F13	VCC	L8	INPUT	N10	I/O
B10	I/O	G1	I/O	L12	I/O	N11	I/O
B11	I/O	G2	I/O	L13	I/O	N12	I/O
B12	I/O	G3	I/O	M1	I/O	N13	I/O

EPM5192 EPLD

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Features

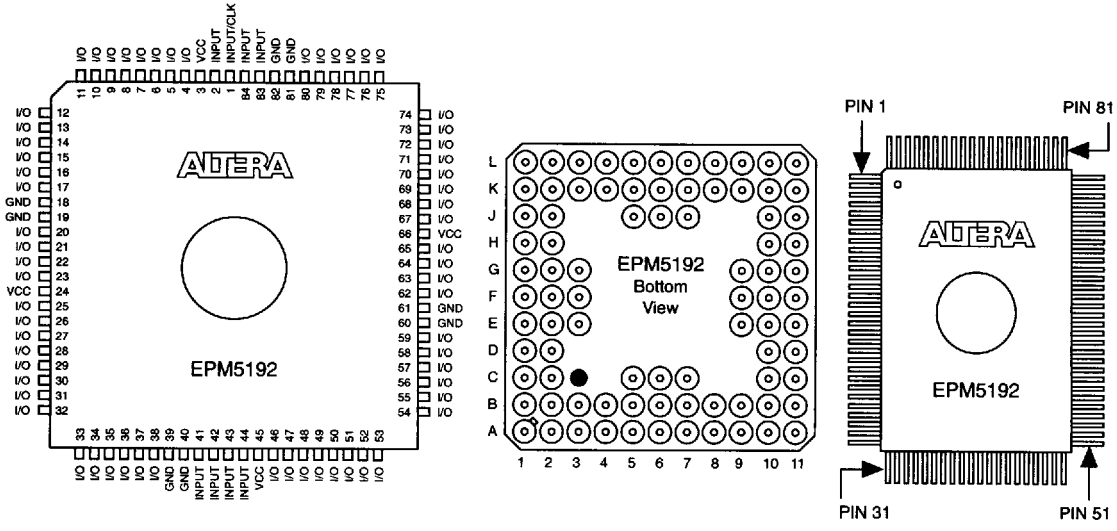
- 192 macrocells for easy replacement of over 100 TTL devices and for integration of complete logic boards into a single package
- 384 shareable expander product terms that offer flexibility for register and combinatorial logic expansion
- Multi-LAB architecture that ensures high speeds
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) J-lead packages, 84-pin windowed ceramic PGA packages, and 100-pin windowed ceramic and plastic OTP QFP packages

General Description

Altera's EPM5192 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that provides high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. Package pin-out diagrams for the EPM5192 EPLD are shown in Figure 24.

Figure 24. EPM5192 Package Pin-Out Diagrams

See Table 5 in this data sheet for QFP pin-outs and Table 6 for PGA pin-outs. Package outlines not drawn to scale.

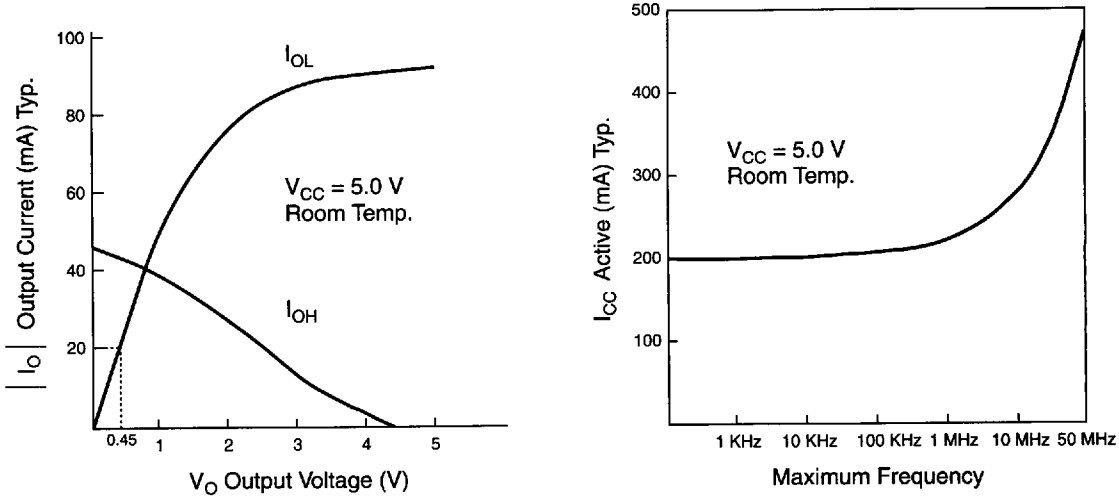


J-Lead PGA QFP

The EPM5192 EPLD can replace over 100 TTL SSI and MSI components and integrate the logic contained in over 20 22V10 devices. In addition, it accommodates other low-density PLDs of all sizes. These features allow the EPM5192 EPLD to easily integrate complete systems into a single device.

Figure 25 shows output drive characteristics of EPM5192 I/O pins and typical supply current versus frequency for the EPM5192 EPLD.

Figure 25. EPM5192 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5192 EPLD consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs) that each contain 16 macrocells and 32 expander product terms (see Figure 26). Because each LAB is very compact, high performance is maintained and device resources are used efficiently.

The EPM5192 EPLD has 8 dedicated input pins, one of which can be used as a global (synchronous) clock. The EPM5192 EPLD can mix global and array (asynchronous) clocking in a single device, facilitating easy integration of multiple subsystems. It also has 64 I/O pins that can be configured for input, output, or bidirectional data flow, providing an interface to high-speed, bus-oriented applications.

Figure 26. EPM5192 Block Diagram

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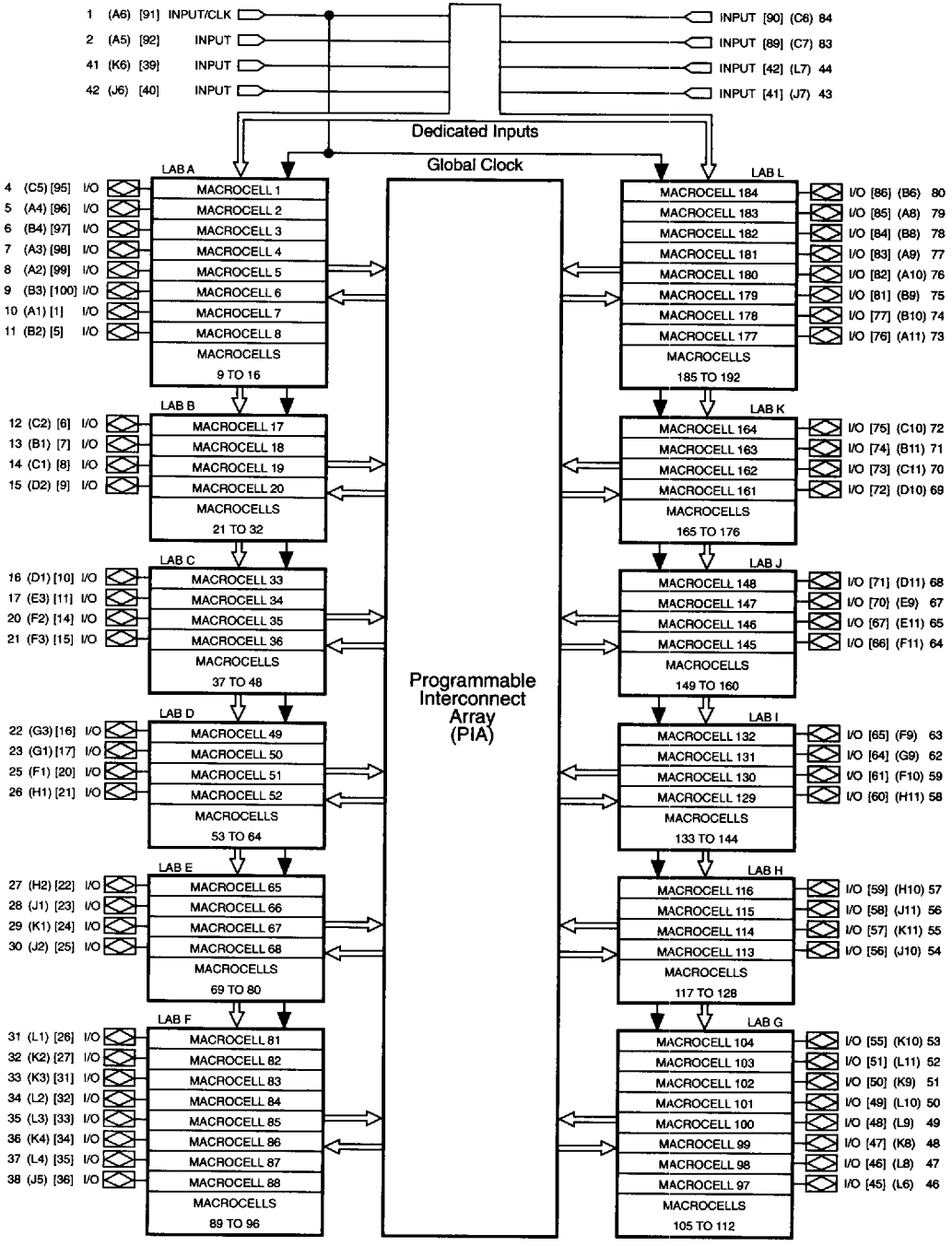
Numbers in parentheses are for PGA packages; numbers in brackets are for QFP packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

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AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
(4) Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40°$ C to 85° C for industrial use.
$V_{CC} = 5\text{ V} \pm 10\%$, $T_C = -55°$ C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM5192-1, EPM5192-2, EPM5192
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Table 5 shows the pin-outs for the EPM5192 QFP package.

Table 5. EPM5192 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	26	I/O	51	I/O	76	I/O
2	NC	27	I/O	52	NC	77	I/O
3	NC	28	NC	53	NC	78	NC
4	NC	29	NC	54	NC	79	NC
5	I/O	30	NC	55	I/O	80	NC
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	I/O	34	I/O	59	I/O	84	I/O
10	I/O	35	I/O	60	I/O	85	I/O
11	I/O	36	I/O	61	I/O	86	I/O
12	GND	37	GND	62	GND	87	GND
13	GND	38	GND	63	GND	88	GND
14	I/O	39	INPUT	64	I/O	89	INPUT
15	I/O	40	INPUT	65	I/O	90	INPUT
16	I/O	41	INPUT	66	I/O	91	INPUT/CLK
17	I/O	42	INPUT	67	I/O	92	INPUT
18	NC	43	VCC	68	NC	93	VCC
19	VCC	44	NC	69	VCC	94	NC
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	I/O	74	I/O	99	I/O
25	I/O	50	I/O	75	I/O	100	I/O

Note: NC represents "not connected."

Table 6 shows the pin-outs for the EPM5192 PGA package.

Table 6. EPM5192 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	I/O	B11	I/O	F9	I/O	K2	I/O
A2	I/O	C1	I/O	F10	I/O	K3	I/O
A3	I/O	C2	I/O	F11	I/O	K4	I/O
A4	I/O	C5	I/O	G1	I/O	K5	GND
A5	INPUT	C6	INPUT	G2	VCC	K6	INPUT
A6	INPUT/CLK	C7	INPUT	G3	I/O	K7	VCC
A7	GND	C10	I/O	G9	I/O	K8	I/O
A8	I/O	C11	I/O	G10	GND	K9	I/O
A9	I/O	D1	I/O	G11	GND	K10	I/O
A10	I/O	D2	I/O	H1	I/O	K11	I/O
A11	I/O	D10	I/O	H2	I/O	L1	I/O
B1	I/O	D11	I/O	H10	I/O	L2	I/O
B2	I/O	E1	GND	H11	I/O	L3	I/O
B3	I/O	E2	GND	J1	I/O	L4	I/O
B4	I/O	E3	I/O	J2	I/O	L5	GND
B5	VCC	E9	I/O	J5	I/O	L6	I/O
B6	I/O	E10	VCC	J6	INPUT	L7	INPUT
B7	GND	E11	I/O	J7	INPUT	L8	I/O
B8	I/O	F1	I/O	J10	I/O	L9	I/O
B9	I/O	F2	I/O	J11	I/O	L10	I/O
B10	I/O	F3	I/O	K1	I/O	L11	I/O