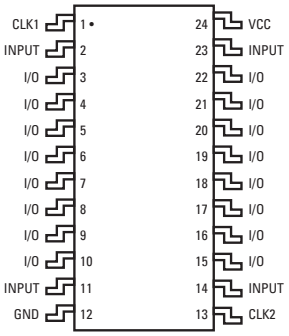
Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 100 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 Clock pins
- The following devices are pin-, function-, and programming file-compatible: EP610, EP610I, EP610T, EP610-XX/B, EP600I, and PALCE610
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 1):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

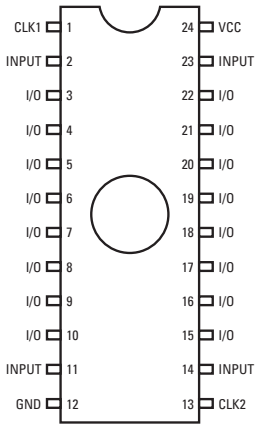
Figure 1. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



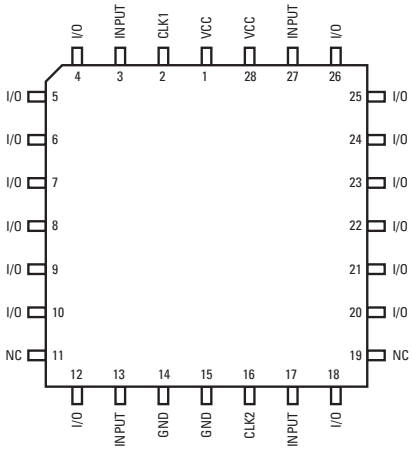
24-Pin SOIC

EP610
EP610T



24-Pin DIP

EP610
EP610T
EP610-XX/B
EP610I



28-Pin J-Lead

EP610
EP610T
EP610I

For complete Rochester ordering guide, please refer to page 2
Please contact factory for specific package availability and Military/Aerospace specifications/availability.

Rochester Ordering Guide

**Most products can also be offered as RoHS compliant, designated by a –G suffix. Please contact factory for more information.*

Rochester Part Number	Altera Part Number	Package	Temperature
EP610DC-25	EP610DC-25	CDIP-24	0° to +70°C
EP610DC-30	EP610DC-30	CDIP-24	0° to +70°C
EP610DC-35	EP610DC-35	CDIP-24	0° to +70°C
EP610DI-30	EP610DI-30	CDIP-24	-40° to +85°C
EP610DI-35	EP610DI-35	CDIP-24	-40° to +85°C
EP610DM-35	EP610DM-35	CDIP-24	-55° to +125°C
EP610DM/B	EP610DM883B	CDIP-24	-55° to +125°C
EP610JC-25	EP610JC-25	LDCC-28, Ceramic	0° to +70°C
EP610JC-30	EP610JC-30	LDCC-28, Ceramic	0° to +70°C
EP610JC-35	EP610JC-35	LDCC-28, Ceramic	0° to +70°C
EP610JI-30	EP610JI-30	LDCC-28, Ceramic	-40° to +85°C
EP610JI-35	EP610JI-35	LDCC-28, Ceramic	-40° to +85°C
EP610JM-35	EP610JM-35	LDCC-28, Ceramic	-55° to +125°C
EP610JM-40	EP610JM-40	LDCC-28, Ceramic	-55° to +125°C
EP610LC-15	EP610LC-15	LDCC-28, Plastic	0° to +70°C
EP610LC-20	EP610LC-20	LDCC-28, Plastic	0° to +70°C
EP610LC-25	EP610LC-25	LDCC-28, Plastic	0° to +70°C
EP610LC-30	EP610LC-30	LDCC-28, Plastic	0° to +70°C
EP610LI-20	EP610LI-20	LDCC-28, Plastic	-40° to +85°C
EP610LI-30	EP610LI-30	LDCC-28, Plastic	-40° to +85°C
EP610LI-35	EP610LI-35	LDCC-28, Plastic	-40° to +85°C
EP610PC-15	EP610PC-15	PDIP-24	0° to +70°C
EP610PC-20	EP610PC-20	PDIP-24	0° to +70°C
EP610PC-25	EP610PC-25	PDIP-24	0° to +70°C
EP610PC-30	EP610PC-30	PDIP-24	0° to +70°C
EP610PC-35	EP610PC-35	PDIP-24	0° to +70°C
EP610PI-30	EP610PI-30	PDIP-24	-40° to +85°C
EP610PI-35	EP610PI-35	PDIP-24	-40° to +85°C
EP610SC-15	EP610SC-15	SOP-24, Plastic	0° to +70°C
EP610SC-20	EP610SC-20	SOP-24, Plastic	0° to +70°C
EP610SC-25	EP610SC-25	SOP-24, Plastic	0° to +70°C
EP610SC-30	EP610SC-30	SOP-24, Plastic	0° to +70°C

Table 1 summarizes EP610 device features

Table 1. EP610 Device Features

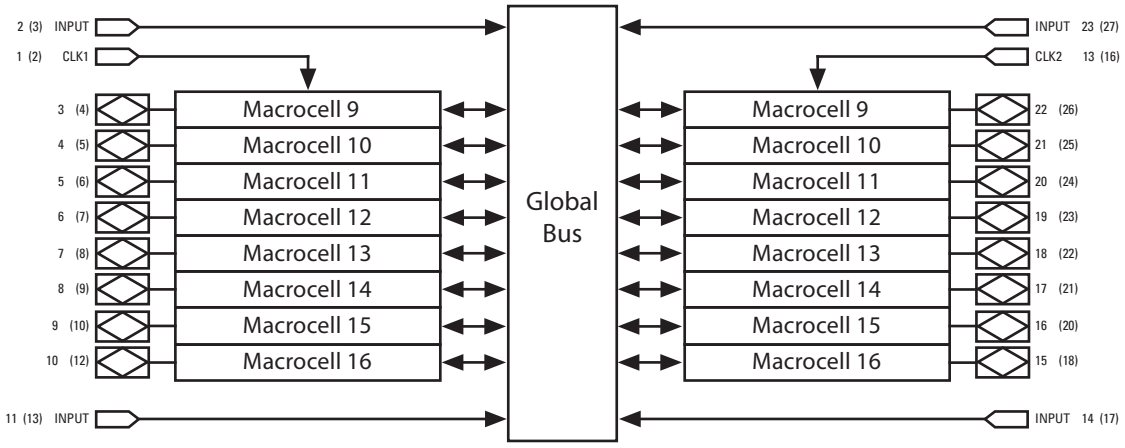
Feature	EP610	EP610T	EP610-XX/B	EP610I
t_{PD}	15 ns	15 ns	35 ns	10 ns
Counter frequency	83 MHz	83 MHz	28.5 MHz	100 MHz
Pipeline data rates	83 MHz	83 MHz	37 MHz	100 MHz
Packages	24-pin SOIC 24-pin CerDIP 24-pin PDIP 24-pin PLCC	24-pin SOIC 24-pin PDIP 28-pin PLCC	24-pin CerDIP	24-pin CerDIP 24-pin PDIP 28-pin PLCC

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global Clock pins (see Figure 2). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true complement forms of either the output of the macrocell of the I/O input. CLK1 is a dedicated Clock input for the registers in macrocells 9 through 16. CLK2 is a dedicated Clock input for registers in macrocells 1 through 8.

Figure 2. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.



Absolute Maximum Ratings

			EP610 EP610T EP610-XX/B		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	-2.0	7.0	V
V_I	DC input voltage		-2.0	7.0	-0.5	V_{CC}+ 0.5	V
I_{MAX}	DC V_{CC} or GND current		-175	175			mA
I_{OUT}	DC output current, per pin		-25	25			mA
P_D	Power dissipation			1000			mW
T_{STG}	Storage temperature	No bias	-65	150	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135 (125)	-10	85	°C
T_J	Junction temperature	Under bias		(150)			°C

Recommended Operating Conditions

			EP610 EP610T EP610-XX/B		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating Temperature	For commerical use	0	70	0	70	°C
T_A	Operating Temperature	For industrial use	-40	85	-40	85	°C
T_C	Case Temperature	For military use	-55	125			°C
t_R	Input rise time			100 (50)		500	ns
t_F	Input fall time			100 (50)		500	ns

Recommended Operating Conditions

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = -4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = -2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage output	V_I = V_{CC} or GND	-10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	-10		10	µA

Capacitance

			EP610 EP610T		EP610-XX/B		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		12	pF

I_{CC} Supply Current: EP610 & EP610T

				EP610			EP610T			
Symbol	**Parameter**	**Conditions**	**Speed Grade**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load			20	150				µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz			5	10 (15)				mA
I_{CC3}	V_{CC} supply current (turbo, active)		-15, -20		60	90 (115)		60	90	mA
			-25, -30, -35		45	60 (75)		60	90	mA

I_{CC} Supply Current: EP610-XX/B & EP610I

			EP610-XX/B			EP610I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load			900		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz			25		3	8	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz			140		65	105	mA

AC Operating Conditions: EP610-15 & EP610-20

			EP610-15 EP610-15T		EP610-20 EP610-20T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**		**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17		22	20	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns
f_{MAX}	Maximum clock frequency		83.3		62.5		0	MHz
t_{SU}	Global clock input setup time		9		11		20	ns
t_{H}	Global clock input hold time		0		0		0	ns
t_{CH}	Global clock high time		6		8		0	ns
t_{CL}	Global clock low time		6		8		0	ns
t_{CO1}	Global clock to output delay			11		13	0	ns
t_{CNT}	Global clock minimum period			12		16	0	ns
f_{CNT}	Global clock internal maximum frequency		83.3		62.5		0	MHz
t_{ASU}	Array clock input setup time		6		8		20	ns
t_{AH}	Array clock input hold time		6		8		0	ns
t_{ACH}	Array clock high time		7		9		0	ns
t_{ACL}	Array clock low time		7		9		0	ns
t_{ACO1}	Array clock to output delay			15		20	20	ns
t_{ACNT}	Array clock minimum period			14		18	0	ns
f_{ACNT}	Array clock internal maximum frequency		71.4		55.6		0	MHz

AC Operating Conditions: EP610-15 & EP610-20 *Note (1)*

			EP610-25 EP610-25T		EP610-20 EP610-20T		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *Note (2)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns
f_{MAX}	Maximum clock frequency	*Note (3)*	47.6		41.7		37.0		0	MHz
t_{SU}	Global clock input setup time		21		24		27		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		10		11		12		0	ns
t_{CL}	Global clock low time		10		11		12		0	ns
t_{CO1}	Global clock to output delay			15		17		20	0	ns
t_{CNT}	Global clock minimum period			25		30		35	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (4)*	40.0		33.3		28.6		0	MHz
t_{ASU}	Array clock input setup time		8		8		8		30	ns
t_{AH}	Array clock input hold time		12		12		12		0	ns
t_{ACH}	Array clock high time		10		11		12		0	ns
t_{ACL}	Array clock low time		10		11		12		0	ns
t_{ACO1}	Array clock to output delay			27		32		37	30	ns
t_{ACNT}	Array clock minimum period			25		30		35	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (4)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = -40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = -55° C to 125° C for military use.

(2) Sample-tested only for an output change of 500 mV.

(3) The f_{MAX} values represent the highest frequency for pipelined data.

(4) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.

AC Operating Conditions: EP610-XX/B *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF *Notes (2), (3)*		35	ns
t_{PD2}	I/O input to non-registered output			37	ns
t_{PZX}	Input to output enable			35	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *Notes (2), (3), (4), (5)*		35	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF *Notes (2), (3)*		37	ns
f_{MAX}	Maximum clock frequency	*Note (2), (6), (7)*	37.0		MHz
t_{SU}	Global clock input setup time	*Note (2), (3)*	27		ns
t_H	Global clock input hold time	*Note (3)*	0		ns
t_{CH}	Global clock high time	*Note (4)*	12		ns
t_{CL}	Global clock low time	*Note (4)*	12		ns
t_{CO1}	Global clock to output delay			20	ns
t_{CNT}	Global clock minimum period	*Note (4), (8)*		35	ns
f_{CNT}	Global clock internal maximum frequency	*Note (8)*	28.5		MHz
t_{ASU}	Array clock input setup time	*Notes (2), (3), (4)*	8		ns
t_{AH}	Array clock input hold time	*Notes (2), (3), (4)*	12		ns
t_{ACH}	Array clock high time	*Notes (3), (4)*	12		ns
t_{ACL}	Array clock low time	*Notes (3), (4)*	12		ns
t_{ACO1}	Array clock to output delay	*Notes (2), (3)*		37	ns
t_{ACNT}	Array clock minimum period	*Notes (4), (8)*		35	ns
f_{ACNT}	Array clock internal maximum frequency	*Notes (4), (8)*	28.6		MHz

Notes to tables:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: V_{CC} = 5 V ± 10%, T_C = -55° C to 125° C for military use.

*(2) All array-dependent delays are specified for an **XOR** pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM cell. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an **XOR** pattern in which only one pure input switches at a time.*

(3) When the Turbo Bit is not set (non-turbo mode), a non-turbo adder of 30 ns (maximum) is added to this parameter to determine worst-case timing. Parameters may not be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.

(4) These parameters may not be tested, but are guaranteed to the limits specified in the table under "Absolute Maximum Ratings" on page 3.

(5) Not tested directly, but guaranteed by testing t_{PD}.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) Not tested directly, but derived from t_{SU}.

(8) Specified with device programmed as a 16-bit counter with no output loading.

AC Operating Conditions: EP610I *Note (1)*

		EP610I-10		EP610I-15		EP610I-25		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		**Unit**
t_{PD1}	Input to non-registered output, *Note (2)*		10		15		25	25	ns
t_{PD2}	I/O input to non-registered output, *Note (2)*		10		15		25	25	ns
t_{PZX}	Input to output enable		15		18		25	25	ns
t_{PXZ}	Input to output disable, *Note (3)*		13		18		25	25	ns
t_{CLR}	Asynchronous output clear time		13		18		25	25	ns
f_{MAX}	Maximum clock frequency	111		83.3		66		0	MHz
t_{SU}	Global clock input setup time	7		12		15		25	ns
t_H	Global clock input hold time	0		0		0		0	ns
t_{CH}	Global clock high time	5		6		7.5		0	ns
t_{CL}	Global clock low time	5		6		7.5		0	ns
t_{CO1}	Global clock to output delay		6.5		8		10	0	ns
t_{CNT}	Global clock minimum period		10		15		25	25	ns
f_{CNT}	Global clock internal maximum frequency, *Note (4)*	100		66		40		0	MHz
t_{ASU}	Array clock input setup time	2		4		5		25	ns
t_{AH}	Array clock input hold time	3		6		8		0	ns
t_{ACH}	Array clock high time	5		7.5		10		0	ns
t_{ACL}	Array clock low time	5		7.5		10		0	ns
t_{ACO1}	Array clock to output delay		12		16		25	25	ns
t_{ACNT}	Array clock minimum period, *Note (4)*		10		15		25	25	ns
f_{ACNT}	Array clock internal maximum frequency, *Note (4)*	100		66		40		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) Measured with eight outputs switching.

(3) Sample-tested only for an output change of 500 mV.

(4) Measured with a device programmed as a 16-bit counter.