Enpirion® Power Datasheet

EN5337QI 3A PowerSoC Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor

Description

The EN5337QI is a Power Supply on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, all small-signal circuits, compensation, and the inductor in an advanced 4mm x 7mm QFN package.

The EN5337QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards, and system level applications in distributed power architectures. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

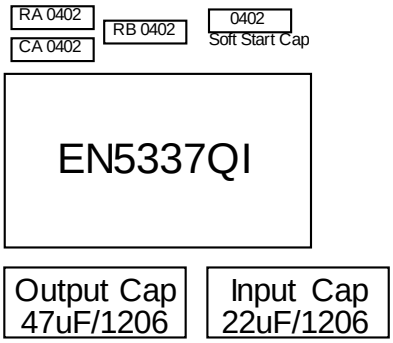


Figure 1: Total Solution Footprint (Not to scale)
Total Area ≈ 75 mm²

Features

- Integrated Inductor, MOSFETS, Controller
- Total Power Solution ≈ 75mm²
- Minimal external components.
- 3A Continuous Output Current Capability
- 5MHz operating frequency. Switching frequency can be phase locked to an external clock.
- High efficiency, up to 92%.
- Wide input voltage range of 2.375V to 5.5V.
- Output Enable pin and Power OK signal.
- Programmable soft-start time.
- Under Voltage Lockout, Over Current, Short Circuit and Thermal Protection.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Noise sensitive applications such as A/V, RF and Gbit I/O
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- Computing, Networking, DSL, STB, DVR, DTV, iPC
- Ripple sensitive applications
- Beat frequency sensitive applications

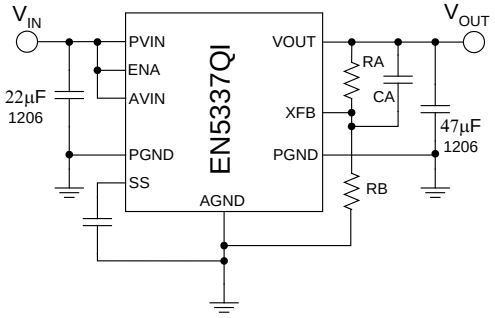


Figure 2: Typical Application Schematic

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5337QI	-40 to +85	38-pin QFN T&R
EVB-EN5337QI	QFN Evaluation Board	

Pin Assignments (Top View)

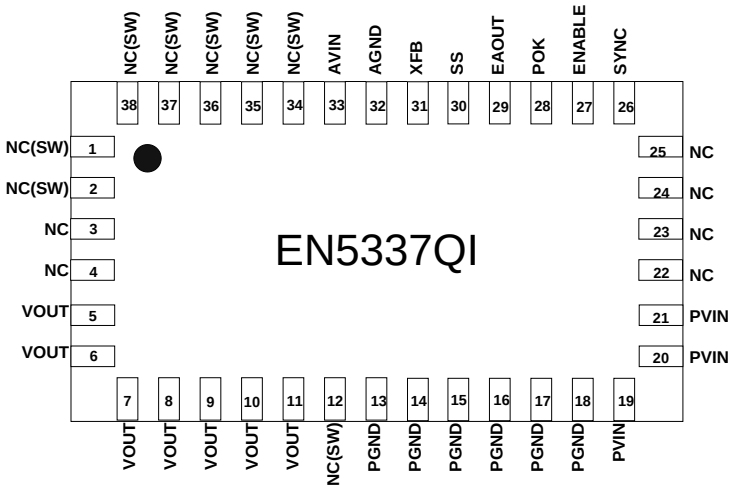


Figure 3: Pinout Diagram (Top View)
NOTE: All perimeter pins must be soldered to PCB.

Pin Description

PIN	NAME	FUNCTION
1-2, 12, 34-38	NC(SW)	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
3-4, 22-25	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
5-11	VOUT	Regulated converter output. Connect these pins to the load, and place output capacitor from these pins and PGND pins 13-15
13-18	PGND	Input/Output power ground. Connect these pins to the ground electrode of the Input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
19-21	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 16-18.
26	SYNC	External Clock Input to synchronize internal switching clock to an external signal
27	ENABLE	Input Enable. Applying logic high enables the output and initiates a soft-start. Applying a logic low disables the output.
28	POK	Power OK is an open drain transistor for power system state indication. POK will be logic high when VOUT is with -10% to +20% of VOUT nominal.
29	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop response.
30	SS	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.
31	XFB	External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid point of the divider is connected to XFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.
32	AGND	Analog Ground. This is the Ground return for the controller. Needs to be connected to a quiet ground.
33	AVIN	Input power supply for the controller. Needs to be connected to input voltage at a quiet point.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on PVIN, AVIN, VOUT	V_{IN}	-0.5	6.0	V
Voltages on Enable, POK		-0.5	V_{IN}	V
Voltages on XFB, EAOUT, SYNC, SS		-0.5	2.5	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating – User pins (based on HBM)			2000	V
ESD Rating - NC pins (based on HBM)			1000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.375	5.5	V
Output Voltage Range	V_{OUT}	0.60	$V_{IN} - V_{DO}$ †	V
Output Current	I_{LOAD}	0	3	A
Operating Junction Temperature	$T_{J\text{-}OP}$	- 40	125	°C
Operating Ambient Temperature	T_{AMB}	- 40	85	°C

† V_{DO} (drop-out voltage) is defined as (I_{LOAD} x Dropout Resistance). Please see Electrical Characteristics table.

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Thermal Shutdown	T_{SD}		150		°C
Thermal Shutdown Hysteresis	T_{SDH}		20		°C
Thermal Resistance: Junction to Ambient (**Note 1**)	θ_{JA}		30		°C/W
Thermal Resistance: Junction to Case	θ_{JC}		3		°C/W

Note 1: Based on a four layer copper board and proper thermal design in line with JEDEC EIJ/JESD51 standards

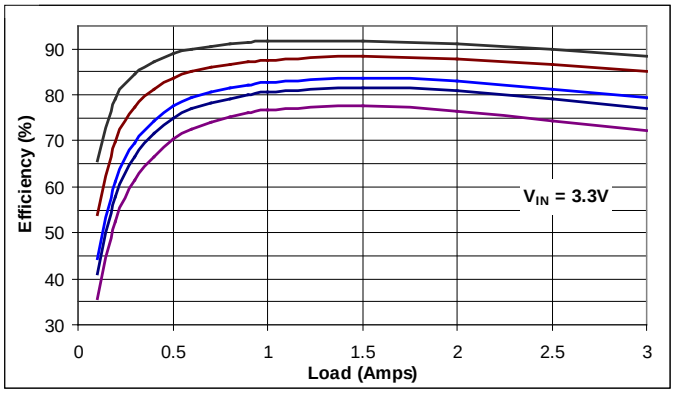
Electrical Characteristics

NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted. Typical values are at TA = 25°C.

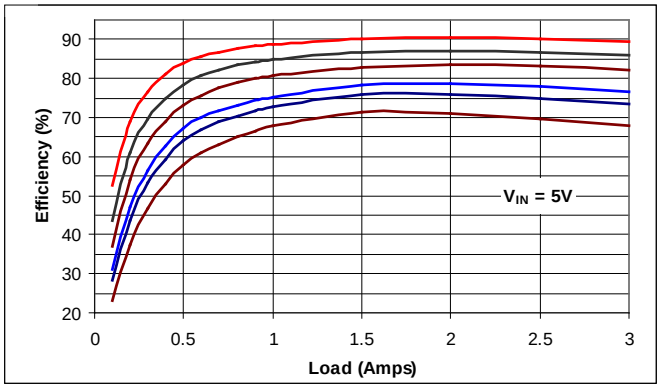
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.375		5.5	V
Under Voltage Lock-out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.2		V
Under Voltage Lock-out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted		2.1		V
Shut-Down Supply Current	I_S	ENABLE=0V		100		µA
Feedback Pin Voltage	V_{XFB}	Feedback node voltage – factory setting – T_A = 25°C	0.735	0.75	0.765	V
Feedback pin Input Leakage Current [1]	I_{XFB}	XFB pin input leakage current	-5		5	nA
Line Regulation	ΔV_{OUT_LINE}	2.375V ≤ V_{IN} ≤ 5.5V		0.02		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ I_{LOAD} ≤ 3A		-0.03		%/A
Temperature Regulation	ΔV_{OUT_TEMP}	-40°C ≤ TEMP ≤ 85°C		0.003		%/°C
V_{OUT} Rise Time	t_{RISE}	Measured from when V_{IN} ≥ V_{UVLOR} & ENABLE pin voltage crosses logic high threshold. (4.7nF ≤ C_{SS} ≤ 100nF)		C_{SS} x 67 kΩ		
Rise Time Accuracy [1]	ΔT_{RISE}	4.7nF ≤ C_{SS} ≤ 100nF	-25		+25	%
Output Drop Out Voltage Resistance [1]	V_{DO} R_{DO}	V_{INMIN} - V_{OUT} at Full load Input to Output Resistance		250 83	500 167	mV mΩ
Maximum Continuous Output Current	$I_{OUT\_Max\_Cont}$		3			A
Over Current Trip Level	I_{OCP}			4.5		A
Disable Threshold	$V_{DISABLE}$	ENABLE pin logic low.	0.0		0.8	V
ENABLE Threshold	V_{ENABLE}	ENABLE pin logic high 2.375V ≤ V_{IN} ≤ 5.5V	1.8		V_{IN}	V
ENABLE Lock-out time	T_{ENLO}	Time for device to re-enable after a falling edge on ENABLE pin		700		µS
ENABLE pin Input Current [1]	I_{ENABLE}	ENABLE pin has ~80kΩ pull down			70	µA
Switching Frequency (Free Running)	F_{SW}	Free Running frequency of oscillator		5		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency	4.5		5.5	MHz
SYNC Input Threshold – Low	V_{SYNC_LO}	SYNC Clock Logic Level			0.8	V
SYNC Input Threshold – High	V_{SYNC_HI}	SYNC Clock Logic Level	1.8		2.5	V
POK Threshold	POK_{TH}	Output voltage as a fraction of expected output voltage		90		%
POK Output Low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	2.375V ≤ V_{IN} ≤ 5.5V			V_{IN}	V
POK pin V_{OH} Leakage Current [1]	I_{POKL}	POK high			1	µA

Note 1: Parameter guaranteed by design

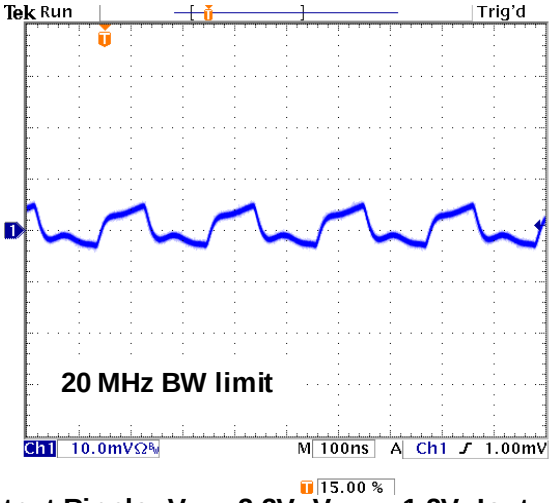
Typical Performance Characteristics



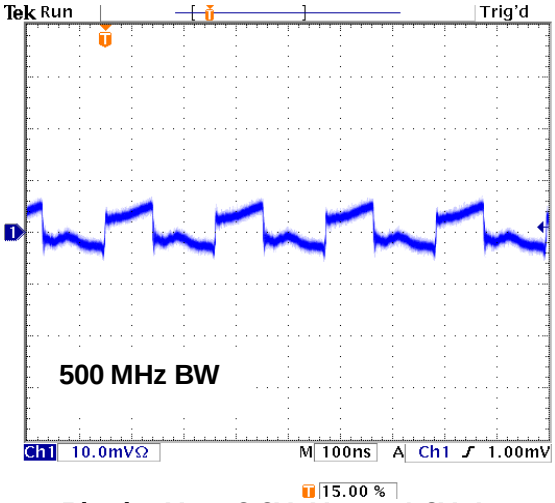
Efficiency V_{IN} = 3.3V
V_{OUT} (From top to bottom) = 2.5, 1.8, 1.2, 1.0, 0.75V



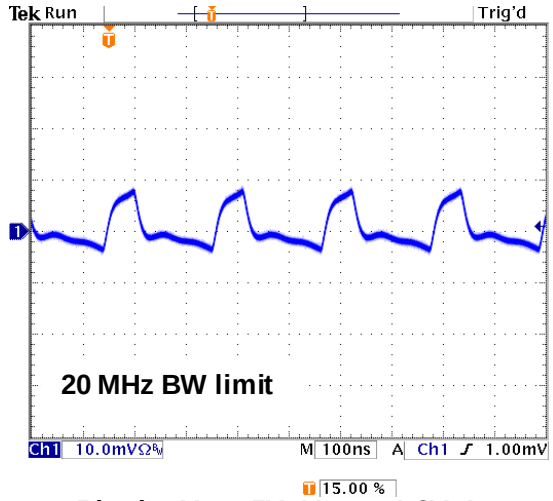
Efficiency V_{IN} = 5.0V
V_{OUT} (From top to bottom) = 3.3, 2.5, 1.8, 1.2, 1.0, 0.75V



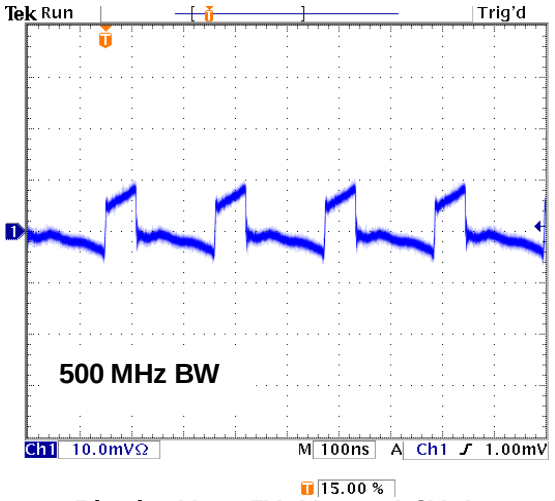
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, Iout = 3A
C_{IN} = 22µF, C_{OUT} = 47µF/1206 + 10uF/0805



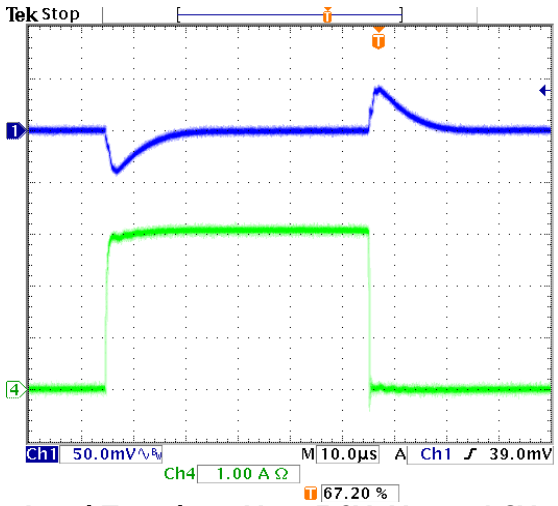
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, Iout = 3A
C_{IN} = 22µF, C_{OUT} = 47µF/1206 + 10uF/0805



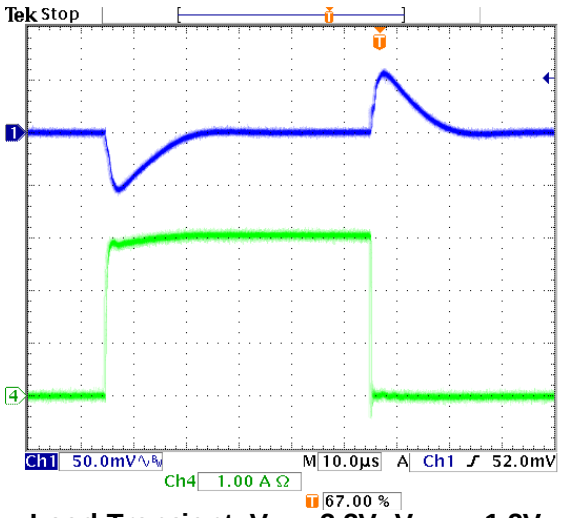
Output Ripple: V_{IN} = 5V, V_{OUT} = 1.2V, Iout = 3A
C_{IN} = 22µF, C_{OUT} = 47µF/1206 + 10uF/0805



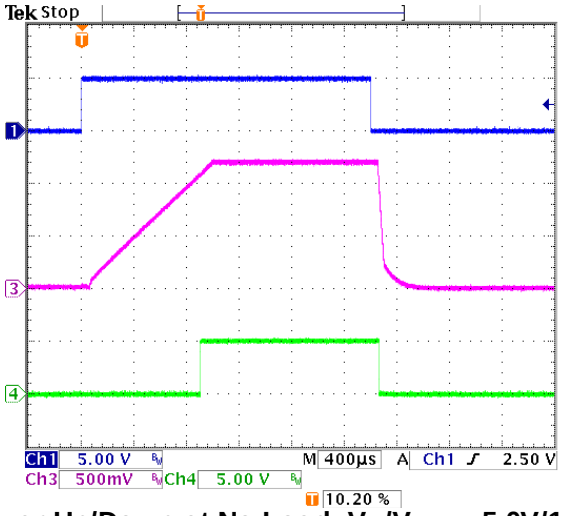
Output Ripple: V_{IN} = 5V, V_{OUT} = 1.2V, Iout = 3A
C_{IN} = 22µF, C_{OUT} = 47µF/1206 + 10uF/0805



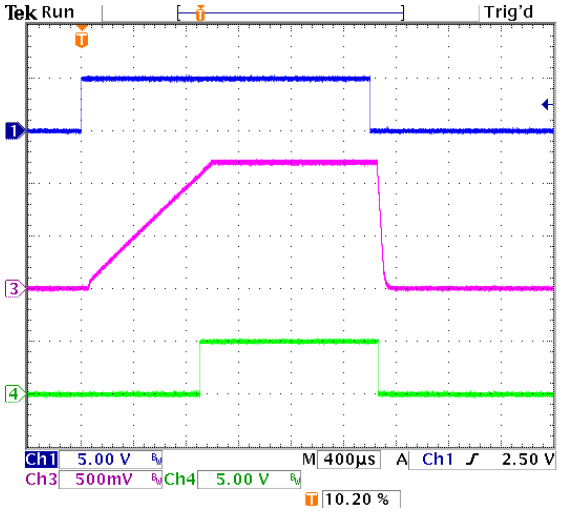
Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.2V
Ch.1: V_{OUT}, Ch.4: I_{LOAD} (slew rate ≥ 10A/µS)
C_{IN} = 22µF, C_{OUT} ≈ 50µF



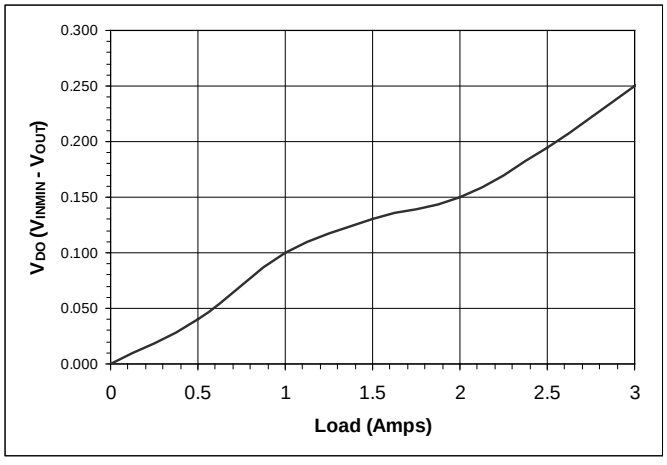
Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.2V
Ch.1: V_{OUT}, Ch.4: I_{LOAD} (slew rate ≥ 10A/µS)
C_{IN} = 22µF, C_{OUT} ≈ 50µF



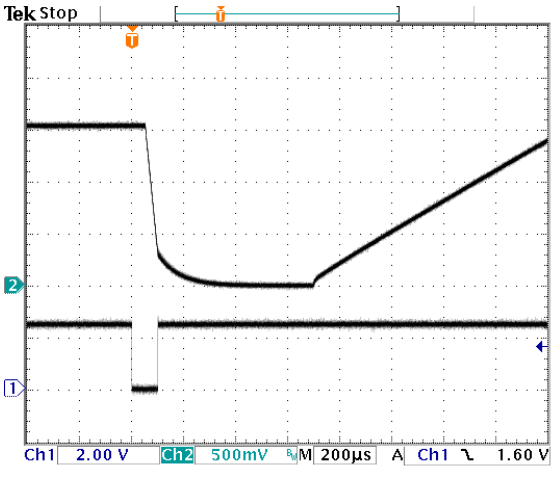
Power Up/Down at No Load: V_{IN}/V_{OUT} = 5.0V/1.2V,
15nF soft-start capacitor,
Ch.1: ENABLE, Ch.3: V_{OUT}, Ch.4; POK



Power Up/Down into 0.4Ω load: V_{IN}/V_{OUT} = 5.0V/1.2V,
15nF soft-start capacitor,
Ch.1: ENABLE, Ch.3: V_{OUT}, Ch.4; POK



Drop-Out Voltage



Enable Lock-out Time,
Ch.1: ENABLE, Ch. 2: V_{OUT}

Functional Block Diagram

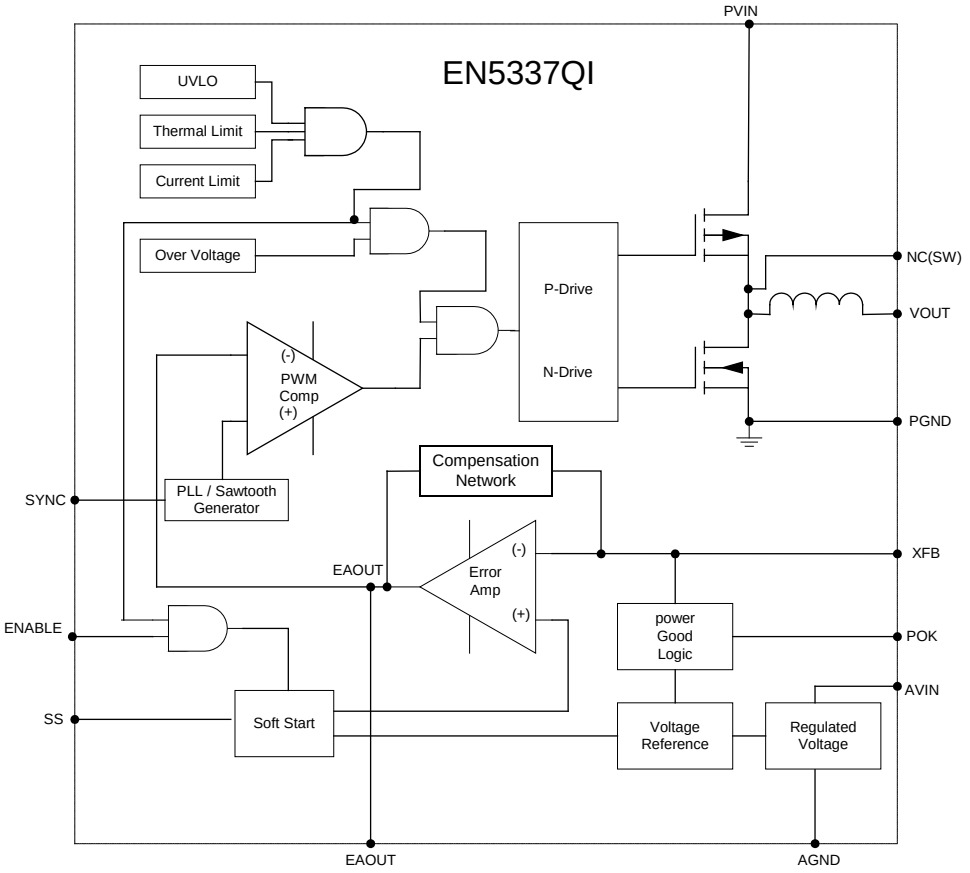


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EN5337QI is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.375V to 5.5V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the type III compensation network. The device uses a low-noise PWM topology. Up to 3A of continuous output current can be drawn from this converter. The 5MHz switching frequency allows the use of small size input / output capacitors, and realizes a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional Features:

- The switching frequency can be phase-locked to an external clock to eliminate or move beat frequency tones out of band.
- Soft-start circuit, limiting the in-rush current when the converter is initially powered up. The soft start time is programmable with appropriate choice of soft start capacitor value.

- Power good circuit indicating the output voltage is between 90% and 120% of programmed value as long as the feedback loop is closed.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. Applying logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The device will remain shut-down for the duration of the ENABLE lockout time (see Electrical Characteristics Table). If the ENABLE signal is re-asserted during this time, the device will power up with a normal soft-start at the end of the ENABLE lockout time.

Pre-Bias Start-up

The EN5337QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EN5337QI is not pre-biased when the EN5337QI is first enabled.

Frequency Synchronization

The switching frequency of the DC/DC converter can be phase-locked to an external clock source to move unwanted beat frequencies out of band. To avail this feature, the clock source should be connected to the SYNC pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 4.5 to 5.5 MHz. When no clock signal is present, the device reverts to the free running frequency of the internal oscillator.

Spread Spectrum Mode

The external clock frequency may be swept between 4.5 MHz and 5.5 MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Soft-Start Operation

Soft start is a means to reduce the in-rush current when the device is enabled. The output voltage is ramped up gradually upon start-up. The output rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 30) and the AGND pin (pin 32).

$$\text{Rise Time: } T_R \approx (C_{ss} * 67k\Omega) \pm 25\%$$

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10uA. The soft start capacitor should be between 4.7nF and 100nf. Typical soft-start rise time is ~1mS with SS capacitor value of 15nF. The rise time is measured from when $V_{IN} \geq V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to V_{IN} or similar voltage) from the converter indicating the output voltage is within the specified range. The POK signal will be logic high (V_{IN}) when the output voltage is above 90% of programmed V_{OUT}. If the output voltage goes below this threshold, the POK signal will be at logic low.

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the Power PFET. When the sensed current exceeds the over current trip point, both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed,

the over-current protection circuit will enable normal PWM operation. If the over-current condition persists, the soft start capacitor will gradually discharge causing the output voltage to fall. When the OCP fault is removed, the output voltage will ramp back up to the desired voltage. This circuit is designed to provide high noise immunity.

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the Junction temperature exceeds approximately 150ºC. After a thermal shutdown event, when the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis, input de-glitch, and output leading edge blanking ensure high noise immunity and prevent false UVLO triggers.

Compensation

The EN5337QI uses a type 3 compensation network. A piece of the compensation circuit is the phase lead capacitor C_A in Figure 5. This network will provide wide loop bandwidth and excellent transient performance for most applications. It is optimized for use with about 50µF of output filter capacitance at the voltage sensing point. Additional load decoupling capacitance may be placed beyond the voltage sensing point outside the control loop. Voltage mode operation provides high noise immunity at light load, and low output impedance.

In some applications modifications to the compensation may be required. For more information, contact Power Applications support.

Application Information

The EN5337QI output voltage is determined by the voltage presented at the XFB pin. This voltage is set by way of a resistor divider between V_{OUT} and AGND with the midpoint going to XFB. A phase lead capacitor C_A is also required for stabilizing the loop. Figure 5 shows the required components and the equations to calculate the values.

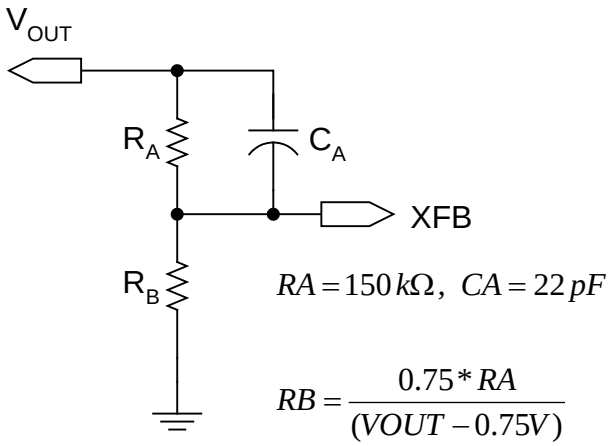


Figure 5: V_{OUT} Resistor Divider Network and Compensation Capacitor C_A

Input Capacitor Selection

The EN5337QI requires between 10uF and 20uF of input capacitance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors

Description	MFG	P/N
10uF, 10V, 10% X7R, 1206 (1-2 capacitors needed)	Murata	GRM31CR71A106KA01L
	Taiyo Yuden	LMK316B7106KL-T
22uF, 10V, 20% X5R, 1206 (1 capacitor needed)	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T

Output Capacitor Selection

The EN5337QI has been optimized for use with approximately 50µF of output filter capacitance at the voltage sensing point

Additional load decoupling capacitance may be placed beyond the voltage sensing point outside the control loop. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

$$Z = ESR + ESL$$

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5335QI Evaluation Board)
1 x 47 uF	30
47 uF + 10 uF	15

Recommended Output Capacitors

Description	MFG	P/N
47uF, 6.3V, 20% X5R, 1206 (1 capacitor needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK212BJ476ML-T
10uF, 6.3V, 10% X5R, 0805 (Optional 1 capacitor in parallel with 47uF above)	Murata	GRM21BR60J106KE19L
	Taiyo Yuden	JMK212BJ106KG-T

Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements.

Thermal Considerations

The Altera Enpirion EN5337QI DC-DC converter is packaged in a 7 x 4 x 1.85mm 38-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C will reduce long-term reliability. The device has a thermal overload protection circuit designed to shut it off at an approximate junction temperature value of 150°C.

The silicon is mounted on a copper thermal pad that is exposed at the bottom of the package. The thermal resistance from the silicon to the exposed thermal pad is very low. In order to take advantage of this low resistance, the exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB). The PCB then acts as a heat sink. In order for the PCB to be an effective heat sink, the device thermal pad should be coupled to copper ground planes or special heat sink structures designed into the PCB (refer to the recommendations at the end of this note).

The junction temperature, T_J, is calculated from the ambient temperature, T_A, the device power dissipation, P_D, and the device junction-to-ambient thermal resistance, θ_{JA} in °C/W::

$$T_J = T_A + (P_D)(\theta_{JA})$$

The junction temperature, T_J, can also be expressed in terms of the device case temperature, T_C, and the device junction-to-case thermal resistance, θ_{JC} in °C/W, as follows:

$$T_J = T_C + (P_D)(\theta_{JC})$$

The device case temperature, T_C, is the temperature at the center of the exposed thermal pad at the bottom of the package.

The device junction-to-ambient and junction-to-case thermal resistances, θ_{JA} and θ_{JC}, are shown in the Thermal Characteristics table on page 3. The θ_{JC} is a function of the device and the 38-pin QFN package design. The θ_{JA} is a function of θ_{JC} and the user's system design parameters that include the thermal effectiveness of the customer PCB and airflow.

The θ_{JA} value shown in the Thermal Characteristics table on page 3 is for free convection with the device heat sunk (through the thermal pad) to a copper plated four-layer PC board with a full ground and a full power plane following JEDEC EIJ/JESD 51 Standards. The θ_{JA} can be reduced with the use of forced air convection. Because of the strong dependence on the thermal effectiveness of the PCB and the system design, the actual θ_{JA} value will be a function of the specific application.

Layout Recommendation

Figure 6 shows critical components and layer 1 traces of a recommended minimum footprint EN5337QI layout with ENABLE tied to V_{IN} in PWM mode. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.altera.com/enpirion for exact dimensions and other layers. Please refer to this Figure while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5337QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5337QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Three PGND pins are dedicated to the input circuit, and three to the output circuit. The slit in Figure 6 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.altera.com/enpirion.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.

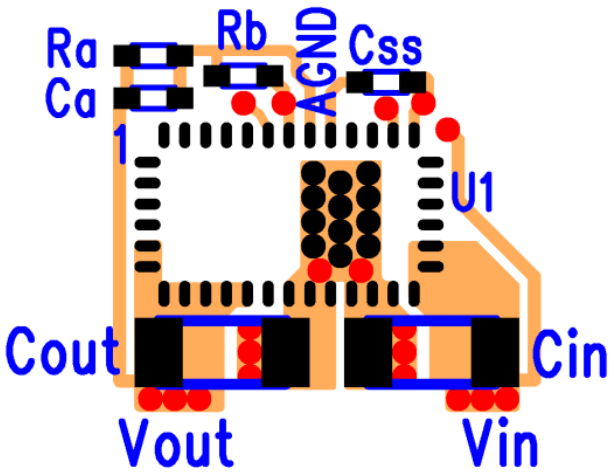


Figure 6: Top PCB Layer Critical Components and Copper for Minimum Footprint

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figures: 7, 8, and 9.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 6. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 6 this connection is made at the input capacitor close to the V_{IN} connection.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 6. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 9: Keep R_A, C_A, and R_B close to the VFB pin (see Figures 6 and 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Design Considerations

Exposed Metal on Bottom of Package

Lead frames offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5337QI should be clear of any metal except for the large thermal pad and the perimeter pads. The "grayed-out" area in Figure 7 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

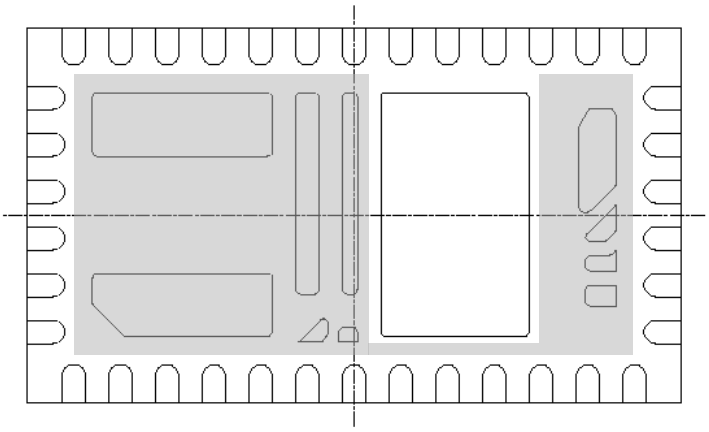


Figure 7: Lead-Frame Exposed Metal (package bottom view). Grey area highlights exposed metal below which there should not be any metal (traces, vias, or planes) on the top layer of PCB.

Recommended PCB Footprint

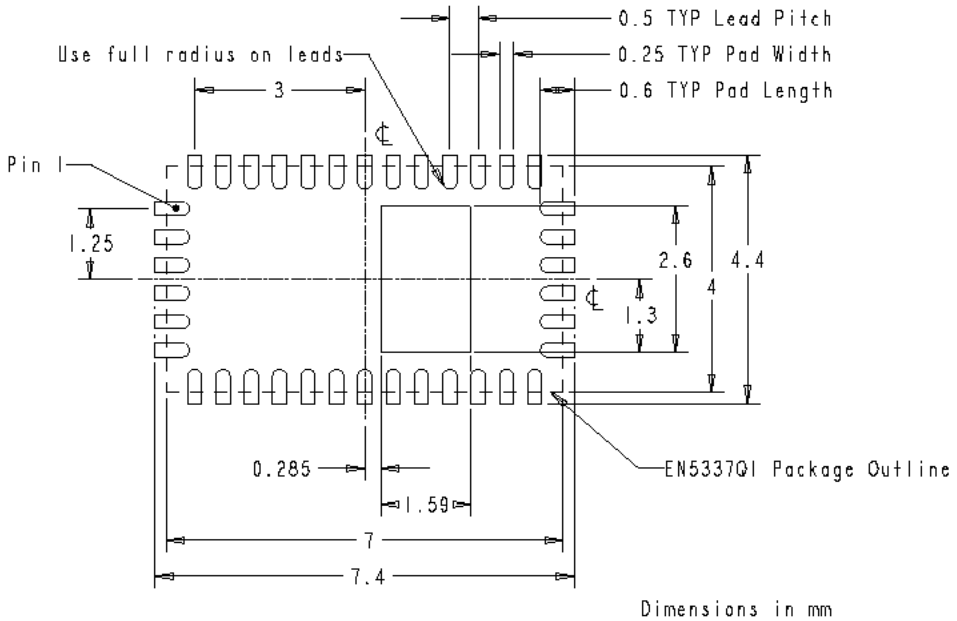


Figure 8: EN5337QI Package PCB Footprint

Package and Mechanical

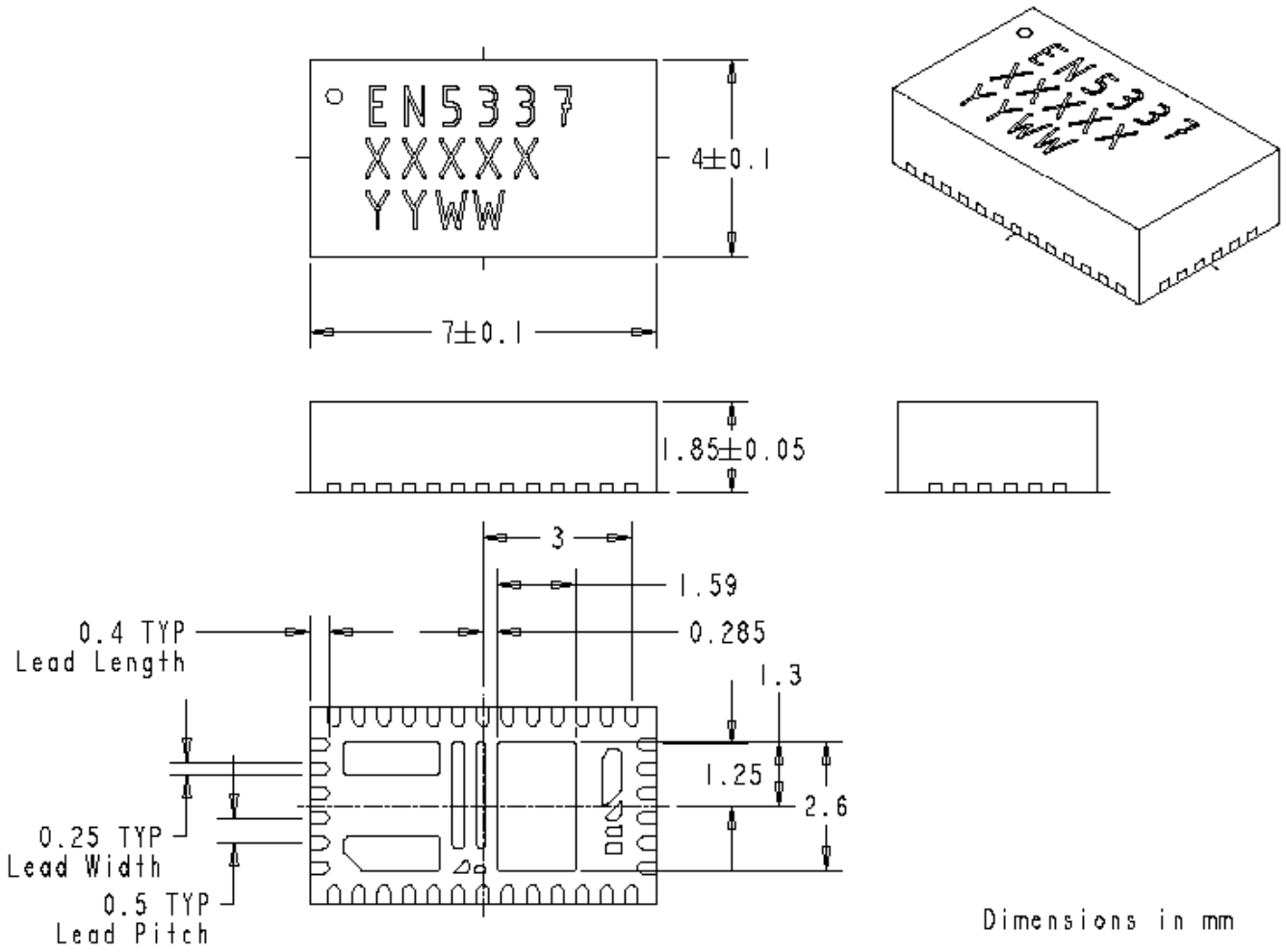


Figure 9: EN5337QI Package Dimensions

Contact Information

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Phone: 408-544-7000
www.altera.com