Enpirion® Power Datasheet
EN2342QI 4A PowerSoC
Voltage Mode Synchronous
PWM Buck with Integrated Inductor

Description

The EN2342QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 8x11x3mm QFN module. It offers high efficiency, excellent line and load regulation over temperature and up to the full 4A load range. The EN2342QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN2342 features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal and over current protection. The device's advanced circuit design, ultra high switching frequency and proprietary integrated inductor technology delivers high-quality, ultra compact, non-isolated DC-DC conversion.

The Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with the Altera Enpirion solution.

All Altera Enpirion products are RoHS compliant, halogen free and are compatible with lead-free manufacturing environments.

Features

- Integrated Inductor, MOSFETs, Controller
- Wide Input Voltage Range: 4.5V – 14V
- Guaranteed 4A I_{OUT} at 85℃ with No Airflow
- Frequency Synchronization (External Clock)
- 1% Initial V_{OUT} Accuracy
- High Efficiency (Up to 95%)
- Output Enable Pin and Power OK signal
- Programmable Soft-Start Time
- Pin Compatible with the EN2340/60/62QI
- Under Voltage Lockout Protection (UVLO)
- Thermal Soft-Shutdown Protection
- Over Current and Short Circuit Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

Applications

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications
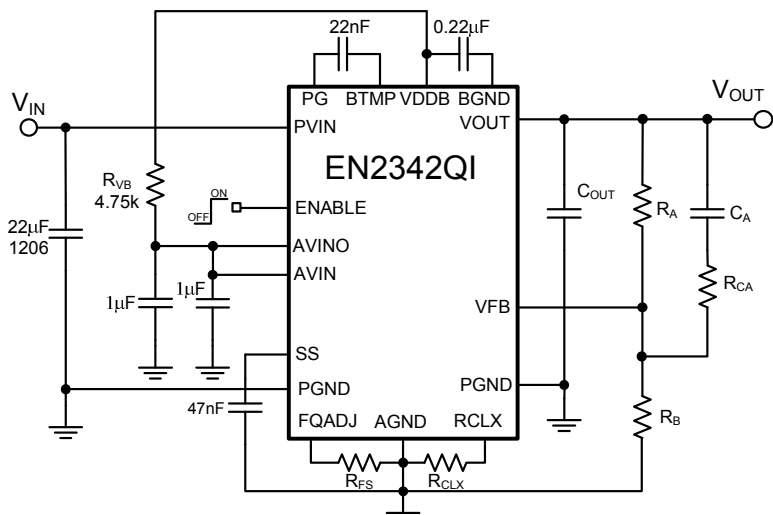

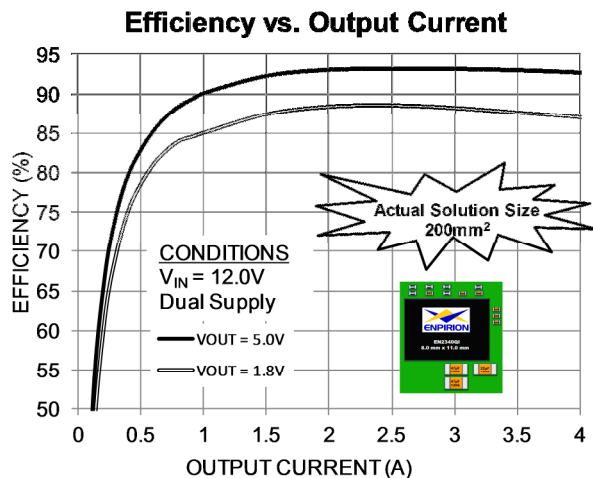**Figure 1.** Simplified Application Circuit

Figure 2. Highest Efficiency in Smallest Solution Size

www.altera.com/enpirion

Ordering Information

Part Number	Package Markings	T$_{AMBIENT}$ Rating (℃)	Package Description
EN2342QI	EN2342QI	-40 to +85	68-pin (8mm x 11mm x 3mm) QFN T&R
EVB-EN2342QI	EN2342QI		QFN Evaluation Board

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
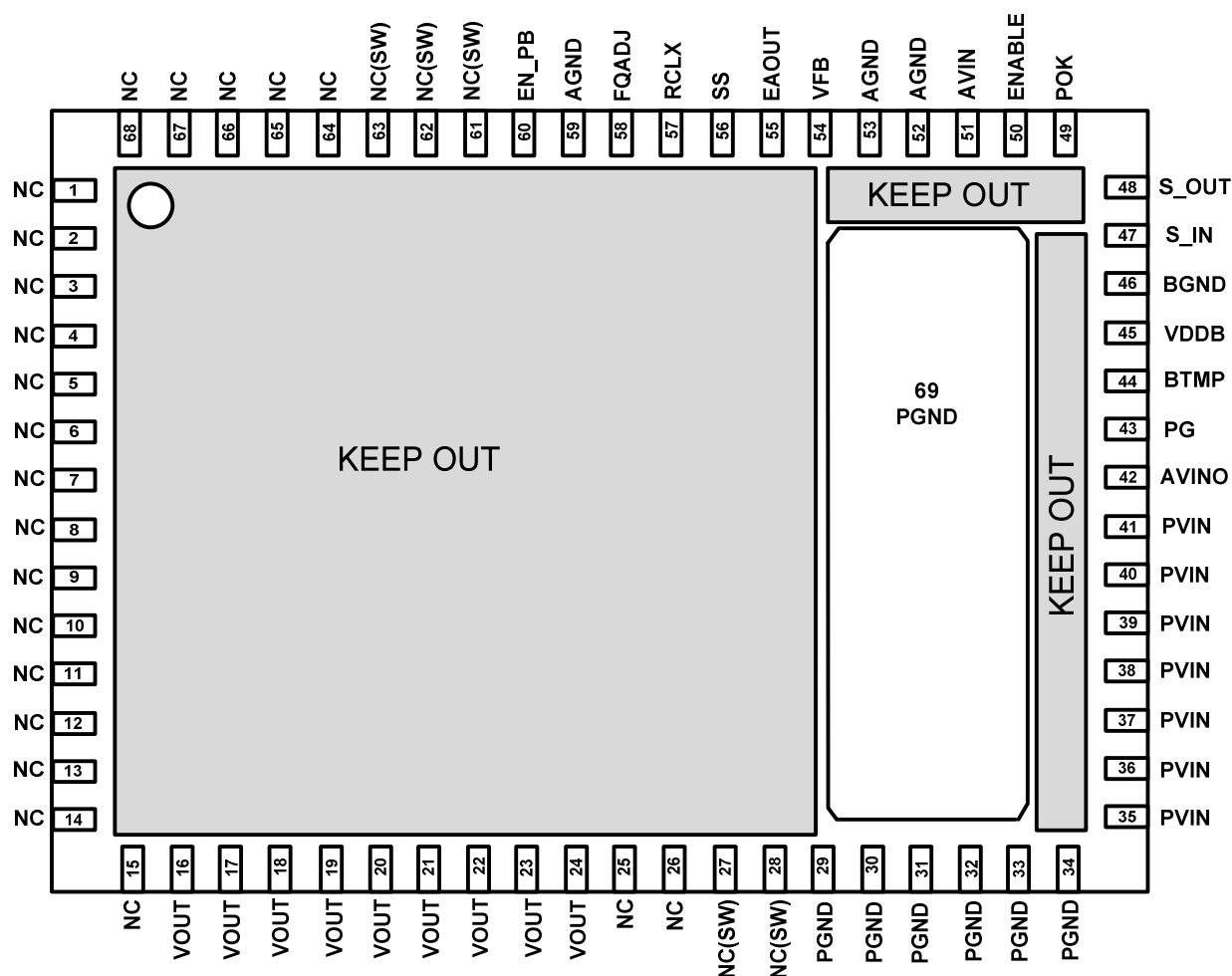
Pin Assignments (Top View)

Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. All pins including NC pins must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 12 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power   G=Ground   NC=No Connect   I=Input O=Output   I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1-15,	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each

PIN	NAME	I/O	FUNCTION
25-26, 59, 64-68			other or to any other electrical signal. Failure to follow this guideline may result in device damage.
16-24	VOUT	O	Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 29-34.
27-28, 61-63	NC(SW)	NC	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
29-34	PGND	G	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
35-41	PVIN	P	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 29-34.
42	AVINO	O	Internal 3.3V linear regulator output. Connect this pin to AVIN (Pin 51) for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO.
43	PG	I/O	PMOS gate. Place a 22nF, X5R/X7R, capacitor between this pin and BTMP.
44	BTMP	I/O	Bottom plate ground. See pin 43 description.
45	VDDB	O	Internal regulated voltage used for the internal control circuitry. Place a 0.22µF, X5R/X7R, capacitor between this pin and BGND.
46	BGND	G	Ground for VDDB. See pin 45 description.
47	S_IN	I	Digital synchronization input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN2342QI. Leave this pin floating if not used.
48	S_OUT	O	Digital synchronization output. PWM signal is output on this pin. Leave this pin floating if not used.
49	POK	O	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal. Leave this pin floating if not used.
50	ENABLE	I	Output enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic low disables the output. ENABLE logic cannot be higher than AVIN (refer to Absolute Maximum Ratings). Do not leave floating.
51	AVIN	P	3.3V Input power supply for the controller. Place a 1µF, X5R/X7R, capacitor between AVIN and AGND.
52, 53, 60	AGND	G	Analog ground. This is the ground return for the controller. All AGND pins need to be connected to a quiet ground.
54	VFB	I/O	External feedback input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead network from this pin to VOUT is also required to stabilize the loop.
55	EAOUT	O	Optional error amplifier output. Allows for customization of the control loop.
56	SS	I/O	Soft-start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.
57	RCLX	I/O	Over-current protection. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table. No current limit protection when this pin is left floating.
58	FQADJ	I/O	Adding a resistor (R_{FS}) to this pin will adjust the switching frequency of the EN2342QI. See Table 1 for suggested resistor values on R_{FS} for various PVIN/VOUT combinations to maximize efficiency. Do not leave floating.
69	PGND		Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on : PVIN, VOUT, PG		-0.5	15	V
Voltages on: ENABLE, POK		-0.3	AV_{IN}+0.3	V
Dual Supply PVIN Rising and Falling Slew Rate (Note 1)			25	V/ms
Single Supply PVIN Rising and Falling Slew Rate (Note 1)			10	V/ms
Pin Voltages – AVINO, AVIN, S_IN, S_OUT		2.5	6.0	V
Pin Voltages – VFB, SS, EAOUT, RCLX, FQADJ, VDDB, BTMP		-0.5	2.75	V
Storage Temperature Range	T_{STG}	-65	150	℃
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	℃
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	℃
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PVIN	4.5	14	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (Note 2)	V_{OUT}	0.75	5	V
Output Current	I_{OUT}		4	A
Operating Ambient Temperature	T_A	-40	+85	℃
Operating Junction Temperature	T_J	-40	+125	℃

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (Note 3)	θ_{JA}	18	℃/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	2	℃/W
Thermal Shutdown	T_{SD}	150	℃
Thermal Shutdown Hysteresis	T_{SDH}	35	℃

Note 1: PVIN rising and falling slew rates cannot be outside of specification. For accurate power up sequencing, use a fast ENABLE logic (>3V/100µs) after both AVIN and PVIN is high.

Note 2: Dropout: Maximum $V_{OUT} \leq V_{IN}$ - 2.5V

Note 3: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: V_{IN}=12V, Minimum and Maximum values are over operating ambient temperature range (-40℃ ≤ T_A ≤ +85℃) unless otherwise noted. Typical values are at T_A = 25℃.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN		4.5		14.0	V
Controller Input Voltage	AVIN		2.5		5.5	V
AVIN UVLO Rising	$AVIN_{UVLOR}$	UVLO is not asserted	2.5	2.75	3	V
AVIN UVLO Falling	$AVIN_{OVLOF}$	UVLO is asserted	2.1	2.35	2.6	V
AVIN UVLO Hysteresis	$AVIN_{HYS}$			400		mV
AVIN Pin Input Current	I_{AVIN}			7	15	mA
Internal LDO Output	AVINO			3.3		V
Shut-Down Supply Current	$IPVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		2		mA
	$IAVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		300		µA
Feedback Pin Voltage	V_{FB}	V_{IN} = 12V, I_{LOAD} = 0, T_A = 25℃ Only	0.7425	0.750	0.7575	V
Feedback Pin Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 14V; 0A ≤ I_{LOAD} ≤ 4A	0.735	0.750	0.765	V
Feedback Pin Input Leakage Current	I_{FB}	VFB pin input leakage current (Note 4)	-5		5	nA
V_{OUT} Rise Time	t_{RISE}	C_{SS} = 47nF (Note 5 and Note 6)		3.2		ms
Soft-Start Capacitor Range	C_{SS_RANGE}		10	47	68	nF
Output Current Range	I_{OUT}		0		4	A
Over Current Trip Level	I_{OCP}	PVIN=12V, V_{OUT}=1.2V	4.15	6		A
Short Circuit Average Input Current	$I_{IN\_AVG\_OCP}$	Short = 10mΩ (Note 7)		100		mA
Disable Threshold	$V_{DISABLE}$	ENABLE pin logic Low	0.0		0.95	V
ENABLE Threshold	V_{ENABLE}	ENABLE pin logic High	1.25		AVIN	V
ENABLE Hysteresis	EN_{HYS}			200		mV
ENABLE Lockout Time	$T_{ENLOCKOUT}$			8		ms
ENABLE Input Current	I_{ENABLE}	370k internal pull-down (Note 4)		4		µA
Switching Frequency	F_{SW}	R_{FS} =3kΩ		1.0		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency (See Table 1)	0.9		1.8	MHz
S_IN Threshold – Low	$V_{S\_IN\_LO}$	S_IN clock logic low level (Note 4)			0.8	V
S_IN Threshold – High	$V_{S\_IN\_HI}$	S_IN clock logic high level (Note 4)	1.8		2.5	V
S_OUT Threshold – Low	$V_{S\_OUT\_LO}$	S_OUT clock logic low level (Note 4)			0.8	V
S_OUT Threshold – High	$V_{S\_OUT\_HI}$	S_OUT clock logic high level (Note 4)	1.8		2.5	V
POK Lower Threshold	POK_{LT}	V_{OUT} / V_{OUT_NOM}		90		%
POK Output low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	PVIN range: 4.5V ≤ V_{IN} ≤ 14V			AVIN	V
POK V_{OH} Leakage Current	I_{POKL}	POK High (Note 4)			1	µA

Note 4: Parameter not production tested but is guaranteed by design.
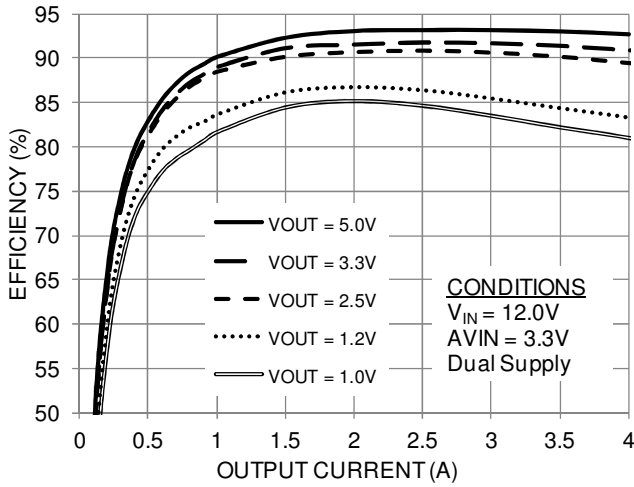
Note 5: Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

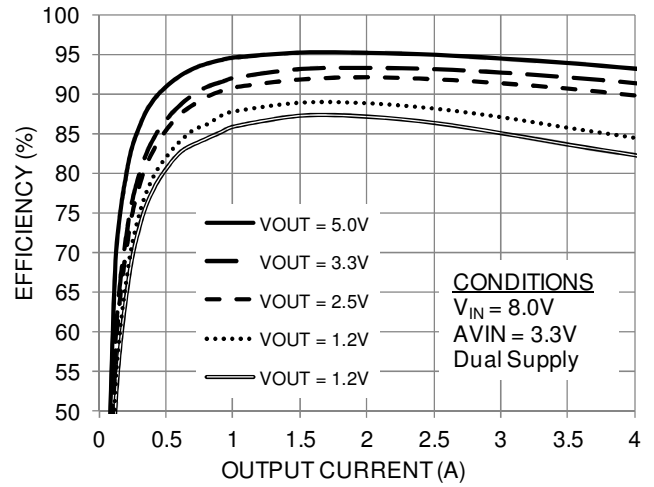**Note 6**: V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

Note 7: Output short circuit condition was performed with load impedance that is greater than or equal to 10mΩ.
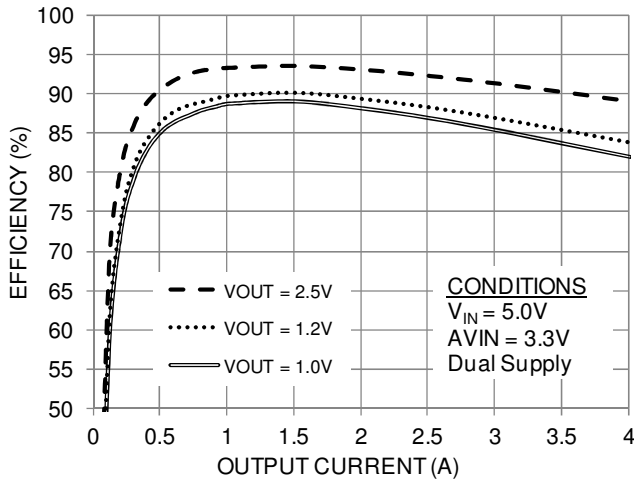
Typical Performance Curves
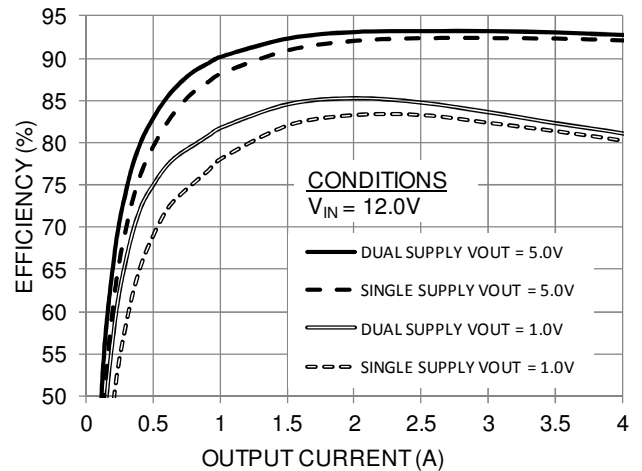
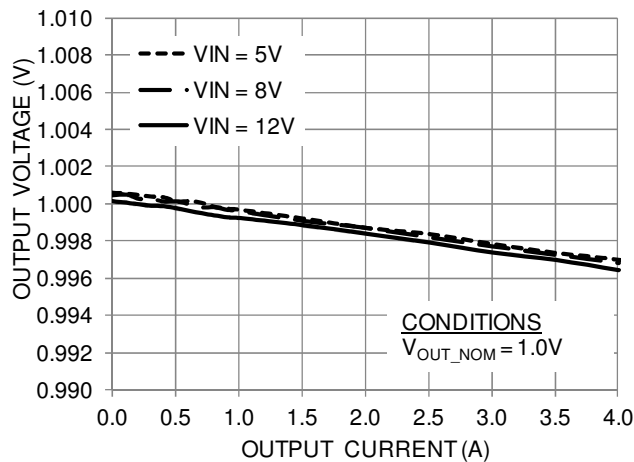### Efficiency vs. Output Current

EFFICIENCY (%)

OUTPUT CURRENT (A)

VOUT = 5.0V
VOUT = 3.3V
VOUT = 2.5V
VOUT = 1.2V
VOUT = 1.0V

CONDITIONS
V_{IN} = 12.0V
AVIN = 3.3V
Dual Supply

Efficiency vs. Output Current

EFFICIENCY (%)

OUTPUT CURRENT (A)

VOUT = 5.0V
VOUT = 3.3V
VOUT = 2.5V
VOUT = 1.2V
VOUT = 1.2V

CONDITIONS
V_{IN} = 8.0V
AVIN = 3.3V
Dual Supply

Efficiency vs. Output Current

EFFICIENCY (%)

OUTPUT CURRENT (A)

VOUT = 2.5V
VOUT = 1.2V
VOUT = 1.0V

CONDITIONS
V_{IN} = 5.0V
AVIN = 3.3V
Dual Supply

Efficiency vs. Output Current

EFFICIENCY (%)

OUTPUT CURRENT (A)

CONDITIONS
V_{IN} = 12.0V

DUAL SUPPLY VOUT = 5.0V
SINGLE SUPPLY VOUT = 5.0V
DUAL SUPPLY VOUT = 1.0V
SINGLE SUPPLY VOUT = 1.0V

Output Voltage vs. Output Current

OUTPUT VOLTAGE (V)

OUTPUT CURRENT (A)

VIN = 5V
VIN = 8V
VIN = 12V

CONDITIONS
V_{OUT_NOM} = 1.0V

Output Voltage vs. Output Current

OUTPUT VOLTAGE (V)

OUTPUT CURRENT (A)

VIN = 8V
VIN = 12V

CONDITIONS
V_{OUT_NOM} = 3.3V

Typical Performance Curves (Continued)

Output Voltage vs. Input Voltage
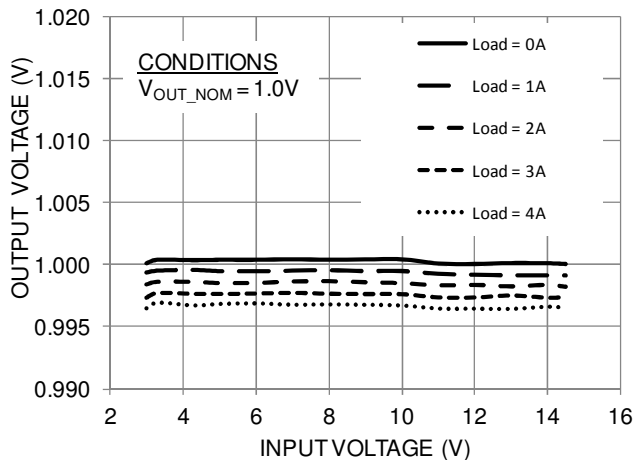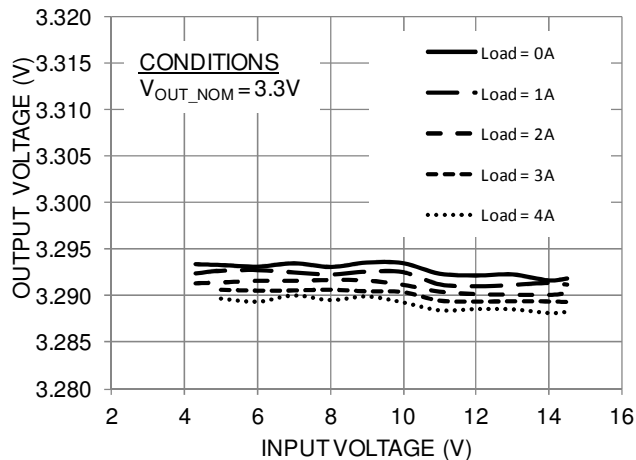
CONDITIONS
$V_{OUT\_NOM} = 1.0V$

Load = 0A
Load = 1A
Load = 2A
Load = 3A
Load = 4A

Output Voltage vs. Input Voltage

CONDITIONS
$V_{OUT\_NOM} = 3.3V$

Load = 0A
Load = 1A
Load = 2A
Load = 3A
Load = 4A

Output Voltage vs. Temperature

CONDITIONS
$V_{IN} = 8V$
$V_{OUT\_NOM} = 1.2V$

LOAD = 0A
LOAD = 1A
LOAD = 2A
LOAD = 3A
LOAD = 4A

Output Voltage vs. Temperature

CONDITIONS
$V_{IN} = 10V$
$V_{OUT\_NOM} = 1.2V$

LOAD = 0A
LOAD = 1A
LOAD = 2A
LOAD = 3A
LOAD = 4A

Output Voltage vs. Temperature

CONDITIONS
$V_{IN} = 12V$
$V_{OUT\_NOM} = 1.2V$

LOAD = 0A
LOAD = 1A
LOAD = 2A
LOAD = 3A
LOAD = 4A

Output Voltage vs. Temperature

CONDITIONS
$V_{IN} = 14V$
$V_{OUT\_NOM} = 1.2V$

LOAD = 0A
LOAD = 1A
LOAD = 2A
LOAD = 3A
LOAD = 4A
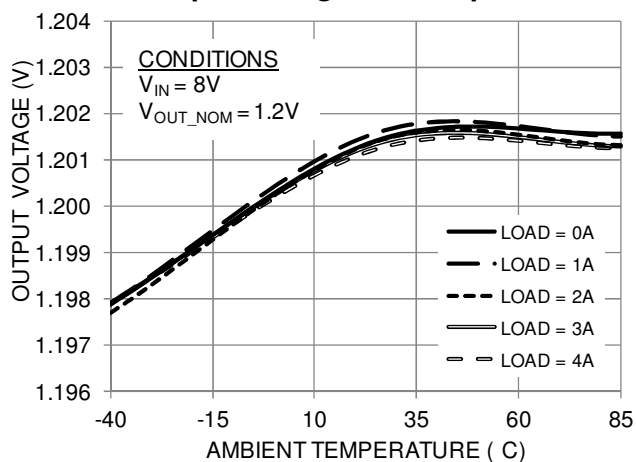
Typical Performance Characteristics

Output Ripple at 20MHz Bandwidth
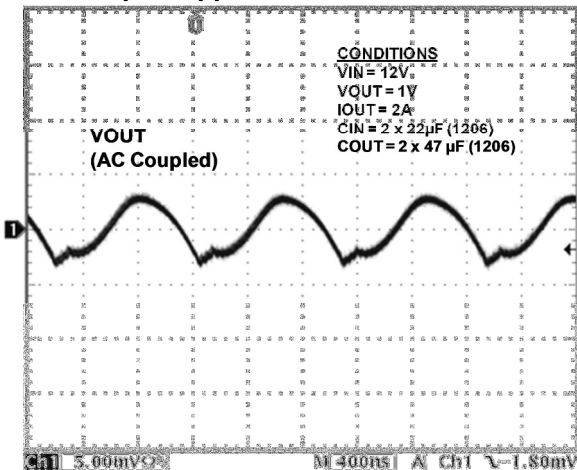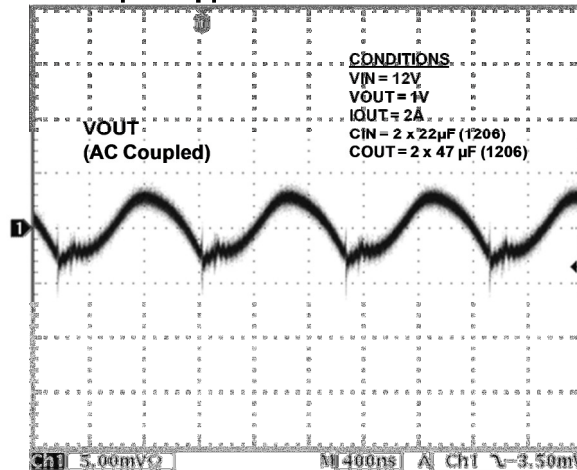
VOUT
(AC Coupled)

CONDITIONS
VIN = 12V
VOUT = 1V
IOUT = 2A
CIN = 2 x 22µF (1206)
COUT = 2 x 47 µF (1206)

Ch1 5.00mV M 400ns A Ch1 ⌐-1.80mV

Output Ripple at 500MHz Bandwidth

VOUT
(AC Coupled)

CONDITIONS
VIN = 12V
VOUT = 1V
IOUT = 2A
CIN = 2 x 22µF (1206)
COUT = 2 x 47 µF (1206)

Ch1 5.00mV M 400ns A Ch1 ⌐-3.50mV

Output Ripple at 20MHz Bandwidth

VOUT
(AC Coupled)

CONDITIONS
VIN = 12V
VOUT = 1V
IOUT = 4A
CIN = 2 x 22µF (1206)
COUT = 2 x 47 µF (1206)

Ch1 3.00mV M 400ns A Ch1 ⌐-1.90mV

Output Ripple at 500MHz Bandwidth

VOUT
(AC Coupled)

CONDITIONS
VIN = 12V
VOUT = 1V
IOUT = 4A
CIN = 2 x 22µF (1206)
COUT = 2 x 47 µF (1206)

Ch1 3.00mV M 400ns A Ch1 ⌐-3.00mV
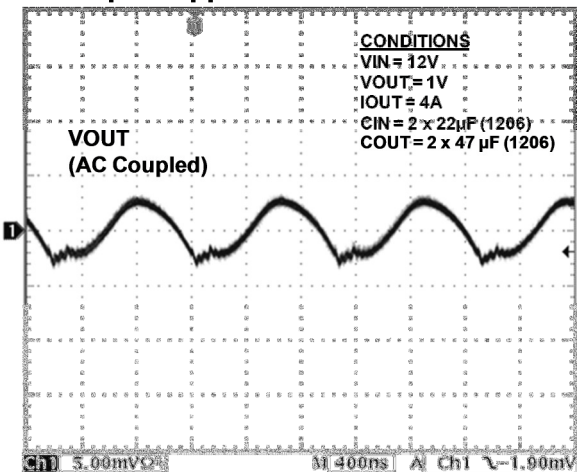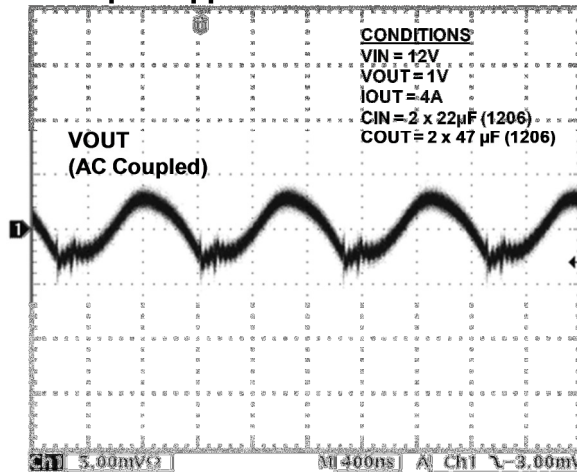
Enable Startup/Shutdown Waveform (0A)

ENABLE

VOUT

POK

LOAD

CONDITIONS
VIN = 12V, VOUT = 1.0V, No Load, Css = 47nF
CIN = 2 x 22µF (1206), COUT = 2 x 47 µF (1206)

Ch1 2.00 V   Ch2 500mV   M 4.00ms A Ch1 ∫ 1.52 V
Ch3 2.00 V   Ch4 200mA Ω

Enable Startup/Shutdown Waveform (4A)

ENABLE

VOUT

POK

LOAD

CONDITIONS
VIN = 12V, VOUT = 1.0V, LOAD = 4A, Css = 47nF
CIN = 2 x 22µF (1206), COUT = 2 x 47 µF (1206)

Ch1 2.00 V   Ch2 500mV   M 4.00ms A Ch1 ∫ 1.52 V
Ch3 2.00 V   Ch4 5.00 A Ω
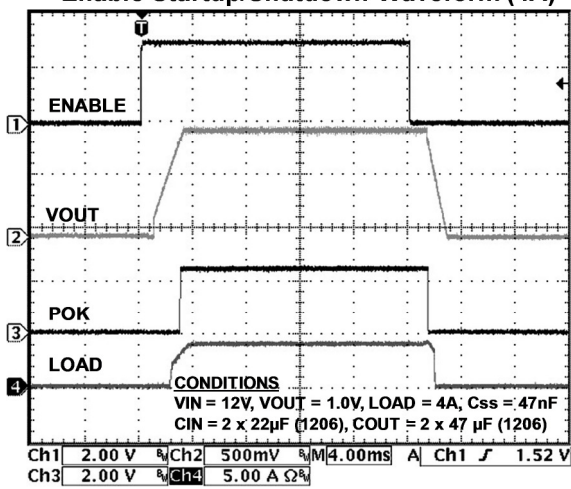
Typical Performance Characteristics (Continued)

Load Transient from 50mA to 2A

VOUT = 1V
(AC Coupled)
20mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 1V
CIN = 22µF (1206)
COUT = 2 x 22µF (0805)
Small Solution Size Configuration

Ch1 20.0mV ∿& M 100µs A Ch4 �“ 480mA
Ch4 2.00 A Ω&

Load Transient from 50mA to 4A

VOUT = 1V
(AC Coupled)
50mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 1V
CIN = 22µF (1206)
COUT = 2 x 22µF (0805)
Small Solution Size Configuration

Ch1 50.0mV ∿& M 100µs A Ch4 �“ 1.24 A
Ch4 2.00 A Ω&
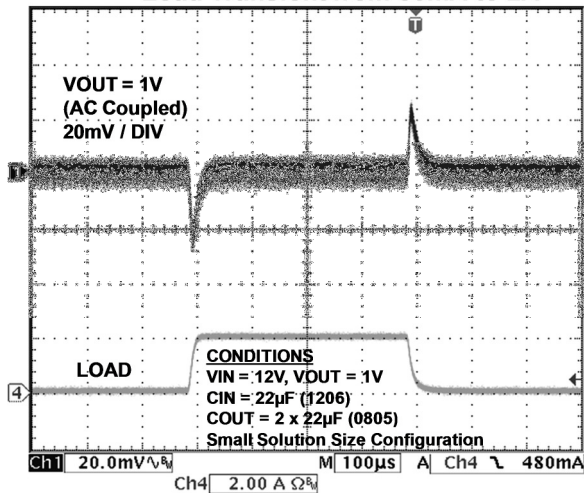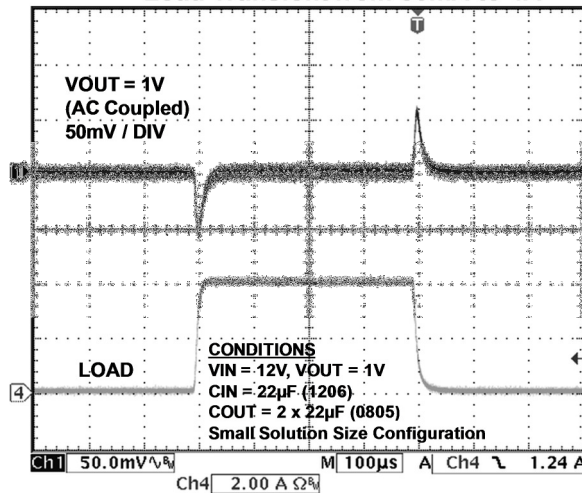
Load Transient from 2A to 4A

VOUT = 1.8V
(AC Coupled)
100mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 1.8V
CIN = 22µF (1206)
COUT = 2 x 22µF (0805)
Small Solution Size Configuration

Ch1 100mV ∿& M 100µs A Ch4 ʃ 3.60 A
Ch4 2.00 A Ω&

Load Transient from 50mA to 4A

VOUT = 1.8V
(AC Coupled)
100mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 1.8V
CIN = 22µF (1206)
COUT = 2 x 22µF (0805)
Small Solution Size Configuration

Ch1 100mV ∿& M 100µs A Ch4 �“ 1.28 A
Ch4 2.00 A Ω&

Load Transient from 50mA to 3A

VOUT = 3.3V
(AC Coupled)
100mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 3.3V
CIN = 22µF (1206)
COUT = 2 x 22µF (0805)
Small Solution Size Configuration

Ch1 100mV ∿ M 100µs A Ch4 ʃ 2.56 A
Ch4 2.00 A Ω&

Load Transient from 50mA to 3A

VOUT = 3.3V
(AC Coupled)
100mV / DIV

LOAD

CONDITIONS
VIN = 12V, VOUT = 3.3V
CIN = 22µF (1206)
COUT = 2 x 47µF (1206)
Best Performance Configuration

Ch1 100mV ∿& M 100µs A Ch4 �“ 1.24 A
Ch4 2.00 A Ω&
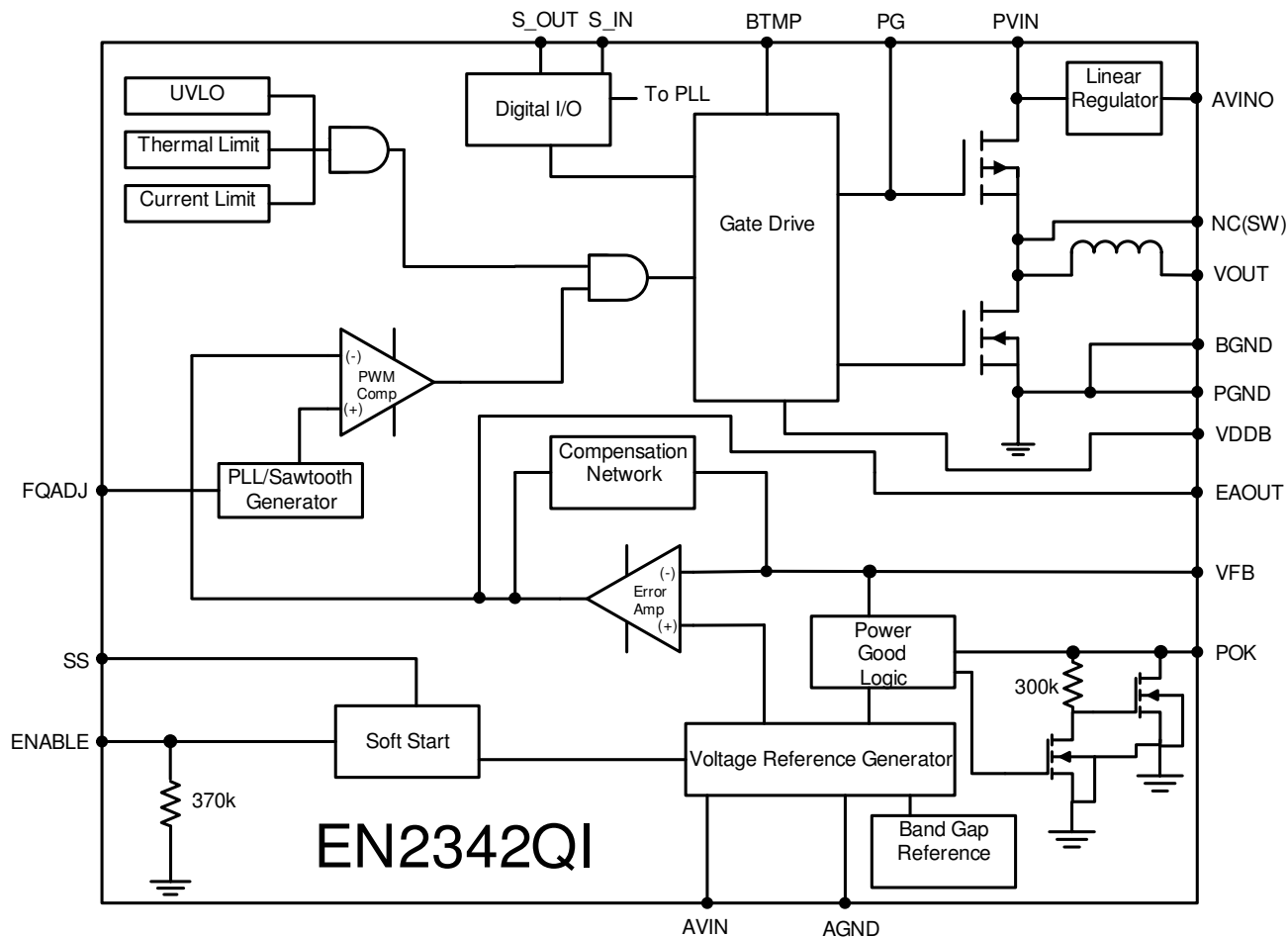
Functional Block Diagram

Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EN2342QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and inductor. The nominal input voltage (PVIN) range is 4.5V to 14V and can support up to 4A of continuous output current. The output voltage is programmed using an external resistor divider network. The control loop utilizes a Type IV Voltage-Mode compensation network and maximizes on a low-noise PWM topology. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the Type IV compensation network.. The high switching frequency of the EN2342QI enables the use of small size input and output filter

capacitors, as well as a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Over-Current and Short Circuit Protection
- Thermal Soft-Shutdown with Hysteresis.
- Under-Voltage Lockout Protection

Additional Features:

- Switching Frequency Synchronization.
- Programmable Soft-Start
- Power OK Output Monitoring

February 21, 2014

Modes of Operation

The EN2342QI is designed to be powered by either a single input supply (PVIN) or two separate supplies: one for PVIN and the other for AVIN. The EN2342QI is not "hot pluggable." Refer to the PVIN Slew Rate specification on page 4.
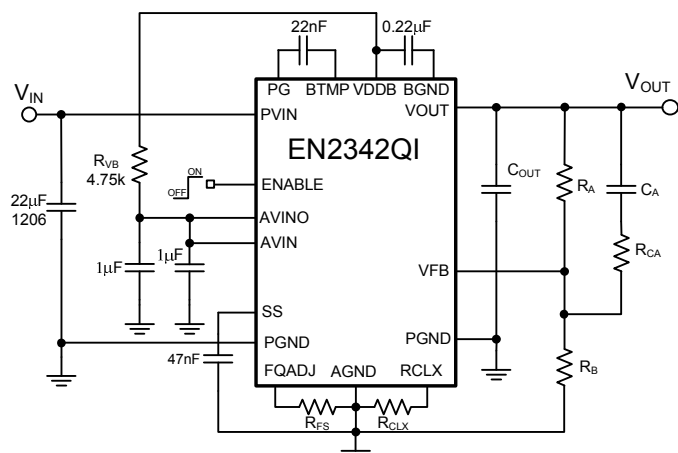
Single Input Supply Application (PVIN Only):

Figure 5: Single Input Supply Schematic

In single input supply mode, the EN2342QI only requires one input voltage rail (typically 12V). The EN2342QI has an internal linear regulator that converts PVIN to 3.3V. The output of the linear regulator is provided on the AVINO pin once the device is enabled. AVINO should be connected to AVIN. Also, in this single supply application, place a resistor (R_{VB}) between VDDB and AVIN, as shown in Figure 5. Altera recommends R_{VB}=4.75kΩ.

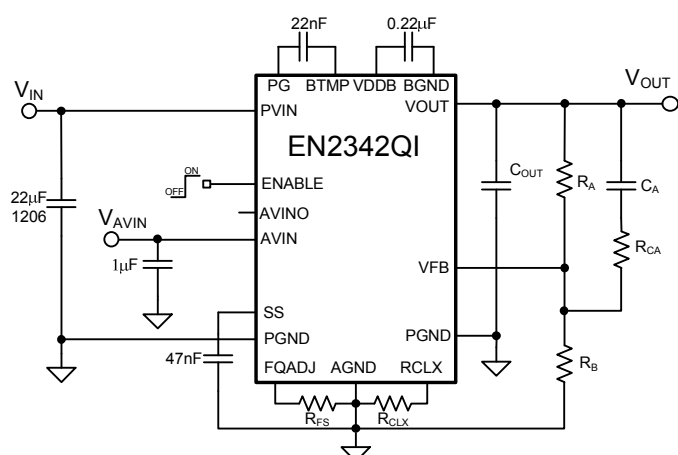Dual Input Supply Application (PVIN and AVIN):

Figure 6: Dual Input Supply Schematic

In dual input supply mode, two input voltage rails are required (typically 12V for PVIN and 3.3V for AVIN). Refer to Figure 6 for the recommended schematic for a dual input supply application. Since AVINO is not used, it can be left open.

Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled. To ensure accurate startup sequencing the ENABLE/DISABLE signal should be faster than 1V/100µs. A slower ENABLE/DISABLE signal may result in a delayed startup and shutdown response. Do not leave ENABLE floating.

Pre-Bias Precaution

The EN2342QI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EN2342QI is not pre-biased when the EN2342QI is first enabled.

Frequency Synchronization

The switching frequency of the EN2342QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN2342QI can be phase locked to a clock signal applied to the S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.9MHz to 1.8MHz. The external clock frequency must be within ±10% of the nominal switching frequency set by the R_{FS} resistor. It is recommended to use a synchronized clock frequency close to the typical frequency recommendations in Table 1. A 3.01kΩ resistor from FQADJ to ground is recommended for clock frequencies within ±10% of 1MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator set by the R_{FS} resistor.

The efficiency performance of the EN2342QI for various PVIN/VOUT combinations can be optimized by adjusting the switching frequency. Table 1 shows recommended R_{FS} values for various PVIN/VOUT combinations in order to optimize performance of the EN2342QI.
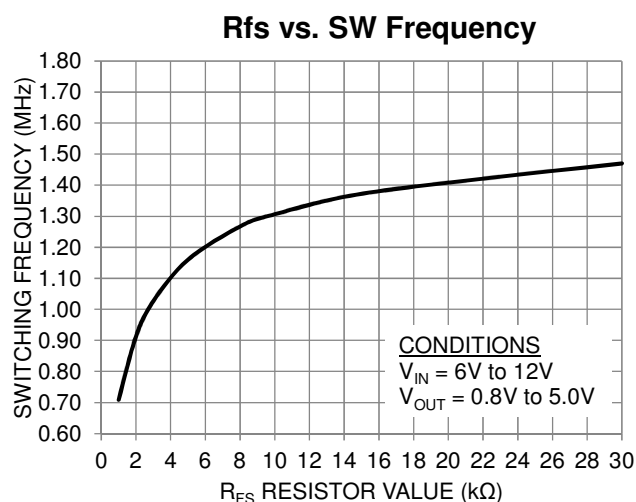
Rfs vs. SW Frequency

CONDITIONS
V_{IN} = 6V to 12V
V_{OUT} = 0.8V to 5.0V

Figure 7. Typical R_{FS} vs. Switching Frequency

PVIN	VOUT	R_{FS}	Typical fsw
4.5V to 14V	5.0V	30k	1.48 MHz
	3.3V	15k	1.38 MHz
	2.5V	10k	1.3 MHz
	1.8V	4.87k	1.15 MHz
	1.5V	3.01k	1.0 MHz
	1.2V	3.01k	1.0 MHz
	<1.0V	3.01k	1.0 MHz

Table 1: Recommended R_{FS} Values

Spread Spectrum Mode

The external clock frequency may be swept between 0.9MHz and 1.8MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 56) and the AGND pin (pin 52). During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10μA. The soft-start time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value. The total soft-start time can be calculated by:

Soft Start Time (ms): $T_{SS} \approx C_{ss}$ [nF] x 0.067

Typical soft-start time is approximately 3.2ms with SS capacitor value of 47nF.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit for more than 32 cycles, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. While in hiccup mode, the device is disabled for a short while and restarted with a normal soft-start. The hiccup time is approximately 32ms. This cycle can continue indefinitely as long as the over current condition persists. The OCP trip point depends on PVIN, VOUT, RCLX, RFS and will vary from part to part. The current limit is meant to protect the device from damage and not recommended as an accurate current limit setting. Generally, the higher the RCLX value, the higher the current limit threshold for a given input and output voltage condition. Since current limit depends on various parameters, follow Table 2 for recommended values to cover most applications.

Note: If the RCLX pin is left open, the output current will be unlimited and the device will not have current limit protection.

PVIN	V_{OUT}	R_{CLX}	R_{FS}
4.5V to 14V	5.0V	68.1k	30k
	3.3V	61.9k	22k
	2.5V	56.2k	10k
	1.8V	54.9k	4.87k
	1.5V	53.6k	3.01k
	1.2V	46.4k	3.01k
	≤1.0V	38.3k	3.01k

Table 2: Recommended R_{CLX} Values

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 150°C. The device will go through a soft-shutdown and allow the output to discharge in a controlled manner. This prevents excessive output ringing in the event of a thermal fault condition. After a thermal shutdown event, when the junction temperature drops by approximately 35°C, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-out (UVLO)

Internal circuits ensure that the converter will not start switching until the AVIN input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

Application Information

Output Voltage Programming and Loop Compensation

The EN2342QI uses a Type IV Voltage Mode compensation network. Type IV Voltage Mode control is a proprietary Altera Enpirion control scheme that maximizes control loop bandwidth to deliver excellent load transient responses and maintain output regulation with pin point accuracy. For ease of use, most of this network has been customized and is integrated within the device package.

The EN2342QI output voltage is programmed using a simple resistor divider network (R_A and R_B). The feedback voltage at VFB is nominally 0.75V. R_A depends on Table 6 and R_B can be calculated based on Figure 8. The values recommended for C_{OUT}, C_A, and R_{CA} make up the external compensation of the EN2342QI. It will vary with each PVIN and VOUT combination to optimize on performance. The EN2342QI solution can be optimized for either smallest size or highest performance. Please see Table 6 for a list of recommended R_A, C_A, R_{CA}, and C_{OUT} values for each solution. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.
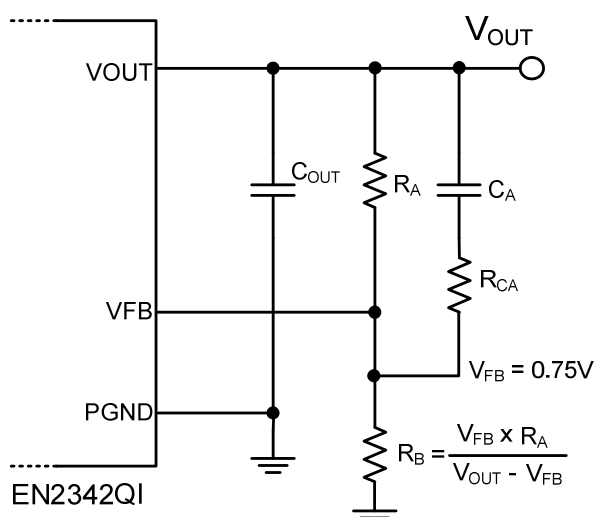

Figure 8: V_{OUT} Resistor Divider & Compensation Components. See Table 6 for details.

Input Capacitor Selection

The EN2342QI requires a 22µF/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Table 3 contains a list of recommended input capacitors.

Recommended Input Capacitors

Description	MFG	P/N
22µF, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22µF, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T

Table 3: Recommended Input Capacitors

Output Capacitor Selection

As seen from Table 6, the EN2342QI has been optimized for use with either two 47µF/1206 or two 22µF/0805 output capacitors. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Table 5 contains a list of recommended output capacitors. In some applications, extra bulk capacitance is required at the load. In this case, up to 1000µF of bulk capacitance may be used at the load as long as the minimum ESR between the device output and the bulk capacitance is maintained. Table 4 shows the recommended compensation components for applications that require bulk capacitance at the load.

PVIN (V)	VOUT (V)	Min. ESR	Compensation
4.5 to 14	≥2.5	4mΩ	C_{OUT} = 2x47µF/1206 Bulk Cap ≤ 1000µF C_A = 100pF R_A = 250kΩ R_{CA} = 5kΩ
≥10	0.6 to 1.5	9mΩ	
	1.5 to 2.5	7mΩ	
<10	0.6 to 1.5	12mΩ	
	1.5 to 2.5	9mΩ	

Table 4: Minimum ESR for Bulk Capacitance at Load

Note that when bulk capacitors are used the converter must work harder during startup in order to raise the output voltage from zero volts into regulation. If there is too much output capacitance, the device can hit current limit before it is able to raise the output into regulation. If current limit is

reached the device stops switching, the output will be discharged and the cycle repeats itself indefinitely. The equation below can be used to estimate the maximum output capacitance allowed based on current limit. Since the maximum output capacitance in the calculation does not account for temperature or part to part variations, it is always good to add margin by using a value that is 80% of the calculated output capacitance value.

$C_{OUT\_MAX} = I_{TOTAL} * dt / dv * 0.8$

C_{OUT_MAX} = Maximum allowable output capacitance
I_{TOTAL} = Max output current of device minus the load during startup
dv = Change in voltage (which is 0 to V_{OUT})
dt = Soft-start time (ms) $\approx C_{ss}$ [nF] x 0.067

The output capacitance can also influence the output ripple. Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as Z, is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T
22µF, 10V, X5R, 20%, 0805	Panasonic	ECJ-2FB1A226M
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T

Table 5: Recommended Output Capacitors

PVIN	V$_{OUT}$	Low V$_{OUT}$ Ripple C$_{IN}$ = 1 x 22µF/1206 C$_{OUT}$ = 2 x 47µF/1206 R$_A$= 180/(Vout$^{0.5}$) kΩ				Smallest Solution Size C$_{IN}$ = 1 x 22µF/1206 C$_{OUT}$ = 2 x 22µF/0805				
		C$_A$ (pF)	R$_{CA}$ (kΩ)	Nominal Ripple (mV)	Nominal Deviation (mV)	R$_A$ (kΩ)	C$_A$ (pF)	R$_{CA}$ (kΩ)	Nominal Ripple (mV)	Nominal Deviation (mV)
14V	≤1.0V	10	30	≤5	≤47	75	27	0.1	≤10	≤34
	1.2V	12	27	6	48	43	39	0.1	13	33
	1.5V	15	27	5	53	56	39	0.1	15	38
	1.8V	22	27	6	54	56	39	0.1	18	41
	2.5V	27	24	8	55	51	39	0.1	26	59
	3.3V	39	18	11	63	51	33	0.1	35	63
	5.0V	47	8.2	18	97	75	22	5.1	42	115
12V	≤1.0V	18	22	≤4	≤48	27	47	0.1	≤10	≤35
	1.2V	22	22	5	49	75	47	0.1	13	37
	1.5V	27	20	5	53	75	47	0.1	15	38
	1.8V	33	20	6	54	75	47	0.1	17	44
	2.5V	47	18	7	54	56	47	0.1	25	59
	3.3V	56	15	10	66	51	39	0.1	32	63
	5.0V	56	10	16	99	75	22	5.1	39	128
10V	≤1.0V	33	18	≤3	≤45	27	82	0.1	≤9	≤35
	1.2V	39	18	4	46	30	100	0.1	13	39
	1.5V	47	18	5	54	30	100	0.1	14	43
	1.8V	56	16	6	56	30	100	0.1	17	50
	2.5V	68	12	7	57	75	56	0.1	26	70
	3.3V	82	10	9	68	56	47	0.1	30	83
	5.0V	100	4.3	14	98	75	33	5.1	33	140
8.0V	≤1.0V	100	8.2	≤3	≤51	100	100	0.1	≤10	≤41
	1.2V	100	8.2	4	51	100	100	0.1	12	43
	1.5V	100	8.2	4	54	100	100	0.1	14	46
	1.8V	100	8.2	5	57	100	100	0.1	16	53
	2.5V	100	8.2	6	64	91	82	0.1	23	71
	3.3V	100	8.2	8	70	75	56	0.1	25	85
	5.0V	100	8.2	10	110	75	56	5.1	30	127
6.6V	≤1.0V	100	8.2	≤3	≤60	100	100	0.1	≤9	≤46
	1.2V	100	8.2	4	63	100	100	0.1	12	51
	1.5V	100	8.2	4	65	100	100	0.1	14	56
	1.8V	100	8.2	5	68	100	100	0.1	16	61
	2.5V	100	8.2	5	75	100	100	0.1	19	83
	3.3V	100	8.2	6	85	91	82	0.1	22	106
5V	≤1.0V	100	8.2	≤3	≤73	100	100	0.1	≤9	≤56
	1.2V	100	8.2	3	75	100	100	0.1	11	63
	1.5V	100	8.2	4	76	100	100	0.1	13	70
	1.8V	100	8.2	4	80	100	100	0.1	13	78
	2.5V	100	8.2	4	88	100	100	0.1	14	98

Table 6: R$_A$, C$_A$, and R$_{CA}$ Values for Various PVIN/VOUT Combinations: Low V$_{OUT}$ Ripple vs. Smallest Solution Size. See Figure 8. Use the equation in Figure 8 to calculate R$_B$ (for low V$_{OUT}$ ripple option). Output Ripple is measured at no load and Nominal Deviation is for a 2A load transient step in one direction. For compensation values of output voltage in between the specified output voltages, choose compensation values of the lower output voltage setting.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Altera Enpirion PowerSoC helps alleviate some of those concerns.

The Altera Enpirion EN2342QI DC-DC converter is packaged in an 8x11x3mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The EN2342QI is guaranteed to support the full 4A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN2342QI.

Example:

V_{IN} = 12V

V_{OUT} = 3.3V

I_{OUT} = 4A

First calculate the output power.

P_{OUT} = 3.3V x 4A = 13.2W

Next, determine the input power based on the efficiency (η) shown in Figure 9.

Efficiency vs. Output Current

Figure 9: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 3.3V at 4A, η ≈ 91%

η = P_{OUT} / P_{IN} = 91% = 0.91

P_{IN} = P_{OUT} / η

P_{IN} ≈ 13.2W / 0.9 ≈ 14.51W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} − P_{OUT}

≈ 14.51W − 13.2W ≈ 1.31W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value ($θ_{JA}$). The $θ_{JA}$ parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN2342QI has a $θ_{JA}$ value of 18 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and $θ_{JA}$.

ΔT = P_D x $θ_{JA}$

ΔT ≈ 1.31W x 18°C/W = 23.5°C ≈ 24°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 24°C ≈ 49°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} − P_D x $θ_{JA}$

≈ 125°C − 24°C ≈ 101°C

The maximum ambient temperature the device can reach is 101°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.
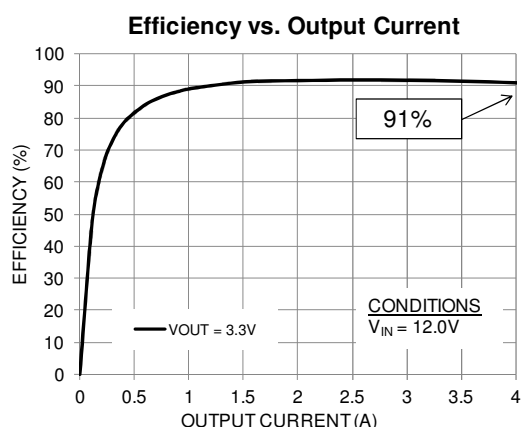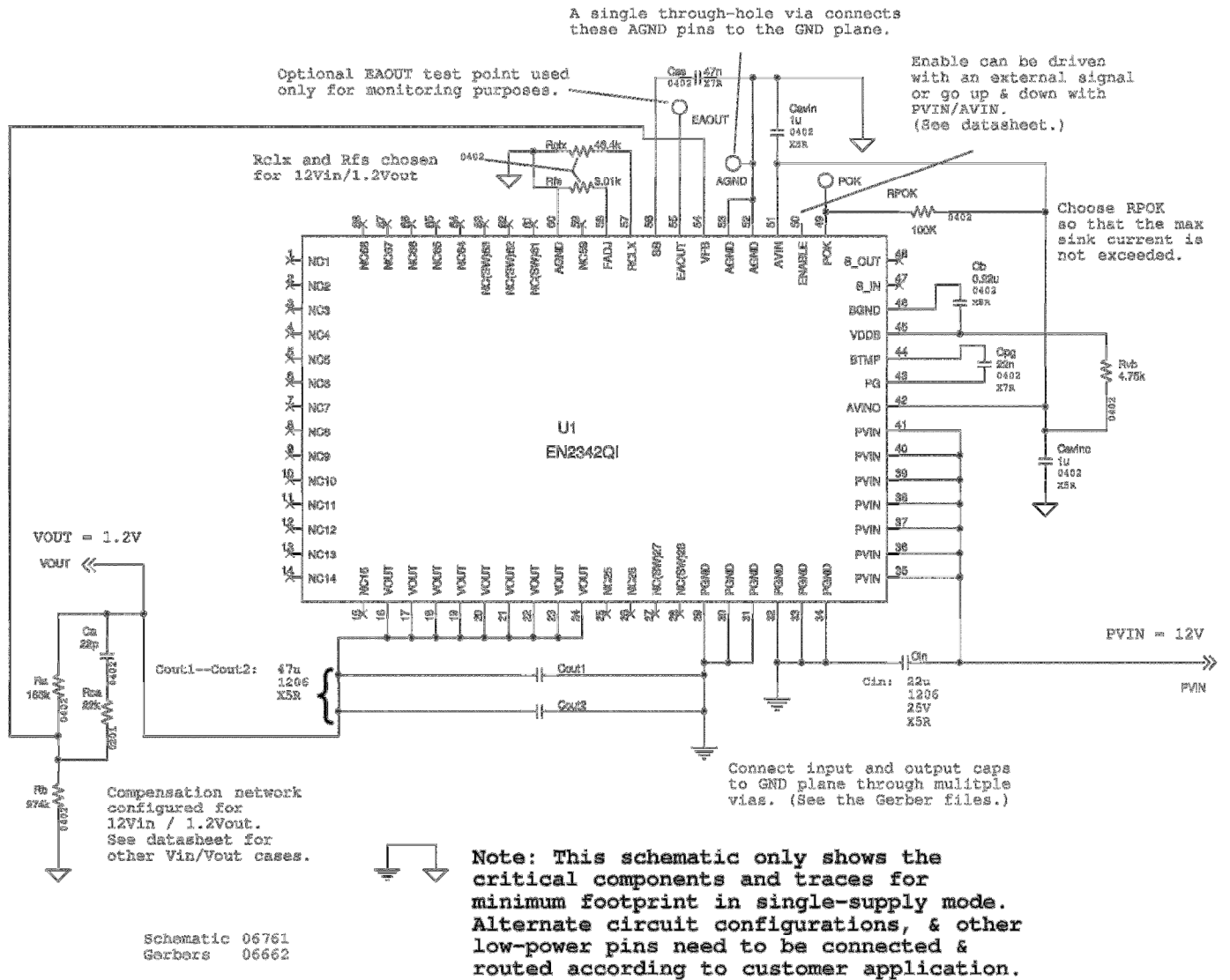
Engineering Schematic

Figure 10: Engineering Schematic with Engineering Notes
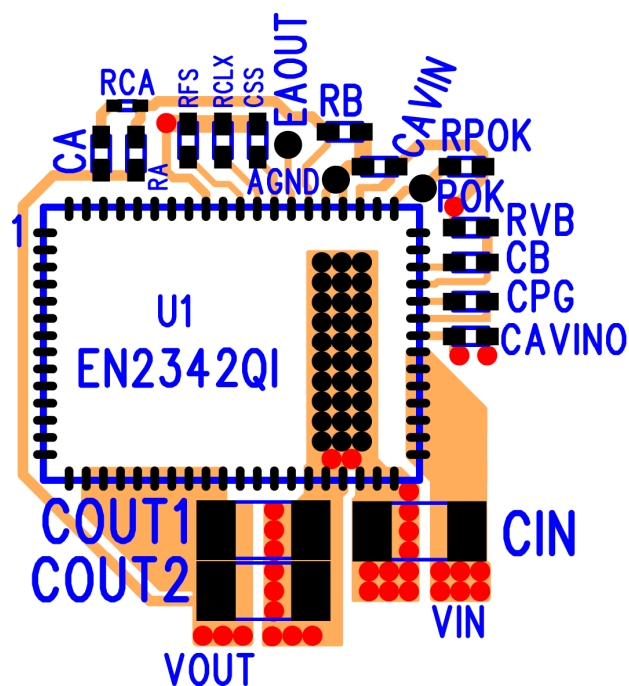
Layout Recommendation

Figure 11: Top Layer Layout with Critical Components (Top View). See Figure 10 for corresponding schematic.

This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at www.altera.com for details on all layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN2342QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN2342QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. AVINO powers AVIN in single supply mode. AVIN and AVINO should have a decoupling capacitor close to each of their pins. Refer to Figure 11.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 11. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Altera MySupport for any remote sensing applications.

Recommendation 9: Keep R_A, C_A, R_B, and R_{CA} close to the VFB pin (Refer to Figure 11). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pins 52 and 53 instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Altera provides schematic and layout reviews for all customer designs. Contact Altera MySupport for detailed support (www.altera.com/mysupport).

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 12.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN2342QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The "shaded-out" area in Figure 12 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.
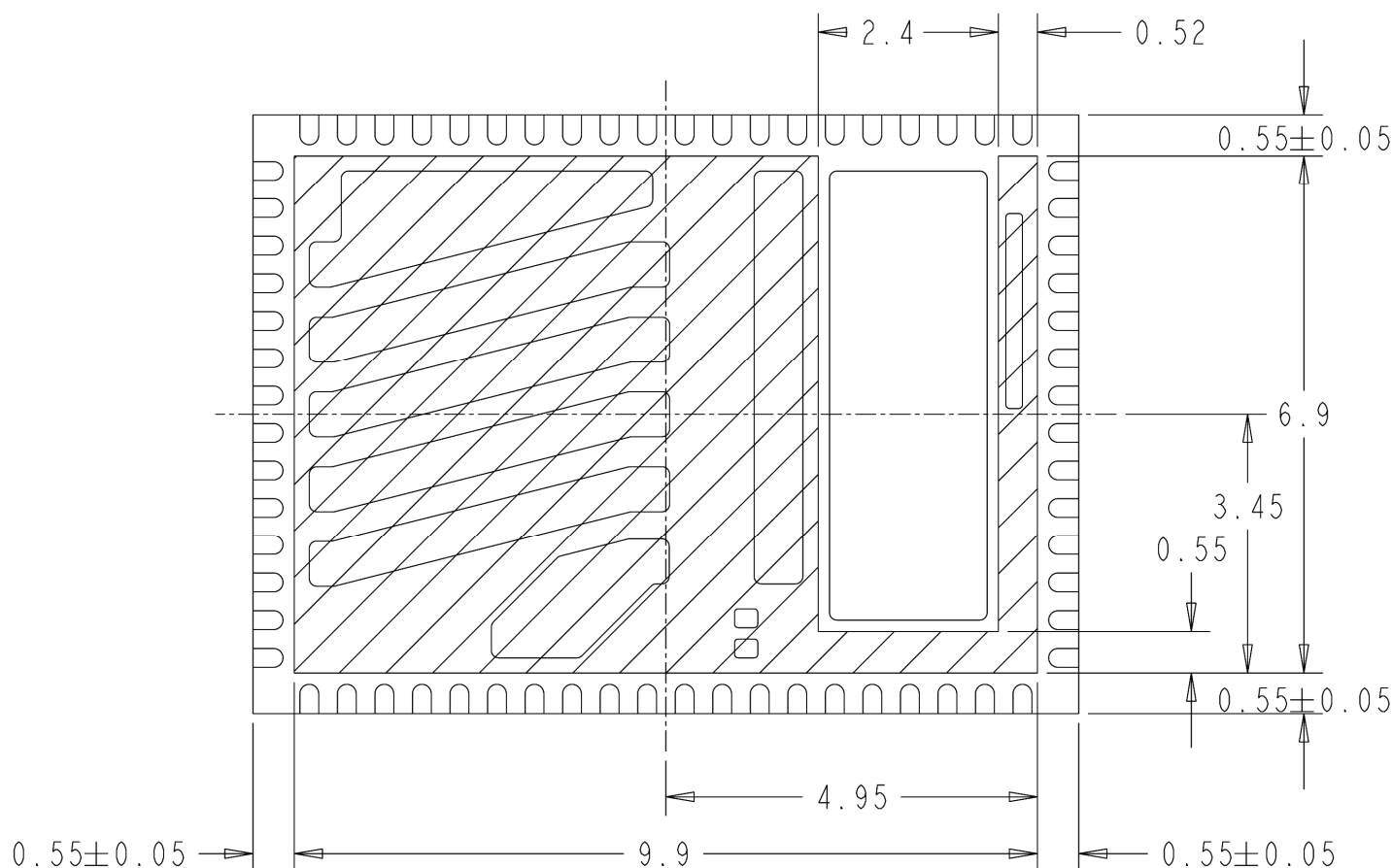
Figure 12: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.
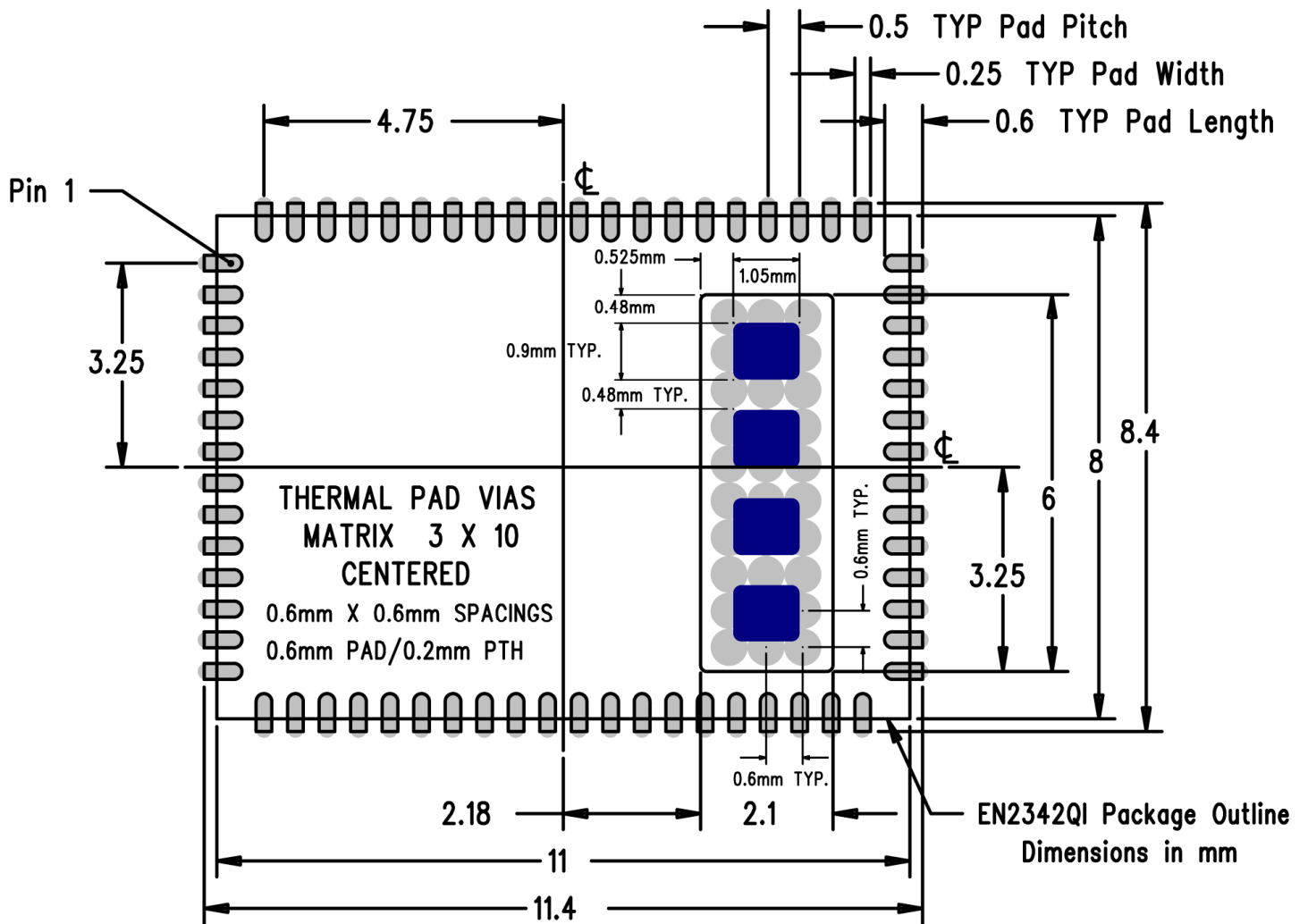
Recommended PCB Footprint

Figure 13: EN2342QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad (shown in blue) is based on Altera's manufacturing recommendations
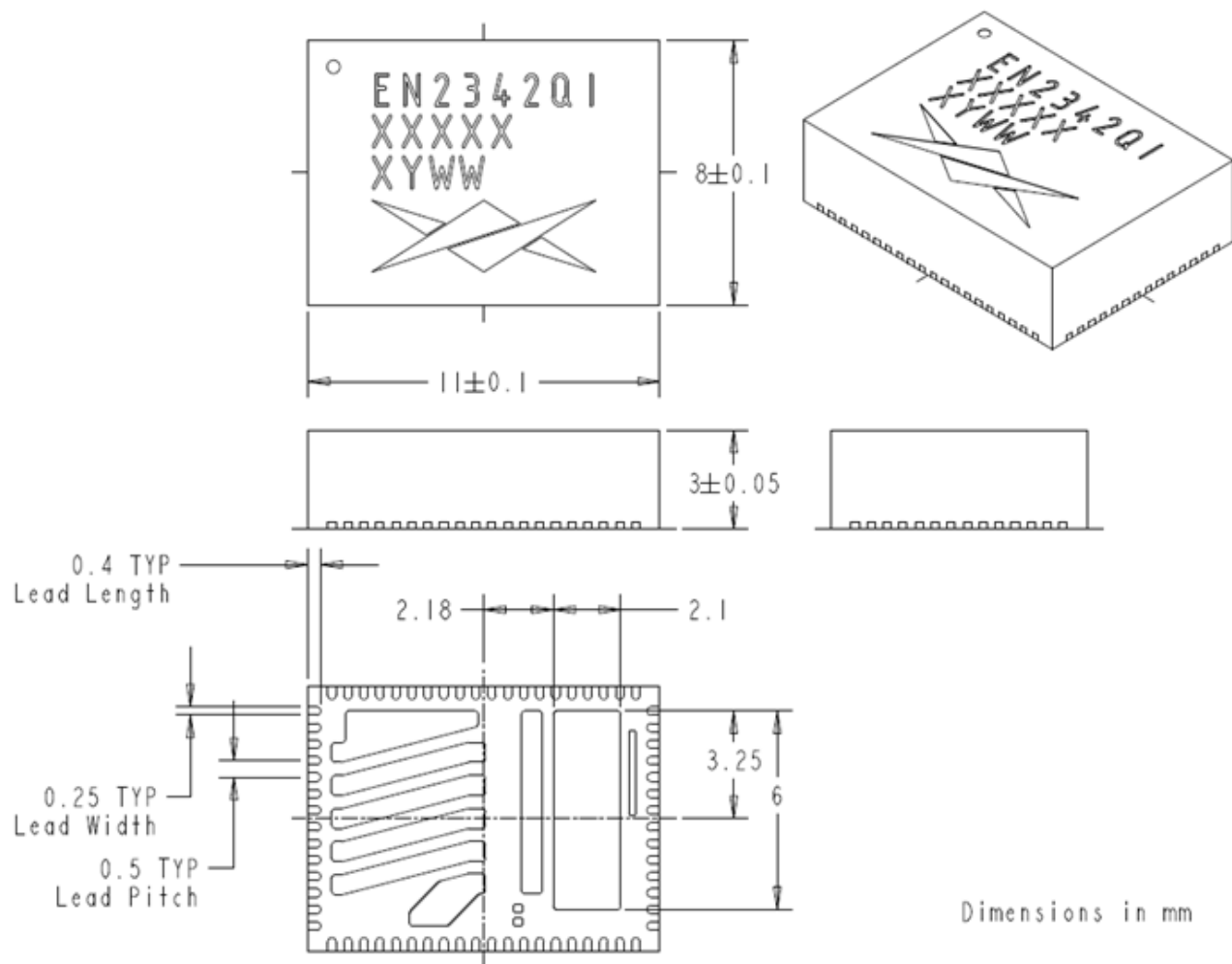
Package and Mechanical

Figure 14: EN2342QI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Contact Information

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