# TDA7375V

## 2 x 35W dual/quad power amplifier for car radio

## 1 FEATURES

- HIGH OUTPUT POWER CAPABILITY:
  - 2 x 40W max./4Ω
  - 2 x 35W/4Ω EIAJ
  - 2 x 35W/4Ω EIAJ
  - 2 x 25W/4Ω @14.4V, 1KHz, 10%
  - 4 x 7W/4Ω @14.4V,1KHz, 10%
  - 4 x 12W/2Ω @14.4V, 1KHz, 10%
- MINIMUM EXTERNAL COMPONENTS COUNT:
  - NO BOOTSTRAP CAPACITORS
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN (26dB BTL)
- ST-BY FUNCTION (CMOS COMPATIBLE)
- NO AUDIBLE POP DURING ST-BY OPERATIONS
- DIAGNOSTICS FACILITY FOR:
  - CLIPPING
  - OUT TO GND SHORT
  - OUT TO $V_S$ SHORT
  - SOFT SHORT AT TURN-ON
  - THERMAL SHUTDOWN PROXIMITY

**Figure 1. Package**

MULTIWATT15

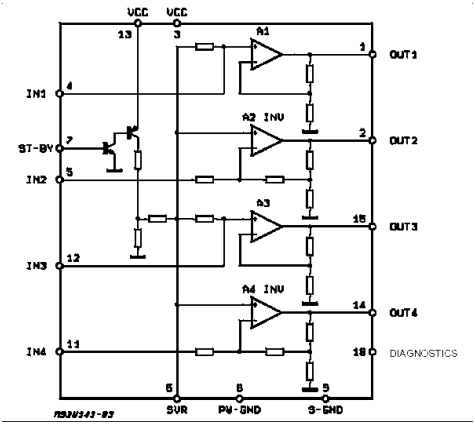
**Table 1. Order Codes**

| Part Number | Package |
|---|---|
| TDA7375V | MULTIWATT 15 (Vertical) |

## 2 PROTECTIONS:

- OUPUT AC/DC SHORT CIRCUIT
  - TO GND
  - TO $V_S$
  - ACROSS THE LOAD
- SOFT SHORT AT TURN-ON
- OVERRATING CHIP TEMPERATURE WITH
- SOFT THERMAL LIMITER
- LOAD DUMP VOLTAGESURGE
- VERY INDUCTIVE LOADS
- FORTUITOUS OPEN GND
- REVERSED BATTERY
- ESD

**Figure 2. Block Diagram**



## 3 DESCRIPTION

The TDA7375V is a new technology class AB car radio amplifier able to work either in DUAL BRIDGE or QUAD SINGLE ENDED configuration.

The exclusive fully complementary structure of the output stage and the internally fixed gain guarantees the highest possible power performances with extremely reduced component count.

The on-board clip detector simplifies gain compression operation. The fault diagnostics makes it possible to detect mistakes during car radio set assembly and wiring in the car.

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{op}$ | Operating Supply Voltage | 18 | V |
| $V_S$ | DC Supply Voltage | 28 | V |
| $V_{peak}$ | Peak Supply Voltage (for t = 50ms) | 50 | V |
| $I_O$ | Output Peak Current (not repetitive t = 100µs) | 4.5 | A |
| $I_O$ | Output Peak Current (repetitive f > 10Hz) | 3.5 | A |
| $P_{tot}$ | Power Dissipation ($T_{case}$ = 85°C) | 36 | W |
| $T_{stg}$, $T_j$ | Storage and Junction Temperature | -40 to 150 | °C |

**Table 3. Thermal Data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal Resistance Junction-case | max | 1.8 | °C/W |

**Figure 3. Pin Connection (Top view)**

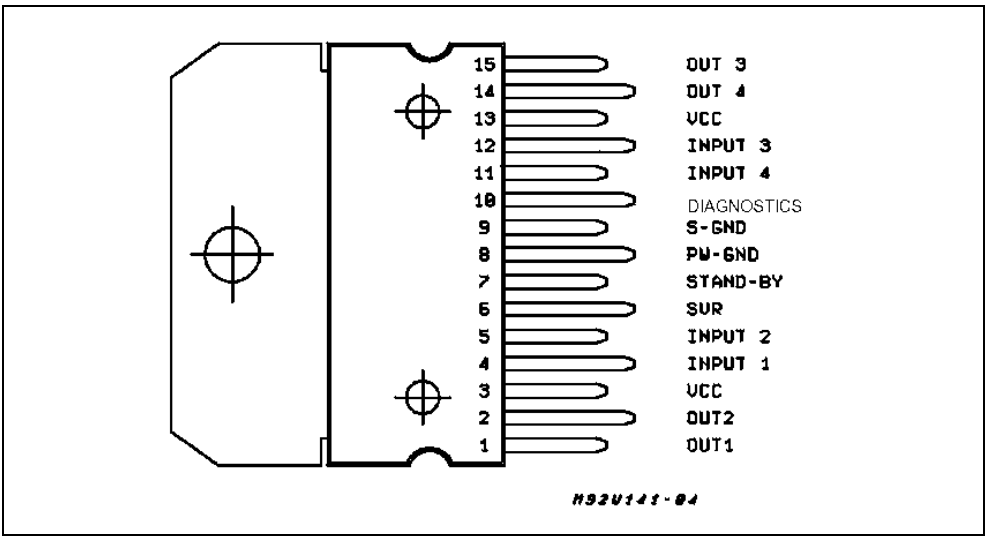


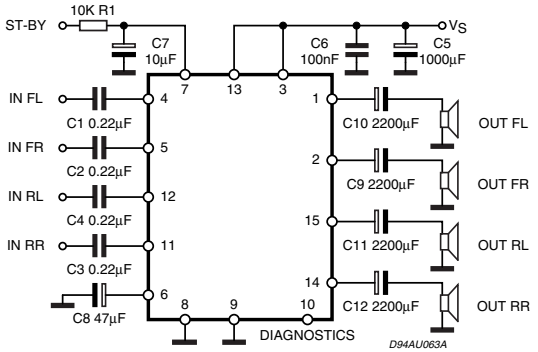
**Table 4. Electrical Characteristcs** (Refer to the test circuit, $V_S$ = 14.4V; $R_L$ = 4Ω; f = 1KHz; $T_{amb}$ = 25°C, unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_S$ | Supply Voltage Range | | 8 | | 18 | V |
| $I_d$ | Total Quiescent Drain Current | $R_L = \infty$ | | | 150 | mA |
| $V_{OS}$ | Output Offset Voltage | | | | 150 | mV |
| $P_O$ | Output Power | THD = 10%; $R_L$ = 4Ω<br>Bridge<br>Single Ended<br>Single Ended, $R_L$ = 2Ω | <br>23<br>6.5 | <br>25<br>7<br>12 | | <br>W<br>W<br>W |
| $P_O$ max | Max. Output Power (***) | $V_S$ = 14.4V, Bridge | 36 | 40 | | W |
| $P_{O\ EIAJ}$ | EIAJ Output Power (***) | $V_S$ = 13.7V, Bridge | 32 | 35 | | W |
| THD | Distortion | $R_L$ = 4Ω<br>Single Ended, $P_O$ = 0.1 to 4W<br>Bridge, $P_O$ = 0.1 to 10W | | <br>0.02<br>0.03 | <br><br>0.3 | <br>%<br>% |
| CT | Cross Talk | f = 1KHz Single Ended | | 70 | | dB |
| | | f = 10KHz Single Ended | | 60 | | dB |
| | | f = 1KHz Bridge | 55 | | | dB |
| | | f = 10KHz Bridge | | 60 | | dB |
| $R_{IN}$ | Input Impedance | Single Ended | 20 | 30 | | KΩ |
| | | Bridge | 10 | 15 | | KΩ |
| $G_V$ | Voltage Gain | Single Ended | 19 | 20 | 21 | dB |
| | | Bridge | 25 | 26 | 27 | dB |
| $G_V$ | Voltage Gain Match | | | | 0.5 | dB |
| $E_{IN}$ | Input Noise Voltage | $R_g$ = 0; "A" weighted, S.E.<br>Non Inverting Channels<br>Inverting Channels | | <br>2<br>5 | | <br>μV<br>μV |
| | | Bridge<br>Rg = 0; 22Hz to 22KHz | | <br>3.5 | | <br>μV |
| SVR | Supply Voltage Rejection | $R_g$ = 0; f = 300Hz | 50 | | | dB |
| $A_{SB}$ | Stand-by Attenuation | $P_O$ = 1W | 80 | 90 | | dB |
| $I_{SB}$ | ST-BY Current Consumption | $V_{ST-BY}$ = 0 to 1.5V | | | 100 | μA |
| $V_{SB}$ | ST-BY In Threshold Voltage | | | | 1.5 | V |
| $V_{SB}$ | ST-BY Out Threshold Voltage | | 3.5 | | | V |
| $I_{pin7}$ | ST-BY Pin Current | Play Mode $V_{pin7}$ = 5V | | | 50 | μA |
| | | Max Driving Curr. Under Fault (*) | | | 5 | mA |
| $I_{cd\ off}$ | Clipping Detector Output Average Current | d = 1% (**) | | 90 | | μA |
| $I_{cd\ on}$ | Clipping Detector Output Average Current | d = 5% (**) | | 160 | | μA |
| $V_{sat\ pin10}$ | Voltage Saturation on pin 10 | Sink Current at Pin 10 = 1mA | | | 0.7 | V |

(*) See built-in S/C protection description
(**) Pin 10 Pulled-up to 5V with 10KΩ; $R_L$ = 4Ω
(***) Saturated square wave output.

# 4 STANDARD TEST AND APPLICATION CIRCUIT

**Figure 4. Quad Stereo**




Note:
C9, C10, C11, C12 could be reduced if the 2W operation is not required.

**Figure 5. Double Bridge**

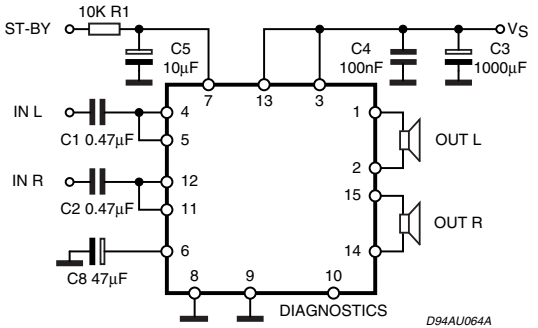



**Figure 6. Stereo/Bridge**

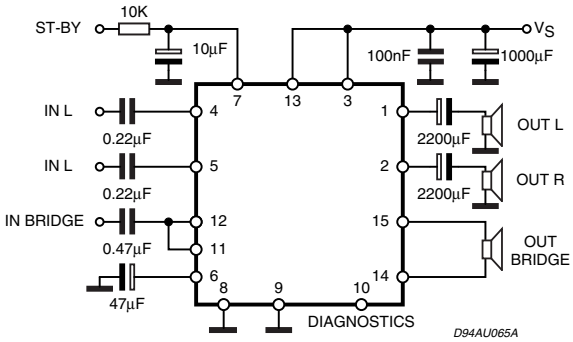


**Figure 7. P.C. Board and Component Layout of the fig.4**

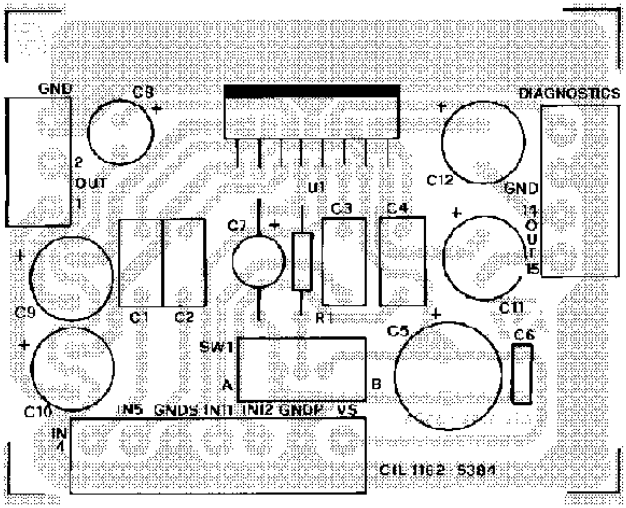



**Figure 8. P.C. Board and Component Layout of the fig.5**

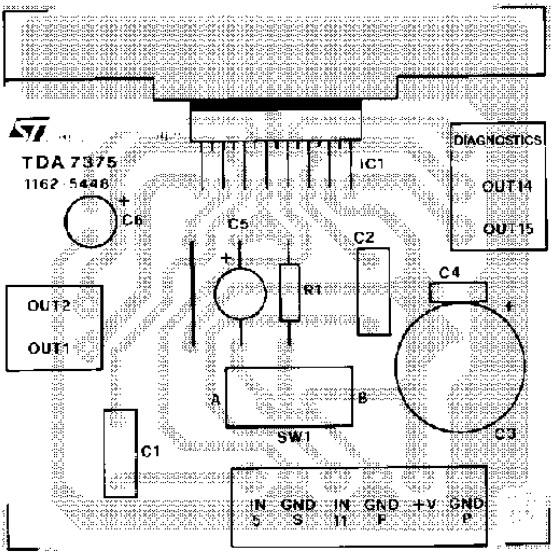


**Figure 9. Quiescent Drain Current vs. Supply Voltage (Single Ended and Bridge).**

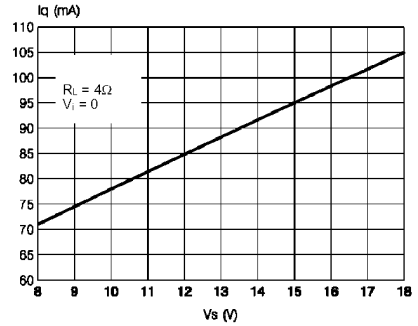



**Figure 10. Quiescent Output Voltage vs. Supply Voltage (Single Ended and Bridge).**

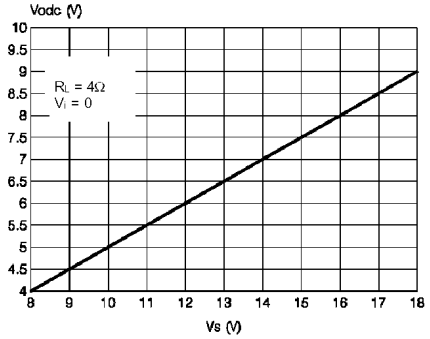



**Figure 11. Output Power vs. Supply Voltage**

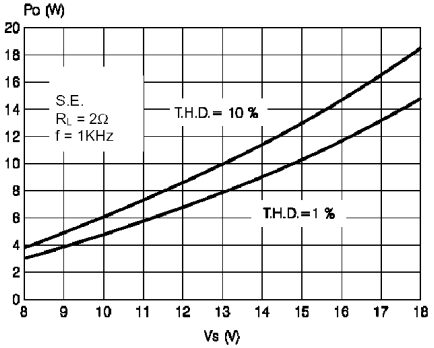



**Figure 12. Output Power vs. Supply Voltage**

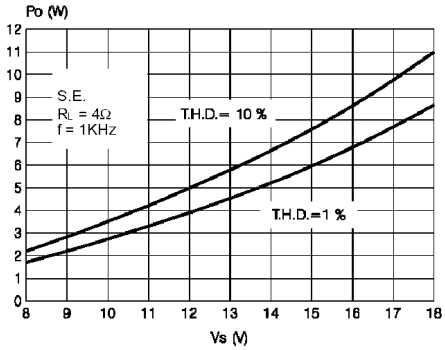



**Figure 13. OutputPower vs. Supply Voltage**

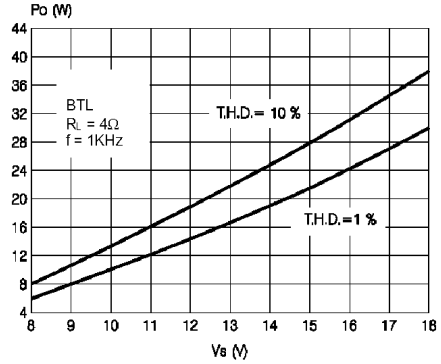



**Figure 14. Distortion vs. Output Power**

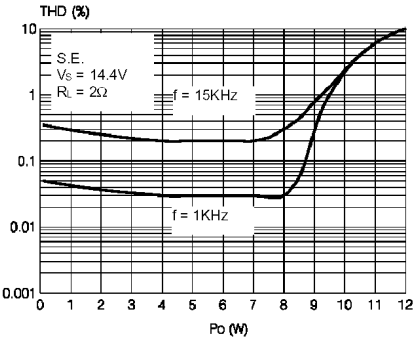


**Figure 15. Distortion vs. Output Power**

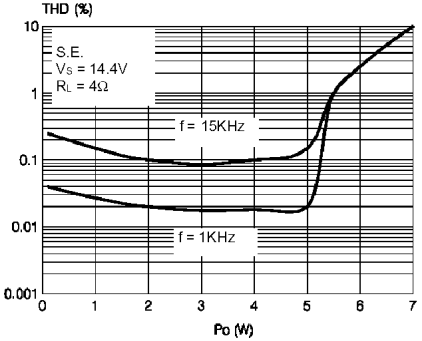



**Figure 16. Distortion vs. Output Power**

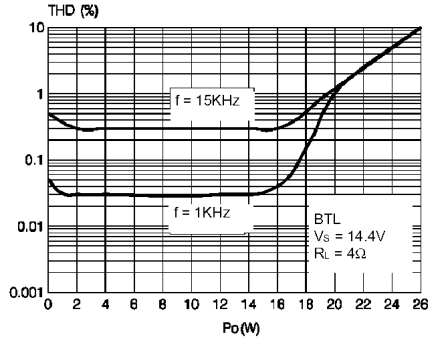



**Figure 17. Cross-talk vs. Frequency**

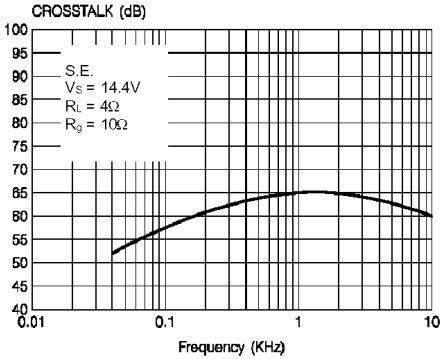



**Figure 18. Supply Voltage Rejection vs. Frequency**

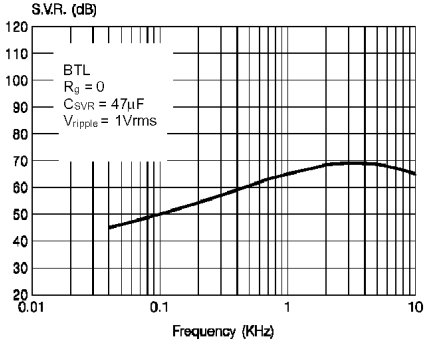



**Figure 19. Supply Voltage Rejection vs. Frequency**

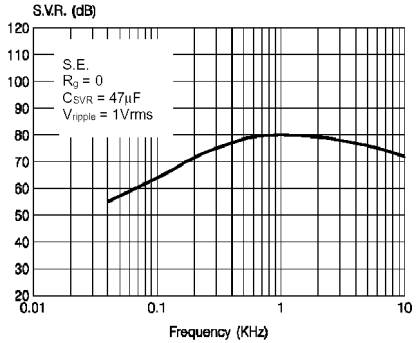



**Figure 20. Stand-by Attenuation vs. Threshold Voltage**

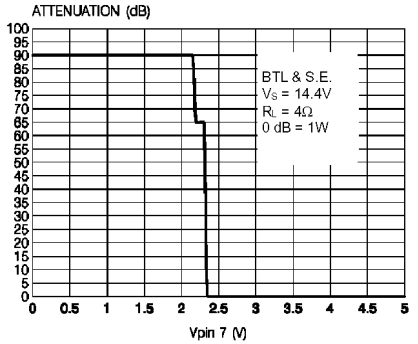


**Figure 21. Total Power Dissipation and Efficiency vs. Output Power**

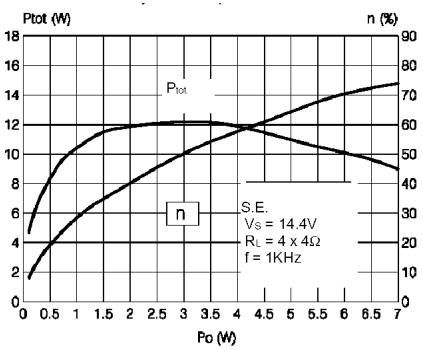
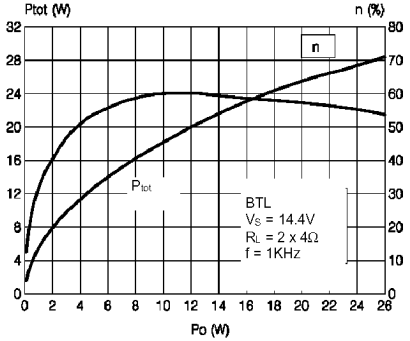



**Figure 22. Total Power Dissipation and Efficiency vs. Output Power**




# 5 GENERAL STRUCTURE

## 5.1 High Application Flexibility

The availability of 4 independent channels makes it possible to accomplish several kinds of applications ranging from 4 speakers stereo (F/R) to 2 speakers bridge solutions.

In case of working in single ended conditions the polarity of the speakers driven by the inverting amplifier must be reversed respect to those driven by non inverting channels. This is to avoid phase inconveniences causing sound alterations especially during the reproduction of low frequencies.

## 5.2 Easy Single Ended to Bridge Transition

The change from single ended to bridge configurations is made simply by means of a short circuit across the inputs, that is no need of further external components.

## 5.3 Gain Internally Fixed to 20dB in Single Ended, 26dB in Bridge

Advantages of this design choice are in terms of:

- componentsand space saving
- output noise, supply voltage rejection and distortion optimization.

## 5.4 Silent Turn On/Off and Muting/Stand-by Function

The stand-by can be easily activated by means of a CMOS level applied to pin 7 through a RC filter.

Under stand-by condition the device is turned off completely (supply current = 1μA typ.; output attenuation = 80dB min.). Every ON/OFF operation is virtually pop free. Furthemore, at turn-on the device stays in muting condition for a time determined by the value assigned to the SVR capacitor.

While in muting the device outputs becomes insensitive to any kinds of signal that may be present at the input terminals. In other words every transient coming from previous stages produces no unplesantacoustic effect to the speakers.

## 5.5 STAND-BY DRIVING (pin 7)

Some precautions have to be taken in the definition of stand-by driving networks: pin 7 cannot be directly

driven by a voltage source whose current capability is higher than 5mA. In practical cases a series resistance has always to be inserted, having it the double purpose of limiting the current at pin 7 and to smooth down the stand-by ON/OFF transitions - in combination with a capacitor - for output pop prevention.

In any case, a capacitor of at least 100nF from pin 7 to S-GND, with no resistance in between, is necessary to ensure correct turn-on.

### 5.6 OUTPUT STAGE

The fully complementary output stage was made possible by the development of a new component: the ST exclusive power ICV PNP.

A novel design based upon the connection shown in fig. 23 has then allowed the full exploitation of its possibilities. The clear advantagesthis new approach has over classical output stages are as follows:

#### 5.6.1 Rail-to-Rail Output Voltage Swing With No Need of Bootstrap Capacitors.

The output swing is limited only by the $V_{CEsat}$ of the output transistors, which is in the range of 0.3Ω ($R_{sat}$) each. Classical solutions adopting composite PNP-NPN for the upper output stage have higher saturation loss on the top side of the waveform.

This unbalanced saturation causes a significant power reduction. The only way to recover power consists of the addition of expensive bootstrap capacitors.

#### 5.6.2 Absolute Stability Without Any External Compensation.

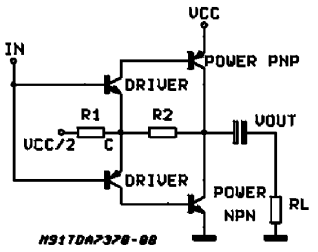
Referring to the circuit of fig. 23 the gain $V_{Out}/V_{In}$ is greater than unity, approximately 1+R2/R1. The DC output ($V_{CC}/2$) is fixed by an auxiliary amplifier common to all the channels.

By controlling the amount of this local feedbackit is possible to force the loop gain (A*β) to less than unity at frequency for which the phase shift is 180°. This means that the output buffer is intrinsically stableand not prone to oscillation.

Most remarkably, the above feature has been achieved in spite of the very low closed loop gain of the amplifier. In contrast, with the classical PNP-NPN stage, the solution adopted for reducing the gain at high frequencies makes use of external RC networks, namely the Boucherot cells.

### 5.7 BUILT–IN SHORTCIRCUIT PROTECTION

**Figure 23. The New Output Stage**



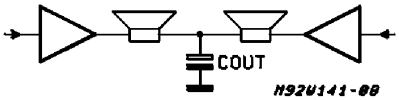

Reliable and safe operation, in presence of all kinds of short circuit involving the outputs is assured by BUILT-IN protectors. Additionally to the AC/DC short circuit to GND, to $V_S$, across the speaker, a SOFT SHORT condition is signalled out during the TURN-ON PHASE so assuring correct operation for the de-

vice itself and for the loudspeaker.

This particular kind of protection acts in a way to avoid that the device is turned on (by ST-BY) when a resistive path (less than 16 ohms) is present between the output and GND. As the involved circuitry is normally disabled when a current higher than 5mA is flowing into the ST-BY pin, it is important, in order not to disable it, to have the external current source driving the ST-BY pin limited to 5mA.

This extra function becomes particularly attractive when, in the single ended configuration, one capacitor is shared between two outputs (see fig. 24). Supposing that the output capacitor Cout for anyreason is shorted, the loudspeaker will not be damaged being this soft short circuit condition revealed.

**Figure 24. Single ended configuaration circuit**




### 5.7.1 Diagnostics Facility

The TDA7375 is equipped with a diagnostic circuitry able to detect the following events:

- Clipping in the output signal
- Thermal shutdown
- Output fault:
  - short to GND
  - short to VS
  - soft short at turn on

The information is available across an open collector output (pin 10) through a current sinking when the event is detected A current sinking at pin 10 is triggered when a certain distortion level is reached at any of the outputs. This function allows gain compression possibility whenever the amplifier is overdriven.

### 5.7.2 Thermal Shutdown

In this case the output 10 will signal the proximity of the junction temperature to the shutdown threshold. Typically current sinking at pin 10 will start ~10°C before the shutdown threshold is reached.

**Figure 25. Clipping Detection Waveforms**

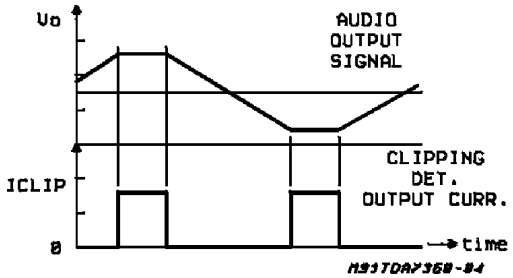


**Figure 26. Output Fault Waveforms (see fig. 27)**

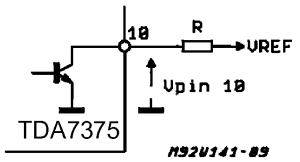
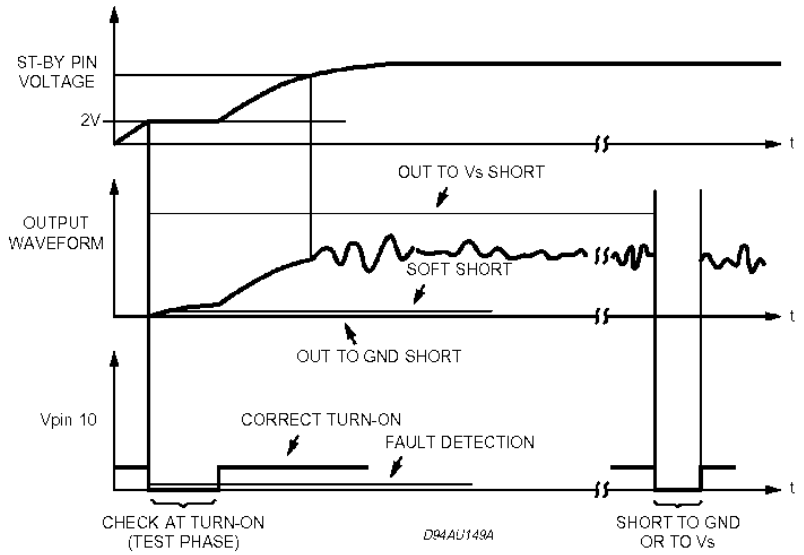



**Figure 27. Fault Waveforms**




### 5.8 HANDLING OF THE DIAGNOSTICS INFORMATION

As various kinds of information is available at the same pin (clipping detection, output fault, thermal proximity), this signal must be handled properly in order to discriminate each event.

This could be done by taking into account the different timing of the diagnostic output during each case.

Normally the clip detector signalling produces a low level at pin 10 that is shorter than that present under faulty conditions; based on this assumption an interface circuitry to differentiate the information is represented in the schematic of fig. 29.

**Figure 28. Waveforms**

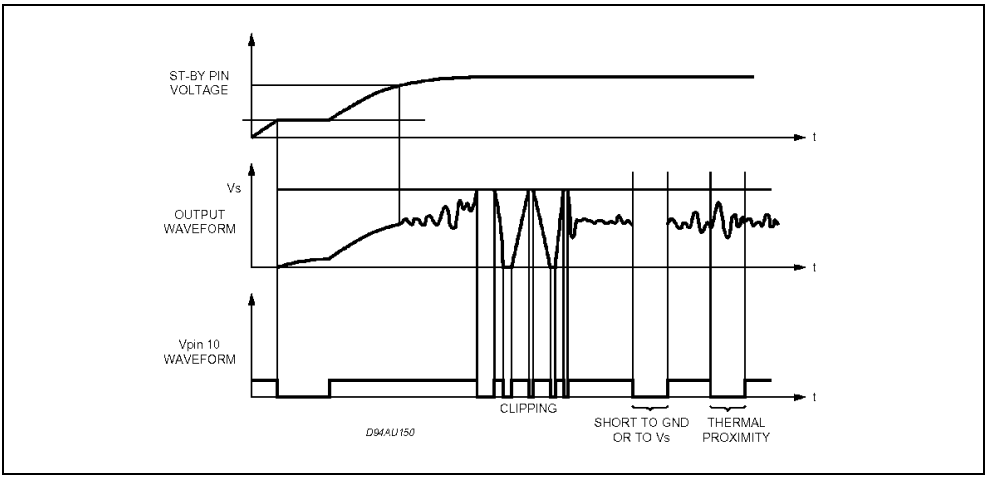
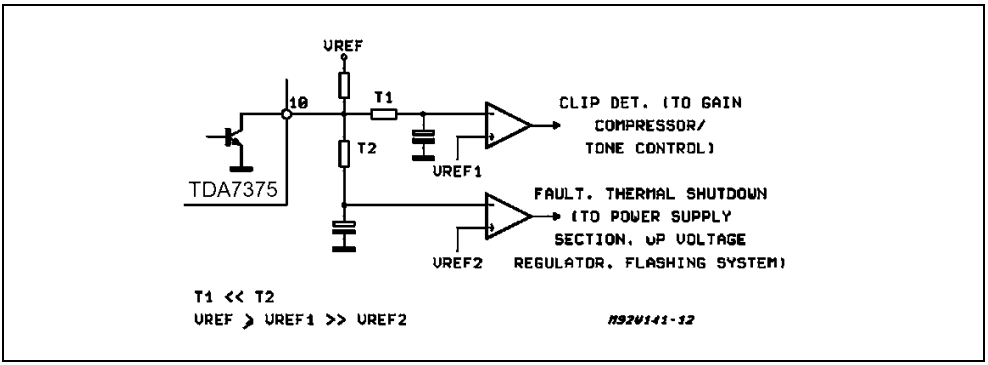



**Figure 29. Interface circuitry to differentiate the information schematic**




### 5.9 PCB-LAYOUT GROUNDING (general rules)

The device has 2 distinct ground leads, P-GND (POWER GROUND) and S-GND (SIGNAL GROUND) which are practically disconnected from each other at chip level. Proper operation requires that P-GND and S-GND leads be connected together on the PCB-layout by means of reasonably low-resistance tracks.

As for the PCB-ground configuration, a star-like arrangement whose center is represented by the supply-filtering electrolytic capacitor ground is highly advisable. In such context, at least 2 separate paths have to be provided, one for P-GND and one for S-GND. The correct ground assignments are as follows:

STANDBY CAPACITOR, pin 7 (or any other standby driving networks): on S-GND

SVR CAPACITOR (pin 6): on S-GND and to be placed as close as possible to the device.

INPUT SIGNAL GROUND (from active/passive signal processor stages): on S-GND.

SUPPLY FILTERING CAPACITORS (pins 3,13): on P-GND.

The (-) terminal of the electrolytic capacitor has to be directly tied to the battery (-) line and this should represent the starting point for all the ground paths.

## 6 PACKAGE INFORMATION

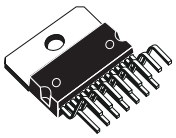
In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

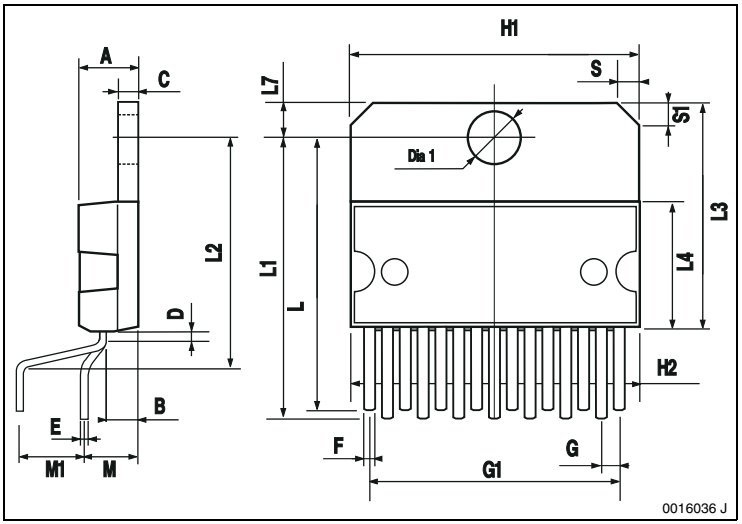
**Figure 30. Multiwatt 15 Mechanical Data & Package Dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A5 | | | | | | 0.197 |
| B | | | 2.65 | | | 0.104 |
| C | | | 1.6 | | | 0.063 |
| D | | 1 | | | 0.039 | |
| E | 0.49 | | 0.55 | 0.019 | | 0.022 |
| F | 0.66 | | 0.75 | 0.026 | | 0.030 |
| G | 1.02 | 1.27 | 1.52 | 0.040 | 0.050 | 0.060 |
| G1 | 17.53 | 17.78 | 18.03 | 0.690 | 0.700 | 0.710 |
| H1 | 19.6 | | | 0.772 | | |
| H2 | | | 20.2 | | | 0.795 |
| L | 21.9 | 22.2 | 22.5 | 0.862 | 0.874 | 0.886 |
| L1 | 21.7 | 22.1 | 22.5 | 0.854 | 0.87 | 0.886 |
| L2 | 17.65 | | 18.1 | 0.695 | | 0.713 |
| L3 | 17.25 | 17.5 | 17.75 | 0.679 | 0.689 | 0.699 |
| L4 | 10.3 | 10.7 | 10.9 | 0.406 | 0.421 | 0.429 |
| L7 | 2.65 | | 2.9 | 0.104 | | 0.114 |
| M | 4.25 | 4.55 | 4.85 | 0.167 | 0.179 | 0.191 |
| M1 | 4.73 | 5.08 | 5.43 | 0.186 | 0.200 | 0.214 |
| S | 1.9 | | 2.6 | 0.075 | | 0.102 |
| S1 | 1.9 | | 2.6 | 0.075 | | 0.102 |
| Dia1 | 3.65 | | 3.85 | 0.144 | | 0.152 |

**OUTLINE AND MECHANICAL DATA**



**Multiwatt15 (Vertical)**



# 7 REVISION HISTORY

**Table 5. Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| July 2004 | 2 | First Issue in EDOCS |
| March 2005 | 3 | Changed the Style-sheet in compliance to the new “Corporate Technical Pubblications Design Guide”.<br>Deleted package Multiwatt15 Horizontal. |
| 01-Jul-2008 | 4 | Updated the root part number in the title of the cover page.<br>Added Ecopack information in “PACKAGE INFORMATION” section. |
| 20-Sep-2013 | 5 | Updated Disclaimer. |