DS34LV87T Enhanced CMOS Quad Differential Line Driver

Check for Samples: DS34LV87T

FEATURES

- **Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation**
- **Interoperable With Existing 5V RS-422 Networks**
- **Ensured V_{OD} of 2V Min Over Operating Conditions**
- **Balanced Output Crossover for Low EMI (Typical Within 40 mV of 50% Voltage Level)**
- **Low Power Design (330 µW @ 3.3V Static)**
- **ESD ≥ 7 kV on Cable I/O Pins (HBM)**
- **Industrial Temperature Range**
- **Ensured AC Parameter:**
  - **Maximum Driver Skew: 2 ns**
  - **Maximum Transition Time: 10 ns**
- **Pin Compatible With DS26C31**
- **Available in SOIC Packaging**

Connection Diagram

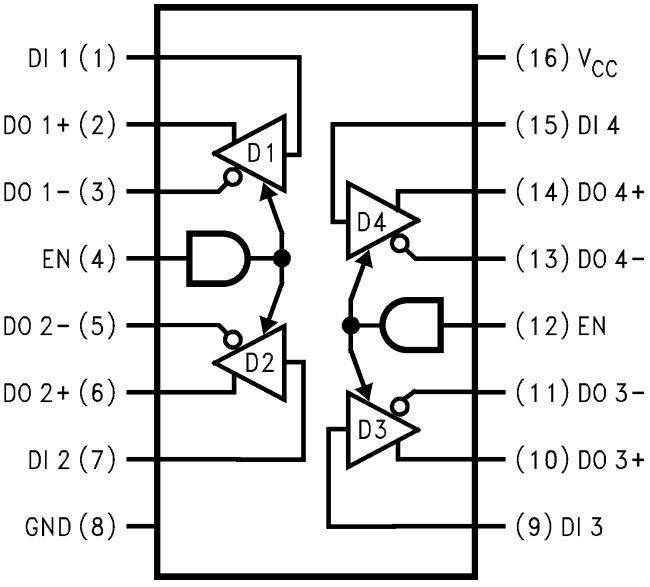


Figure 1. Dual-In-Line Package (Top View)
See Package Number D0016A

DESCRIPTION

The DS34LV87T is a high speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV87T features low static I_{CC} of 100 µA max which makes it ideal for battery powered and power conscious applications. The TRI-STATE enable, EN, allows the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning devices on or off.

Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI and EN) are compatible with LVTTL and LVCMOS devices. Differential outputs have the same V_{OD} (≥2V) ensure as the 5V version. The outputs have enhanced ESD Protection providing greater than 7 kV tolerance.

TRUTH TABLE(1)

Enables	Input	Outputs	
EN	DI	DO+	DO−
L	X	Z	Z
H	H	H	L
H	L	L	H

(1) L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})		−0.5V to +7V
Enable Input Voltage (EN)		−0.5V to V_{CC} + 0.5V
Driver Input Voltage (D_I)		−0.5V to V_{CC} + 0.5V
Clamp Diode Current		±20 mA
DC Output Current, per pin		±150 mA
Driver Output Voltage	(Power Off: DO+, DO−)	−0.5V to +7V
Maximum Package Power Dissipation @+25°C	D Package	1226 mW
Derate D Package		9.8 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range (Soldering, 4 sec.)		+260°C
ESD Ratings (HBM, 1.5k, 100 pF)	Driver Outputs	≥ 7 kV
	Other Pins	≥ 2.5 kV

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Units
Supply Voltage (V_{CC})		3.0	3.3	3.6	V
Operating Free Air	Temperature Range (T_A) DS34LV87T	−40	25	+85	°C
Input Rise and Fall Time				500	ns

ELECTRICAL CHARACTERISTICS(1)(2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Output Differential Voltage	R_L= ∞, (No Load)	DO+, DO−		3.3	4.0	V
V_{OD2}	Output Differential Voltage	R_L = 100Ω See Figure 2		2	2.6		V
ΔV_{OD2}	Change in Magnitude of Output Differential Voltage			−400	7	400	mV
V_{OD3}	Output Differential Voltage	R_L = 3900Ω (V.11), See Figure 2(3)			3.2	3.5	V
V_{OC}	Common Mode Voltage	R_L = 100Ω See Figure 2			1.5	2	V
ΔV_{OC}	Change in Magnitude of Common Mode Voltage			−400	6	400	mV
I_{OZ}	TRI-STATE Leakage Current	V_{OUT} = V_{CC} or GND Drivers Disabled			±0.5	±20	µA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V V_{IN} = V_{CC} or GND(4)		−40	−70	−150	mA
I_{OFF}	Output Leakage Current	V_{CC}= 0V, V_{OUT} = 3V			0.03	100	µA
		V_{CC} = 0V, V_{OUT} = −0.25V			−0.08	−100	µA
V_{IH}	High Level Input Voltage		DI, EN	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN}= V_{CC}				10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND		−10			µA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA				−1.5	V
I_{CC}	Power Supply Current	No Load, V_{IN} (all) = V_{CC} or GND	V_{CC}			100	µA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V_{OD1}, V_{OD2}, V_{OD3}.
(2) All typical values are given for V_{CC}= 3.3V and T_A = +25°C.
(3) This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.
(4) Only one output shorted at a time. The output (true or complement) is configured High.

SWITCHING CHARACTERISTICS(1)(2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 50 pF See Figure 3 and Figure 4	6	10.5	16	ns
t_{PLHD}	Differential Propagation Delay Low to High		6	11	16	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$			0.5	2.0	ns
t_{SK1}	Skew, Pin to Pin (same device)			1.0	2.0	ns
t_{SK2}	Skew, Part to Part(3)			3.0	5.0	ns
t_{TLH}	Differential Transition Time Low to High (20% to 80%)			4.2	10	ns
t_{THL}	Differential Transition Time High to Low (80% to 20%)			4.7	10	ns
t_{PHZ}	Disable Time High to Z	See Figure 5 and Figure 6		12	20	ns
t_{PLZ}	Disable Time Low to Z			9	20	ns
t_{PZH}	Enable Time Z to High			22	32	ns
t_{PZL}	Enable Time Z to Low			22	32	ns
f_{MAX}	Maximum Operating Frequency(4)			32		MHz

(1) f = 1 MHz, t_r and t_f ≤ 6 ns (10% to 90%).
(2) See TIA/EIA-422-B specifications for exact test conditions.
(3) Devices are at the same V_{CC} and within 5°C within the operating temperature range.
(4) All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is ensured by design and characterization.

PARAMETER MEASUREMENT INFORMATION

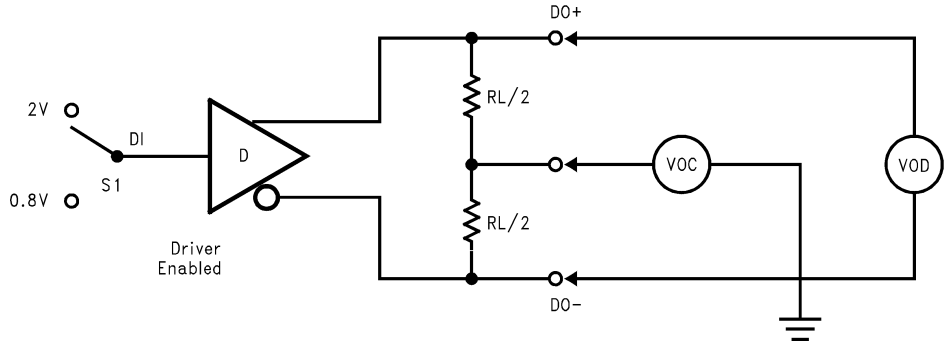


Figure 2. Differential Driver DC Test Circuit

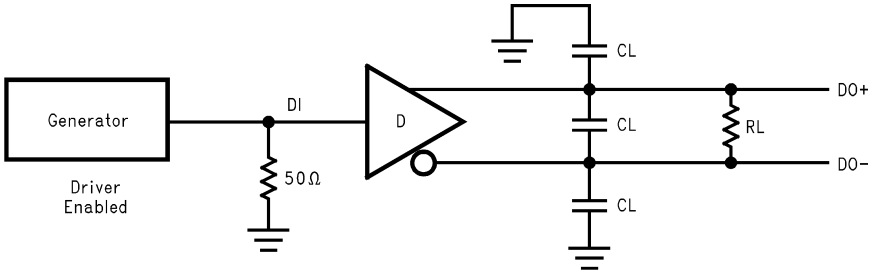
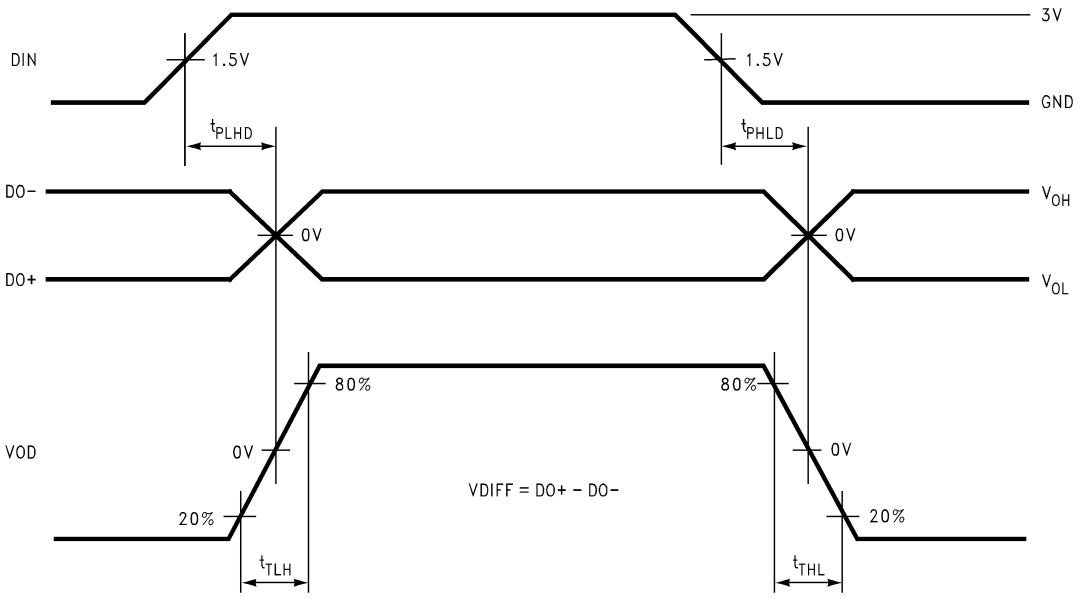


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit



Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_o = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

C_L includes probe and fixture capacitance.

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

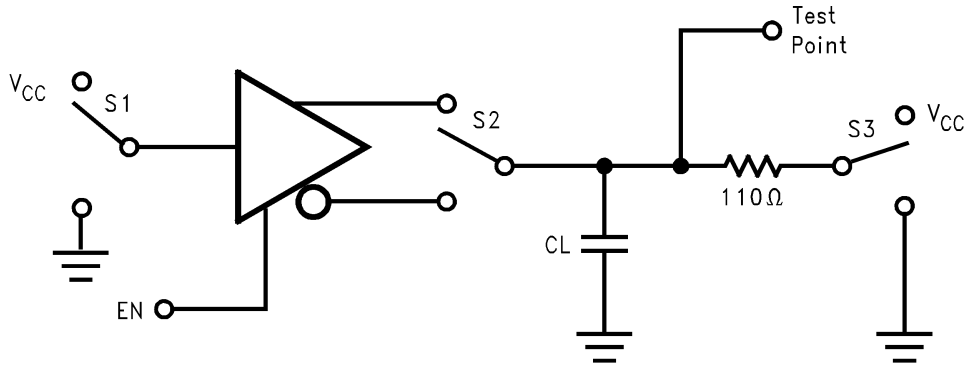


Figure 5. Driver Single-Ended Tri-state Test Circuit

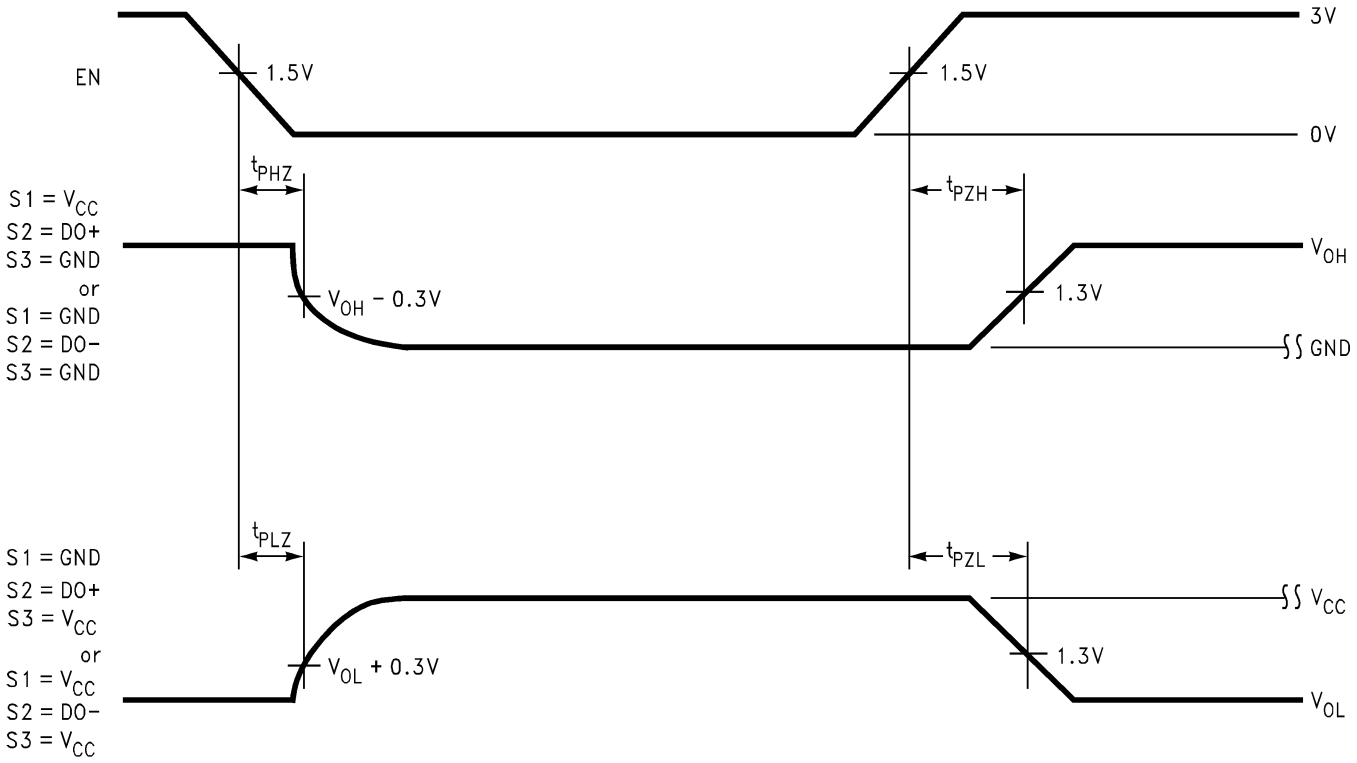


Figure 6. Driver Single-Ended Tri-state Waveforms

TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423(SNLA137)
- A Comparison of Differential Termination Techniques(SNLA304)

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in parallel with 0.01 µF at the power supply pin. A 10 µF or greater tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

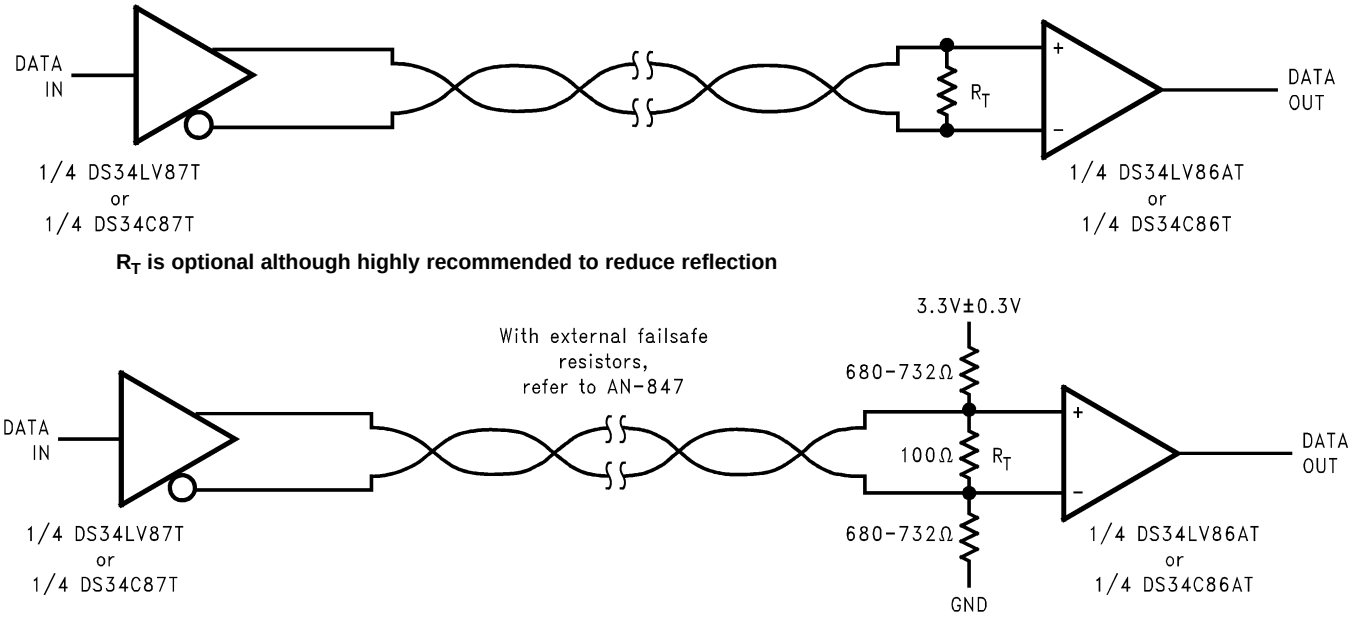


Figure 7. Typical Driver Connection

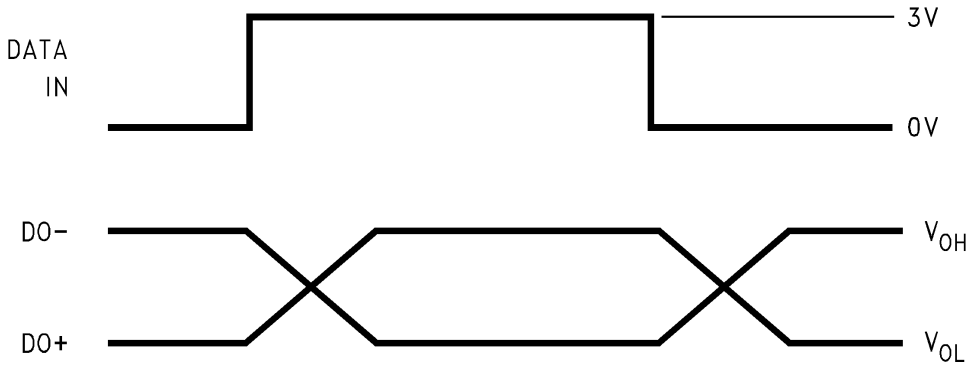


Figure 8. Typical Driver Output Waveforms

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34LV87TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS34LV87 TM	
DS34LV87TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM	Samples
DS34LV87TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS34LV87 TM	
DS34LV87TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

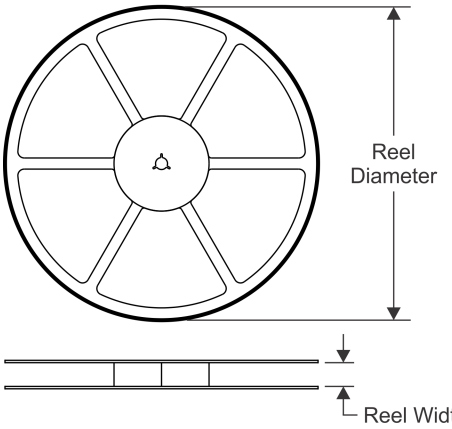
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

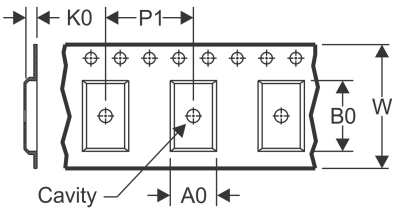
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

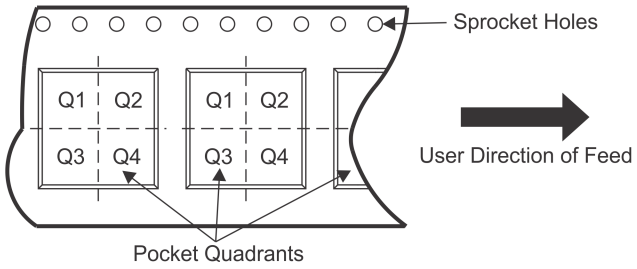


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

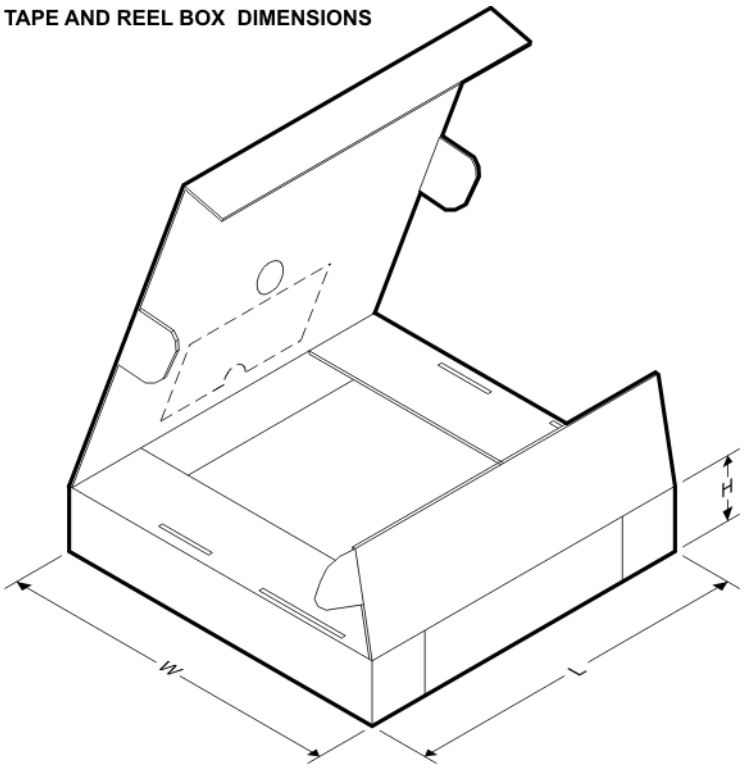
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34LV87TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS34LV87TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

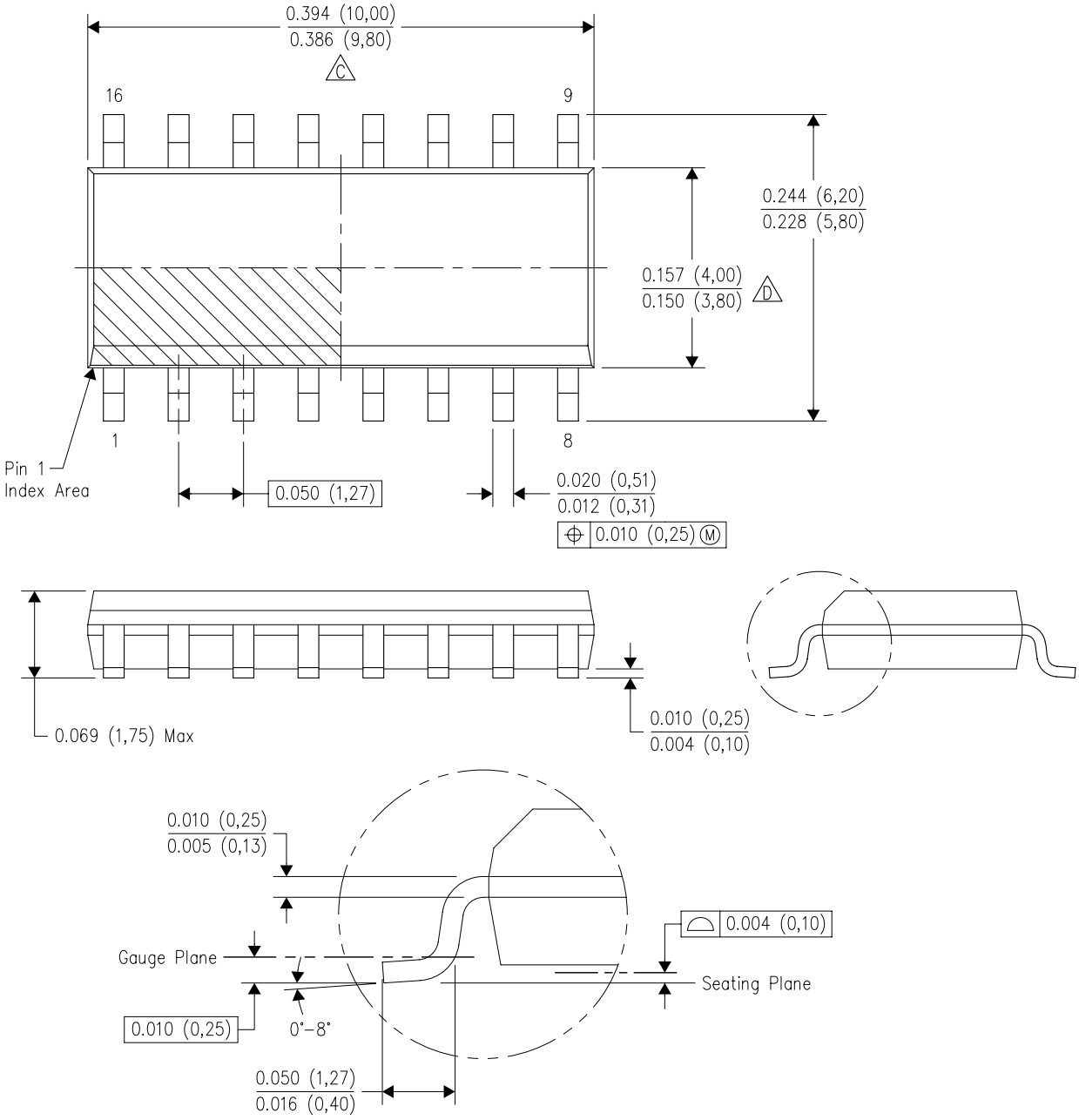
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34LV87TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS34LV87TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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