Rev: 030508

DS33X11 Demo Kit

General Description

The DS33X11 demo kit (DK) is an easy-to-use evaluation board for the DS33X11 Ethernet-over-PDH device. The demo kit contains an option for either T3/E3 or T1/E1 serial links. All PDH links are complete with line interface, transformers, and network connections. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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Ordering Information

PART	TYPE
DS33X11DK	Demo card, T3/E3, T1/E1

Demo Kit Contents

DS33X11DK Main Board
CD-ROM Includes:
- ChipView Software and Manual
- DS33X11DK Data Sheet
- Configuration Files

Features

- **Demonstrates Key Functions of DS33X11 Ethernet Transport Chipset**
- **Includes DS26521 T1/E1 SCT, DS3170 T3/E3 SCT, Transformers, BNC, and RJ48 Network Connectors and Termination**
- **Includes Ethernet PHY Supporting 10/100 and Gigabit Modes**
- **Provides Support for Hardware and Software Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33X11, DS26528, DS3170, and PHY Registers**
- **All DS33X11 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

Demo Kit Board

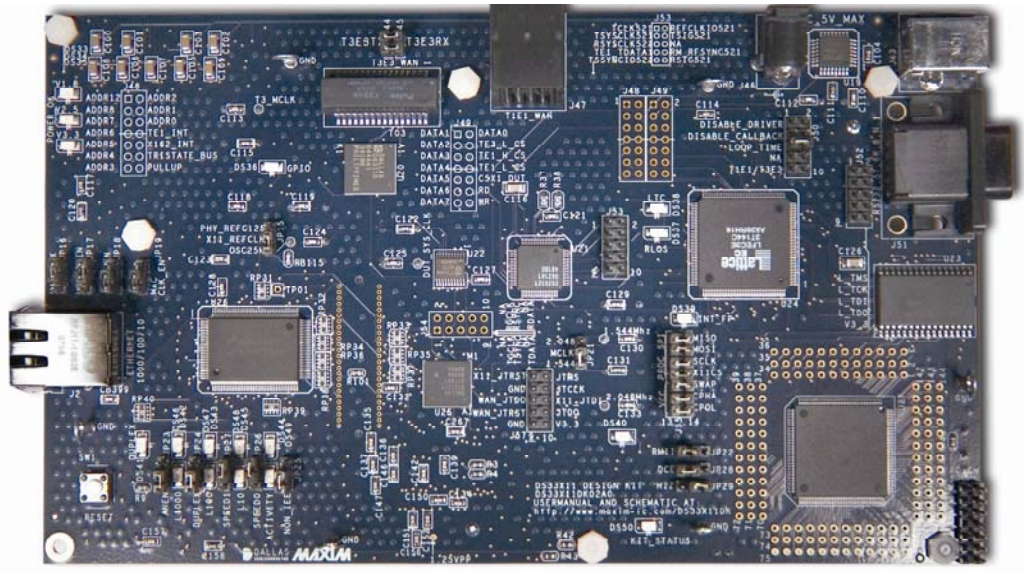

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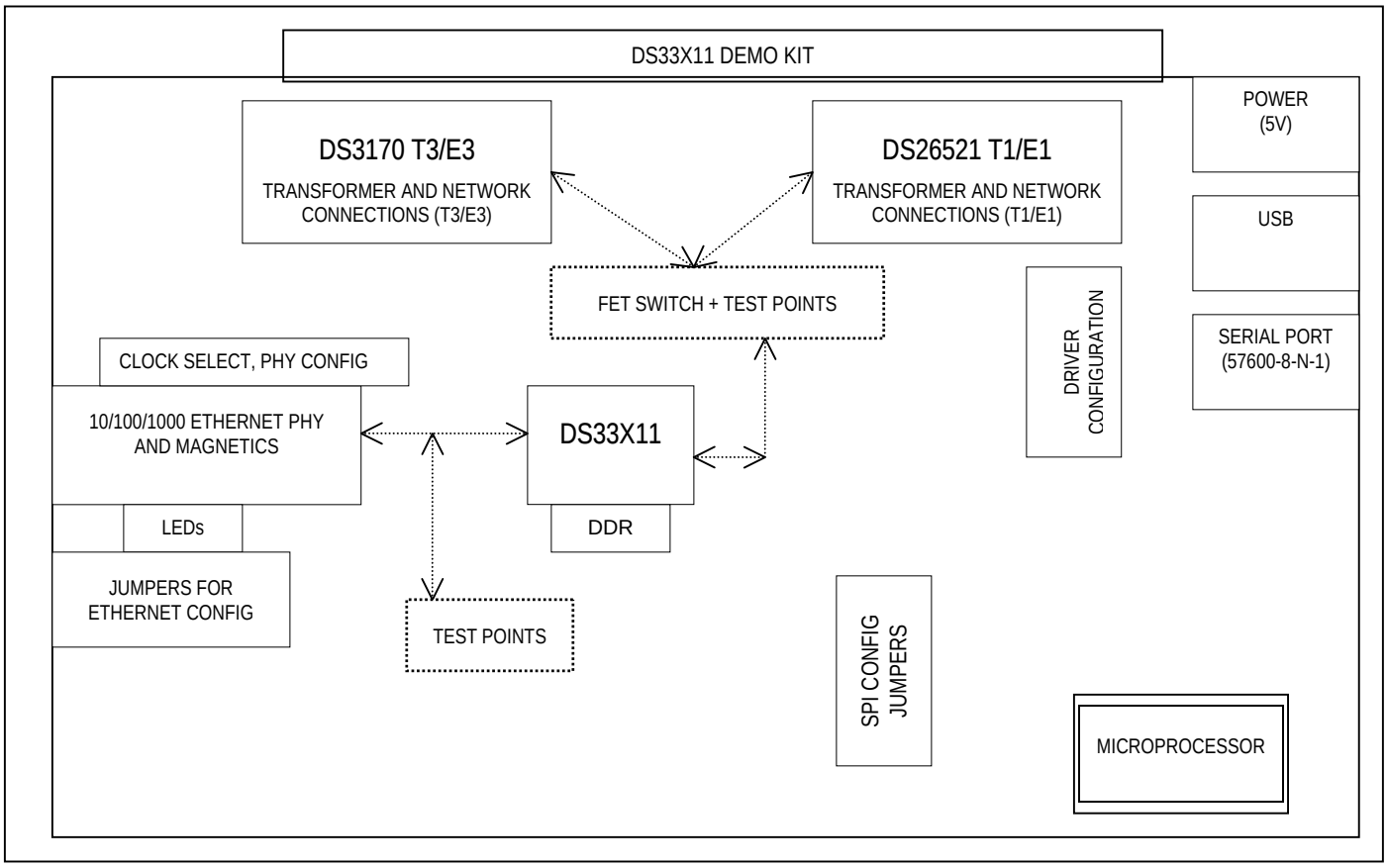
Figure 1-1. DS33X11 System Floorplan



2. PCB Errata

DS33X11DK01A0 board errata:

- SSTL_TESTI pin should have been pulled high (done via rework).
- Needs a reset controller (added by rework).
- Silkscreen at JP21 was backwards (fixed by swapping oscillators to make silkscreen correct).
- Three-pin bias jumpers are missing +- silkscreen.

DS33X11DK02A0 board errata:

- There are no errata for DS33X11DK02A0.

3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD-ROM and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33X11DK.

All locations are given relative to the top directory of the CD-ROM/zip file. The DS33X11, DS3170, and DS26521 register definition files and configuration files are listed in Table 3-1.

Table 3-1. File Details

FILE NAME	FILE USAGE
.\DS33X11_cfg_demo_gui_ds33x161_GlobalMicroport.def	Top-level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33X11. (Note that the wan files still need to be loaded (either DS).)
.\DS33X11_cfg_demo_gui\ds33x161_Lan.def .\DS33X11_cfg_demo_gui\ds33x161_BufferMan.def .\DS33X11_cfg_demo_gui\ds33x161_EncapDecap.def .\DS33X11_cfg_demo_gui\ds33x161_Vcat.def .\DS33X11_cfg_demo_gui\ds33x161_SerialPort.def	DS33X11 dependent files. These are called by the _ds33x161_GlobalMicroport.def file listed above.
.\DS33X11_cfg_demo_gui\ds33x11_lan_T3wan_ext.mfg	File for manually configuring the DS33X11 to interface with the DS3170.
.\DS33X11_cfg_demo_gui\ds33x11_lan_T1wan_ext.mfg	File for manually configuring the DS33X11 to interface with the DS26521.
.\DS33X11_cfg_demo_gui\x11_wan1.eset	GUI interface for loading settings when running the Xchip plug-in (launched from the **Tools** menu of the ChipView program).
.\DS33X11_cfg_demo_gui\te3_ds3170\ds3170_evbrd.def	Top-level definition file to select the DS3170 T3/E3 transceiver. This file will autoload the remaining definition files for the DS3170.
.\DS33X11_cfg_demo_gui\te3_ds3170\misc1_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\feac_frac_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\ttrace_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\ds3_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\e3751_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\e3832_p1.def .\DS33X11_cfg_demo_gui\te3_ds3170\port1.def	DS3170 dependent files. These are called by the ds3170_evbrd.def file listed above.
.\DS33X11_cfg_demo_gui\te3_ds3170\70_t3_sct_needscoaxlb.mfg	Configuration file for T3 mode.
.\DS33X11_cfg_demo_gui\ds26521\DS26521_GLOBAL_T1.def	Top-level definition file to select the DS26521 T1/E1 transceiver. This file will autoload the remaining definition files for the DS26521.
.\DS33X11_cfg_demo_gui\ds26521\DS26521_1_LIU_BERT.def .\DS33X11_cfg_demo_gui\ds26521\DS26521_1_T1.def	DS26521dependent files. These are called by DS26521_GLOBAL_T1.def file listed above.
.\DS33X11_cfg_demo_gui\ds26521\t1_config.mfg	Configuration file for T1 mode.

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the demo kit (DK) software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect the PCB power jack to the wall adapter.
- Connect the RS232 serial cable or USB cable between the host PC and the demo kit.
- Verify that the jumpers are configured as described in Table 5-1.

4.1.1 General

- Upon power-up the power LEDs (DS33, DS34, DS35 green) will be lit. Transceiver RLOS + LTC LED (DS38, DS37 red) will be lit.
- PHY LINK LED (DS07 green) should be lit if the Ethernet is connected. Ensure that the JP15 (DS33X11 RefClk) setting matches link mode. For Gigabit mode JP15 should be set to drive RefClk with 125MHz. For 10/100Mb modes, RefClk should be driven with 25MHz.

Following are several basic system initializations.

4.2 Basic DS33X11 Initialization

This section covers three basic methods for configuring the DS33X11.

1) Device Driver-Based Configuration. If the pins J50.1+J50.2 are unjumpered, the device driver will auto configure the DS33X11 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Refer to the device driver documentation for further details.
2) Register-Based Configuration—T1 Mode
    a) Install jumper J50.1+J50.2 to disable device drivers, and then reset the board. Ensure that J50.9+J50.10 is not installed.
    b) Launch **ChipView.exe** and select **Register View**.
    c) When prompted for a definition file, pick the file named **_ds33x161_GlobalMicroport.def**, Six additional definition files will load.
    d) Go to the **File** menu and select **File→Definition File**. When prompted, select **DS26521_GLOBAL_T1.def**.
    e) Go to the **File** menu and select **File→Memory Config File→Load .MFG** file. When prompted, select the file named **ds33x11_lan_T1wan_ext.mfg**.
    f) Go to the **File** menu and select **File→Memory Config File→Load .MFG** file. When prompted, select the file named **t1_config.mfg**.
3) Register-Based Configuration—T3 Mode
    a) Install Jumper J50.1+J50.2 to disable device drivers, and then reset the board. Ensure that J50.9+J50.10 is installed.
    b) Launch **ChipView.exe** and select **Register View**.
    c) When prompted for a definition file, pick the file named **_ds33x161_GlobalMicroport.def**. Six additional definition files will load.
    d) Go to the **File** menu and select **File→Definition File**. When prompted select **ds3170_evbrd.def**.
    e) Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **ds33x11_lan_T3wan_ext.mfg**.
    f) Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **70_t3_sct_needscoaxlb.mfg**.

4.2.1 Additional Configuration for DS33X11

- Using a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the T1E1 network side; RLOS and LTC LEDs should go out (DS38, DS37).
- At this point any packets sent to the DS33X11 are echoed back. Incoming packets (i.e., ping) should cause the **Activity LED** to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is *not* recommended. The ping command goes through the computer's TCPIP stack and sometimes will not be sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a PC with only one adapter cannot ping itself (a local ping gets sent to "local host" instead of out the connector). However, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at www.tamos.com/products/commview.
- Wireshark is an excellent (and free) packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating -system-based network traffic is sent out of the default adapter; usually this is the adapter that has recently had connection to a live network.

5. LEDs, Configuration Switches, Jumpers, and Connectors

The DS33X11DK has several configuration switches, oscillators, and jumpers. Table 5-1 provides a description of these signals, given in order of appearance on the PC board, from top to bottom and then left to right (with the board held so that the RS232 and USB connectors are on the right-hand side of the board).

Table 5-1. Main Board PCB Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J44+J45	WAN Network Connection	—	40	T3/E3 jumpers for network interface. Used with 2-pin coax adapter (provided).
J47	WAN Network Connection	—	42	T1/E1 RJ45 connector for network interface.
J46	Power Jack	—	28	System power. Always connected to 5V wall adapter (provided).
J43	USB	—	32	USB interface.
J51	RS232 DB9 Connector	—	32	RS232 DB9 connector, operates in ASCII mode at 57.6K,8,N,1.
DS33, DS34, DS35	LED	ON	35	Power OK LEDs for 1.8V, 2.5V, and 3.3V power supplies. All three LEDs must be lit.
J48+J49	Test Points	Not used	42	Address Data Bus Test Points. See Section 6.2 regarding control by external processor. Silkscreen for these signals is provided a few inches to the left of the signals.
YB08 (PCB solder side)	Oscillator	—	40	Oscillator for T3/E3 MCLK. Silkscreen and target are provided on top side of PCB.
DS36	LED	User setting (OFF)	40	DS3170 general-purpose I/O LED. Not configured by ini files.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J50	Configuration	• P1+P2: Jumper to enable drivers (remove to disable drivers). • P3+P4: Jumper to enable interrupt handlers (this jumper is only valid when drivers are enabled). • P5+P6: Jumper to set for looptime—WAN TxClock driven by RxClock. Remove to set for source time WAN TxClock driven by oscillator (this jumper is only valid when drivers are enabled). • P7+P8: Reserved, currently has no impact on system. • P9+P10: Jumper to enable T3/E3 mode, remove jumper to set T1/E1 mode. This jumper controls FET switches U22 and UB34.		
J52	FPGA JTAG	Not used	34	JTAG Test Points for Lattice FPGA. Not shared with other devices.
J53	Test Point	—	41	DS26521 Test Points (see silkscreen at top of board). TCLK, REFCLKIO, TSYSCLK, TSIG, RSYSCLK, TSSYNCIO, TSER, RM_RFSYNC, RSIG.
DS37–DS38	DS26521 LEDs	—	41	DS26521 LTC and RLOS Pins. Should be off when configured and connected to another device. Check TCLK setting if LEDs flicker on/off.
JP16	Bias PHY ManMDIX	Jumper P1+2 (high)	37	Default MDIX Setting. P1+2 PHY is set to straight mode; P2+3 PHY is in crossover mode.
JP17	Bias PHY MultiEn	Jumper P1+2 (high)	37	PHY Advertisement Setting. P2+3 selects multiple node priority (switch or hub). P1+2 selects single node priority (NIC).
JP18	Bias PHY MdixEn	Jumper P2+3 (low)	37	P2+3 enables pair swap mode. P1+3 disables pair swap mode.
JP19	Bias PHY MacClkEn	Jumper P2+3 (low)	37	P2+3 PHY clock to MAC output is enabled. P1+2 PHY clock to MAC output is disabled.
JP20	PHY Clock In	Jumper P1+2 (high)	38	PHY Clock Input. Always set for P1+2, driving PHY with 25MHz oscillator. Setting P2+3 would drive with DS33X11 RefClk and work in MII mode, but not in GMII mode (this jumper is removed in DS33X11DK02A0).
YB09 (PCB solder side)	125MHz Oscillator	Not populated	24	125MHz Oscillator. Can be jumpered to DS33X11 RefClk. This oscillator is not populated. In GMII mode RefClk is driven by PHY clock out (using jumper JP101).
YB10 (PCB solder side)	25MHz Oscillator	—	24	25MHz Oscillator. Used for PHY clock in (MII+GMII). Used for DS33X11 RefClk in MII mode.
YB11	125MHz Oscillator	—	24	DS33X11 SysClock.
JB05+JB04 (PCB solder side)	Connector/Test Points	—	36	Test Points for interface signals between PHY and DS33X11.
J54	DS33X11 Test Points	—	22	Test Points for RGCLK, RSYNC, RDAT, TGCLK, TSYNC, TDAT.
JP15, JP101	DS33X11 RefClk	JP15.1+JP15.2, JP101 installed	24	JP15 selects DS33X11 RefClk source: • JP15.1+2 to select PHY MacClkOut (GMII mode). • JP15.2+3 to select 25MHz oscillator (MII mode). JP101 should always be installed as it connects MacClkOut to JP15.1.
J2	Ethernet Connection	—	38	RJ45 Ethernet Connector. Used in 10/100 and Gigabit modes.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
JP26	Bias PHY ANEN	Jumper P2+3 (high)	38	Jumper P2+3 to enable auto negotiation.
JP24	Bias PHY Duplex	Jumper P2+3 (high)	38	Jumper P2+3 to enable full duplex. Jumper P1.2 to force half duplex.
JP27+JP26	Bias PHY Speed1 + Speed0	Jumper P1+2 (low) P1+2 (low)	38	If auto negotiation is enabled, this setting advertises capability for 10/100/1000 speeds. If auto negotiation is disabled, this setting forces 10Mb mode.
JP25	Bias PHY NonIEEE	Jumper P2+3 (high)	38	Jumper P2+3 to enable IEEE-compliant operation.
DS41	LED Duplex	—	36	LED is on in full-duplex mode.
DS46+42 DS47+43 DS48+45	LED Link Speed	1 of the 6 should be lit (when linked)	36	LED to indicate link speed—1000Mbps, 100Mbps, or 10Mbps. Only one of the six LEDs should be lit. See the JP15+JP101 description for setting in GMII vs. MII mode.
DS44+39	LED Activity	—	36	Flashes for PHY TX-RX activity.
J57	JTAG	Jumpered P1+3 P7+9	27	JTAG for DS33X11, DS26521, and DS3170. DS33X11 can be isolated from DS26521 and DS3170. Jumpers on P1+3 and P7+9 prevent the devices from entering JTAG mode.
JP21	DS26521 MCLK Select	Jumpered P2+3	42	Jumper P2+3 for 1.544MHz.
YB12, YB13				Jumper P1+2 for 2.048MHz.
J55.1–J55.8	DS33X11 SPI Test Points	Jumpered P1+2 P3+4 P5+6 P7+8	27	SPI Test Points for DS33X11. The first four jumpers are installed to connect the DS33X11 to the processor SPI port (MISO, MOSI, SCLK, CS).
J55.9+J55.10	DS33X11 Bias SPI SWAP	Jumpered P9+10 (high)	27	Processor default is to transfer MSB first. Jumper P9+10 to match this setting.
J55.11–J55.14	DS33X11 Bias SPI CPHA Bias SPI CPOL	Both jumpered	27	Processor default is to have normal phase and idle high. See the SPI section (Section 6.3) for further detail.
DS40	LED	—	27	DS33X11 interrupt LED.
JP22	DS33X11 Bias RMII	Jumpered P1+2 (low)	27	Jumper P1+2 for MII mode. Jumper P2+3 for RMII mode (RMII mode is not available in this demo kit).
JP28	DS33X11 Bias DCE	Jumpered P1+2 (low)	27	Jumper P1+2 for DTE mode. Jumper P2+3 for DCE mode. (This demo kit does not support DCE mode.)
J58	OnCe	Not used	32	OnCe debug connector for MMC2107 microcontroller.
JB06 (PCB solder side)	Flash VPP	Not used	32	For programming flash memory.
DS50	LED	ON	32	LED to display kit status. Should be on.

6. Register Access

6.1 Address Map

The external device address space begins at 0x81000000. All offsets given in Table 6-1 are relative to this offset.

Table 6-1. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification.
0X1000 to 0X1FFF	—	Reserved.
0X4000 to 0X5FFF	DS26521	DS26521 T1/E1 device. Uses CS_X2.
0X8000 to 0X9FFF	DS3170	DS3170 T3/E3 device. Uses CS_X4.

All device registers can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

6.2 Control Through External Processor

The demo kit is intended to be controlled using the on-board microcontroller and a host PC. However, the demo kit has jumper points to allow it to be controlled by an external processor. The DS33X11 can be controlled in SPI mode by attaching to the signals at J55 pins 2, 4, 6, 8. The transceivers (DS26521 and DS3170) can be controlled by jumpering J49.12+14. Doing so pulls up the tristate_bus signal and places the FPGA in a high-impedance mode (see the Address Map section).

6.3 SPI Mode

The DS33X11 uses SPI mode and is addressed differently than devices that use a parallel address/data bus. The DS33X11 does not have an address offset. Its base address starts at 0x00. Table 5-1 details the default bias levels for SPI configuration pins. To change these settings the processor's SPI settings must also change. The processor SPI settings can be changed in ChipView's terminal mode using the **SPISG S** function.

6.4 MAC and PHY Registers

The MAC and PHY are accessed indirectly. This process is automated by the indirect register module. To load this module, first select the DS33X162 device driver demo plugin using the **Tools→Plugins** menu. Once the device driver demo loads, select the indirect register module from the **Tools→Indirect register** menu. The first tab of the menu has a selection for the device bus mode. Select **SPI mode** when using the DS33X11.

To test that the indirect register section is working, try to reset the PHY. Select the **PHY** tab, change the **Padd** field to 00001 to select the PHY at MDIO address 1. In the **Data write** field enter 00 00 80 00. Click the **Write PHY** button. At this point the link LED of the PHY should go out (and turn back on in a few seconds).

7. Additional Information/Resources

7.1 DS33X11 Information

For more information about the DS33X11, refer to the DS33X11 data sheet available on our website at www.maxim-ic.com/DS33X11.

7.2 DS33X11DK Information

For more information about the DS33X11DK, including software downloads, refer to the DS33X11DK data sheet available on the our website at www.maxim-ic.com/DS33X11DK.

7.3 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

8. Component List

Table 8-1 shows the component list for the DS33X11 and DS33X162 demo kits and resource cards. This BOM contains the part listing for four boards. These boards are the DS33X11DK, DS33X162DK, DualPhyRC, and GigPhyRC. Each reference designator is only used once. For example, U25 only appears on the DS33X11DK and is not used on any of the other boards. See Table 5-1.

Table 8-1. Component List

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C02, C22, C145, CB19, CB23, CB42, CB95, CB129, CB303, CB319, CB445, CB447, CB452, CB460, CB463	15	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
Reference designators shown on next row	231	0603 CERAM 4.7uF 6.3V MULTILAYER	UNK	ECJ-1VB0J475M
C03, C08, C11, C14, C15, C16, C17, C21, C24, C29, C33, C45, C49, C51, C52, C91, C92, C96, C97, C115, C119, C120, C122, C123, C129, C137, C138, C141, C142, C146, C149, C151, C153, C158, C258, C263, C265, CB01, CB04, CB06, CB09, CB13, CB16, CB17, CB21, CB24, CB26, CB27, CB28, CB36, CB37, CB41, CB44, CB45, CB46, CB47, CB48, CB58, CB60, CB66, CB67, CB74, CB75, CB76, CB78, CB80, CB84, CB92, CB93, CB98, CB99, CB100, CB104, CB107, CB114, CB115, CB116, CB118, CB123, CB125, CB126, CB137, CB138, CB141, CB144, CB151, CB155, CB158, CB163, CB164, CB166, CB170, CB171, CB172, CB179, CB181, CB183, CB185, CB186, CB188, CB189, CB191, CB192, CB193, CB195, CB197, CB198, CB201, CB204, CB209, CB215, CB218, CB221, CB222, CB227, CB229, CB230, CB231, CB234, CB235, CB239, CB243, CB249, CB251, CB255, CB258, CB263, CB264, CB267, CB270, CB271, CB273, CB276, CB277, CB278, CB284, CB287, CB293, CB294, CB297, CB298, CB302, CB304, CB306, CB307, CB320, CB322, CB327, CB328, CB341, CB343, CB344, CB345, CB347, CB348, CB351, CB352, CB353, CB357, CB358, CB364, CB365, CB366, CB367, CB369, CB370, CB371, CB375, CB376, CB379, CB380, CB388, CB392, CB393, CB395, CB396, CB399, CB400, CB401, CB404, CB405, CB406, CB407, CB408, CB409, CB415, CB416, CB423, CB424, CB425, CB427, CB431, CB436, CB438, CB441, CB442, CB446, CB449, CB453, CB454, CB462, CB467, CB760, CB766, CB768, CB777, CB779, CB789, CB790, CB791, CB792, CB793, CB795, CB798, CB802, CB804, CB805, CB807, CB808, CB810, CB812, CB813, CB815, CB816, CB817, CB818, CB824, CB827, CB856, CB857, CB859				
Reference designators shown on next row	114	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C04, C05, C06, C07, C09, C10, C18, C20, C32, C37, C40, C41, C42, C50, C57, C70, C89, C98, C104, C113, C114, C118, C125, C133, C134, C136, C148, C150, C261, C266, CB03, CB11, CB14, CB20, CB30, CB34, CB52, CB55, CB61, CB69, CB71, CB73, CB83, CB103, CB109, CB112, CB119, CB120, CB128, CB139, CB150, CB157, CB161, CB167, CB173, CB187, CB194, CB205, CB206, CB207, CB213, CB216, CB217, CB219, CB223, CB224, CB225, CB228, CB240, CB256, CB259, CB261, CB275, CB285, CB295, CB300, CB308, CB332, CB350, CB354, CB359, CB361, CB381, CB385, CB391, CB398, CB402, CB413, CB414, CB419, CB428, CB432, CB435, CB439, CB443, CB444, CB448, CB451, CB466, CB468, CB761, CB765, CB770, CB771, CB772, CB776, CB794, CB803, CB806, CB811, CB819, CB823, CB853, CB855				
C110, C112, CB86, CB87	4	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C156, C259, CB51, CB762, CB763, CB764, CB767, CB769, CB773, CB774, CB775, CB780, CB782, CB786, CB787, CB788	16	0603 CERAM 0.1uF 16V 10%	Phycomp	06032R104K7B20D
C25, C126, CB10, CB31, CB33, CB88, CB89, CB102, CB145, CB146, CB147, CB315, CB333, CB338, CB363, CB368, CB383, CB417, CB418, CB437	20	L_1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
C28, C31, C132, CB25, CB32, CB35, CB38, CB40, CB43, CB56, CB68, CB81, CB85, CB96, CB105, CB313, CB321, CB324, CB372, CB373, CB384, CB394, CB397, CB410, CB411, CB412, CB422, CB450	28	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K
C39, C44, C54, C55, C56, C60, C61, C64, C99, C100, C101, C102, C103, C105, C106, C107, C108, C109	18	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C58, C63, C67, C69, C73, C76, C77, C86, C87, CB108, CB153, CB208, CB238, CB252, CB253, CB254	16	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
C59, C62, C65, C66, C68, C71, C72, C75, C78, C79, C80, C81, C82, C83, C84, C85, C116	17	1206 CERAM 560pf 50V 5%	AVXZ	12065A561JAT2A
Reference designators shown on next row (begins with C01)	226	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C01, C12, C13, C19, C23, C26, C27, C30, C34, C35, C36, C38, C43, C46, C47, C48, C53, C74, C88, C90, C93, C94, C95, C111, C117, C121, C124, C127, C128, C130, C131, C135, C139, C140, C143, C144, C147, C152, C154, C155, C157, C260, C262, C264, CB02, CB05, CB07, CB12, CB18, CB22, CB29, CB39, CB49, CB53, CB57, CB59, CB62, CB63, CB64, CB65, CB70, CB72, CB77, CB79, CB82, CB90, CB91, CB94, CB97, CB101, CB106, CB110, CB111, CB113, CB117, CB121, CB122, CB124, CB130, CB131, CB132, CB133, CB134, CB135, CB136, CB140, CB142, CB148, CB149, CB152, CB154, CB156, CB159, CB160, CB162, CB165, CB168, CB169, CB174, CB175, CB176, CB177, CB178, CB180, CB182, CB184, CB190, CB196, CB199, CB200, CB202, CB203, CB210, CB211, CB212, CB214, CB220, CB226, CB232, CB233, CB236, CB237, CB241, CB242, CB244, CB245, CB246, CB247, CB248, CB250, CB257, CB260, CB262, CB266, CB268, CB269, CB272, CB274, CB280, CB282, CB283, CB286, CB288, CB289, CB296, CB299, CB301, CB305, CB309, CB310, CB311, CB312, CB314, CB316, CB317, CB318, CB323, CB325, CB326, CB329, CB330, CB331, CB334, CB335, CB336, CB337, CB339, CB340, CB342, CB346, CB349, CB355, CB356, CB360, CB362, CB374, CB377, CB378, CB382, CB386, CB387, CB389, CB390, CB403, CB420, CB421, CB426, CB430, CB433, CB434, CB440, CB455, CB456, CB457, CB458, CB459, CB461, CB464, CB465, CB469, CB470, CB757, CB758, CB759, CB778, CB781, CB783, CB784, CB785, CB796, CB797, CB799, CB800, CB801, CB809, CB814, CB820, CB821, CB822, CB825, CB826, CB828, CB829, CB852, CB854, CB858				
CB08, CB15, CB54, CB127, CB143, CB279, CB281, CB290, CB291, CB292	10	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
CB265, CB429	2	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
DB01, DB02, DB03	3	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS02, DS03, DS33, DS34, DS35, DS41, DS42, DS43, DS44, DS45, DS46, DS47, DS48, DS49, DS75, DS76, DS77, DS78, DS79, DS80, DS81, DS82, DS83	24	LED, GREEN, SMD	Panasonic	LN1351C
DS04, DS05, DS06, DS07, DS17, DS18, DS19, DS20, DS21, DS24, DS25, DS26, DS36, DS37, DS38, DS39, DS40	17	L_LED, RED, SMD	Panasonic	LN1251C
DS08, DS50, DS63, DS64, DS65, DS66	6	L_LED, GREEN, SMD	Panasonic	LN1351C
DS09, DS10, DS11, DS12, DS13, DS14, DS15, DS16, DS22, DS23, DS27, DS28, DS29, DS30, DS31, DS32, DS71, DS72, DS73, DS74	20	LED, RED, SMD	Panasonic	LN1251C
DS67, DS68, DS69, DS70	4	LED, AMBER, SMD	Panasonic	LN1451C
H01, H02, H03, H04, H05, H06, H07, H08, H09, H10, H11, H12	12	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	4-40KIT4
J01, J12, J13, J17, J18	5	TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	TSW-108-07-T-D
J02, J50	2	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	NA
J03, J43	2	TYPE B SINGLE RT ANGLE, BLACK	MOL	NA
J04, J51	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J05, J06, J48, J49	4	NON POPULATED HEADER, 14 PIN, DUAL ROW, VERT	Samtec	NOPOP-HDR-TSW-107-14-T-D
J07, J08, J10, J11	4	NOPOP TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	NOPOP-TSW-108-07-T-D

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
J09, J14, J20, J21, J22, J23, J52, J53, J57	9	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J15, J46	2	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	DIGIKEY	CP-002AH-ND
J16, J24	2	CONNECTOR, STACKED OCTAL JACK, 64-PIN, SHIELDED	MOL	SD-44520-001
J19, J25, JB06	3	100 MIL 2 POS JUMPER	NA	NA
J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J44, J45	18	L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	TSW-102-07-T-S
J42, J58	2	100 MIL 2*7 POS JUMPER	NA	NA
J47	1	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J54, J93, J94, J95, J96	5	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE	DNP	DNP
J55	1	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J56, J98	2	CONNECTOR, PULSEJACK, 16 PIN	Pulse	JK0654218Z
J91, J92	2	CONNECTOR, FASTJACK SINGLE, 8 PIN FOR NATIONAL PHY	Halo Electronics	HFJ11-2450E
J97, J99	2	SOCKET, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	TFM-125-02-S-D-LC
JB01, JB05	2	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
JB02, JB04	2	TESTPOINTS FOR SMD 50 PIN, 2 ROW VERTICAL	NA	NA_NOTPOPULATED
JB03	1	100 MIL 2 POS JUMPER DO NOT POPULATE	NOPOP	NA
Reference designators shown on next row (begins with JP01)	49	100 MIL 3 POS JUMPER	NA	NA
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP67, JP68, JP69, JP70, JP71, JP72, JP73, JP74, JP75, JP76, JP77, JP78, JP79, JP80, JP81, JP82, JP83, JP84, JP85, JP86				
R01, R02, R42, R43, RB01, RB02, RB04, RB39, RB46, RB47, RB62, RB87, RB88, RB89, RB90, RB91, RB107, RB128, RB231, RB232	20	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
R03, R05, RB09, RB10, RB12, RB14, RB26, RB28, RB96, RB97, RB100, RB113, RB114, RB115, RB116, RB118, RB120, RB122, RB123	19	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
R04, RB03, RB05, RB07, RB13, RB18, RB23, RB24, RB25, RB92, RB99, RB101, RB104, RB106, RB121	15	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R06, R07, R39, R41	4	RES 0603 24.3 Ohm 1/16W 1%	Panasonic	ERJ-3EKF24R3V
R08, RB06, RB15, RB17, RB19, RB20, RB21, RB43, RB45	9	L_RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R09, R10, R11, R12, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, RB32, RB33, RB48, RB49, RB50, RB51	32	RES 1206 61.9 Ohm 1/8W 1%	Panasonic	ERJ-8ENF61R9V
R13, RB30, RB31, RB60, RB61, RB109, RB110, RB111, RB127	9	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
R36, R40	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R37, R38	2	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB08, RB41, RB98, RB108	4	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB11, RB95	2	RES 0603 1.5K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ152V
RB119, RB246	2	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
RB125, RB126, RB129, RB245, RB248, RB249	6	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB16, RB22, RB131, RB132	4	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
RB233, RB234, RB235, RB236, RB239, RB241	6	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB237, RB238	2	RES 0603 4.87K Ohm 1/16W 1%	Panasonic	ERJ-3EKF4871V
RB27, RB124, RB130, RB247	4	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB29, RB34, RB35, RB36, RB37, RB38	6	RES 0603 51 Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	ERJ-3GEY0R00V
RB40, RB44, RB112, RB240, RB242, RB243, RB244	7	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
RB42, RB117	2	RES 0805 10K Ohm 1/10W 1%	Panasonic	ERJ-6ENF1002V
RB52, RB53, RB54, RB55, RB56, RB57, RB58, RB59, RB63, RB64, RB65, RB66, RB67, RB68, RB69, RB70, RB103, RB105	18	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
RB71, RB72, RB73, RB74, RB75, RB76, RB77, RB78, RB79, RB80, RB81, RB82, RB83, RB84, RB85, RB86, RB93, RB94, RB102	19	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
RP01, RP02, RP03, RP04, RP05, RP06, RP41, RP42, RP43, RP44, RP48, RP49, RPB07, RPB10, RPB109, RPB110	16	4 PACK RESISTOR 24 OHM 2 PCT	KOA	CN1J4TTD240G
RP07, RP08, RP09, RP10, RP12, RP45, RP46, RP47, RP50, RP51, RPB15, RPB19, RPB93, RPB98, RPB107, RPB108, RPB131, RPB132, RPB144, RPB145	20	4 PACK RESISTOR 50 OHM 2 PCT	KOA	CN1J4TTD500G
See next row (begins with RP11)	62	4 PACK RESISTOR 30 OHM 5% QUAD 0402	PANASONIC	EXB-N8V300JX

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
RP11, RP13, RP15, RP16, RP17, RP18, RP19, RP20, RP25, RP26, RP27, RP28, RP29, RP30, RP31, RP32, RP33, RP34, RP35, RP36, RP37, RP38, RP39, RP84, RP85, RP86, RP87, RP88, RP89, RP91, RP92, RP93, RP94, RPB05, RPB08, RPB09, RPB11, RPB13, RPB16, RPB18, RPB21, RPB24, RPB25, RPB30, RPB35, RPB43, RPB44, RPB51, RPB52, RPB58, RPB59, RPB60, RPB61, RPB62, RPB63, RPB64, RPB65, RPB84, RPB87, RPB91, RPB99, RPB143				
RP14, RPB04, RPB06, RPB14, RPB20, RPB22, RPB54, RPB55, RPB56, RPB66, RPB77, RPB79, RPB89, RPB92, RPB94, RPB95, RPB96, RPB97, RPB100, RPB101, RPB103, RPB150	22	4 PACK RESISTOR 10K OHM 5% QUAD 0402	PANASONIC	EXB-N8V103JX
RP21, RP22, RP23, RP24, RPB26, RPB27, RPB28, RPB29, RPB31, RPB32, RPB33, RPB34, RPB36, RPB38, RPB39, RPB40, RPB41, RPB42, RPB45, RPB46, RPB47, RPB49, RPB50, RPB53	24	4 PACK RESISTOR 20 OHM 5% QUAD 0402	PANASONIC	EXB-N8V200JX
RP40, RP90, RPB01, RPB02, RPB03, RPB12, RPB17, RPB37, RPB57, RPB67, RPB68, RPB69, RPB70, RPB71, RPB74, RPB78, RPB80, RPB82, RPB83, RPB85, RPB90, RPB104, RPB149	23	4 PACK RESISTOR 1K OHM 5% QUAD 0402	PANASONIC	EXB-N8V102JX
RPB23, RPB48, RPB72, RPB73, RPB75, RPB76, RPB81, RPB86, RPB102, RPB105, RPB133, RPB135, RPB147	13	4 PACK RESISTOR 330 OHM 5% QUAD 0402	PANASONIC	EXB-N8V331JX
RPB88, RPB106, RPB134, RPB136, RPB137, RPB138, RPB139, RPB140, RPB141, RPB142, RPB146, RPB148	12	4 PACK RESISTOR 2.2K OHM 5% QUAD 0402	PANASONIC	EXB-N8V222JX
SW01	1	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
T01, T02, T03	3	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TB01, TB02, TB03, TB04	4	XFMR, XMIT/RCV, 1 TO 2 AND 1 TO 1, SMT 32 PIN	Pulse	TX1475
TB05	1	XFMR, 1CT_1CT & 1CT_2CT, 12P SMT	Pulse	TX1277
TP01, TPB01, TPB02, TPB07, TPB08, TPB09	6	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U01, U19	2	USB UART (USB - 8 bit FIFO), 32 PIN LQFP	FTD	FT245BM
U02	1	ETHERNET EXTENSION DEVICE 16 WAN 2 LAN	DALLAS SEMICONDUCTOR	NA
U03, UB29	2	SPI SERIAL EEPROM 2M 8 PIN SOIC 2.7V to 3.6V	Atmel	AT25F2048N-10SU-2.7
U04, U05, U06, U07, U11, U22, UB12, UB14, UB15, UB17, UB19, UB34	12	IC, OCT BUFFER FET SWITCH 5V 20-PIN TSSOP	Philips	CBT3244APW
U08, U15	2	IC, OCTAL TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS26528N
U09, U10, U12, UB13, UB18, UB20	6	BAD PARTNUM IC, OCT BUFFER FET SWITCH 5V TSOP	Philips	CBT3244APW-T
U13, U23, UB22, UB33	4	CYPRESS SRAM, LAB STOCK	NA	NA
U14, U24	2	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	Lattice	LFEC3E-3T144C

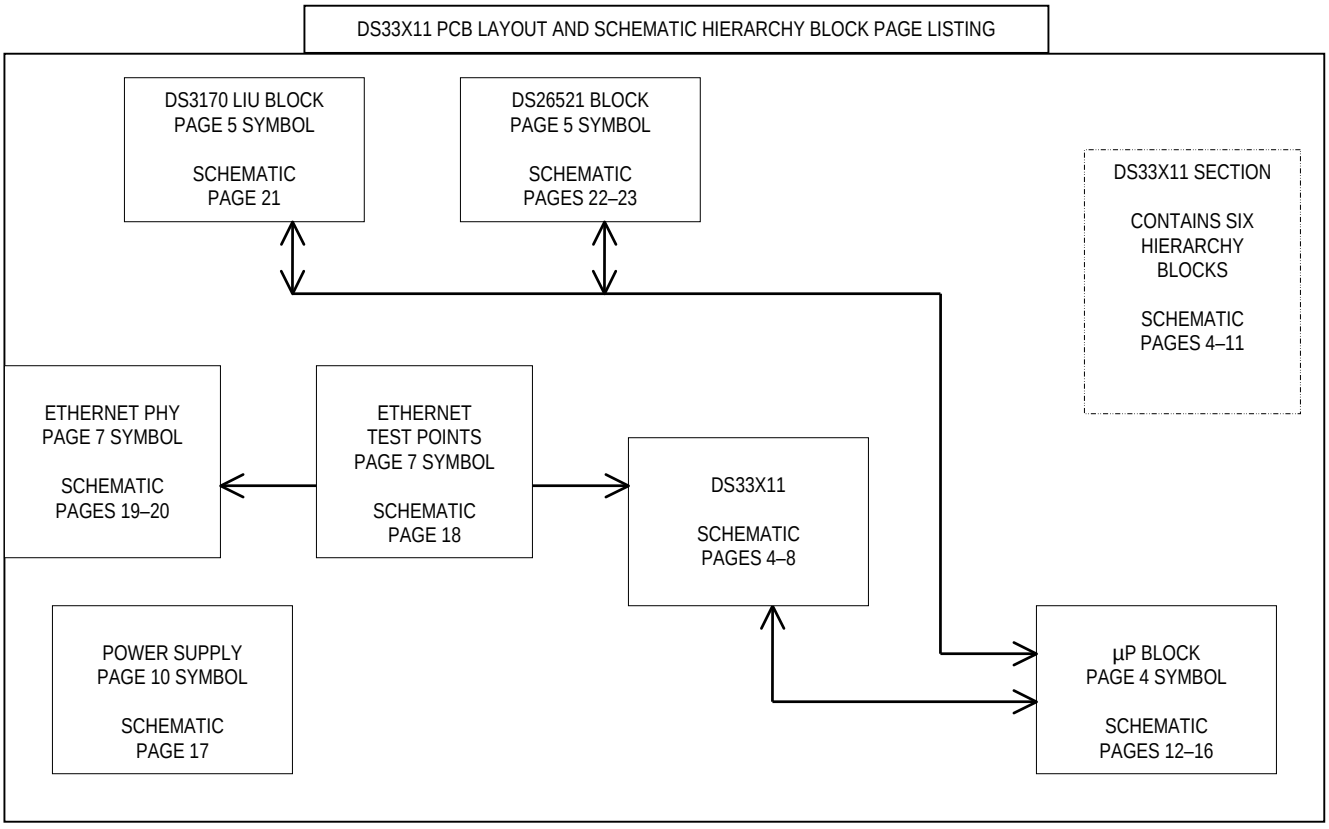
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U16, U17	2	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYs FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U18, U27	2	MMC2107 PROCESSOR	Motorola	MMC2107
U20	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U21	1	IC, SINGLE T1 E1 J1 TRANSCEIVER, 10X10 LQFP, 64-PIN	Dallas Semiconductor	DS26521
U25	1	ETHERNET EXTENSION DEVICE 1 WAN 2 LAN	Dallas Semiconductor	NA
U26, U33	2	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865BVH
U31, U32	2	IC, DP83848C PHYTER 10/100 ETHERNET TRANSCEIVER, 48 PIN TQFP	National Semiconductor	DP83848C
UB01, UB28, UB70	3	HIGH SPEED BUFFER	FAIRCHILD	NC7SZ86
UB02, UB36	2	SINK SOURCE DDR TERMINATION REGULATOR	AVNET	LP2995M
UB03, UB35	2	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	NA
UB04, UB30	2	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB05, UB06, UB37, UB38	4	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB07, UB08, UB09, UB11, UB16, UB23, UB24, UB25, UB26, UB27	10	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB10, UB31	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
UB21, UB32	2	IC, LDO REGULATOR WITH RESET,1.20V OUTPUT 300 MA, 6 PIN SOT23	Maxim	MAX1963EZT120-T
XB01, XB02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, YB07	2	XTAL, LOW PROFILE, 6.00 MHZ	Pletronics	LP49-26-6.00M
YB01, YB03, YB09, YB11	4	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 125.000 MHZ	ECLIPTEK	EC1325HSTS-125.000M+SOCKET
YB02, YB10	2	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB04	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB05	1	OSCILLATOR + Socket, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	SOCKET+NTH039A3-2.0480

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
YB06	1	OSCILLATOR + Socket, CRYSTAL CLOCK, 5V - 1.544 MHZ	SaRonix	SOCKET+NTH039A-1.5440
YB08	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
YB12	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 1.544 MHZ	SaRonix	NTH039A3-1.5440
YB13	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

9. Schematics

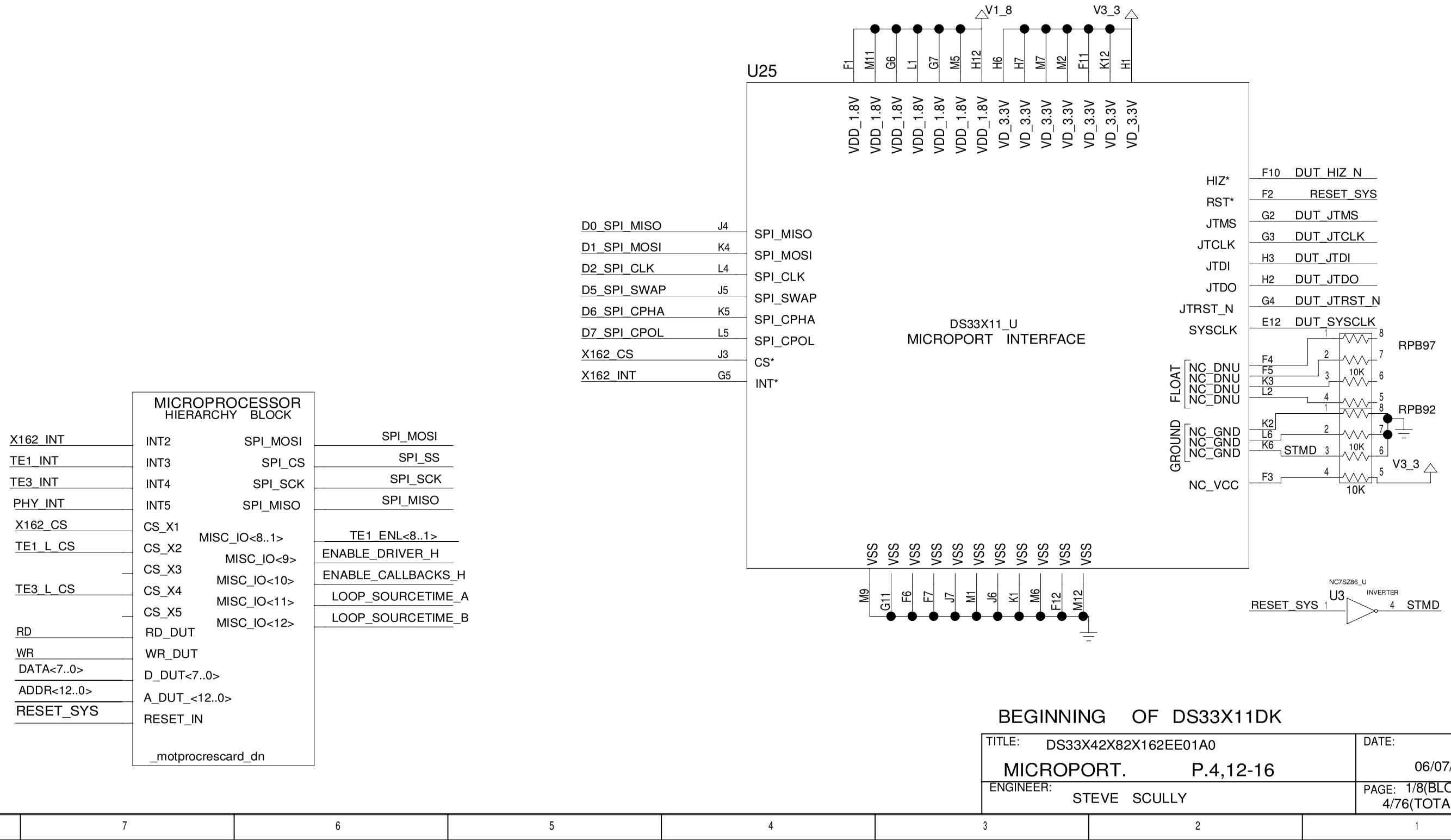
The DS33X11DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation follows. The schematic contains six hierarchal blocks: the microcontroller, DS26521, DS3170, Ethernet PHY, Ethernet Test Points, and Power Supply.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.



Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

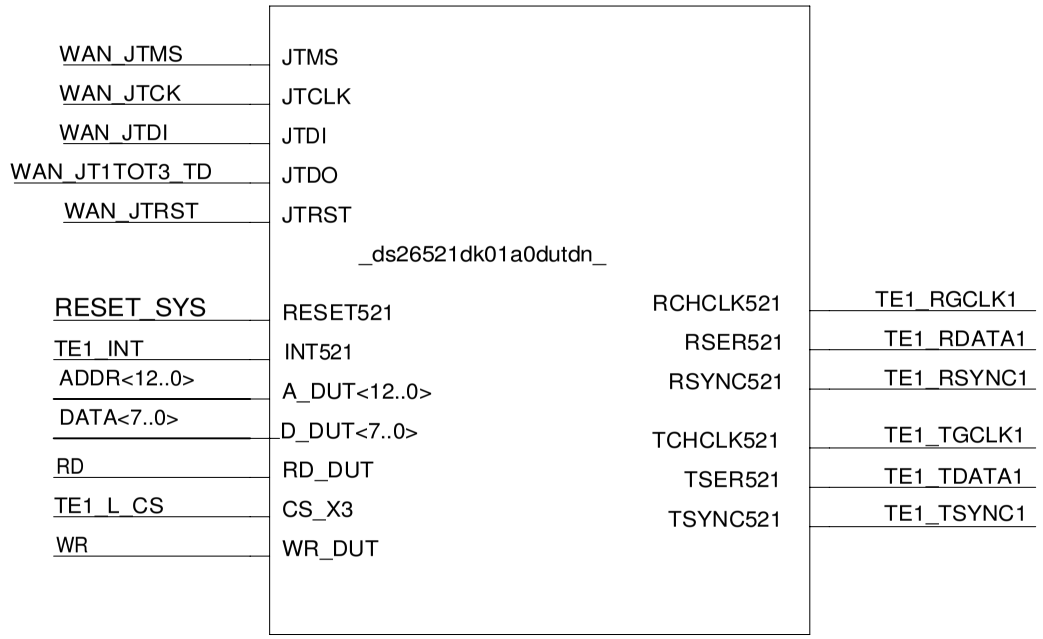
DS33X11DK CONTENTS / INDEX

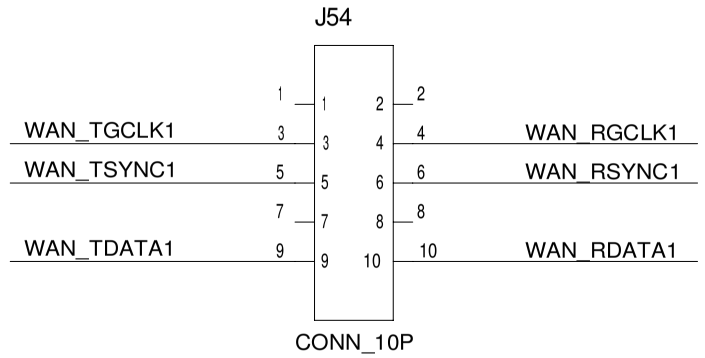


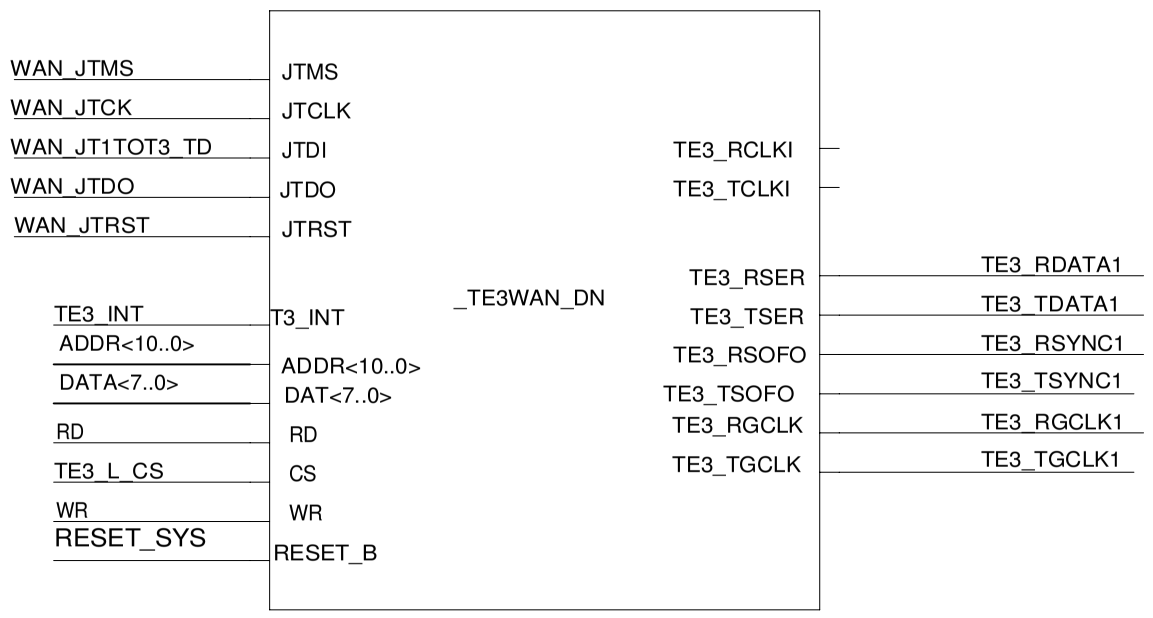
BEGINNING OF DS33X11DK

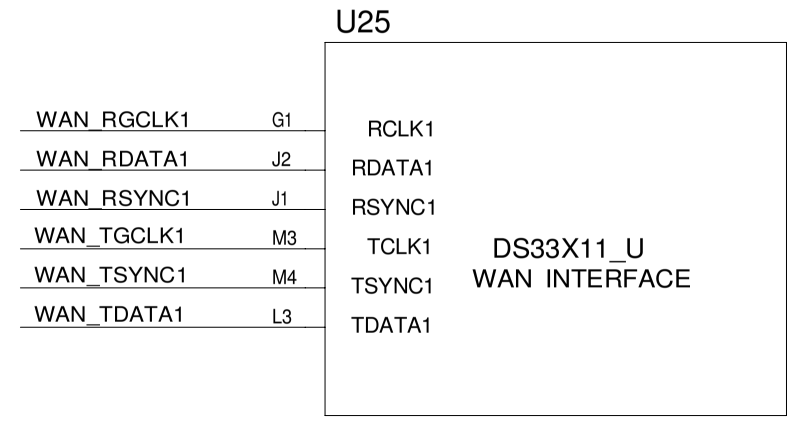
TITLE: DS33X42X82X162EE01A0 MICROPORT. P.4,12-16	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 4/76(TOTAL)

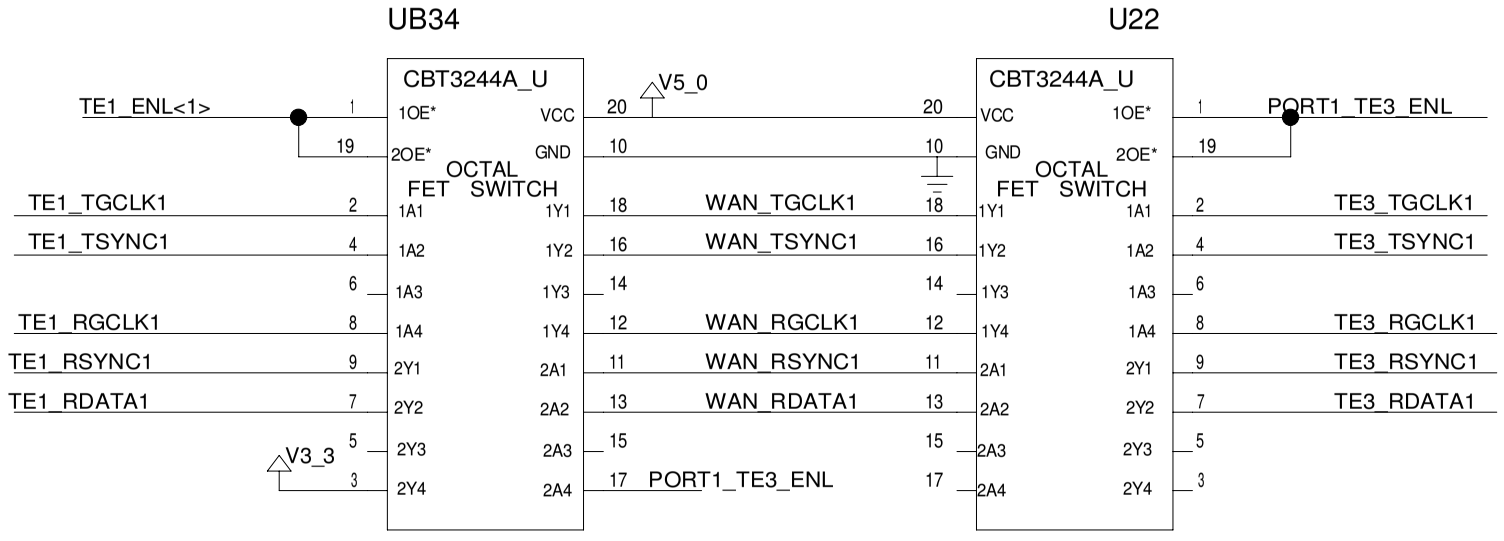
BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\

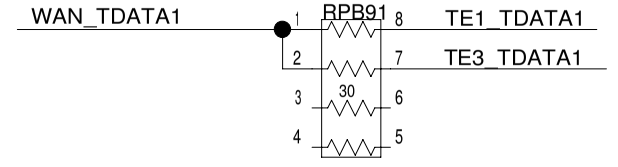








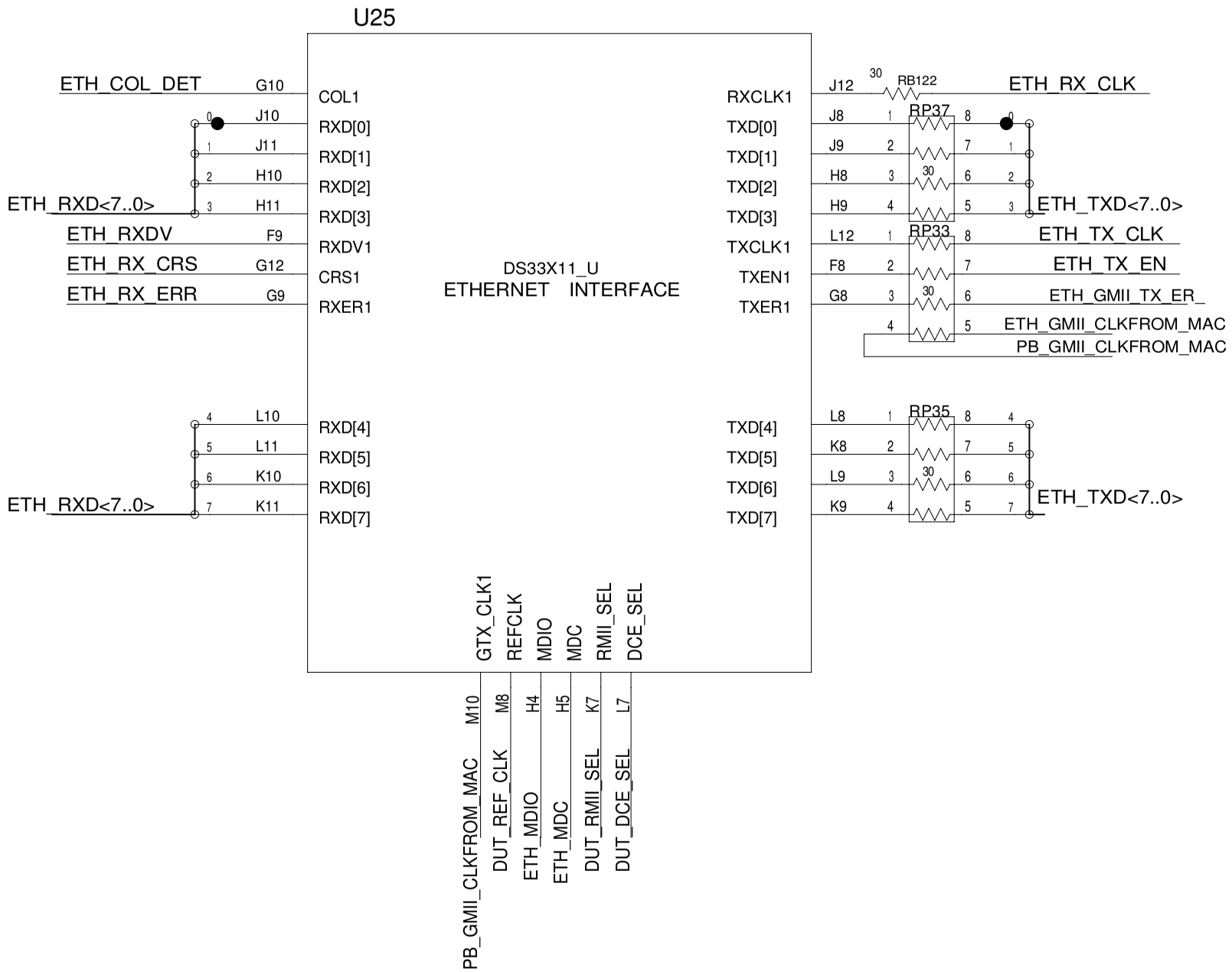




WAN. P.5,21(T3),22-23(T1)

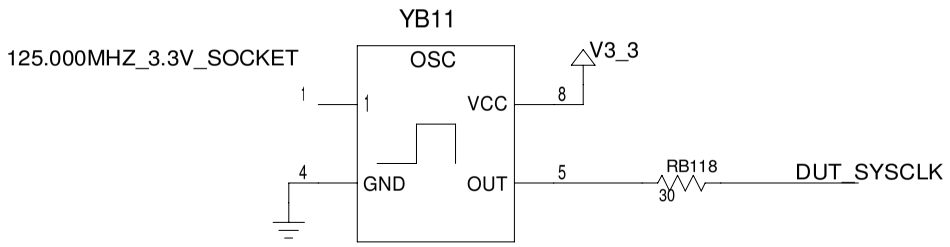
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/8(BLOCK) 5/76(TOTAL)

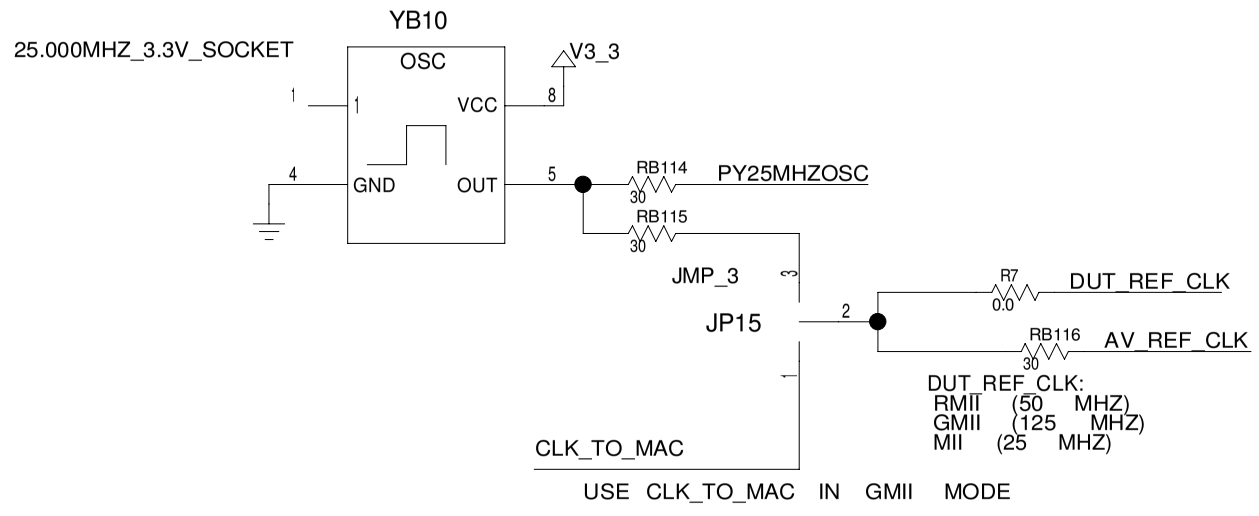
BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\

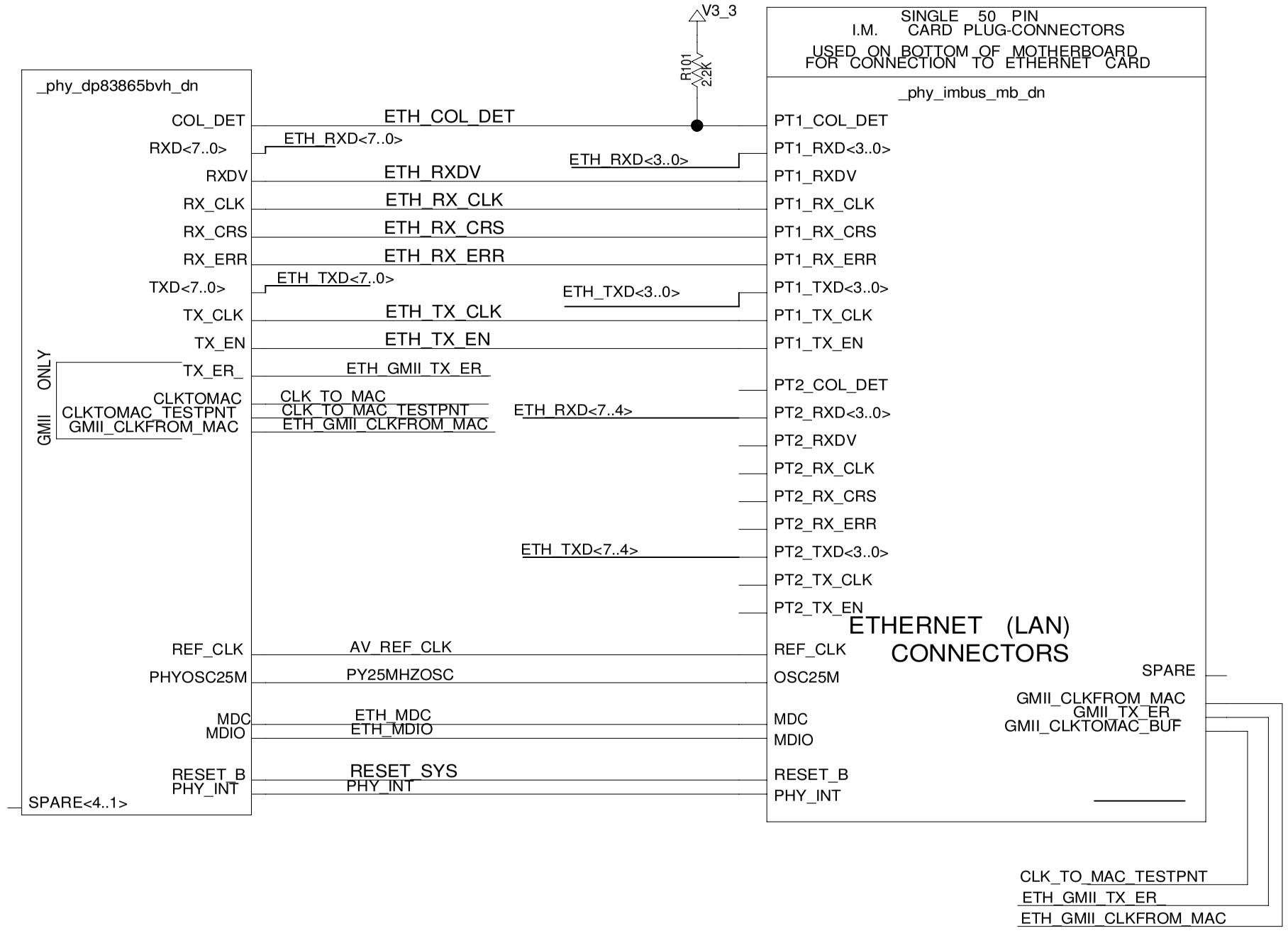


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ETHERNET. P.6-7,18,19-20	
ENGINEER: STEVE SCULLY	PAGE: 3/8(BLOCK) 6/76(TOTAL)

BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\







ETHERNET CONNECTOR (I.M. BUS)
IS INTENDED FOR USE AS TESTPOINTS
NOT CONNECTION TO A RESOURCE CARD

TITLE: DS33X42X82X162EE01A0 ETHERNET. P.6-7,18,19-20	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/8(BLOCK) 7/76(TOTAL)

BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\

RESISTOR DIVIDER COMPONENT VALUES
OF 4.87K 1% WAS CHOSEN TO SIMPLIFY BOM
(THE DP83848 PHY USES THE SAME VALUE RESISTOR)

V2_5
R3 4.87K
R4 4.87K
C150 .01UF
C267 4.7UF
C134 .01UF
CB443 4.7UF
VREF_FROM_VREG
TPB02

V1_8
V2_5
V2_5
VREF_FROM_VREG

U25

D12 AVDD_1.8V
C7 VDDQ_2.5V
A2 VDDQ_2.5V
E10 VDDQ_2.5V
B12 VDDQ_2.5V
E4 VDDQ_2.5V
B1 VDDP_2.5V
C6 VDDP_2.5V
D6 VREF

DS33X11_U
DDR INTERFACE

DDR_A<12..0>
0 A3 SD_A[0]
1 D2 SD_A[1]
2 B2 SD_A[2]
3 D1 SD_A[3]
4 C1 SD_A[4]
5 E1 SD_A[5]
6 C2 SD_A[6]
7 E2 SD_A[7]
8 B3 SD_A[8]
9 A4 SD_A[9]
10 C3 SD_A[10]
11 B4 SD_A[11]
12 D3 SD_A[12]
DDR_BA0 D4 SD_BA[0]
DDR_BA1 C4 SD_BA[1]
DDR_CAS D5 SD_CAS*
DDR_RAS B5 SD_RAS*
DDR_WE C5 SD_WE*
DDR_CKE E5 SD_CLKEN
DDR_CKINV A7 SD_CLK*
DDR_CK A8 SD_CLK
DDR_CS A5 SD_CS*
DDR_LDM E6 SD_LDM
DDR_UDM E7 SD_UDM

SD_UDQS D7 DDR_UDQS
SD_LDQS E8 DDR_LDQS
DDR_DQ<15..0>
SD_DQ[15] A9 15
SD_DQ[14] B9 14
SD_DQ[13] D9 13
SD_DQ[12] C9 12
SD_DQ[11] E9 11
SD_DQ[10] B8 10
SD_DQ[9] D8 9
SD_DQ[8] C8 8
SD_DQ[7] C10 7
SD_DQ[6] D10 6
SD_DQ[5] B10 5
SD_DQ[4] A10 4
SD_DQ[3] C11 3
SD_DQ[2] D11 2
SD_DQ[1] B11 1
SD_DQ[0] A11 0

VSSO A12
VSSO E11
VSSO E3
VSSO A6
VSSO B6
VSSO B7
VSSO A1
AVSS C12

V2_5
18 33 15 55 9 3 61 VDD VDD VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ
49 VREF
VREF_FROM_VREG

UB35
MT46V16M16BG75

DDR_UDM 47 UDM
DDR_LDM 20 LDM
DDR_CKINV 46 CK_INV
DDR_CS 24 CS
DDR_CK 45 CK
DDR_CKE 44 CKE
DDR_WE 21 WE
DDR_RAS 23 RAS
DDR_CAS 22 CAS
DDR_BA1 27 BA1
DDR_BA0 26 BA0
12 42 A12
11 41 A11
10 28 A10/AP
9 40 A9
8 39 A8
7 38 A7
6 37 A6
5 36 A5
4 35 A4
3 32 A3
2 31 A2
1 30 A1
0 29 A0
DDR_A<12..0>

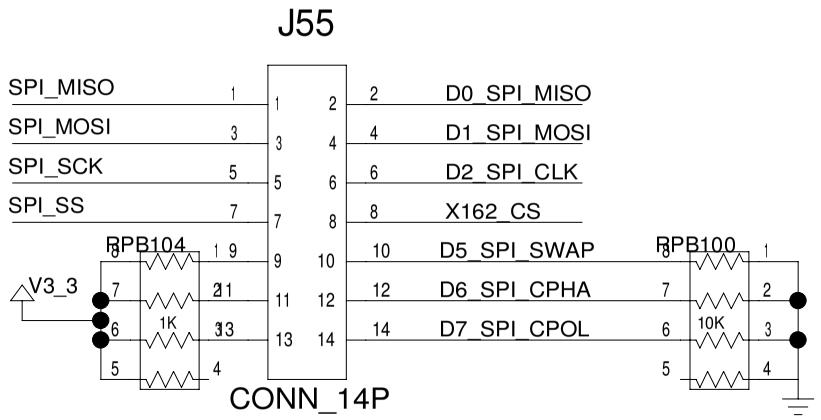
UDQS 51 DDR_UDQS
LDQS 16 DDR_LDQS
DQ15 65 15
DQ14 63 14
DQ13 62 13
DQ12 60 12
DQ11 59 11
DQ10 57 10
DQ9 56 9
DQ8 54 8
DQ7 13 7
DQ6 11 6
DQ5 10 5
DQ4 8 4
DQ3 7 3
DQ2 5 2
DQ1 4 1
DQ0 2 0
DDR_DQ<15..0>

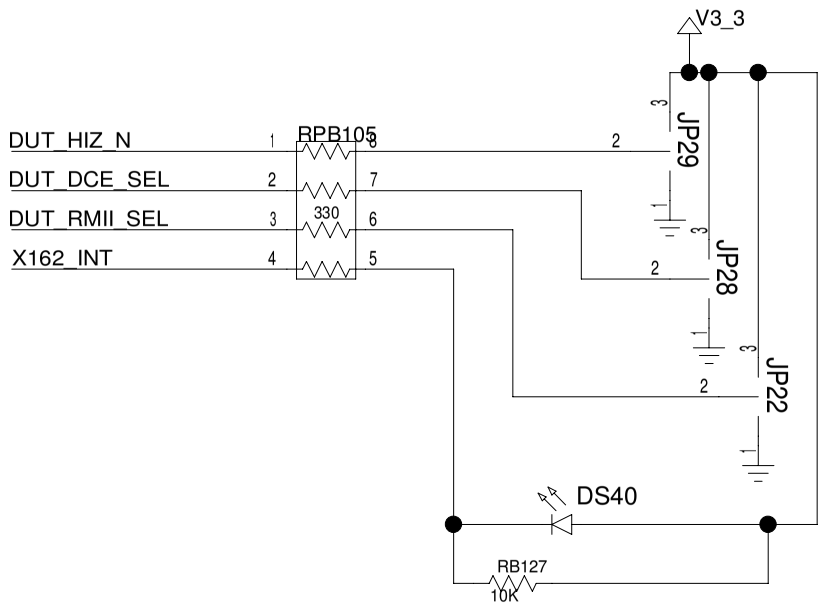
DNU 19
DNU 50
NC 14
NC 53
NC 43
NC 25
NC 17
VSSQ 58
VSSQ 6
VSSQ 64
VSSQ 12
VSSQ 52
VSS 48
VSS 34
VSS 66

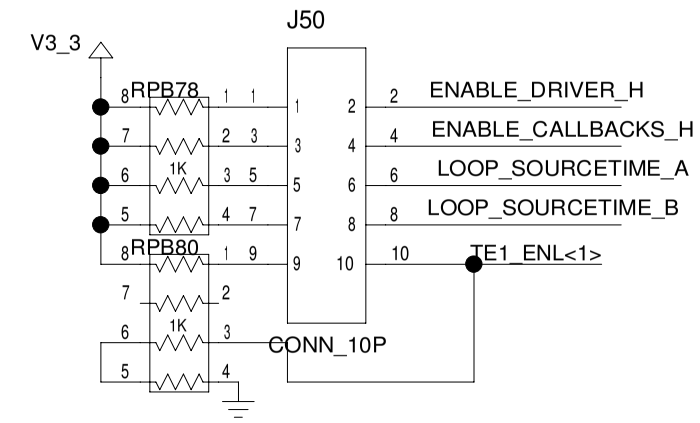
V2_5 FOR DDR
CB431 4.7UF
CB425 4.7UF
C156 0.1UF
C135 .1UF
C152 .1UF
C139 .1UF
CB461 .1UF
C142 4.7UF
C151 4.7UF
C146 4.7UF
C136 .01UF

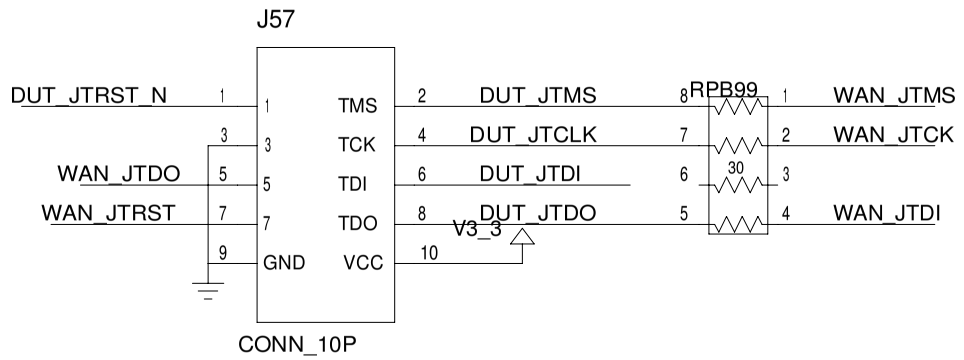
TITLE: DS33X42X82X162EE01A0 DDR MEMORY. P.8	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/8(BLOCK) 8/76(TOTAL)

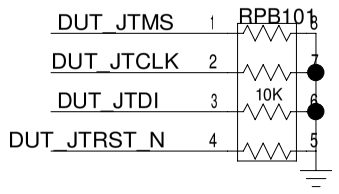
BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\











DEVICE DRIVER SETTINGS

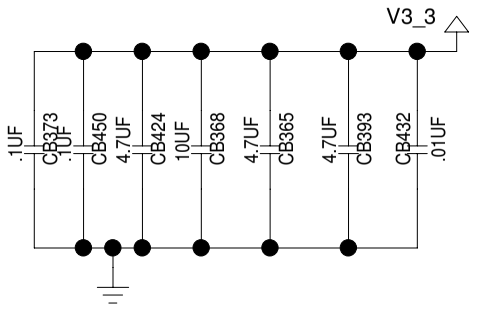
ENABLE_DRIVER_H: ENABLES DEVICE DRIVERS WHEN JUMPER IS INSTALLED
ENABLE_CALLBACKS_H: ENABLES INTERRUPT HANDLING WHEN JUMPER IS INSTALLED

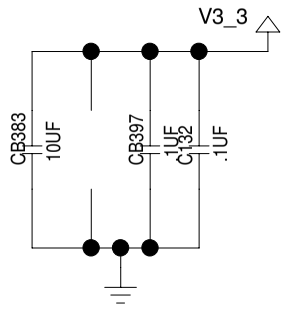
LOOP_SOURCETIME_A: (IN DRIVER MODE ONLY)
WHEN JUMPER IS INSTALLED WAN PORTS 1-4 AND 9-12 HAVE TCLK<=RCLK
WHEN JUMPER IS NOT INSTALLED WAN PORTS 1-4 AND 9-12 HAVE TCLK<=REFCLKIO

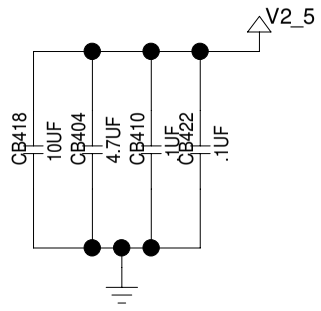
LOOP_SOURCETIME_B: IS NOT USED WITH DS33X11

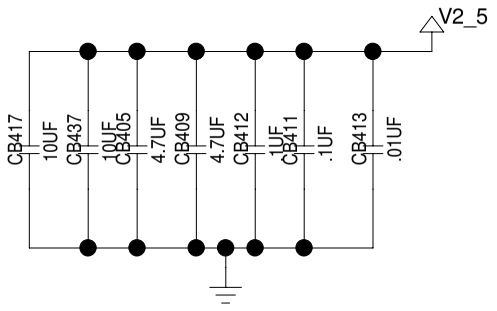
TITLE: DS33X42X82X162EE01A0 BIAS+CONFIG. P.9	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 6/8(BLOCK) 9/76(TOTAL)

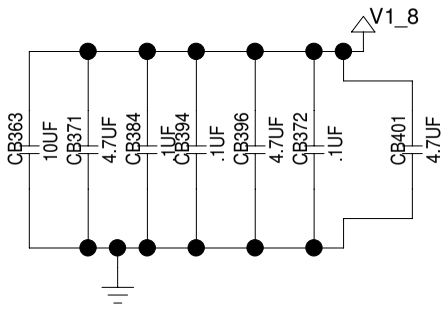
BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\

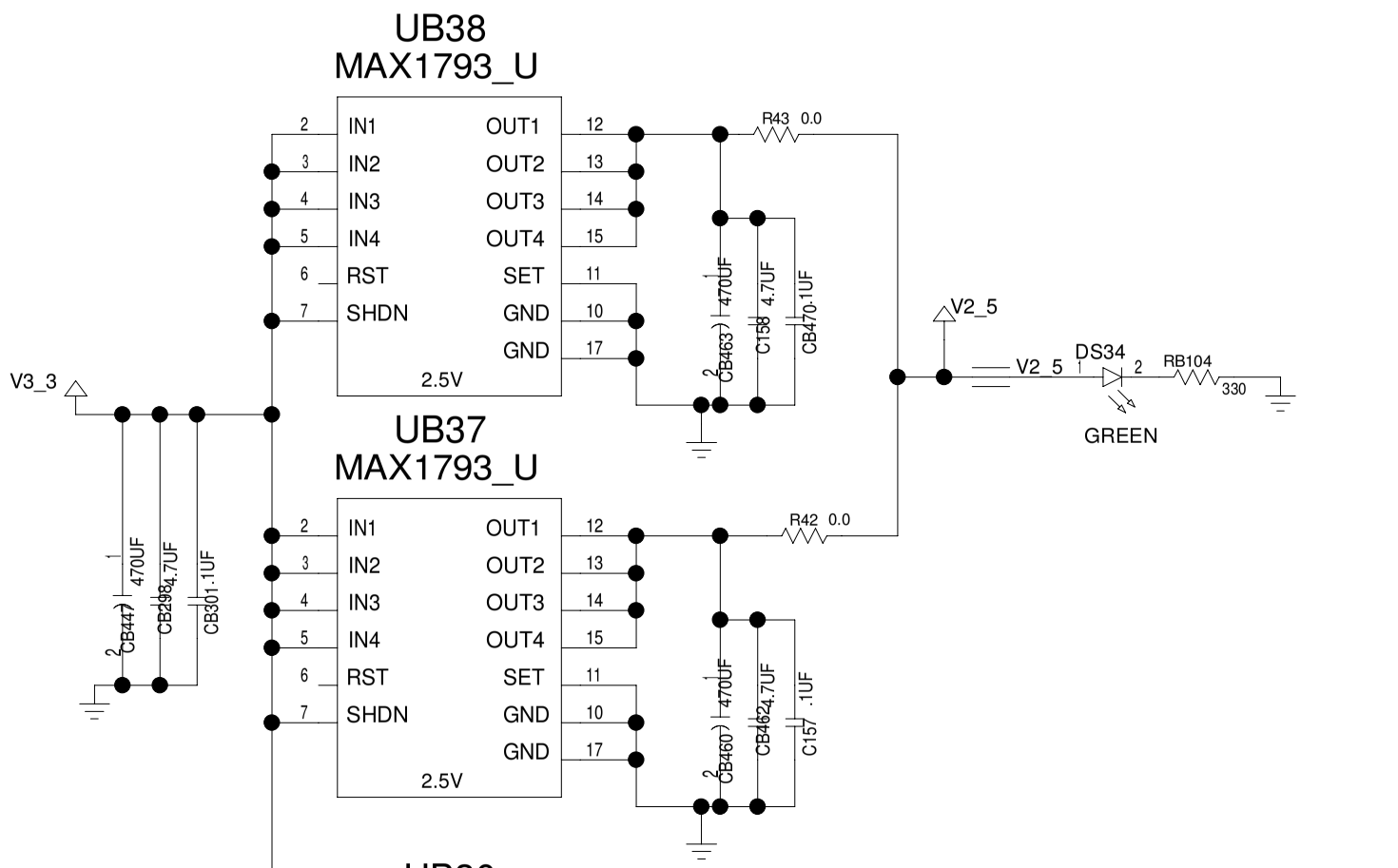


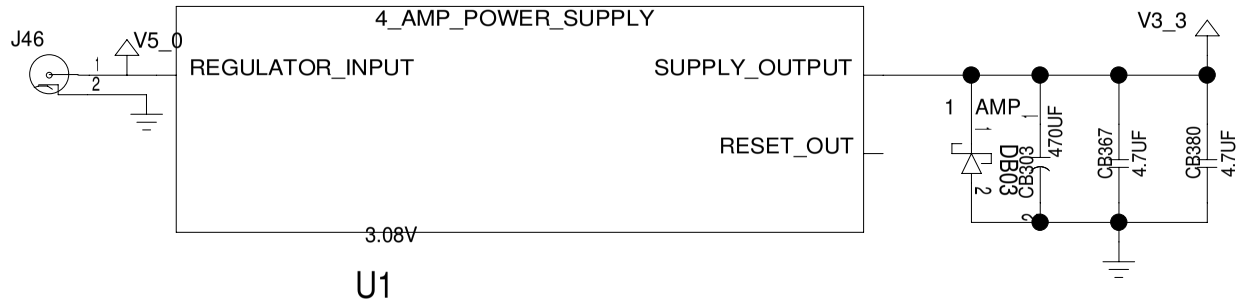


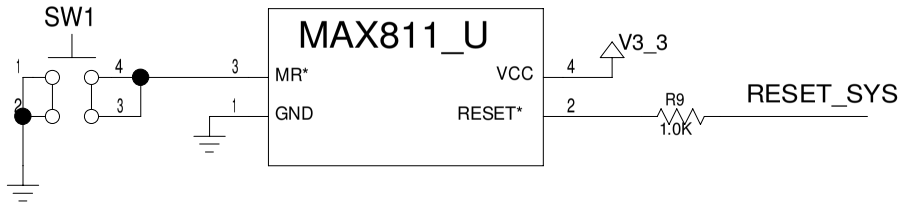








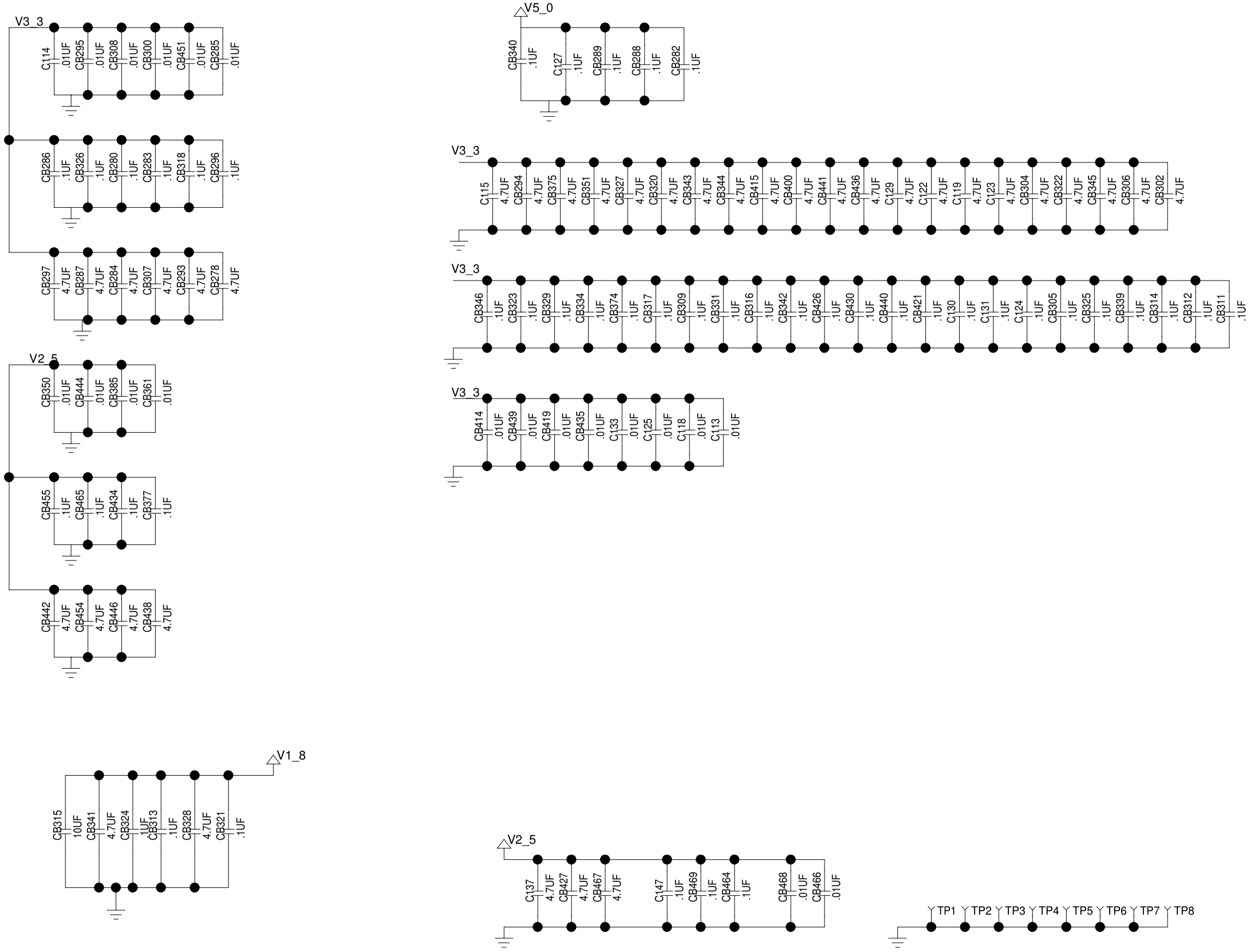




TRACES BETWEEN REGULATOR OUTPUT AND V2.5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

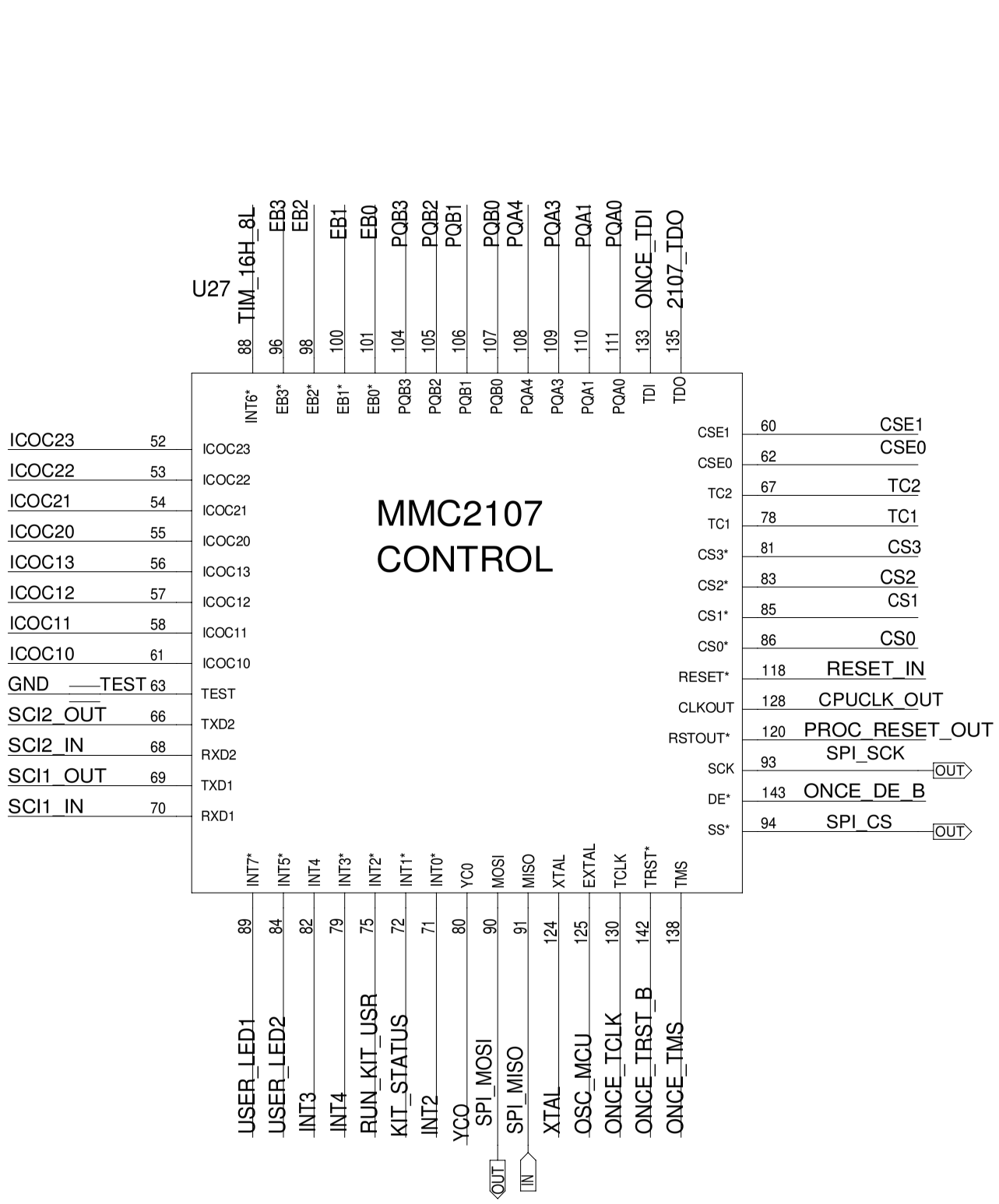
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
POWER. P.10-11,17	
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 10/76(TOTAL)

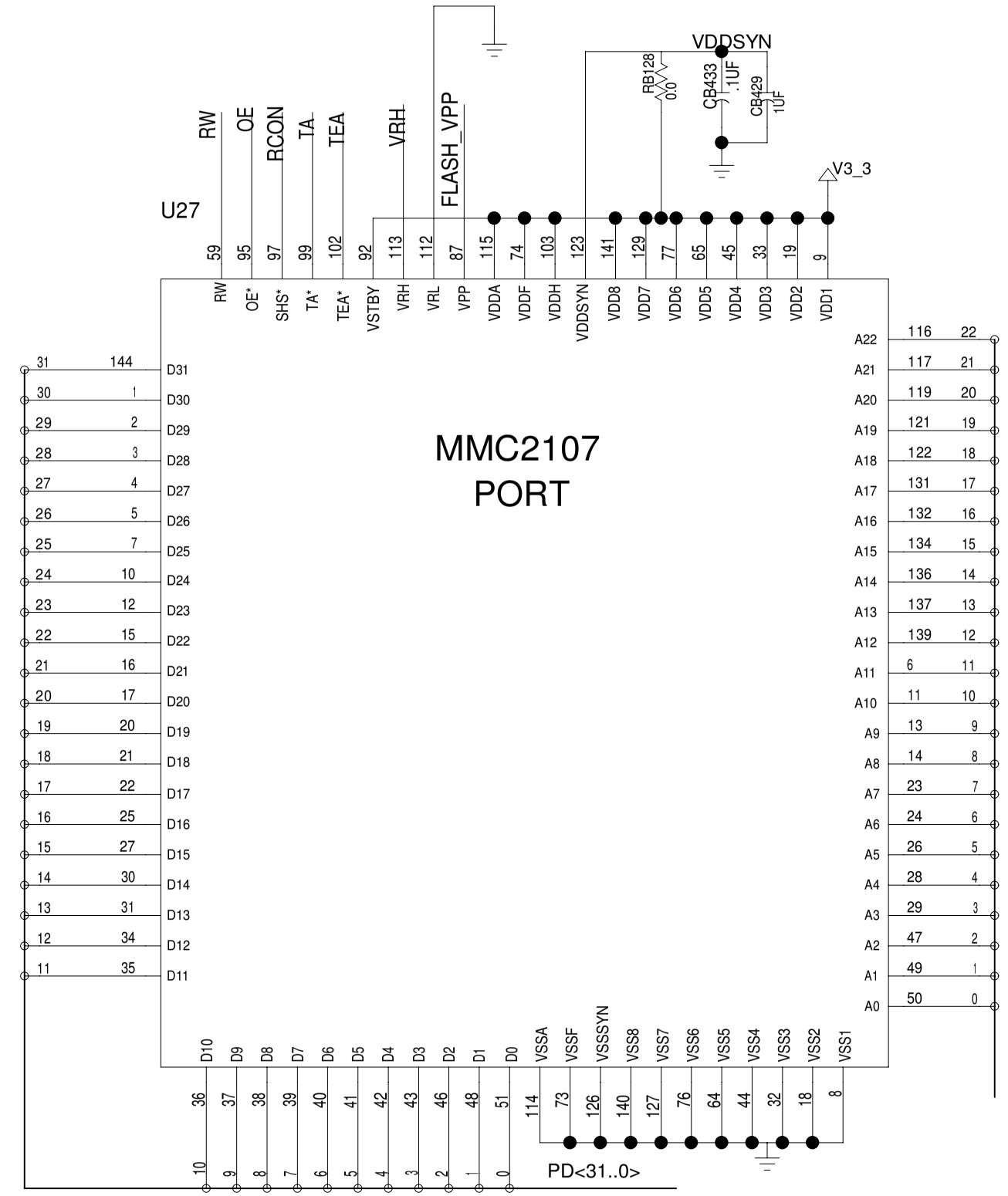
BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\



.50STA[illegible]NUT DS33X42X82X162EE01A0	DATE: 06/07/2006
POWER. P.10-11,17	
ENGINEER: STEVE SCULLY	PAGE: 8/8(BLOCK) 11/76(TOTAL)

BLOCK NAME: _ds33x11dk_dn. PARENT BLOCK: _rc_top_dn_\





BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 12/76(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x11dk_dn\

PRINTED Mon May 14 11:03:56 2007

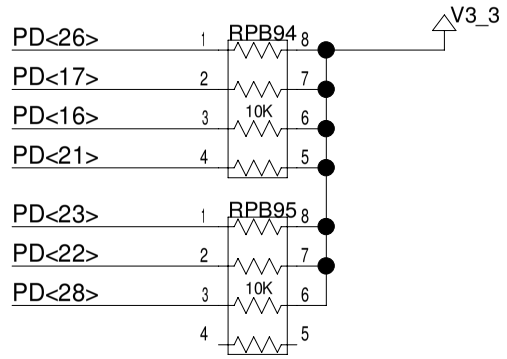
RESET CONFIGURATION

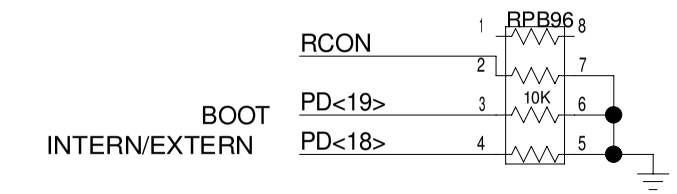
MASTER MODE

FULL DRIVE

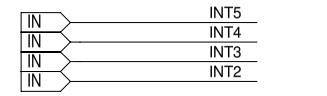
XTAL W/ PLL

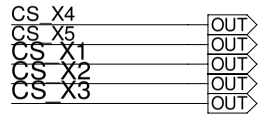
INTERNAL
FLASH ENABLE

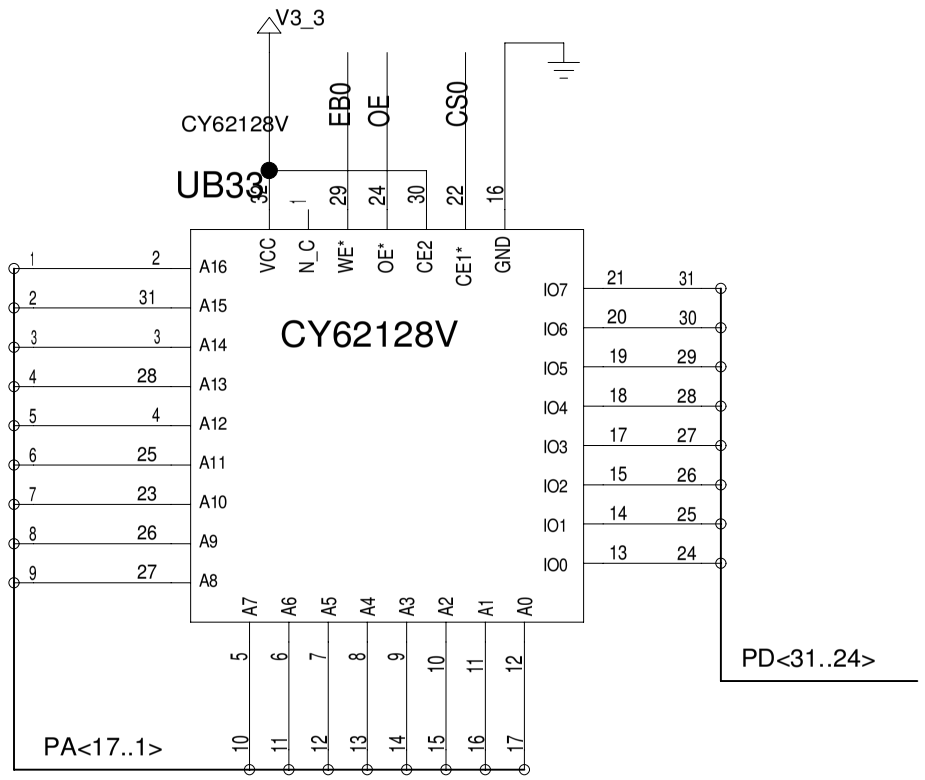


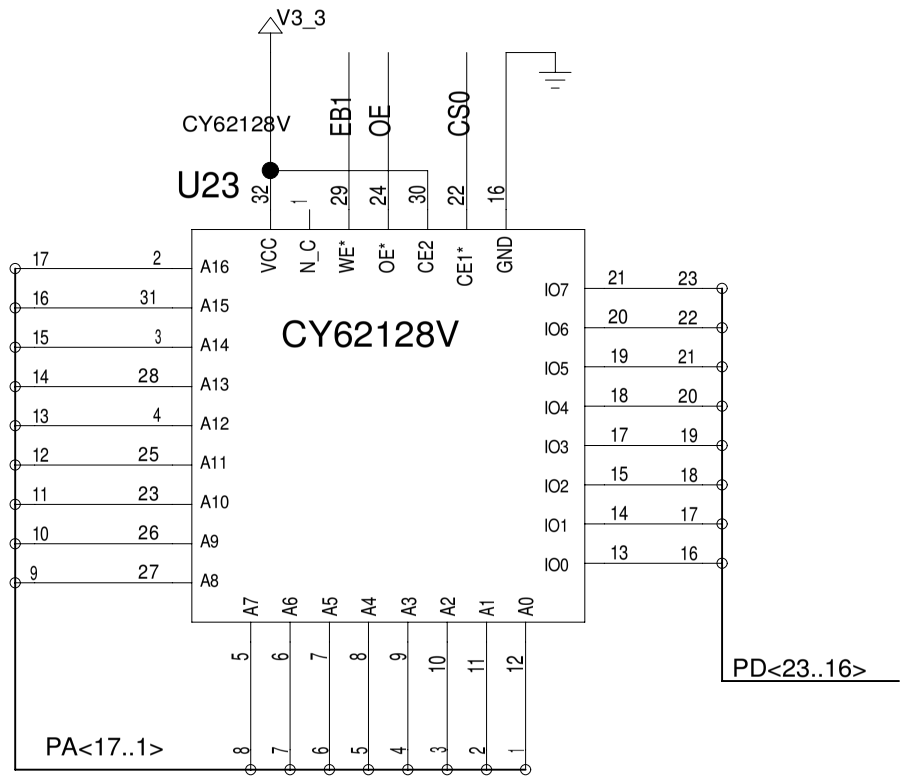


WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND



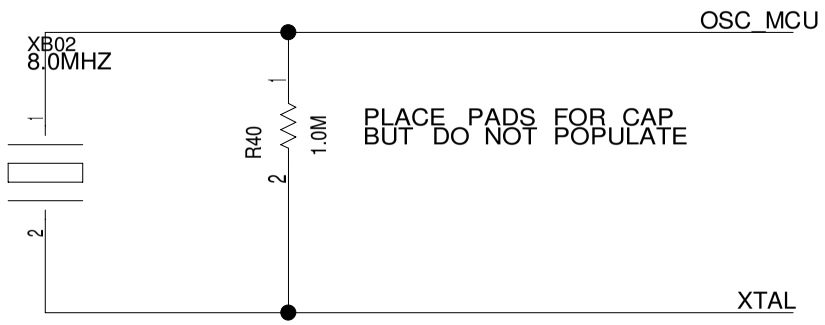


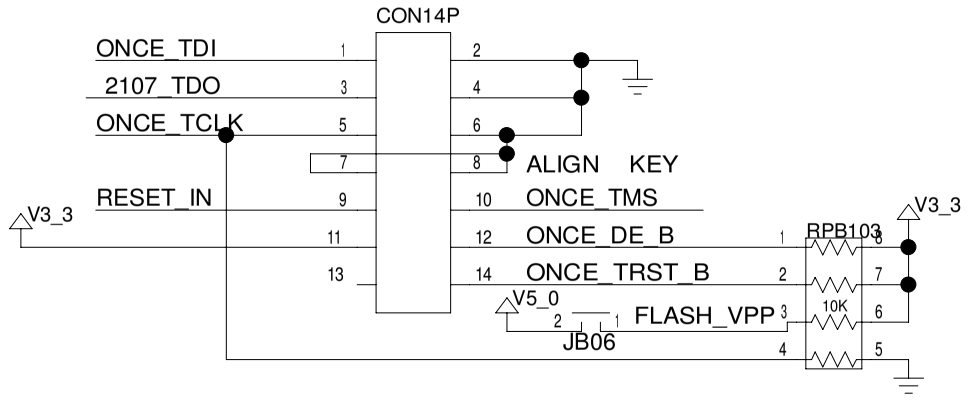


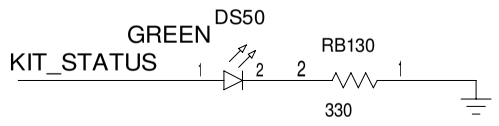


TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 13/76(TOTAL)

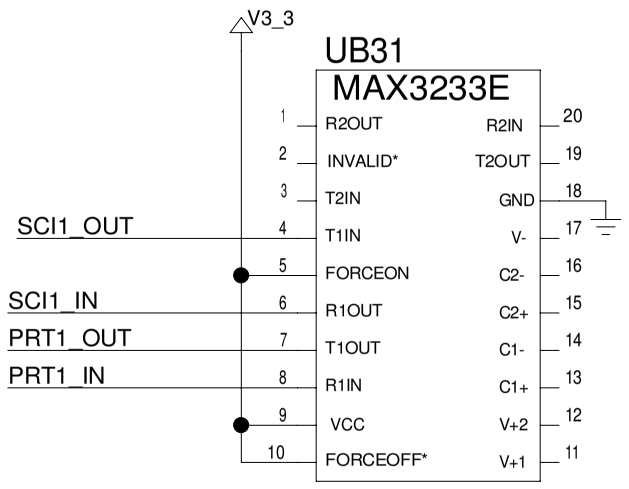
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x11dk_dn\

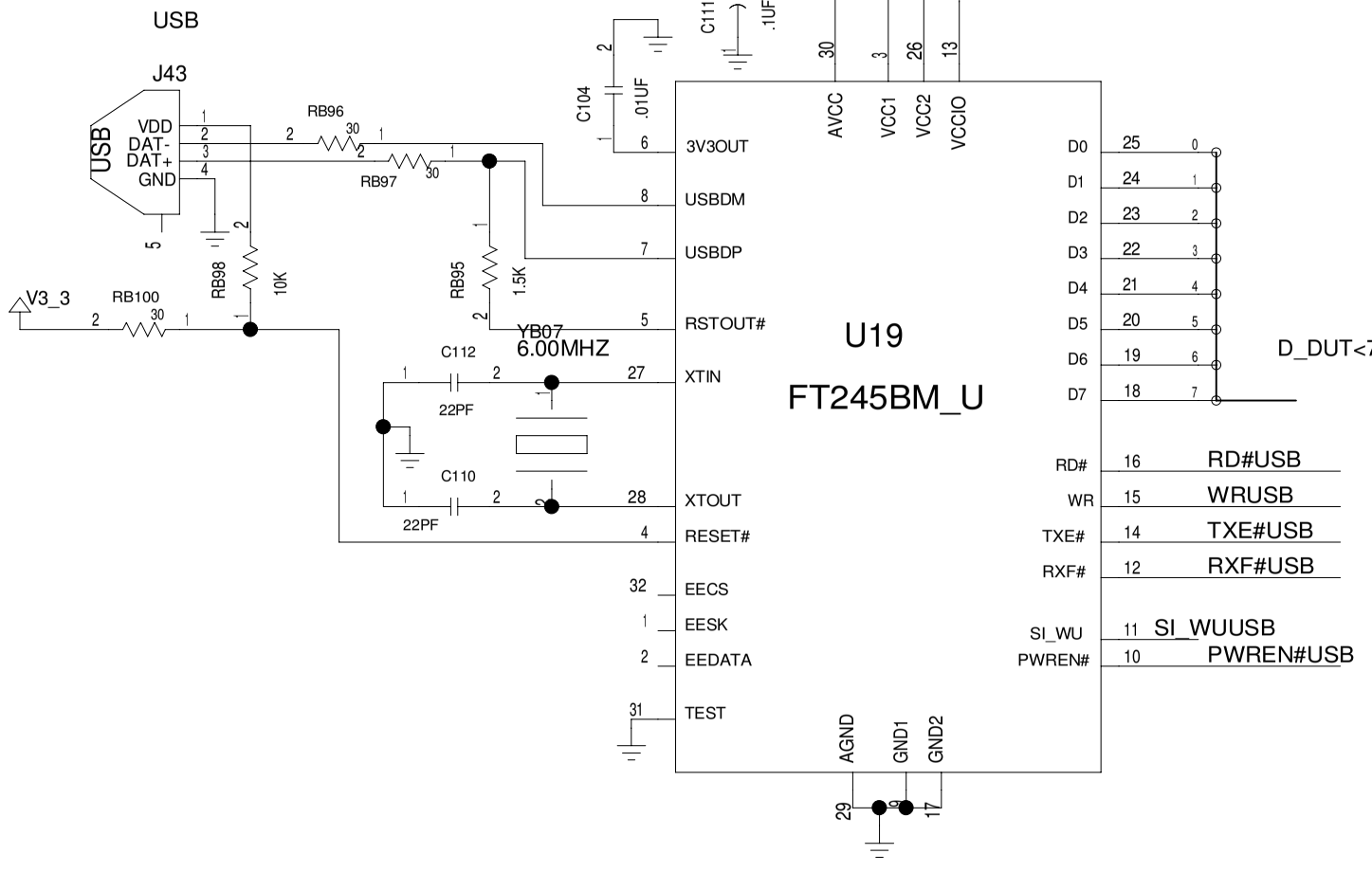


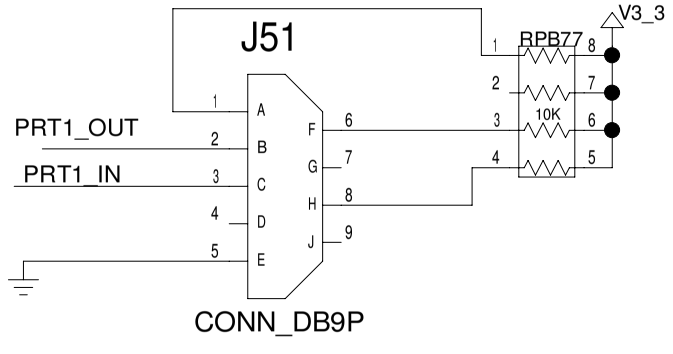




TODO_REMOVETHISNOTE: 330OHM AVCC RES USED TO BE 470OHM (BOM CONSOLDIATE)

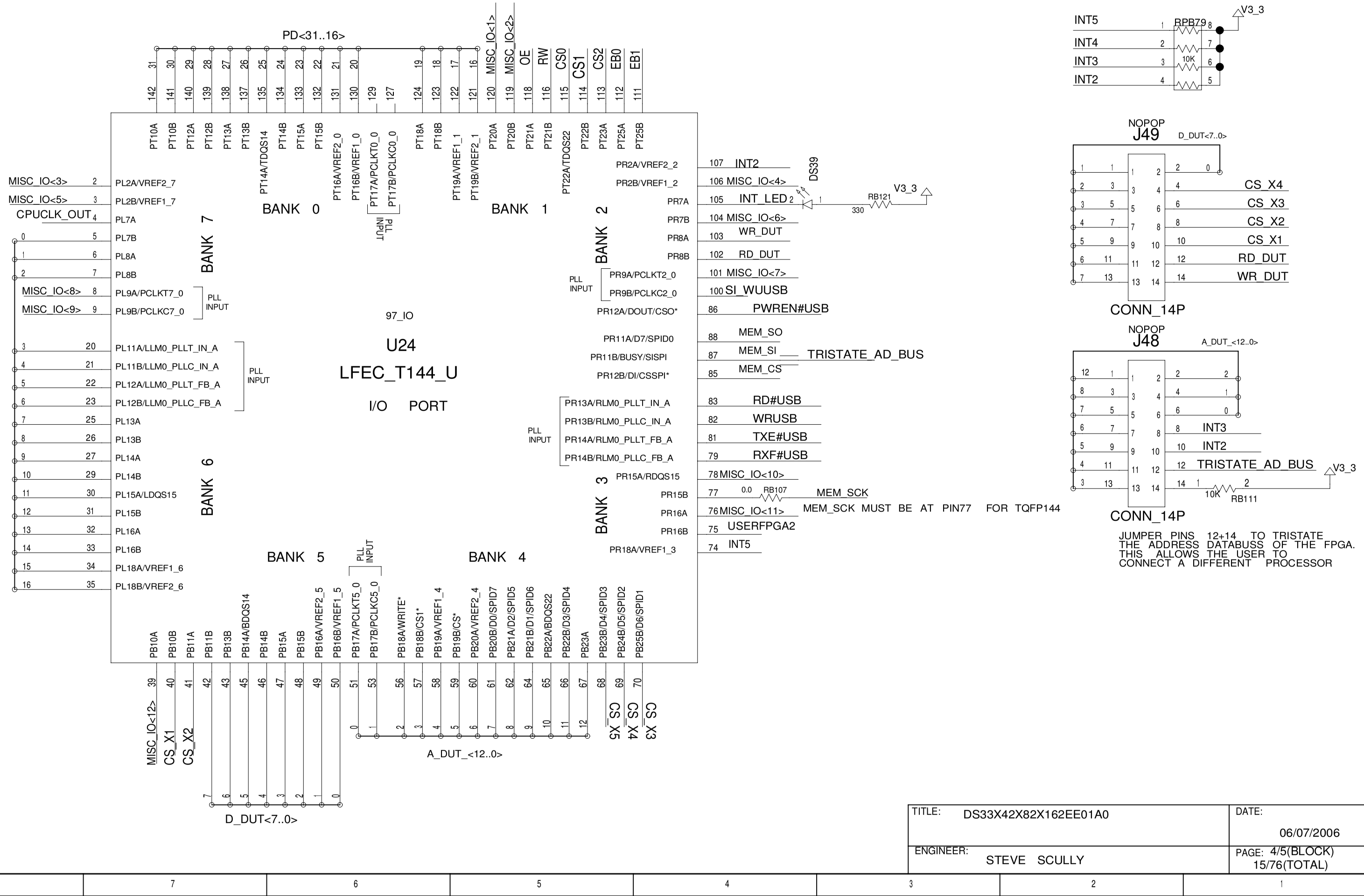






TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 14/76(TOTAL)

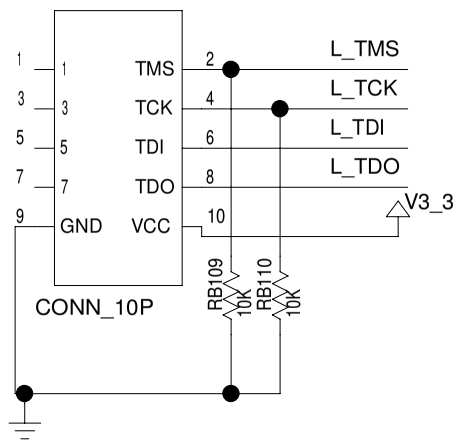
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x11dk_dn\



TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 4/5(BLOCK) 15/76(TOTAL)

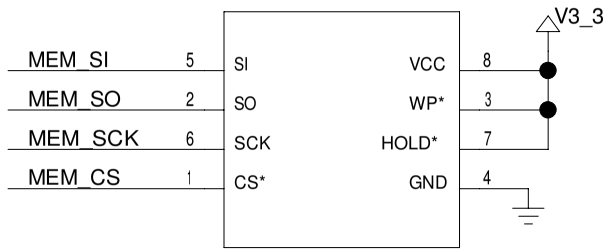
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x11dk_dn\

I24
J52



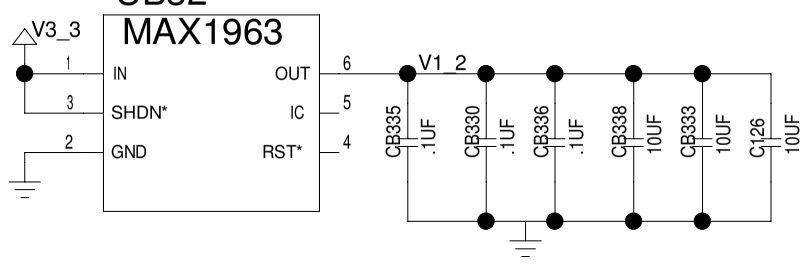
I26
2.7V

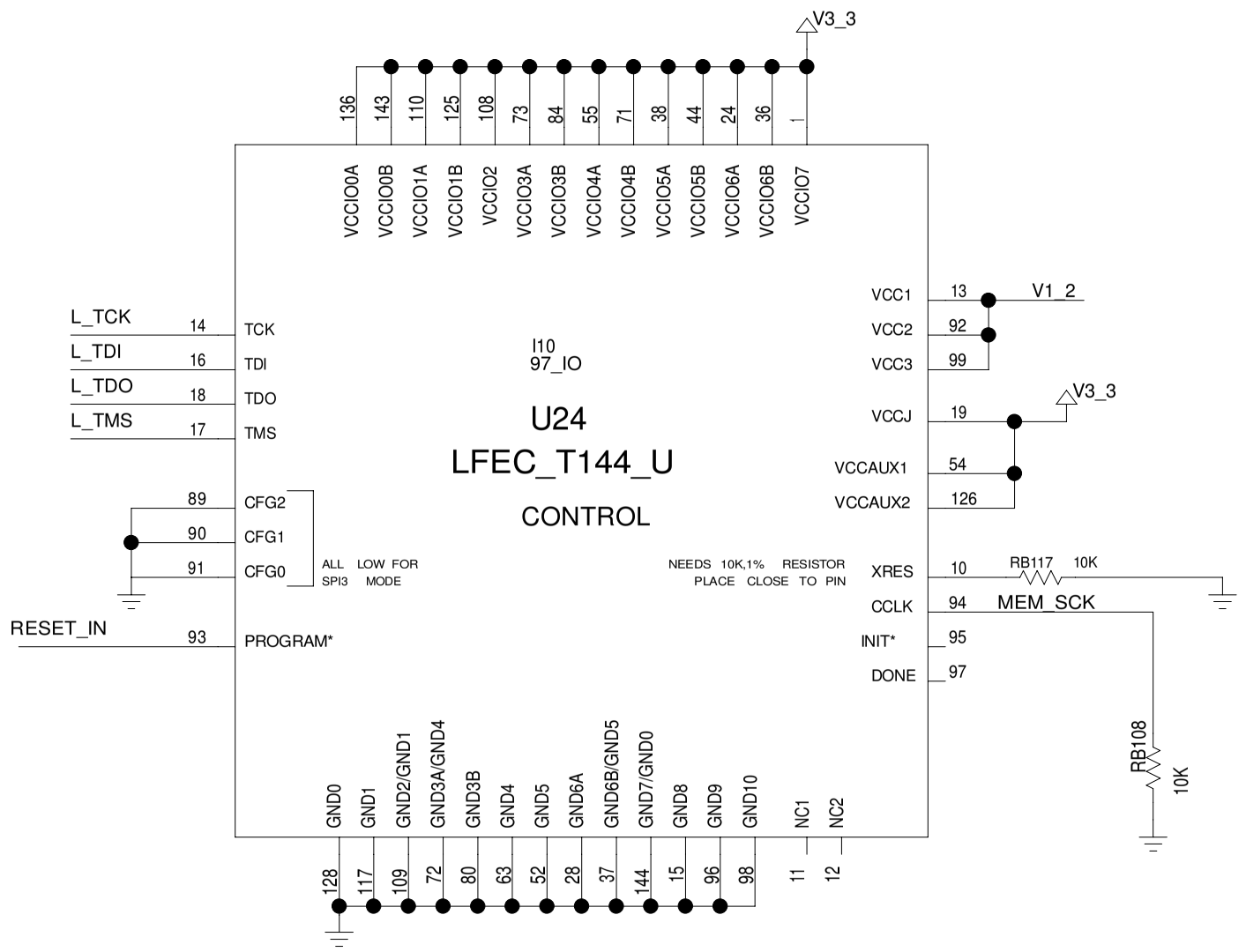
UB29



AT25160A_U

I28
UB32
MAX1963

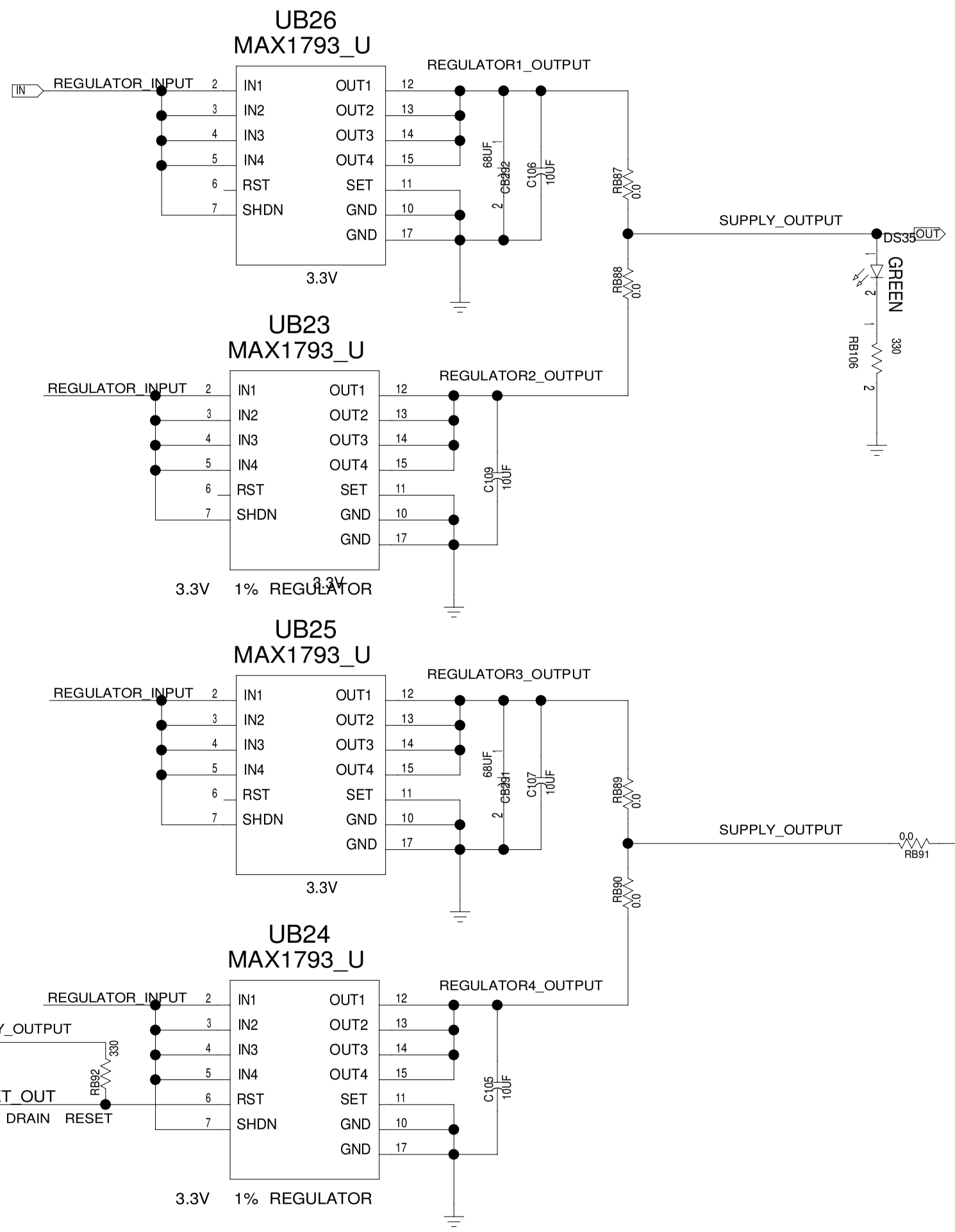


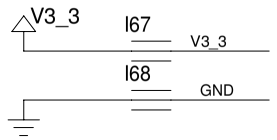


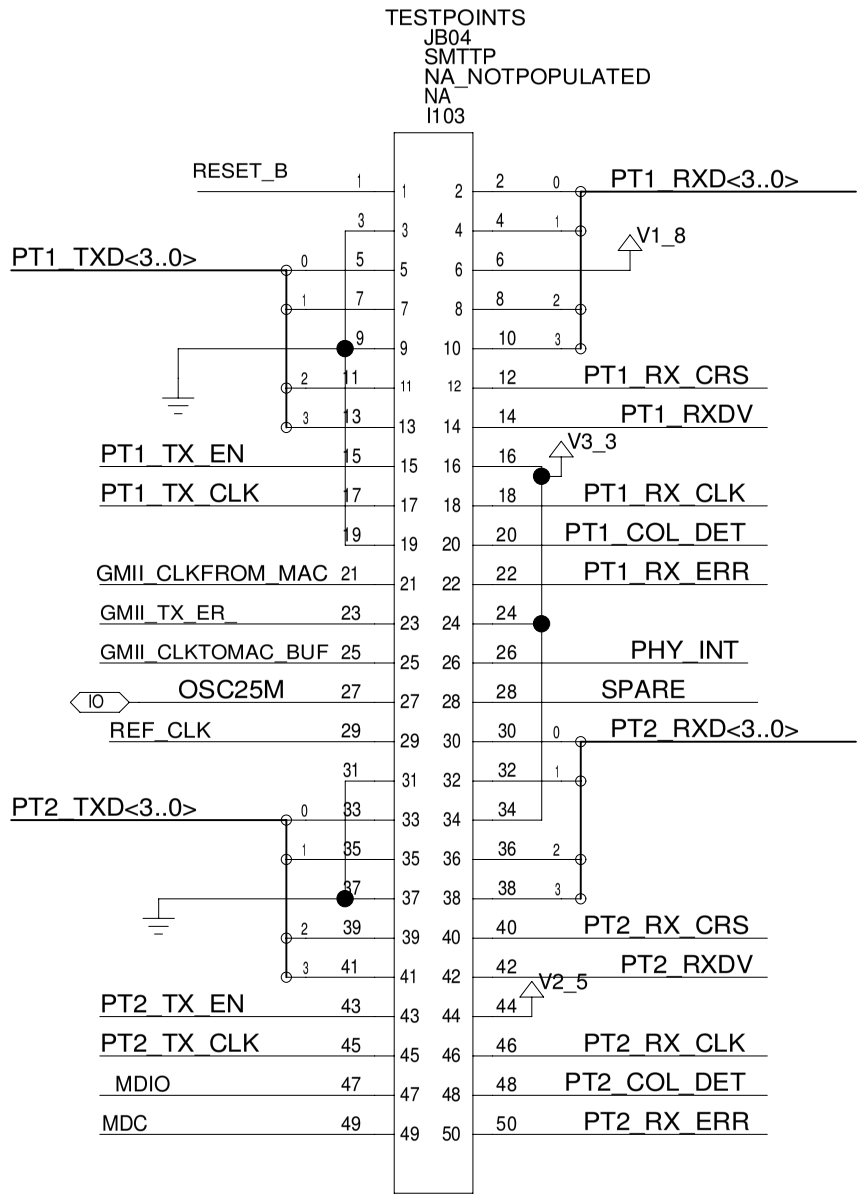
END OF PROCESSOR HIERARCHY BLOCK

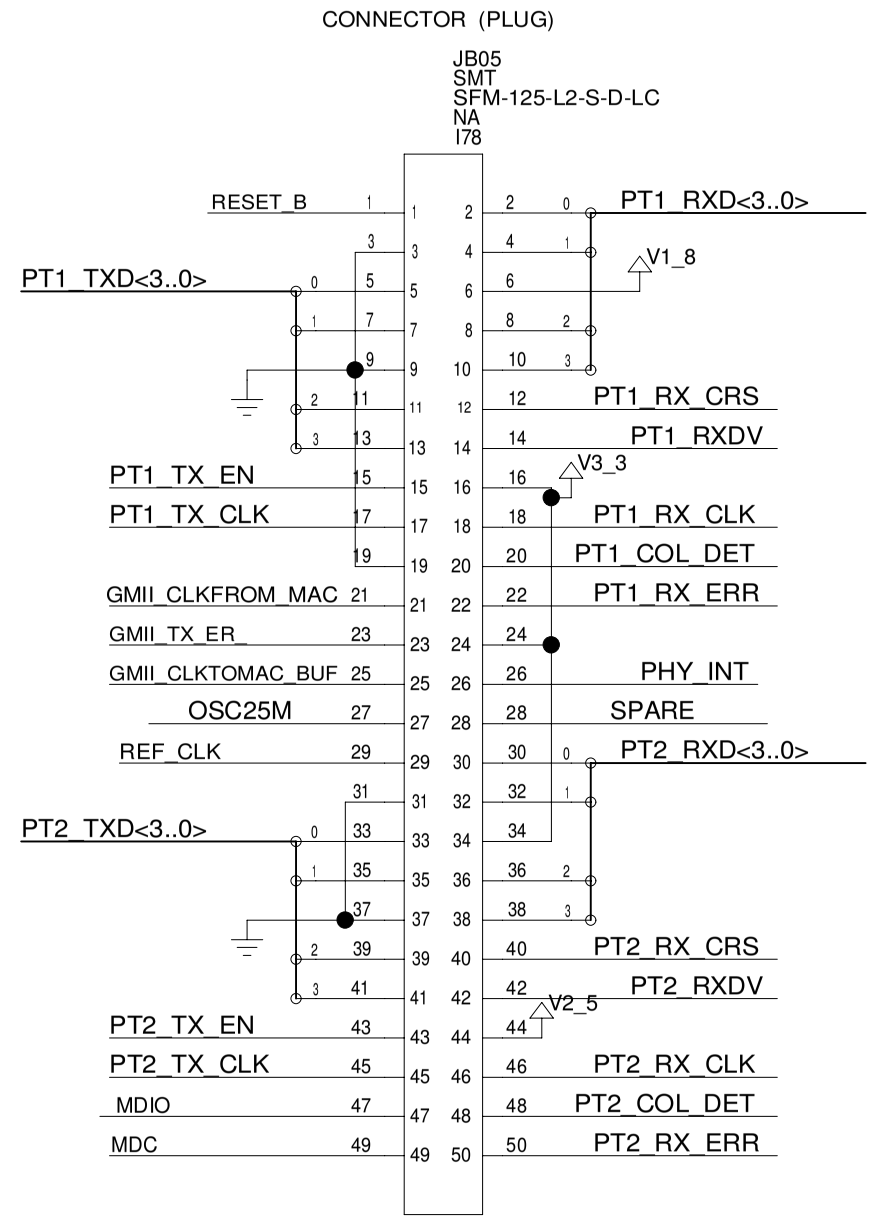
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 16/76(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds33x11dk_dn\


UB26
MAX1793_U
REGULATOR_INPUT
IN
IN1
IN2
IN3
IN4
RST
SHDN
OUT1
OUT2
OUT3
OUT4
SET
GND
GND
REGULATOR1_OUTPUT
68UF
CB292
C106
10UF
3.3V
RB87
0.0
RB88
0.0
SUPPLY_OUTPUT
DS35
OUT
GREEN
RB106
330
UB23
MAX1793_U
REGULATOR_INPUT
REGULATOR2_OUTPUT
C109
10UF
3.3V
3.3V 1% REGULATOR
UB25
MAX1793_U
REGULATOR_INPUT
REGULATOR3_OUTPUT
68UF
CB291
C107
10UF
3.3V
RB89
0.0
RB90
0.0
SUPPLY_OUTPUT
UB24
MAX1793_U
REGULATOR_INPUT
REGULATOR4_OUTPUT
SUPPLY_OUTPUT
RB92
330
OUT
RESET_OUT
OPEN DRAIN RESET
C105
10UF
3.3V 1% REGULATOR
TRACES BETWEEN REGULATOR OUTPUT AND V3.3 SHOULD
BE LONG ENOUGH TO BUILD 0.06 OHM OF RESISTANCE
TO ENSURE LOAD SHARING BETWEEN THE 3.3V 1% REGULATORS
TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER
5V DC POWER SUPPLY
REVERSE BIAS PROTECTION
REGULATOR_INPUT
DB02
1 AMP
68UF
CB279
68UF
CB281
C103
10UF
C101
10UF
C102
10UF
C100
10UF
3.3V
UB27
MAX1793_U
REGULATOR5_OUTPUT
RB91
0.0
SUPPLY_OUTPUT
REGULATOR_INPUT
10UF
C108
68UF
CB330
BEGINNING / END OF PHY
POWER SUPPLY HIERARCHY BLOCK
TITLE: DS33X42X82X162EE01A0
DATE: 06/07/2006
ENGINEER: STEVE SCULLY
PAGE: 1/1(BLOCK)
17/76(TOTAL)
BLOCK NAME: power_supply_4amp_dn.
PARENT BLOCK: _ds33x11dk_dn\







PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

REF_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

SPARE IO

GMII_CLKFROM_MAC IO
GMII_TX_ER_ IO
GMII_CLKTOMAC_BUF IO

CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD

BEGINNING & END OF PHY CONNECTOR + TESTPOINT HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 18/76(TOTAL)

BLOCK NAME: _phy_imbus_mb_dn. PARENT BLOCK: _ds33x11dk_dn\

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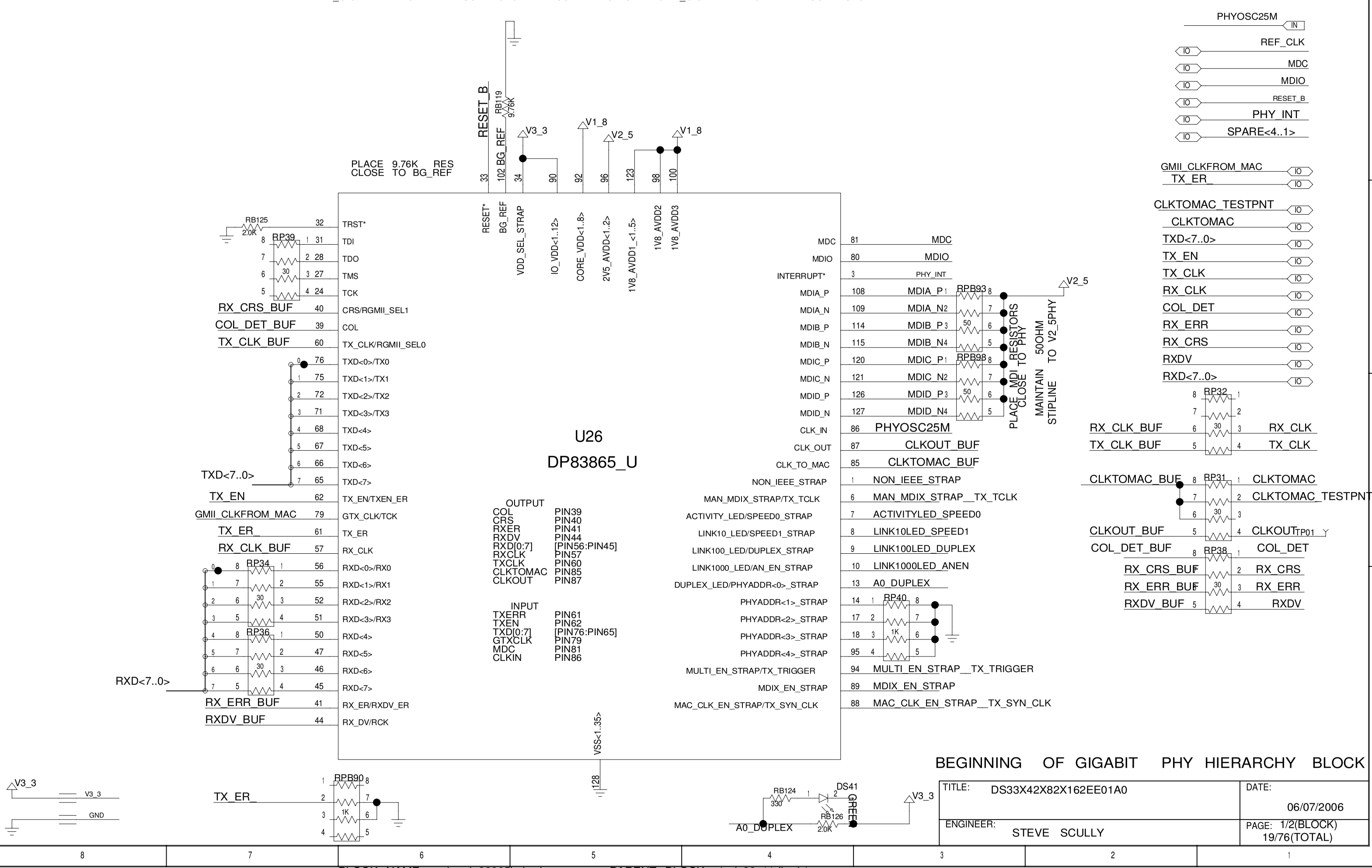
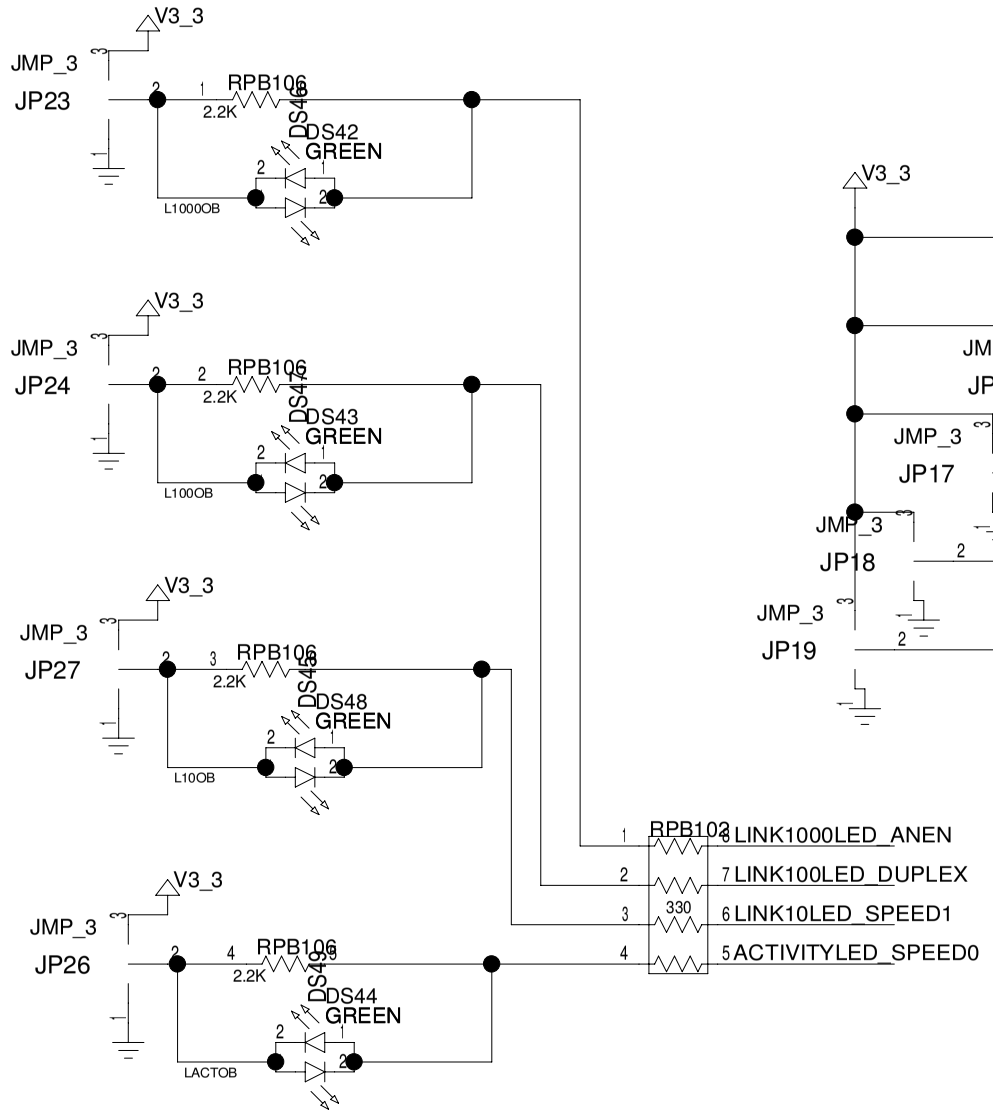


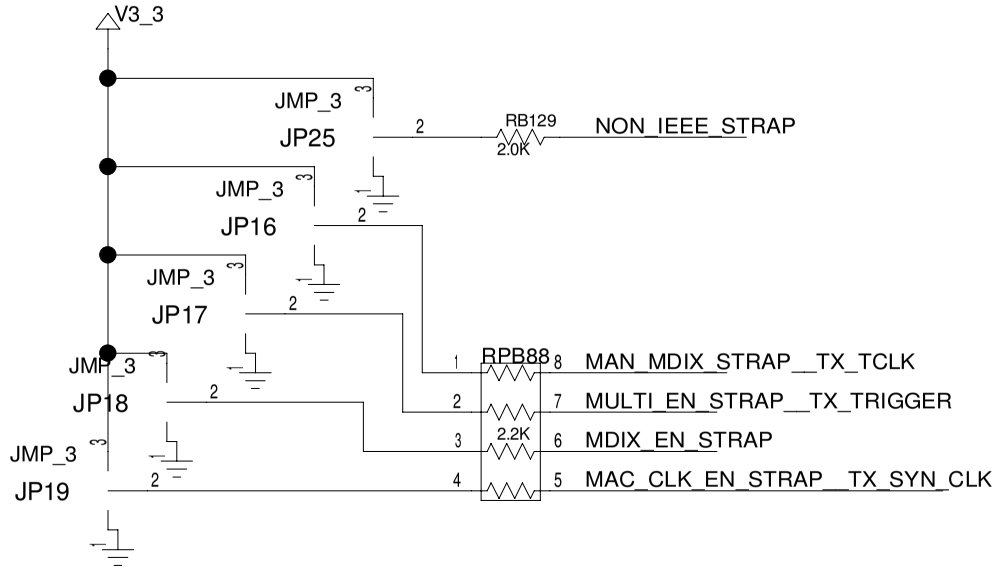
BEGINNING OF GIGABIT PHY HIERARCHY BLOCK

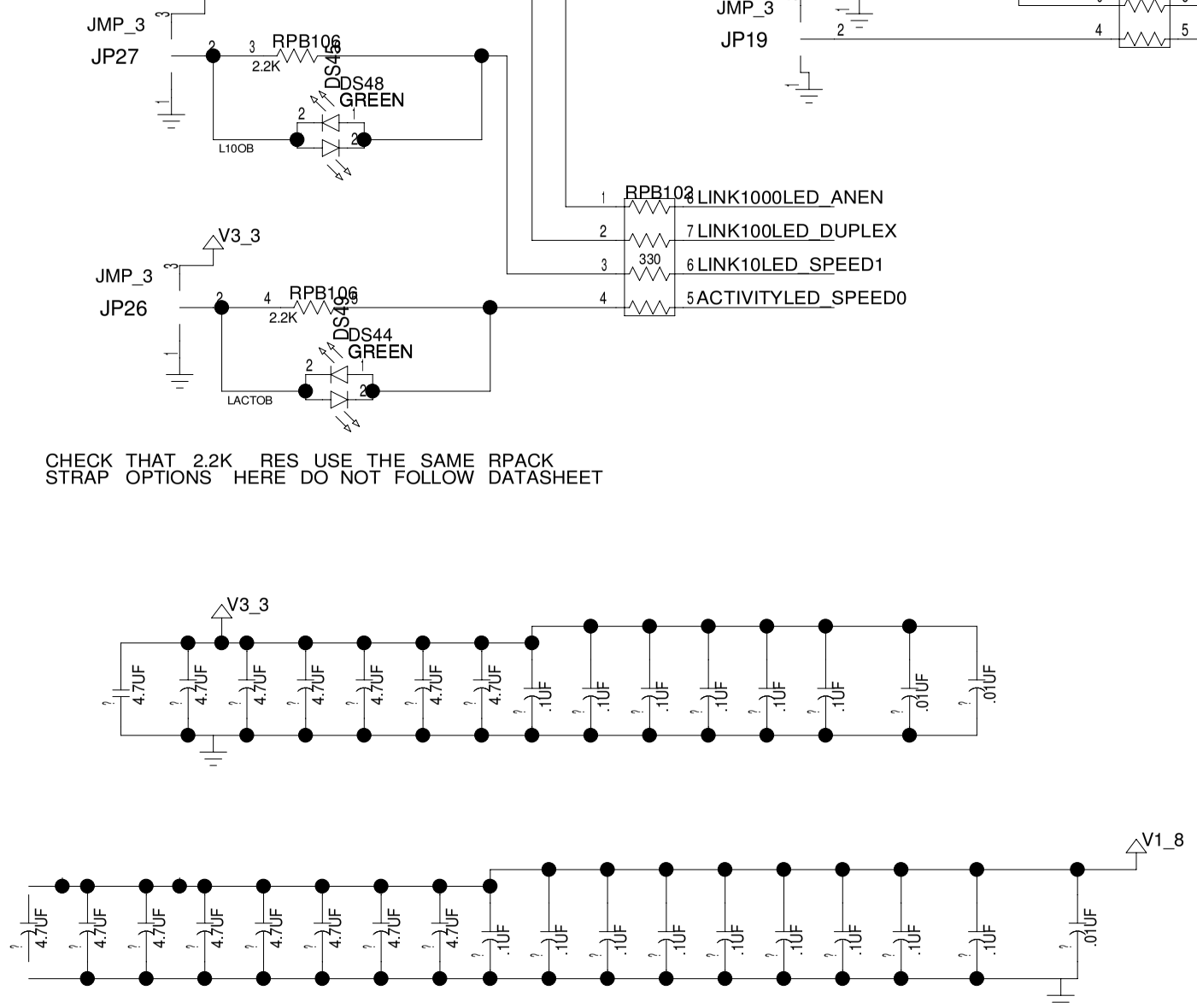
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 19/76(TOTAL)

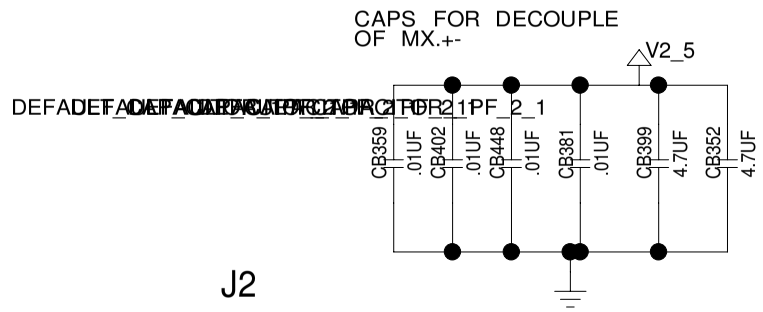
<TXT_GIGABITPHYMOTHERBRDCONNECTOR>. SCHEMATIC ON <PGNM_GIGABITPHYMOTHERBRDCONNECTOR>

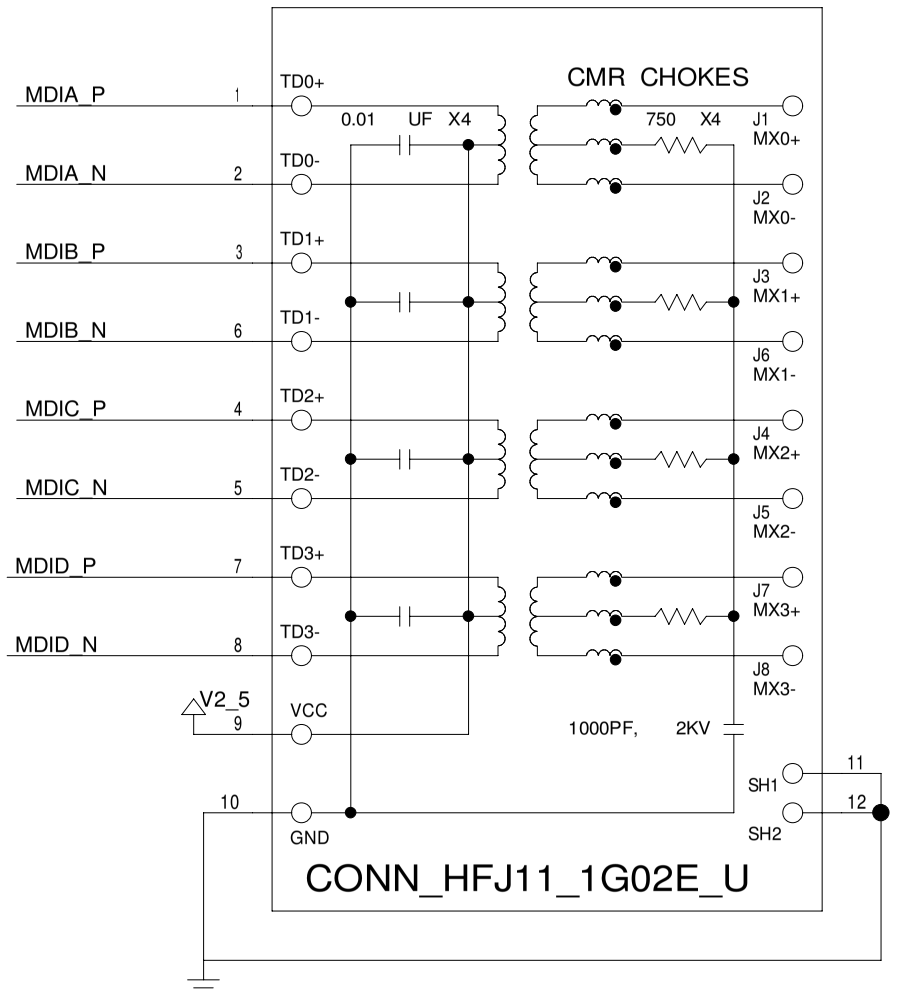


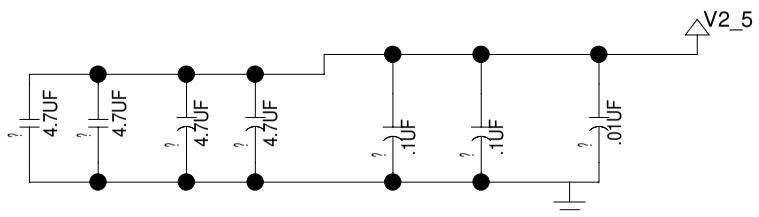
CHECK THAT 2.2K RES USE THE SAME RPACK
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET











END OF GIGABIT PHY HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 20/76(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _ds33x11dk_dn\

PRINTED Mon Feb 11 13:39:17 2008

44.736MHZ_3.3V

YB08

OSC

V3_3

VCC

GND

OUT

RB102 51

T3MCLK

ADDR<10..0>

DAT<7..0>

RPB82 1K

RPB83 1K

U20

DS3170_BGA_U

RPB81 330

RESET_B

T3_INT

MODE

WIDTH

TE3_TXP

TE3_TXN

TE3_RXP

TE3_RXN

RB105 332

RB103 332

RB94 51

RB93 51

T03

J44

J45

TREF1

RREF1

2:1

75 OHM 2P

RPB84 30

RB112 30

TE3_TCLKI

TE3_RCLKI

TE3_TSER

TE3_TGCLK

TE3_TSOFO

TE3_RSER

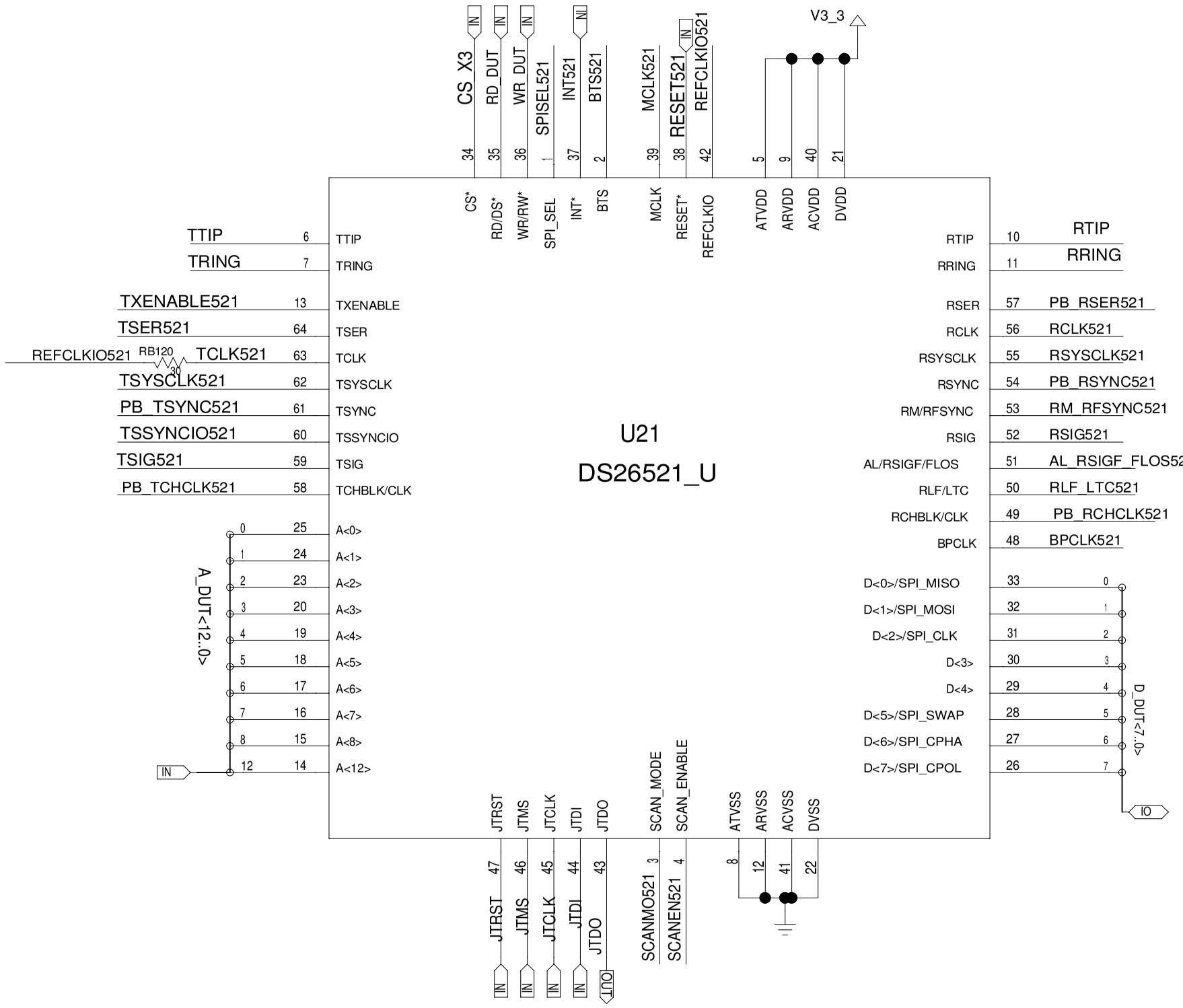
TE3_RGCLK

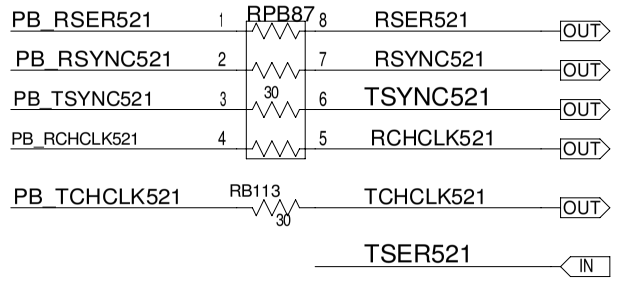
TE3_RSOFO

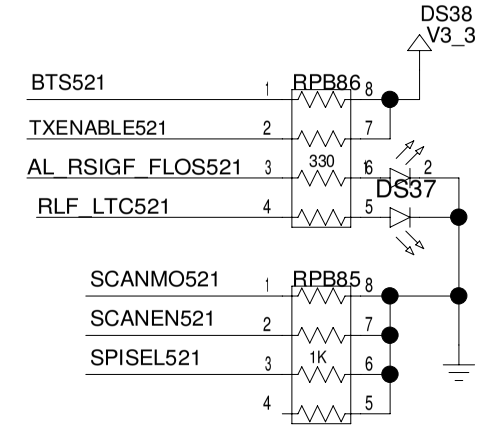
BEGINNING & END DS33X11 TE3 WAN BLOCK
(DS3170 SCT, TRANSFORMERS AND CONNECTORS)

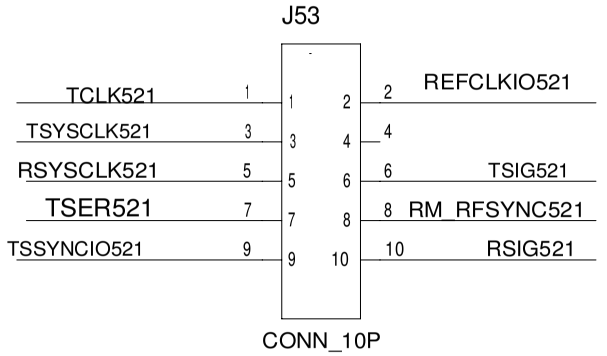
TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 21/76(TOTAL)

BLOCK NAME: _te3wan_dn. PARENT BLOCK: _ds33x11dk_dn\







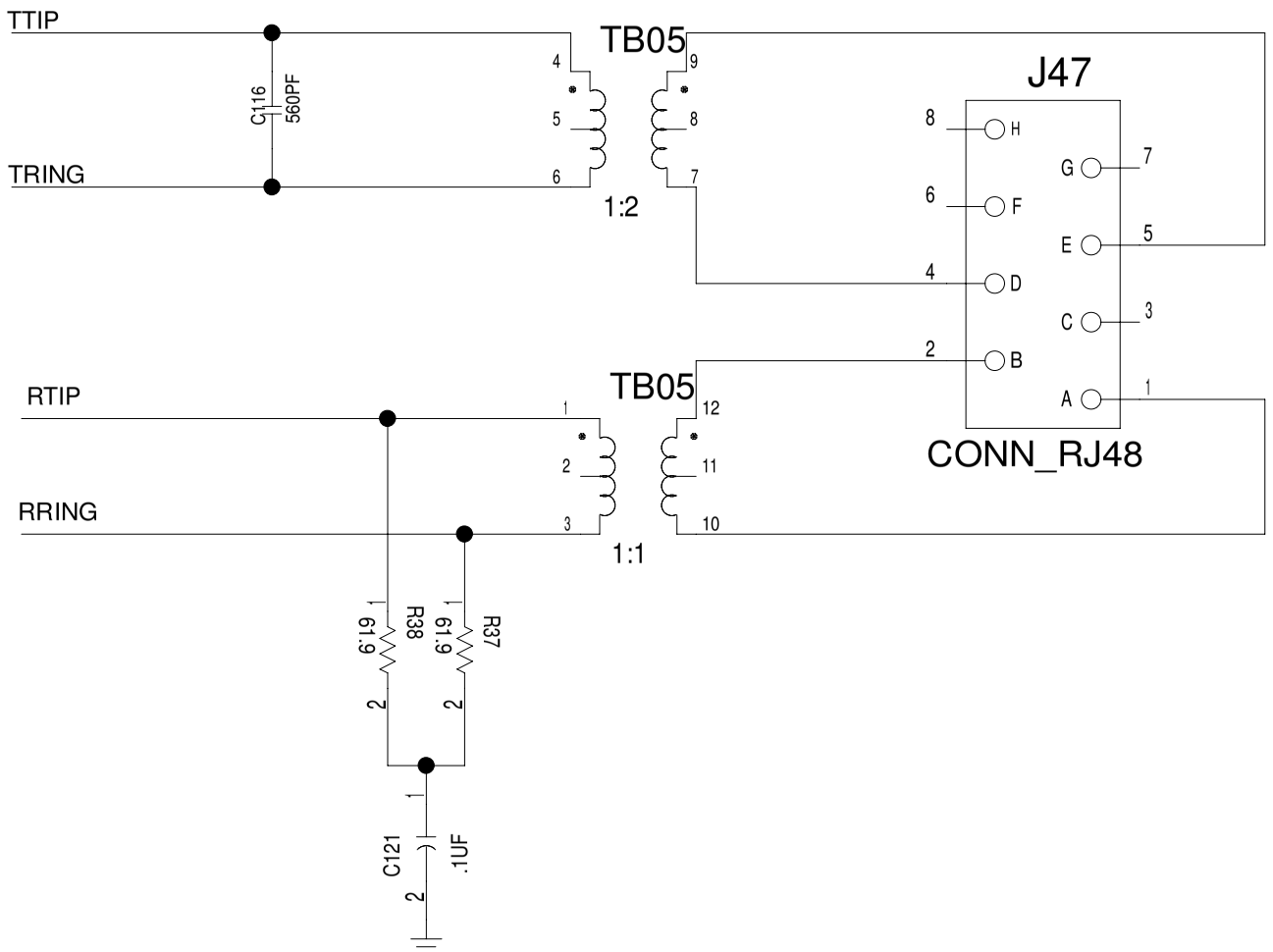


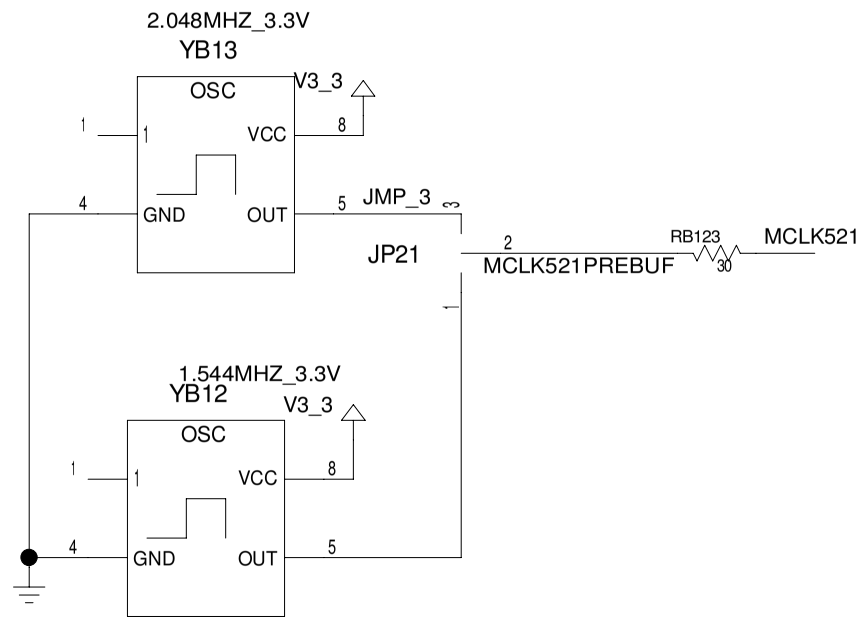
INT_LED AND TESTPOINTS FOR ADDR/DATA/CTRL ARE IN THE MICRO PROCESSOR BLOCK

BEGINNING OF DS26521DK HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 22/76(TOTAL)

BLOCK NAME: _ds26521dk01a0dutdn_. PARENT BLOCK: _ds33x11dk_dn\





END OF DS26521DK HIERARCHY BLOCK

TITLE: DS33X42X82X162EE01A0	DATE: 06/07/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 23/76(TOTAL)

BLOCK NAME: _ds26521dk01a0dutdn_. PARENT BLOCK: _ds33x11dk_dn\