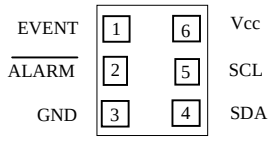
DALLAS SEMICONDUCTOR

DS1682
Total Elapsed Time Recorder with Alarm

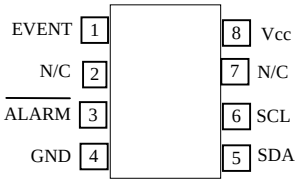
FEATURES

- Records the total time that the Event Input has been active and the number of events that have occurred
- Elapsed Time Counter to monitor event durations with quarter second resolution
- Built in 32 bit non-volatile Total Time Accumulator Register (34 years)
- Non-volatile 17-bit Event Counter records the total number of times an event has occurred
- Programmable 32 bit non-volatile alarm trip point to trigger Alarm# output
- Alarm# output to alert the user that the total accumulated time limit has been reached
- Calibrated, Temperature Compensated RC time base (accurate to 1% typ)
- Stores the contents of the Elapsed Time Counter with the previous total and increments the event counter at the end of each event or power down
- Reset Enable bit to allow the device to be cleared to zero, if desired
- 10 bytes of write protectable EEPROM user memory
- Write Disable bit to prevent the memory from being changed or erased
- Anti-Glitch filter will prevent noise spikes from triggering false events on the Event Input
- 2-wire serial communication
- Wide power supply range (2.5V – 5.5V)

PIN ASSIGNMENT



Bottom View
DS1682X 6-pin Flip Chip



Top View
DS1682S 8-Pin SOIC (150 mil)

PIN DESCRIPTION

EVENT	- Event Input
ALARM	- Alarm Output
GND	- Ground
SDA	- 2-wire Data Input/Output
SCL	- 2-wire Clock Input
V_{CC}	- Voltage Supply
N/C	- No Connect

ORDERING INFORMATION

DS1682	8-Pin µSOP
DS1682S	8-Pin SOIC (150 mil)
DS1682X	6-Pin Flip Chip Package

** For more information of Flip Chip Packaging, go to www.dalsemi.com to the Released Data Sheets section and select Chip Scale and Flip Chip Package Data Index.

DESCRIPTION

The DS1682 is an integrated elapsed time recorder that will provide the total amount of time that an event is/has been active since the DS1682 was last reset to zero via the 2-wire bus. When the total time accumulated is equal to the preset alarm trip point and the polarity bit is set to a zero, the Alarm# output will become active to alert the user, or with the polarity bit set to a one, the Alarm# output will become inactive when the values match. This is ideal for applications such as monitoring the total amount of time that something is turned on or in operation, how long something has been used, or the total number of uses since the last calibration or repair.

The DS1682 uses a calibrated, temperature compensated RC time base to increment an elapsed time counter while an event is active. When the event becomes active, the contents of the non-volatile Total Time Accumulator register are downloaded to the Elapsed Time Counter (ETC) and as the event continues, the ETC is incremented in quarter second increments. When the event becomes inactive or the power is removed, the DS1682 will increment the 17-bit non-volatile Event Counter register and put the contents of the ETC into the 32-bit non-volatile Total Accumulated Time register which can hold up to 34 years of active event time. A storage cap may be required on V_{CC} to provide enough power to store the value in the ETC to the Total Time Accumulator register if power is taken away at the same time the event ends.

When the 32-bit non-volatile Alarm Trip Point register is programmed to a non-zero number via the 2-wire bus and the AoR bit in the Configuration register set to a zero, the Alarm# output will be enabled and the DS1682 will begin to monitor the values in the ETC for the programmed value in the Alarm Trip Point register. Once the number in the ETC is equal to or greater than the value in the Alarm Trip Point register, and the polarity bit is set to a zero, the Alarm# output will become active to alert the user, or with the polarity bit set to a one, the Alarm# output will become inactive when the values match. The DS1682 will activate the Alarm# output by pulling the pin low four times at power up, when the alarm becomes active, or when the Alarm# pin is pulled low and released if the AOS bit is set to a 1. If the AOS bit is a 0, the Alarm# output will be constantly low when the alarm is active.

In order to reset the device, the Reset Enable bit or the AoR bit in the Configuration register must be set to a 1. With the Reset Enable bit set to a 1 or the AoR bit set to a 1 with the Alarm# pin held high, the DS1682 can be reset by the Reset command sent over the 2-wire bus. If the Write Disable flag in the Configuration register is set to a 1 by writing the Write Disable command two times, the Configuration registers and Alarm Trip Point register will not be able to be written. If the Write Disable flag is set to a 1, the Total Time Accumulator, Elapsed Time Counter, and Event Counter will be able to be reset, if the Reset Enable or AoR bits have been set to a 1, but the status of the Reset Enable or AoR bits will not be able to be changed since the Configuration register is locked by the WDF being set to a 1.

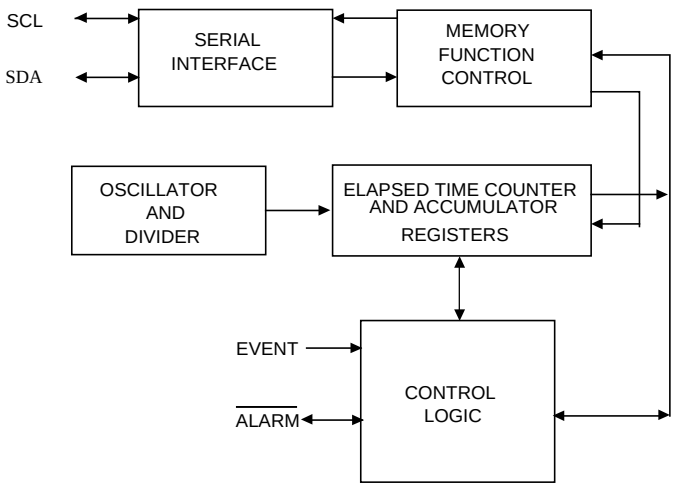
The Write Memory Disable is similar to the Write Disable and is used to control the writability of the 10 bytes of EEPROM User memory. The Write Memory Disable Flag is also set to a 1 when the Write Memory Disable command is written twice and can not be changed once it is set to a 1. If the Write Memory Disable bit is set to a 1, the 10 bytes of memory will not be able to be written or erased. If the Write Memory Disable bit is a 0, the user will have full access to the bytes with the standard EEPROM write time restrictions. If the Write Disable is a 0, the device is fully writable or erasable except for the User Memory and the Write Memory Disable flag, which are only controlled by the Write Memory Disable command. With both the Write Disable and Write Memory Disable set to 1's, the only inputs that will be accessible are the Reset command if it is enabled, the Event input and the Alarm# input/output. The rest of the part will be read only.

When data is written to the device, the device slave address will be sent first followed by the address pointer and the desired byte of data. Once a single byte of data is sent, there must be at least 200 mS to allow the EEPROM to update the data.

OVERVIEW

The block diagram in Figure 1 shows the relationship between the major control and memory I/O sections of the DS1682. The device has three major components: 1) clock generator and control blocks, 2) elapsed time counter and accumulator registers, and 3) 2-wire interface.

DS1682 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

The following paragraphs describe the function of each pin.

V_{CC} – V_{CC} is a +3-5 volt input supply. A capacitor or other temporary energy source may be required to hold the Voltage 150 mS after the event has completed if the system power is removed at the same time as the event ends in order to allow the contents of the ETC to be stored properly. With less than the 150 mS of power after the end of the event, the data may be lost. The LSB is written first to be sure that the most likely changed data is saved first.

GND - Ground

SCL (2-wire Serial Clock Input) – The SCL pin is the serial clock input for the 2-wire synchronous communications channel. The SCL pin is an open drain input, which requires an external pull–up resistor.

SDA (2-wire Input/Output) – The SDA pin is the data Input/Output signal for the 2-wire synchronous communications channel. The SDA pin is an open drain I/O, which requires an external pull–up resistor.

EVENT (Event Interrupt Input) – The Event pin is an input that will be activated by an external device to signify an event has occurred and should be logged. When the pin is pulled high, the Elapsed Time Counter (ETC) will begin to keep track of the time with quarter second resolution and when the pin is pulled low, the contents of the ETC will be stored to the non-volatile Total Time Accumulator register and the Event Counter register will be incremented. A pull-down resistor has been internally connected to the Event input to prevent power-up glitches from triggering a false event. The Event input has a Glitch filter to prevent very short noise spikes from triggering an event. A capacitor or other temporary energy source may be required to hold the Voltage 150 mS after the event has completed if the system power is removed at the same time as the event ends in order to allow the contents of the ETC to be stored properly. With less than the 150 mS of power after the end of the event, the data may be lost. The LSB is written first to be sure that the most likely changed data is saved first. When the Event pin changes states, the 2-wire bus will be unavailable for communications for 200 mS.

ALARM# (Alarm Output) - When there is a non-zero number programmed into the Alarm Trip Point register and a zero in the AoR bit of the Configuration register, the Alarm# output will be enabled and the DS1682 will begin to monitor the values in the ETC for the programmed value in the Alarm Trip Point register. When the Polarity bit in the Configuration register is set to a zero the Alarm# output will become active when the Alarm Trip Point is exceeded. When the Polarity bit is set to a one, the Alarm# output will be inactive until the Alarm Trip Point is exceeded. With the AoR bit in the Configuration register set to a one, the Reset Enable input will be mapped to the Alarm# pin.

N/C (No Connect) – This pin is not connected internally.

MEMORY MAP

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
00	AoR	AF	WDF	WMDF	AOS	RE	AP	ERO	Config. Register
01	Low Byte								Alarm
02	Low-Middle Byte								Trip
03	High-Middle Byte								Point
04	High Byte								
05	Low Byte								Total
06	Low-Middle Byte								Time
07	High-Middle Byte								Accumulator
08	High Byte								
09	Low Byte								Event
0A	High Byte								Counter
0B	Byte One								
0C	Byte Two								
0D	Byte Three								User
0E	Byte Four								Memory
0F	Byte Five								
10	Byte Six								
11	Byte Seven								
12	Byte Eight								
13	Byte Nine								
14	Byte Ten								
15	Not Used (reads 00h)								Not Used
16									
17									
18									
19									
1A									
1B									
1C									
1D	Reset Command								Reset Command
1E	Write Disable								Write Disable
1F	Write Memory Disable								Memory Disable

DATA LOGGING

When the DS1682 is powered-up, the contents of the Total Time Accumulate register (TTA) are downloaded to the ETC and the device begins looking for events that trigger the Event input. When an event triggers the input by transitioning to a high level input, the ETC begins incrementing in quarter second resolution. When the Event input falls below $0.5*V_{CC}$ to indicate the end of an Event, a power failure, or power-down, the contents of the ETC are stored to the non-volatile Total Time Accumulator register, the Event Counter register is incremented and the ETC is prepared for the next event. There is a built in pull-down on the Event input to prevent power-up glitches from triggering a false event. As the ETC is being incremented, there is a non-zero value in the ATP register and the AoR bit in the Configuration register is set to a 0, the DS1682 will compare the value in the ETC to the value in the Alarm Trip Point register to see when the value in the ETC is equal to or greater than the value in the Alarm Trip Point register. When the value in the ETC exceeds the value in the Alarm Trip Point register, the Alarm# output is enabled/disabled depending on the value of the Polarity bit.

The ETC will not roll over to 0000h once FFFFh is reached. The DS1682 will stop counting time once FFFFh is reached. This should take approximately 34 years with the event pin pulled high. When the Event pin is transitioned, the 2-wire bus is not available for communications for 200 mS.

CLOCK

The clock circuitry consists of a calibrated, temperature compensated RC time base and a 32-bit Elapsed Time Counter (ETC) which increments on the quarter second. The total time of all events is stored in the non-volatile Total Time Accumulator register. As the ETC is being incremented and there is a non-zero value in the ATP register and the AoR bit in the Configuration register is set to a 0, the DS1682 will compare the value in the ETC to the value in the Alarm Trip Point register to see when the value in the ETC is equal to or greater than the value in the Alarm Trip Point register. When the value in the ETC exceeds the value in the Alarm Trip Point register, the Alarm# output is enabled/disabled depending on the value of the Polarity bit.

TOTAL TIME ACCUMULATOR REGISTER

The Total Time Accumulator register is an EEPROM based 32 bit register that holds the total “ON” time of all events up to a total of about 34 years worth of event time. This value is not erasable when the Reset Enable and AoR bits in the Configuration register are set to a zero and does not require a power source to insure the data’s integrity. This register can only be cleared when the Reset Enable bit in the Configuration register is set to a one or the AoR bit is set to a 1 with the Alarm# pin held high, and the Reset command is sent via the 2-wire bus. A capacitor or other temporary energy source may be required to hold the Voltage 150 mS after the event has completed if the system power is removed at the same time as the event ends in order to allow the contents of the ETC to be stored properly. With less than the 150 mS of power after the end of the event, the data may be lost. The LSB is written first to be sure that the most likely changed data is saved first.

ALARM TRIP POINT REGISTER

The Alarm Trip Point register (ATP) is a 32-bit register that holds the time value in quarter seconds that is set by the user via the 2-wire bus to enable/disable the Alarm# output when the value is equal to or greater than the value in the ETC.

EVENT COUNTER REGISTER

This 17-bit register set provides the total number of data samples that have been logged during the life of the product up to 131,072 separate events. The Event Counter consists of 2-bytes of memory in the memory map and the MSb being the Event Roll Over flag in the Configuration Register. The Event Roll

Over bit is set to a 1 the first time that the 2 byte Event Counter reaches FFh and rolls over to 00h. Once the Event Roll Over bit is set to a 1 and the Event Counter reaches FFh, event counting will stop and the event counter will not roll over to 00h again. This value is not erasable when the Reset Enable and the AoR bits in the Configuration register are set to a zero and does not require a power source to maintain the contents to insure the data's integrity. This register can only be cleared when the Reset Enable bit is set to a one or the AoR bit is set to a 1 and the Alarm# pin is held high, and the Reset command is sent via the 2-wire bus.

RESET COMMAND

The DS1682 can only be reset when the Reset Enable bit is set to a one or the AoR bit is set to a one with the Alarm# pin held high, and the Reset command is sent via the 2-wire bus by writing 55h into memory location 1Dh. With the Reset Enable bit set to a 0, the AoR bit set to a 0 or the AoR bit set to a 1 and the Alarm# pin held low, the Reset command is ignored by the DS1682. With the Write Disable flag set to a 1, the contents of the Alarm Trip Point and the Configuration register that are protected/locked by this bit can not be written to or erased, even if the Reset Enable bit is set to a 1. The Reset command when the Reset Enable bit is set to a one or the AoR bit set to a 1 and Alarm# held high, will erase the contents of the Elapsed Time Counter, Total Time Accumulator, and Event Counter. The Reset Command will always read 0 if the memory location is read by the user.

CONFIGURATION REGISTER

MSb							LSb
AoR	AF	WDF	WMDF	AOS	RE	AP	ERO

AoR – Alarm or Reset Enable - The Alarm or Reset Enable bit maps either the Alarm output or the Reset Enable Input to the Alarm# pin. With the AoR bit set to a zero, the Alarm output will be mapped to the Alarm# pin. When the AoR bit is set to a one, the Reset Enable input will be mapped to the Alarm# pin. The standard factory setting for the AoR bit is 0. The Reset Enable input is OR'ed with the RE bit and will perform the same function only from outside the device.

The Reset Enable input, if pulled high, will allow the D1682 to accept the Reset command via the 2-wire bus to clear the Total Time Accumulator and Event Counter. If the Reset Enable input is pulled low, the DS1682 will not respond to the 2-wire command to reset the Total Time Accumulator register or the Event Counter to zero. This input allows the designer to permanently enable the reset function, enable the function during the manufacturing process and then disable it, or turn it on and off when the authorized repair person has completed repairing or calibrating the equipment. There is no security provided to this pin to prevent someone from enabling the reset function at any time by pulling the pin high. The security will have to be provided by the system and/or enclosure, if required. If a switch or button is used to Configuration the Reset Enable input, a debounce capacitor should be used to prevent spikes on the input.

AF – Alarm Flag - The Alarm Flag is set to a 1 when the Alarm# output is activated. If the Alarm# pin is not activated or enabled, the Alarm Flag will be set to a 0. This bit can be cleared by the reset command, but will be set again at the end of the next event in which the ETC and ATP values cause the Alarm# pin to be enabled or activated. This bit can not be written by the user.

WDF – Write Disable Flag – When the Write Disable Command is written to AAh twice at memory location 1Eh, the WDF will be set to a 1 and can not be cleared or reset. When the WDF is set to a 1, the Alarm Trip Point and Configuration register are read-only. The Total Time Accumulator, Elapsed Time Counter, and Event Counter will also be read only if the Reset Enable and AoR bits are set to a 0. When

the WDF is set to a 0, the Alarm Trip Point, Configuration register, Total Time Accumulator, Elapsed Time Counter, and Event Counter can be written to(if user writable), erased or read.

WMDF – Write Memory Disable Flag – When the Write Memory Disable command is written to F0h twice at memory location 1Fh, the WMDF will be set to a 1 and will not be able to be reset or cleared. Once the WMDF is set to a 1, the 10 byte User Memory will become read-only. When the WMDF is a 0, the User Memory will function like normal EEPROM.

AOS – Alarm Output Select – The AOS bit selects the output type for the Alarm# pin. With the AOS bit set to a 0, the output will be a constant low when Alarm# is active to burn a fuse, interrupt a processor or send a logic signal to other digital circuitry. With the AOS bit a 1, the output of the Alarm# pin will be pulled low four times to flash an LED or communicate with an other device at power up, when the Alarm# pin is pulled low and release or when the alarm becomes active.

RE – Reset Enable – The Reset Enable bit will allow the device to be reset by enabling the Reset command. The sections of the 1682 that will be reset is then dependent on the value in the Write Disable Flag. With the WDF set to 0 and the Reset Enable bit set to a 1, the Reset command will clear the Elapsed Time Counter, Total Time Accumulate, and Event Counter. When the Reset Enable bit is set to a 0, the Reset command will be disabled.

AP – Alarm Polarity – The Alarm Polarity bit is intended to allow the Alarm to become active or enabled when the Total Time Accumulate register is equal to or greater than the Alarm Trip Point register value (AP=1), or conversely, to allow the Alarm to become active or enabled when the Total Time Accumulate register is less than the Alarm Trip Point register value (AP=0). This feature allows the user to have the Alarm output after the values match (AP=1) or up until the values match (AP=0).

ERO – Event Counter Roll Over – The ERO bit acts like the 17^{th} bit of the Event Counter. When the Event Counter reaches FFh the first time, the next event will cause the ERO to transition from a 0 to a 1 and the Event Counter will roll over to 00h. Once the ERO is set to a 1, the Event Counter will not roll over again. The Event Counter will stop counting events when the ERO is set to 1 and the Event Counter is set to FFh.

WRITE DISABLE/WRITE MEMORY DISABLE

The 1682 has two 8 bit registers designed to prevent parts of the device from being written to or erased. These registers will always read 0 if read by the user, but the Write Disable Flag (WDF) and Write Memory Disable Flag (WMDF) in the Configuration register will indicate the ability or inability to write the memory locations.

Write Memory Disable – This register when written two times consecutively to F0h at memory location 1Fh will disable the ability to write to the 10 Bytes of User memory. It will not affect the Alarm Trip Point register, Total Time Accumulate register, Configuration register, Event Counter, Write Disable register, or the Reset command. Once the Write Memory Disable written is written to F0h, it will set the Write Memory Disable Flag in the Configuration register to a 1 and it can not be reset to 0 to allow writing to the User memory and the memory is permanently disabled from future writes. The memory becomes Read-Only.

Write Disable – After being written two times consecutively to AAh at memory location 1Eh, will disabled writes to the device by setting the Write Disable flag in the Configuration register to a 1, permanently. The Reset command, if the Reset Enable bit in the Configuration register is set to a 1, and the User memory, if the Write Memory Disable flag is still set to 0, will be the only areas of the 1682 that

will be able to be written. Once written twice to AAh, the Write Disable to set the Write Disable flag to a 1, it will not be able to be reset and the Configuration register, Total Time Accumulate register, Event Counter, and Alarm Trip Point register will become Read-Only. The User memory is not affected by the Write Disable register.

GLITCH CONTROL CIRCUIT

The DS1682 has a built in glitch control circuit to prevent input noise on the EVENT pin from triggering false events or corrupting the data.

USER MEMORY

There are 10 bytes of user programmable, EEPROM memory. Once the Write Memory Disable Flag is set to a one, the memory can not be erased or written to again. This is good for locating serial numbers, manufacture dates, warrantee information, or other important information. With the Write Memory Disable Flag set to a 0, the user memory is readable, writable and erasable.

SERIAL INTERFACE

The DS1682 provides two-wire serial communications.

2-WIRE SERIAL DATA BUS

The DS1682 supports a bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1682 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (See Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1682 only supports the standard mode of operations.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Depending upon the state of the R/W* bit, two types of data transfer are possible:

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1682 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1682 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1682, this is set as 1101 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). These bits are set to 011 (A2=0, A1=1, A0=1) for the DS1682. They are used by the master device to select which of eight devices are to be accessed. The set bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/W*) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1682 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1101 code and appropriate device select bits of 011, the DS1682 outputs an acknowledge signal on the SDA line.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

- This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

- The Dallas Semiconductor DS1682X is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, the DS1682X is not exposed to environmental stresses, such as burn-in, that some industrial applications require. For specific reliability information on this product, please contact the factory in Dallas at (972) 371-4448.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.5		5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

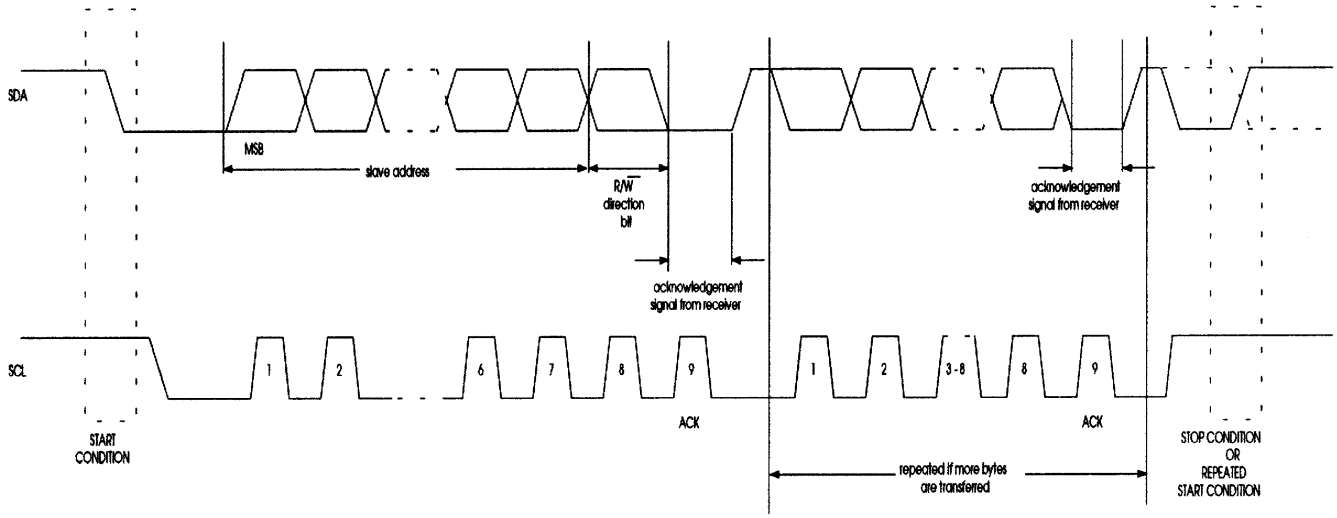
DC ELECTRICAL CHARACTERISTICS (-40°C to 85°C; V_{CC} = 2.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	
Logic 0 Output	V_{OL}			0.4	V	
ALARM# Output Constant Current @ 0.8V	I_{OL}	10			mA	
SDA & SCL Pins Output Current @ 0.8V	I_{OL}	4			mA	
Active Supply Current	I_{CCA}		100	300	µA	
EEPROM Write Current	I_{EE}		30	100	µA	
Event Trip Point	V_{ETP}		0.5*V_{CC}		V	

AC ELECTRICAL CHARACTERISTICS (-40°C to 85°C; V_{CC} = 2.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
EEPROM Lockout Time after event	t_{EEV}	500			ms	
Time from Event = (0.5*V_{CC}) until ETC Fully Stored (V_{CC} > 2.7V)	t_{PF}	50		100	ms	
EEPROM Write Time	t_{EW}		150	200	ms	
Alarm# Output Active Low Pulse Width	t_{SL}		62.5		ms	
Alarm# Output Active High Pulse Width	t_{SH}		437.5		ms	
Alarm# Input Pulled Low and Released Pulse Width	t_{SPL}		500		ms	
Minimum Signal Hold Time	t_{SIG}	TBD			ms	
Minimum Event Hold	t_{EVNT}	TBD			ms	
Input Capacitance	Ci		5		pF	
SCL clock frequency	fscl			100	kHz	
Bus free time between a STOP and START condition	tbuf	4.7			µs	
Hold time (repeated) START condition.	thd:sta	4.0			µs	2
LOW period of SCL	tlow	4.7			µs	
HIGH period of SCL	thigh	4.0			µs	
Set-up time for a repeated START	tsu:sta	4.7			µs	
Data hold time	thd:dat	0			µs	
Data set-up time	tsu:dat	250			ns	
Rise time of both SDA and SCL signals	tr			1000	ns	
Fall time of both SDA and SCL signals	tf			1000	ns	
Set-up time for STOP	tsu:sto	4.0			µs	
Capacitive load for each bus line	Cb			400	pF	3

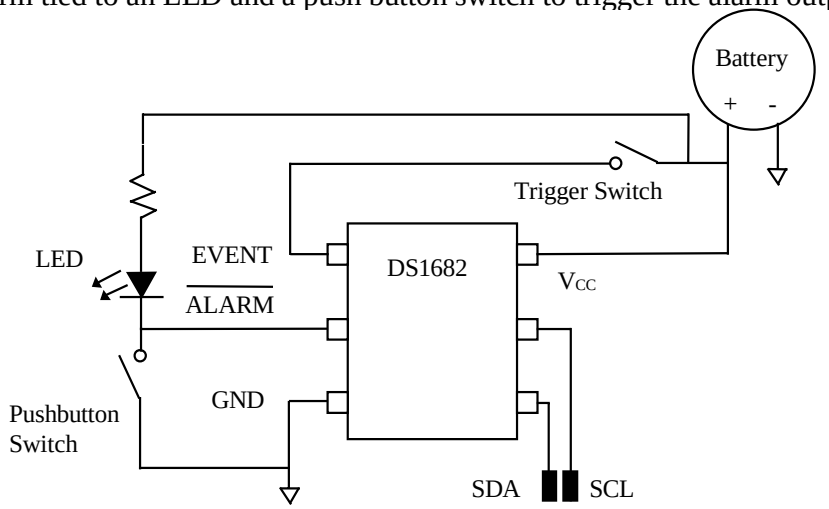
TIMING DIAGRAM: DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 2



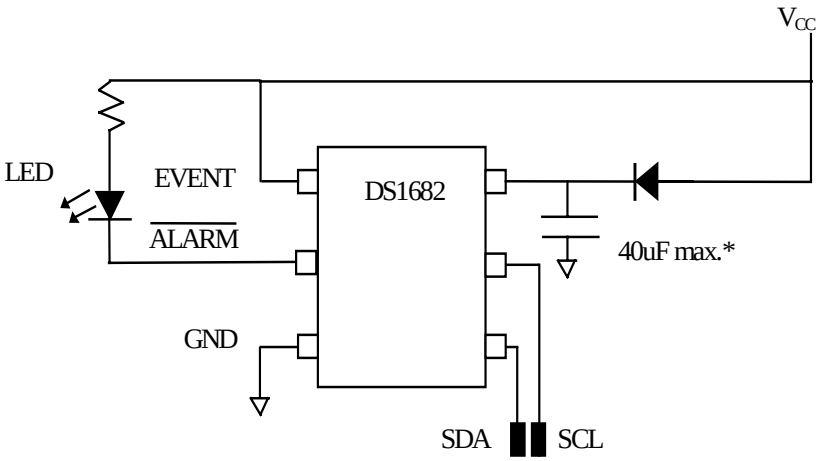
NOTES:

1. All voltages are referenced to ground,
2. After this period, the first clock pulse is generated.
3. Cb - total capacitance of one bus line in pF.

The DS1682 measuring total run time and operating off of a battery with the alarm tied to an LED and a push button switch to trigger the alarm output.



DS1682 in a Total Time of Use application with AC Power that may be removed at the same time as the end of the event.



* The V_{CC} holding capacitor value of 40 uF is calculated for the worst case conditions of 100 uA EEPROM write current, 200 ms of EEPROM write time, and V_{CC} and temperature extremes. In many applications, this value will be able to be reduced.