STEPPER MOTOR CONTROLLER IC

FEATURES

- **Pulse Width Modulation (PWM) Microstepping Motor Driver**
  - **Built-In 1/256-Step Microstepping Indexer**
  - **Drives External N-Channel MOSFETs**
  - **Optional STEP/DIR Pins**
  - **Optional PWM Control Interface for DC Motors**
- **Flexible Decay Modes, Including Automatic Mixed Decay Mode**
- **Stall Detection With Optional BEMF Output**
- **Highly cConfigurable Va SPI Serial Interface**
- **Internal Reference and Torque DAC**
- **8-V to 52-V Operating Supply Voltage Range**
- **Scalable Output Current**
- **Thermally Enhanced Surface Mount Package**
- **5-V Regulator Capable of 10-mA Load**
- **Protection and Diagnostic Features**
  - **Overcurrent Protection (OCP)**
  - **Overtemperature Shutdown (OTS)**
  - **Undervoltage Lockout (UVLO)**
  - **Individual Fault Condition Indication Bits**
  - **Fault Condition Indication Pin**

APPLICATIONS

- **Office Automation Machines**
- **Factory Automation**
- **Textile Machines**
- **Robotics**

DESCRIPTION

The DRV8711 is a stepper motor controller that uses external N-channel MOSFETs to drive a bipolar stepper motor or two brushed DC motors. A microstepping indexer is integrated, which is capable of step modes from full step to 1/256-step.

An ultra-smooth motion profile can be achieved using adaptive blanking time and various current decay modes, including an auto-mixed decay mode. Motor stall is reported with an optional back-EMF output.

A simple step/direction or PWM interface allows easy interfacing to controller circuits. A SPI serial interface is used to program the device operation. Output current (torque), step mode, decay mode, and stall detection functions are all programmable via a SPI serial interface.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature. Fault conditions are indicated via a FAULTn pin, and each fault condition is reported via a dedicated bit through SPI.

The DRV8811 is packaged in a PowerPAD™ 38-pin HTSSOP package with thermal pad (Eco-friendly: RoHS and no Sb/Br).

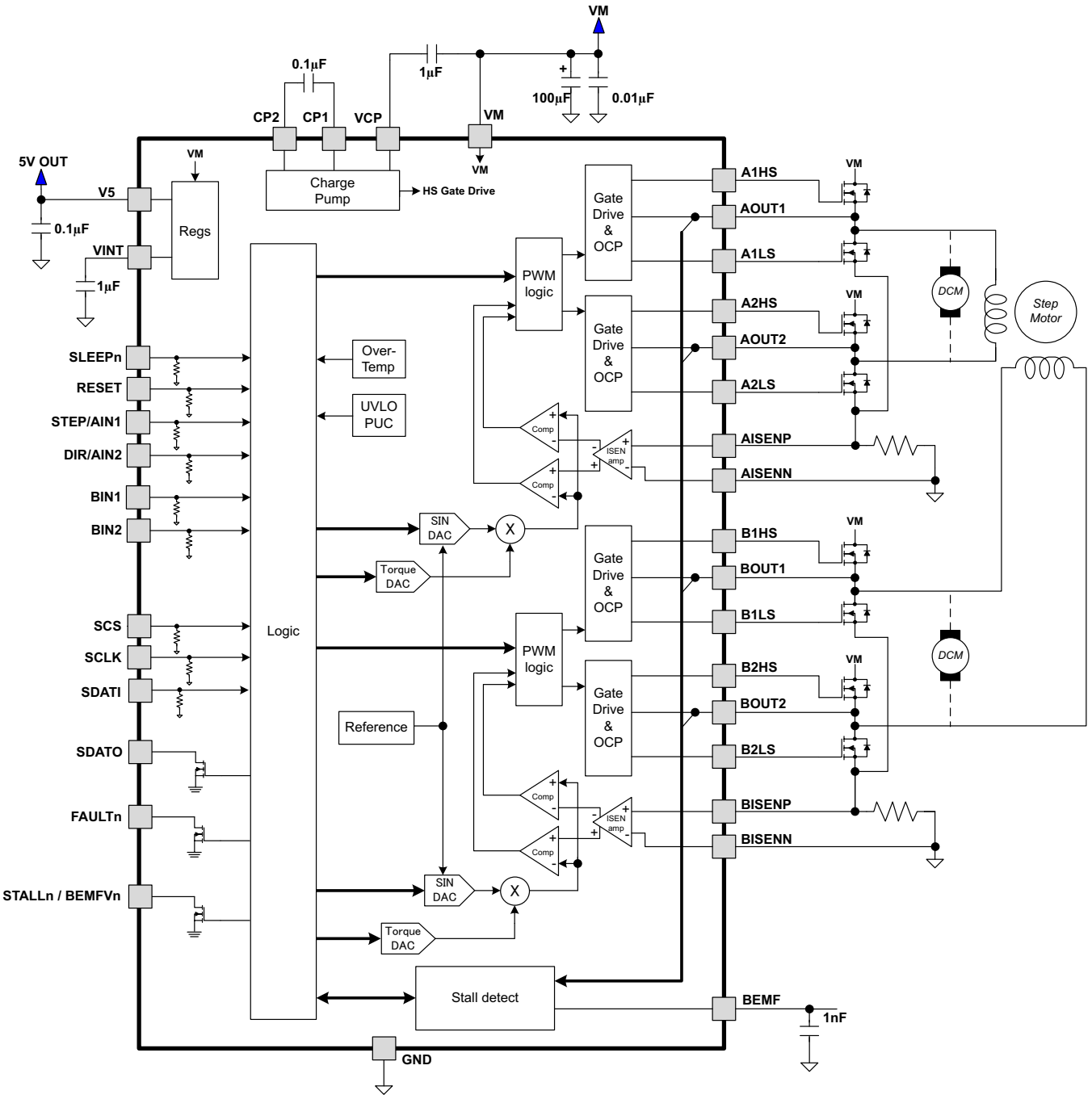
ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (HTSSOP) – PWP	Reel of 2000	DRV8711DCPR	DRV8711
		Tube of 40	DRV8711DCP	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	NO.	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	5, 29, 38, PPAD	-	Device ground	All pins must be connected to ground
VM	4	-	Bridge A power supply	Connect to motor supply voltage. Bypass to GND with a 0.01-µF ceramic capacitor plus a 100-µF electrolytic capacitor.
VINT	7	-	Internal logic supply voltage	Logic supply voltage. Bypass to GND with a 1-µF 6.3-V X7R ceramic capacitor.
V5	6	O	5-V regulator output	5-V linear regulator output. Bypass to GND with a 0.1-µF 10-V X7R ceramic capacitor.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.1-µF X7R capacitor between CP1 and CP2. Voltage rating must be greater than applied VM voltage.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 1-µF 16-V X7R ceramic capacitor to VM
CONTROL				
SLEEPn	8	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
STEP/AIN1	10	I	Step input/Bridge A IN1	Indexer mode: Rising edge causes the indexer to move one step. External PWM mode: controls bridge A OUT1 Internal pulldown.
DIR/AIN2	11	I	Direction input/Bridge A IN2	Indexer mode: Level sets the direction of stepping. External PWM mode: controls bridge A OUT2 Internal pulldown.
BIN1	12	I	Bridge B IN1	Indexer mode: No function External PWM mode: controls bridge B OUT1 Internal pulldown.
BIN2	13	I	Bridge B IN2	Indexer mode: No function External PWM mode: controls bridge B OUT2 Internal pulldown.
RESET	9	I	Reset input	Active-high reset input initializes all internal logic and disables the H-bridge outputs. Internal pulldown.
SERIAL INTERFACE				
SCS	16	I	Serial chip select input	Active high to enable serial data transfer. Internal pulldown.
SCLK	14	I	Serial clock input	Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.
SDATI	15	I	Serial data input	Serial data input from controller. Internal pulldown.
SDATO	17	O	Serial data output	Serial data output to controller. Open-drain output requires external pull-up.
STATUS				
STALLn/ BEMFVn	19	OD	Stall/Back EMF valid	Internal stall detect mode: logic low when motor stall detected. External stall detect mode: Active low when valid back EMF measurement is ready. Open-drain output requires external pullup.
FAULTn	18	OD	Fault	Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, PDF, OTS, UVLO
BEMF	20	O	Back EMF	Analog output voltage represents motor back EMF. Place a 1-nF low-leakage capacitor to ground on this pin.
OUTPUTS				
A1HS	36	O	Bridge A out 1 HS gate	Connect to gate of HS FET for bridge A out 1
AOUT1	37	I	Bridge A output 1	Connect to output node of external FETs of bridge A out 1
A1LS	35	O	Bridge A out 1 LS gate	Connect to gate of LS FET for bridge A out 1
A2HS	31	O	Bridge A out 2 HS gate	Connect to gate of HS FET for bridge A out 2
AOUT2	30	I	Bridge A output 2	Connect to output node of external FETs of bridge A out 2
A2LS	32	O	Bridge A out 2 LS gate	Connect to gate of LS FET for bridge A out 2
AISENP	34	I	Bridge A Isense + in	Connect to current sense resistor for bridge A
AISENN	33	I	Bridge A Isense - in	Connect to ground at current sense resistor for bridge A
B1HS	27	O	Bridge B out 1 HS gate	Connect to gate of HS FET for bridge B out 1

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

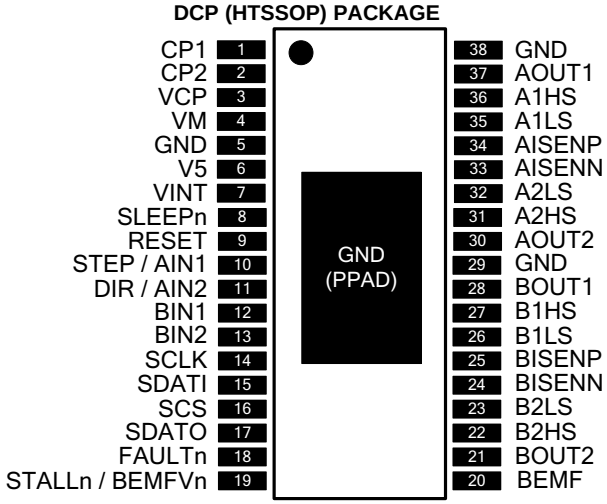
TERMINAL FUNCTIONS (continued)

NAME	NO.	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
BOUT1	28	I	Bridge B output 1	Connect to output node of external FETs of bridge B out 1
B1LS	26	O	Bridge B out 1 LS gate	Connect to gate of LS FET for bridge B out 1
B2HS	22	O	Bridge B out 2 HS gate	Connect to gate of HS FET for bridge B out 2
BOUT2	21	I	Bridge B output 2	Connect to output node of external FETs of bridge B out 2
B2LS	23	O	Bridge B out 2 LS gate	Connect to gate of LS FET for bridge B out 2
BISENP	25	I	Bridge B Isense + in	Connect to current sense resistor for bridge B
BISENN	24	I	Bridge B Isense - in	Connect to ground at current sense resistor for bridge B

CRITICAL COMPONENTS

PIN	NAME	COMPONENT
4	VM	100-µF electrolytic rated for VM voltage to GND 0.01-µF ceramic rated for VM voltage to GND
3	VCP	1-µF ceramic X7R rated 16 V to VCP
1, 2	CP1, CP2	0.1-µF rated for VM + 12 V between these pins
6	V5	0.1-µF ceramic X7R rated 6.3 V to GND
7	VINT	1-µF ceramic X7R rated 6.3 V to GND
17	SDATO	Requires external pullup to logic supply
18	FAULTn	Requires external pullup to logic supply
19	STALLn/BEMFVn	Requires external pullup to logic supply
20	BEMF	1-nF low-leakage capacitor to GND

DCP (HTSSOP) PACKAGE



ABSOLUTE MAXIMUM RATINGS(1) (2) (3)

over operating free-air temperature range (unless otherwise noted)

	DRV8711	UNIT
Power supply voltage range	-0.6 to 60	V
Charge pump voltage range (CP1, CP2, VCP)	-0.6 to VM + 12	V
5V regulator voltage (V5)	-0.6 to 5.5	V
Internal regulator voltage (VINT)	-0.6 to 2.0	V
Digital pin voltage range (SLEEPn, RESET, STEP/AIN1, DIR/AIN2, BIN1, BIN2, SCS, SCLK, SDATI, SDATO, FAULTn, STALLn/BEMFVn)	-0.6 to 5.5	V
High-side gate drive pin voltage range (A1HS, A2HS, B1HS, B2HS)	-0.6 to VM + 12	V
Low-side gate drive pin voltage range (A1LS, A2LS, B1LS, B2LS)	-0.6 to 12	V
Phase node pin voltage range (AOUT1, AOUT2, BOUT1, BOUT2)	-0.6 to VM	V
ISENSEx pin voltage (AISENP, AISENN, BISENP, BISENN)	-0.7 to +0.7	V
BEMF pin voltage range (BEMF)	-0.6 to VM	V
Operating virtual junction temperature range, T_J	-40 to 150	°C
Storage temperature range, T_{stg}	-60 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8711 DCP 38 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	32.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	17.2	
θ_{JB}	Junction-to-board thermal resistance(4)	14.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	14.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range	8		52	V
I_{VS}	V5 external load current	0		10	mA
T_A	Operating ambient temperature range	-40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	V_M operating supply current	V_M = 24 V		17	20	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 24 V, SLEEPn = 0		65	98	µA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		7.1	8	V
		V_M falling		6.3		
Internal Linear Regulators						
V_5	V5 output voltage	$V_M \geq$ 12 V, I_{OUT} = 1 mA - 10 mA	4.8	5	5.2	V
V_{INT}	VINT voltage	No external load – reference only	1.7	1.8	1.9	V
Logic-Level Inputs						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		1.5			V
V_{HYS}	Input hysteresis voltage			300		mV
I_{IL}	Input low current	V_{IN} = 0 V	-5		5	µA
I_{IH}	Input high current	V_{IN} = 5 V	30	50	70	µA
SDATAO, STALLn, FAULTn OUTPUTS (Open-Drain Outputs)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
MOSFET Drivers						
V_{OUTH}	High-side gate drive output voltage	V_M = 24 V, I_O = 100 µA		VM+10		V
V_{OUTL}	Low-side gate drive output voltage	V_M = 24 V, I_O = 100 µA		10		V
t_{DEAD}	Output dead time digital delay (dead time is enforced in analog circuits)	DTIME = 00		400		ns
		DTIME = 01		450		
		DTIME = 10		650		
		DTIME = 11		850		
I_{OUTH}	Peak output current gate drive (source)	IDRIVEP = 00		50		mA
		IDRIVEP = 01		100		
		IDRIVEP = 10		150		
		IDRIVEP = 11		200		
I_{OUTI}	Peak output current gate drive (sink)	IDRIVEN = 00		100		mA
		IDRIVEN = 01		150		
		IDRIVEN = 10		200		
		IDRIVEN = 11		400		
t_{DRIVE}	Peak current drive time (source)	TDRIVEP = 00		250		ns
		TDRIVEP = 01		500		
		TDRIVEP = 10		1000		
		TDRIVEP = 11		2000		
t_{DRIVE}	Peak current drive time (sink)	TDRIVEN = 00		250		ns
		TDRIVEN = 01		500		
		TDRIVEN = 10		1000		
		TDRIVEN = 11		2000		
Motor Driver						
t_{OFF}	PWM off time adjustment range	Set by TOFF register	0.5		128	µs
t_{BLANK}	Current sense blanking time	Set by TBLANK register	0.5		5.12	µs

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

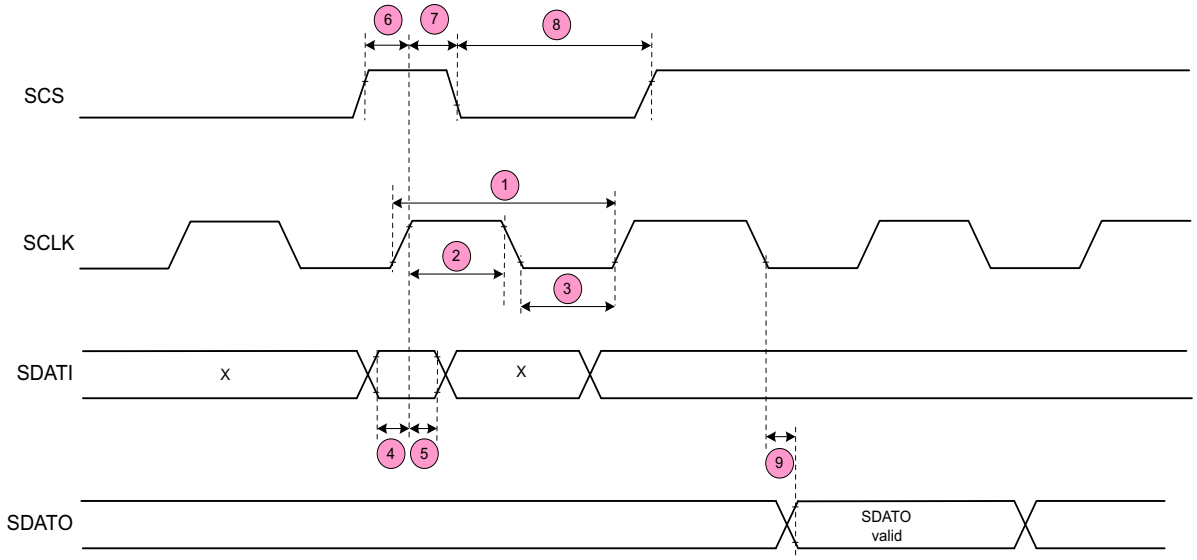
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Protection Circuits						
V_{OCP}	Overcurrent protection trip level (Voltage drop across external FET)	OCPTH = 00	160	250	320	mV
		OCPTH = 01	380	500	580	
		OCPTH = 10	620	750	850	
		OCPTH = 11	840	1000	1200	
t_{TSD}	Thermal shutdown temperature(1)	Die temperature	150	160	180	°C
t_{HYS}	Thermal shutdown hysteresis			20		°C
Current Sense Amplifiers						
A_V	Gain	ISGAIN = 00		5		V/V
		ISGAIN = 01		10		
		ISGAIN = 10		20		
		ISGAIN = 11		40		
t_{SET}	Settling time (to ±1%)	ISGAIN = 00, ΔVIN = 400 mV		150		ns
		ISGAIN = 01, ΔVIN = 200 mV		300		
		ISGAIN = 10, ΔVIN = 100 mV		600		
		ISGAIN = 11, ΔVIN = 50 mV		1.2		µs
V_{OFS}	Offset voltage	ISGAIN = 00, input shorted			4	mV
V_{IN}	Input differential voltage range		-300		300	mV
Current Control DACs						
	Resolution			256		steps
	Full-scale step response	10% to 90%			5	µs
V_{REF}	Full-scale (reference) voltage		2.50	2.75	3	V

(1) Not tested in production - guaranteed by design.

SPI INTERFACE TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

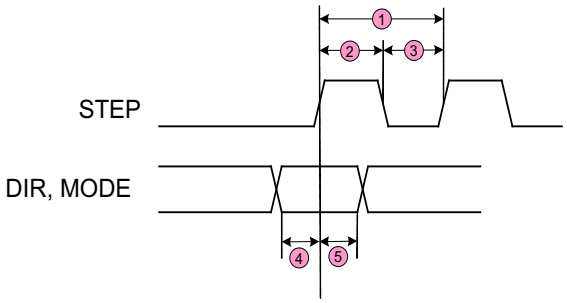
No.	PARAMETER	CONDITIONS	MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	250		ns
2	t_{CLKH}	Clock high time	25		ns
3	t_{CLKL}	Clock low time	25		ns
4	$t_{SU(SDATI)}$	Setup time, SDATI to SCLK	5		ns
5	$t_{H(SDATI)}$	Hold time, SDATI to SCLK	1		ns
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5		ns
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1		ns
8	$t_{L(SCS)}$	Inactive time, SCS (between writes)	100		ns
9	$t_{D(SDATO)}$	Delay time, SCLK to SDATO (during read)		10	ns
	t_{SLEEP}	Wake time (SLEEPn inactive to high-side gate drive enabled)		1	ms
	t_{RESET}	Delay from power-up or RESETn high until serial interface functional		10	µs



INDEXER TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

No.	PARAMETER	CONDITIONS	MIN	MAX	UNIT
1	f_{STEP}	Step frequency		250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9		µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9		µs
4	$t_{SU(STEP)}$	Setup time, command to STEP rising	200		ns
5	$t_{H(STEP)}$	Hold time, command to STEP rising	200		ns



FUNCTIONAL DESCRIPTION

PWM Motor Drivers

The DRV8711 contains two H-bridge motor pre-drivers with current-control PWM circuitry.

More detailed descriptions of the sub-blocks are described in the following sections.

Direct PWM Input Mode

Direct PWM mode is selected by setting the PWMMODE bit in the OFF register. In direct PWM input mode, the AIN1, AIN2, BIN1, and BIN2 directly control the state of the output drivers. This allows for driving up to two brushed DC motors. The logic is shown below:

Table 1. Direct PWM Input Mode Logic

xIN1	xIN2	xOUT1	xOUT2	OPERATION
0	0	Z	Z	Asynchronous Fast Decay
0	1	L	H	Reverse Drive
1	0	H	L	Forward Drive
1	1	L	L	Slow Decay

Note that if mixed or auto mixed decay modes are used, they will apply to every cycle, since current change information is not available.

In direct PWM mode, the current control circuitry is still active. The full-scale VREF is set to 2.75 V. The TORQUE register may be used to scale this value, and the ISEN sense amp gain may still be set using the ISGAIN bits of the CTRL register.

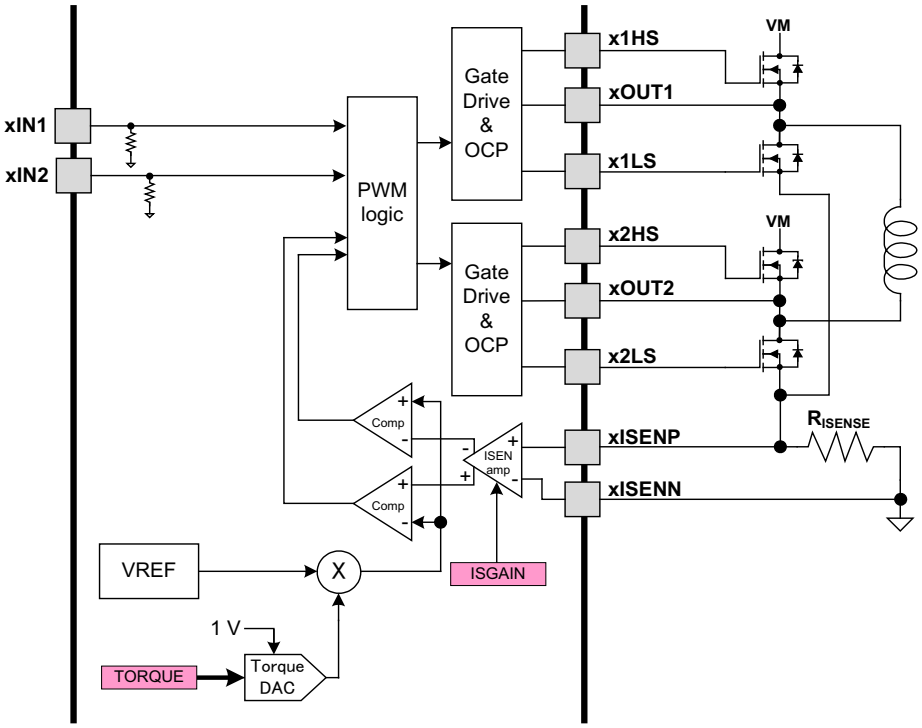


Figure 1. Direct PWM Input Mode

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge disables the current for a fixed period of time, which is programmable between 500 nS and 128 µS by writing to the TOFF bits in the OFF register. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

The chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISENx pins, multiplied by the gain of the current sense amplifier, with a reference voltage. The current sense amplifier is programmable in the CTRL register.

When driving in PWM mode, the chopping current is calculated as follows:

$$I_{CHOP} = \frac{2.75V \bullet TORQUE}{256 \bullet ISGAIN \bullet R_{ISENSE}} \quad (1)$$

Where TORQUE is the setting of the TORQUE bits, and ISGAIN is the programmed gain of the ISENSE amplifiers (5, 10, 20, or 40).

Microstepping Indexer

Built-in indexer logic in the DRV8711 allows a number of different stepping configurations. The MODE bits in the CTRL register are used to configure the stepping format as shown in the table below:

Table 2. Microstepping Indexer Logic

MODE3	MODE2	MODE1	MODE0	STEP MODE
0	0	0	0	Full step (2-phase excitation) with 71% current
0	0	0	1	1/2 step
0	0	1	0	1/4 step
0	0	1	1	1/8 step
0	1	0	0	1/16 step
0	1	0	1	1/32 step
0	1	1	0	1/64 step
0	1	1	1	1/128 step
1	0	0	0	1/256 step

Table 3 shows the relative current and step directions for full-step through 1/8-step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle; BOUT current is the cosine of the electrical angle.

The reset state is 45°. This state is entered at power-up or application of RESETn. This is shown in the table below by cells shaded in yellow.

Table 3. Step Directions

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
	1	1	1	0	100	0
			2	20	98	11.325
		2	3	38	92	22.5
			4	56	83	33.75
1	2	3	5	71	71	45 (home state)
			6	83	56	56.25
		4	7	92	38	67.5
			8	98	20	78.75
	3	5	9	100	0	90
			10	98	-20	101.25
		6	11	92	-38	112.5
			12	83	-56	123.75
2	4	7	13	71	-71	135
			14	56	-83	146.25
		8	15	38	-92	157.5
			16	20	-98	168.75
	5	9	17	0	-100	180
			18	-20	-98	191.25
		10	19	-38	-92	202.5
			20	-56	-83	213.75
3	6	11	21	-71	-71	225
			22	-83	-56	236.25
		12	23	-92	-38	247.5
			24	-98	-20	258.75
	7	13	25	-100	0	270
			26	-98	20	281.25
		14	27	-92	38	292.5
			28	-83	56	303.75
4	8	15	29	-71	71	315
			30	-56	83	326.25
		16	31	-38	92	337.5
			32	-20	98	348.75

At each rising edge of the STEP input, or each time a '1' is written to the RSTEP bit in the CTRL register, the indexer travels to the next state in the table. The direction is shown with the DIR pin high and the RDIR bit in the CTRL register set to '0', or the DIR pin low and the RDIR bit set to '1'. If the DIR pin is low with the RDIR bit '0', or the DIR pin is high with the RDIR bit '1', the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that if the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODE setting at the rising edge of STEP.

Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge disables the current for a fixed period of time, which is programmable between 500 nS and 128 µS by writing to the TOFF bits in the OFF register. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISENx pins, multiplied by the gain of the current sense amplifier, with a reference voltage. The current sense amplifier is programmable in the CTRL register.

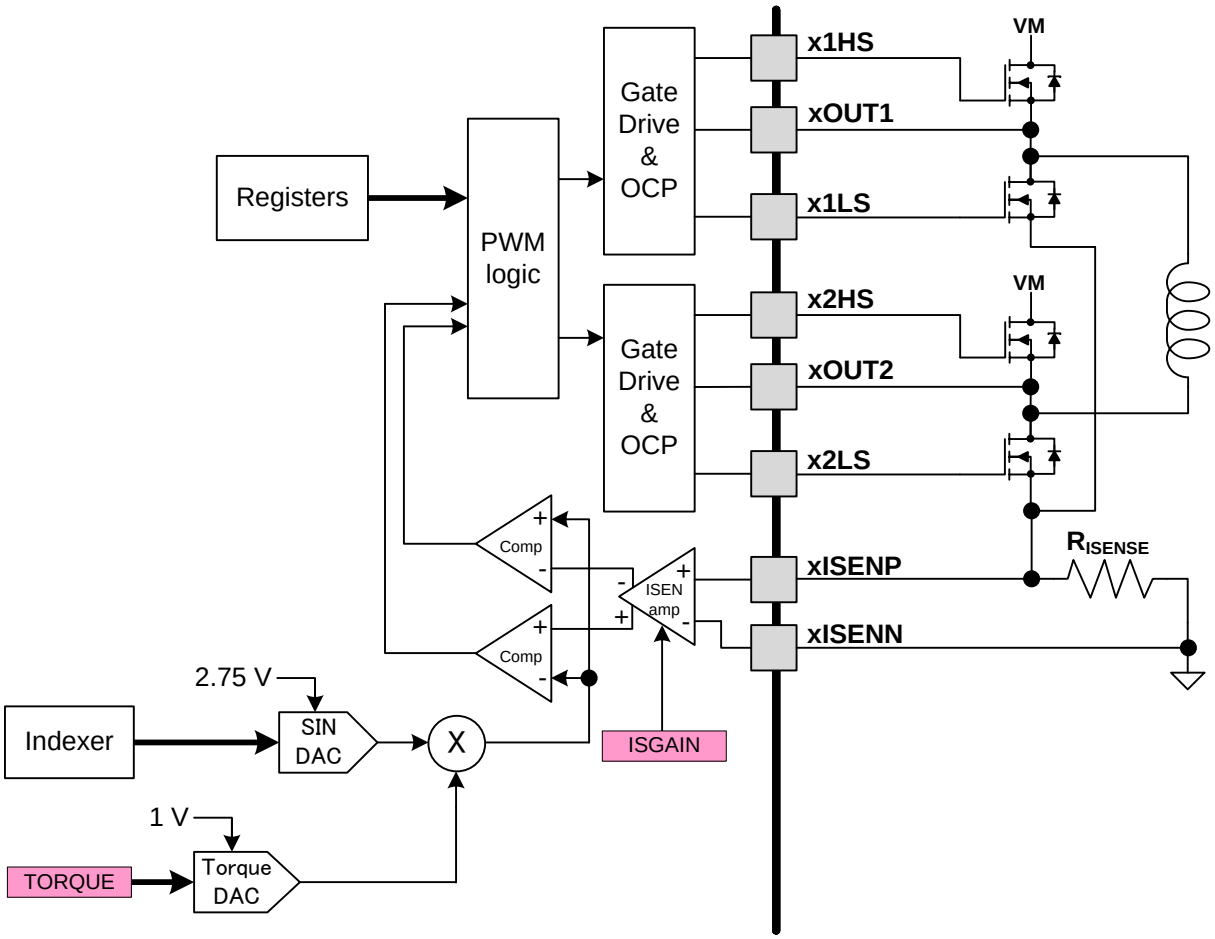


Figure 2. PWM Chopping Current

To generate the reference voltage for the current chopping comparator, the output of a sine lookup table is multiplied by the value of the bits in the TORQUE register. This result is applied to a sine-weighted DAC, whose full-scale output voltage is 2.75 V.

Therefore, the full-scale (100%) chopping current is calculated as follows:

$$I_{FS} = \frac{2.75V \bullet TORQUE}{256 \bullet ISGAIN \bullet R_{ISENSE}} \quad (2)$$

Where TORQUE is the setting of the TORQUE bits, and ISGAIN is the programmed gain of the ISENSE amplifiers (5, 10, 20, or 40).

Example:

If a 0.1-Ω sense resistor is used, ISGAIN is set to 0 (gain of 5), and TORQUE is set to 255, the full-scale (100%) chopping current will be (2.75V * 255) / (256 * 5 * 0.1Ω) = 5.5A.

Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 3, Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in Figure 3, Item 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 3, Item 3.

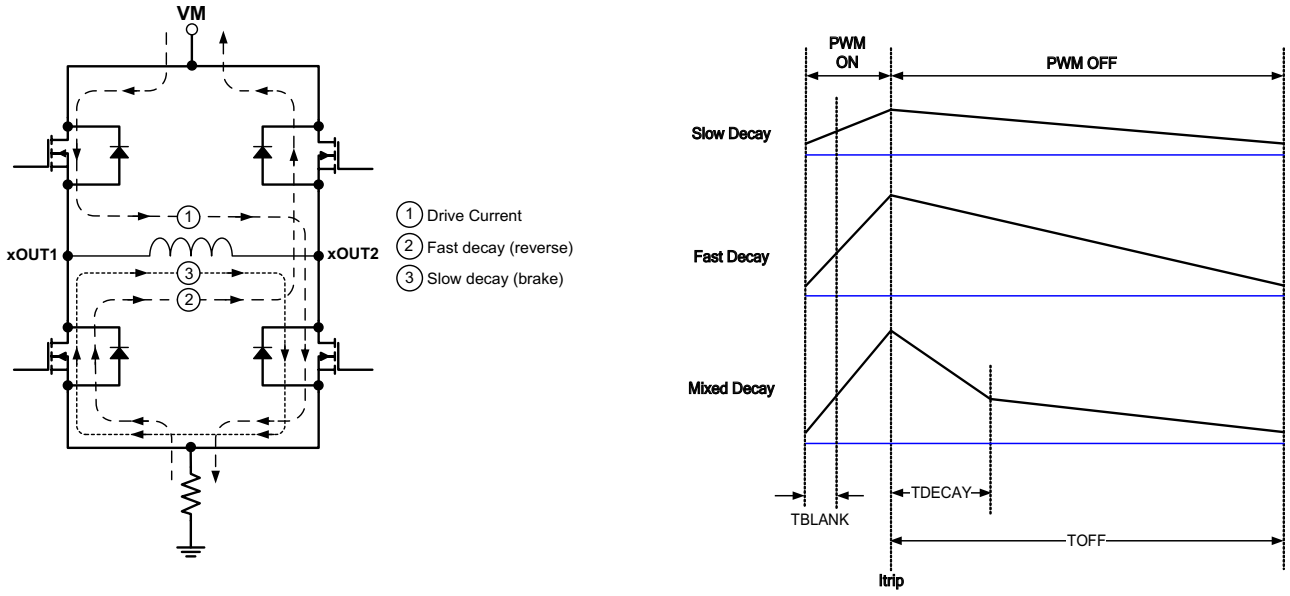


Figure 3. Decay Modes

The DRV8711 supports fast decay and slow decay modes in both indexer and direct PWM modes. In addition, in indexer mode only, it supports fixed mixed decay and auto mixed decay modes. Decay mode is selected by the DECMOD bits in the DECAY register.

Mixed decay mode begins as fast decay, but after a programmable period of time (set by the TDECAY bits in the DECAY register) switches to slow decay mode for the remainder of the fixed off time. Even if mixed decay is selected, if the current is increasing or remaining the same (per the step table), then slow decay is used.

Auto mixed decay mode samples the current level at the end of the blanking time, and if the current is above the Itrip threshold, immediately changes the H-bridge to fast decay. During fast decay, the (negative) current is monitored, and when it falls below the Itrip threshold (and another blanking time has passed), the bridge is switched to slow decay. Once the fixed off time expires, a new cycle is started.

If the bridge is turned on and at the end of TBLANK the current is below the Itrip threshold, the bridge remains on until the current reaches Itrip. Then slow decay is entered for the fixed off time, and a new cycle begins.

Refer to Figure 4 and Figure 5.

The upper waveform shows the behavior if I < Itrip at the end of tBLANK. Note that (at slow motor speeds, where back EMF is not significant), the current increase during the ON phase is the same magnitude as the current decrease in fast decay, since both times are controlled by tBLANK, and the rate of change is the same (full VM is applied to the load inductance in both cases, but in opposite directions). In this case, the current will gradually be driven down until the peak current is just hitting Itrip at the end of the blanking time, after which some cycles will be slow decay, and some will be mixed decay.

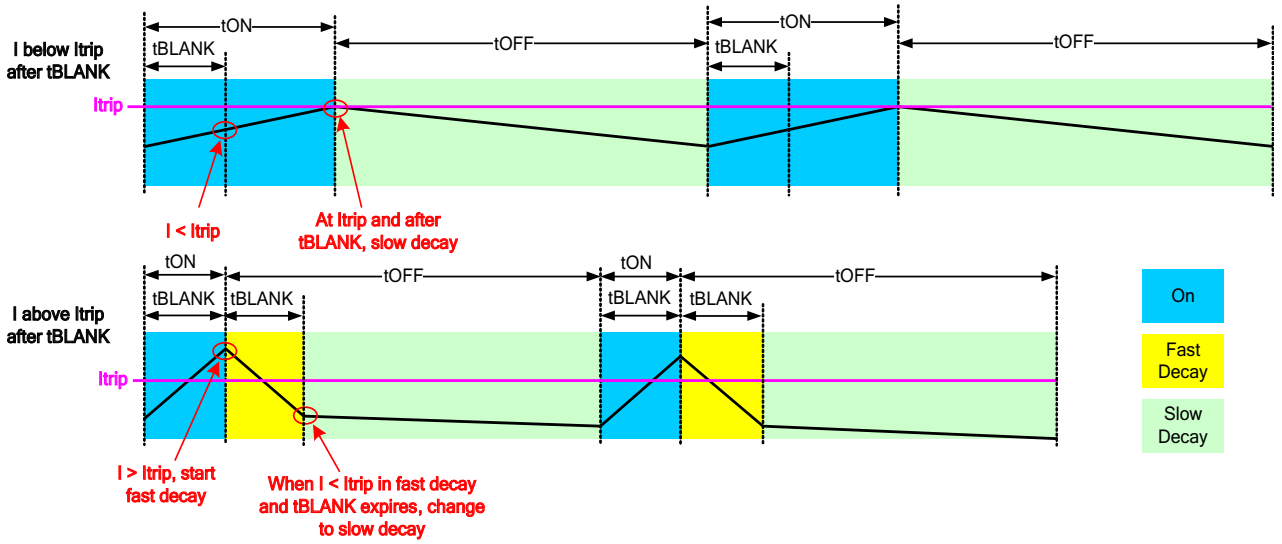


Figure 4. I < Itrip at the End of tBLANK

If the Itrip level changes during a PWM cycle (in response to a step command to the indexer), the current cycle is immediately terminated, and a new cycle is begun. Refer to the drawing below.

If the Itrip level has increased, the H-bridge will immediately turn on; if the Itrip level has decreased, fast decay mode is begun immediately. The top waveform shows what happens when the Itrip threshold decreases during a PWM cycle. The lower Itrip level results in the current being above the Itrip threshold at the end of tBLANK on the following cycle. Fast decay is entered until the current is driven below the Itrip threshold.

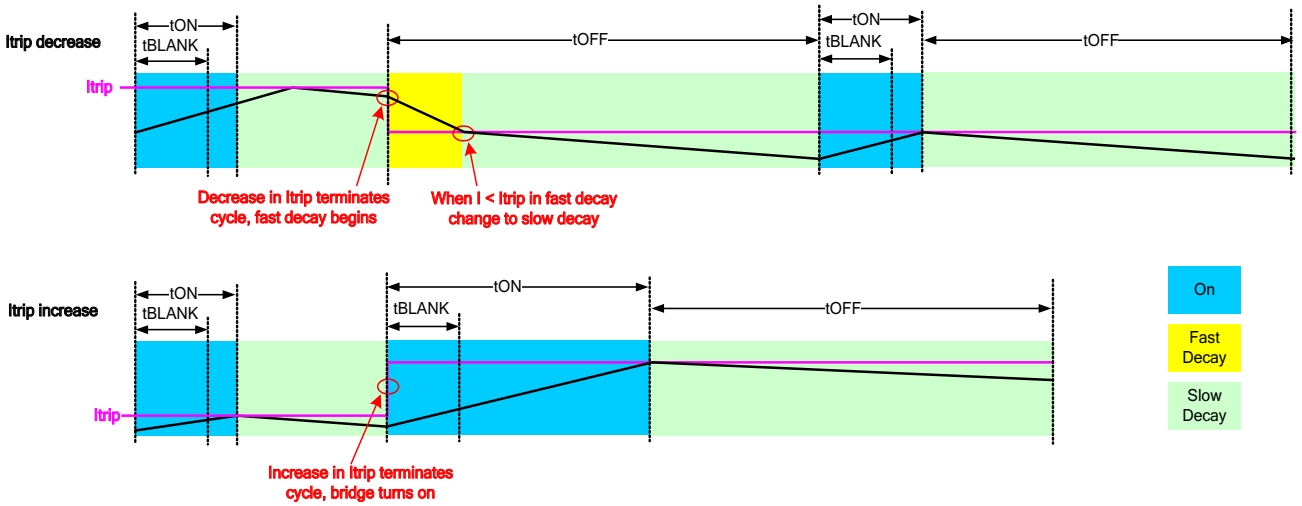


Figure 5. Itrip Level Changing During a PWM Cycle

Blanking Time

After the current is enabled in an H-bridge, the voltage on the ISEN pin is ignored for a period of time before enabling the current sense circuitry. This blanking time is adjustable from 1 µS to 5.12 µs, in 20 ns increments, by setting the TBLANK bits in the BLANK register. Note that the blanking time also sets the minimum on time of the PWM.

The same blanking time is applied to the fast decay period in auto decay mode. The PWM will ignore any transitions on Itrip after entering fast decay mode, until the blanking time has expired.

To provide better current control at very low current steps, an adaptive blanking time mode can be enabled by setting the ABT bit in the BLANK register. If ABT is set, at current levels below 30% of full scale current (as determined by the step table), the blanking time (so also the minimum on time) is cut in half, to 50% of the value programmed by the TBLANK bits.

For higher degrees of micro-stepping it is recommended to enable ABT bit for better current regulation.

Pre-Drivers

An internal charge pump circuit and pre-drivers inside the DRV8711 directly drive N-channel MOSFETs, which drive the motor current.

The peak drive current of the pre-drivers is adjustable by setting the bits in the DRIVE register. Peak source currents may be set to 50 mA, 100 mA, 150 mA, or 200 mA. The peak sink current is approximately 2x the peak source current. Adjusting the peak current will change the output slew rate, which also depends on the FET input capacitance and gate charge.

When changing the state of the output, the peak current is applied for a short period of time (tDRIVE), to charge the gate capacitance. After this time, a weak current source is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to fully charge and discharge the gate during the time when driven at full current, or excessive power will be dissipated in the FET.

During high-side turn-on, the low-side gate is pulled low. This prevents the gate-source capacitance of the low-side FET from inducing turn-on.

The pre-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. Additional dead time is added with digital delays. This delay can be selected by setting the DTIME bits in the CTRL register.

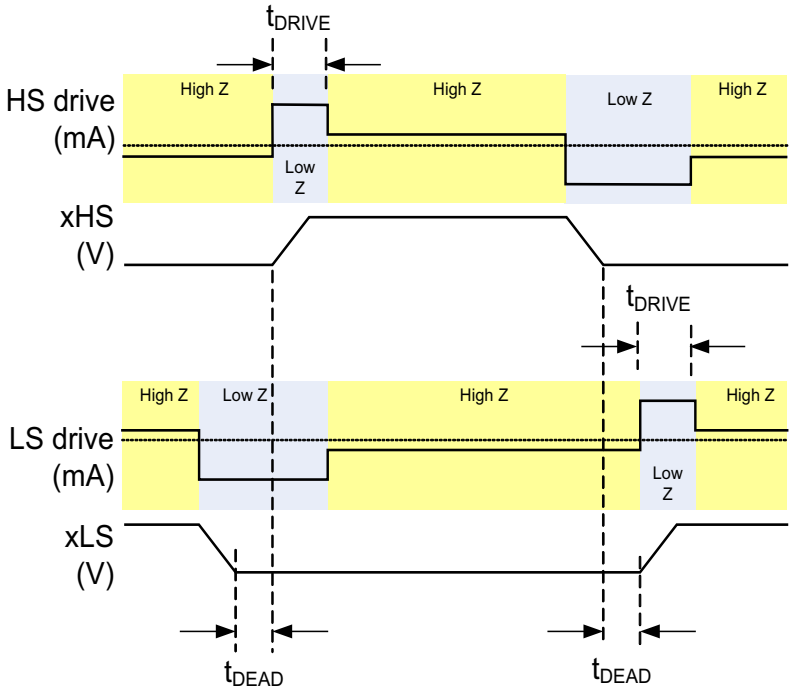


Figure 6. Pre-Drivers

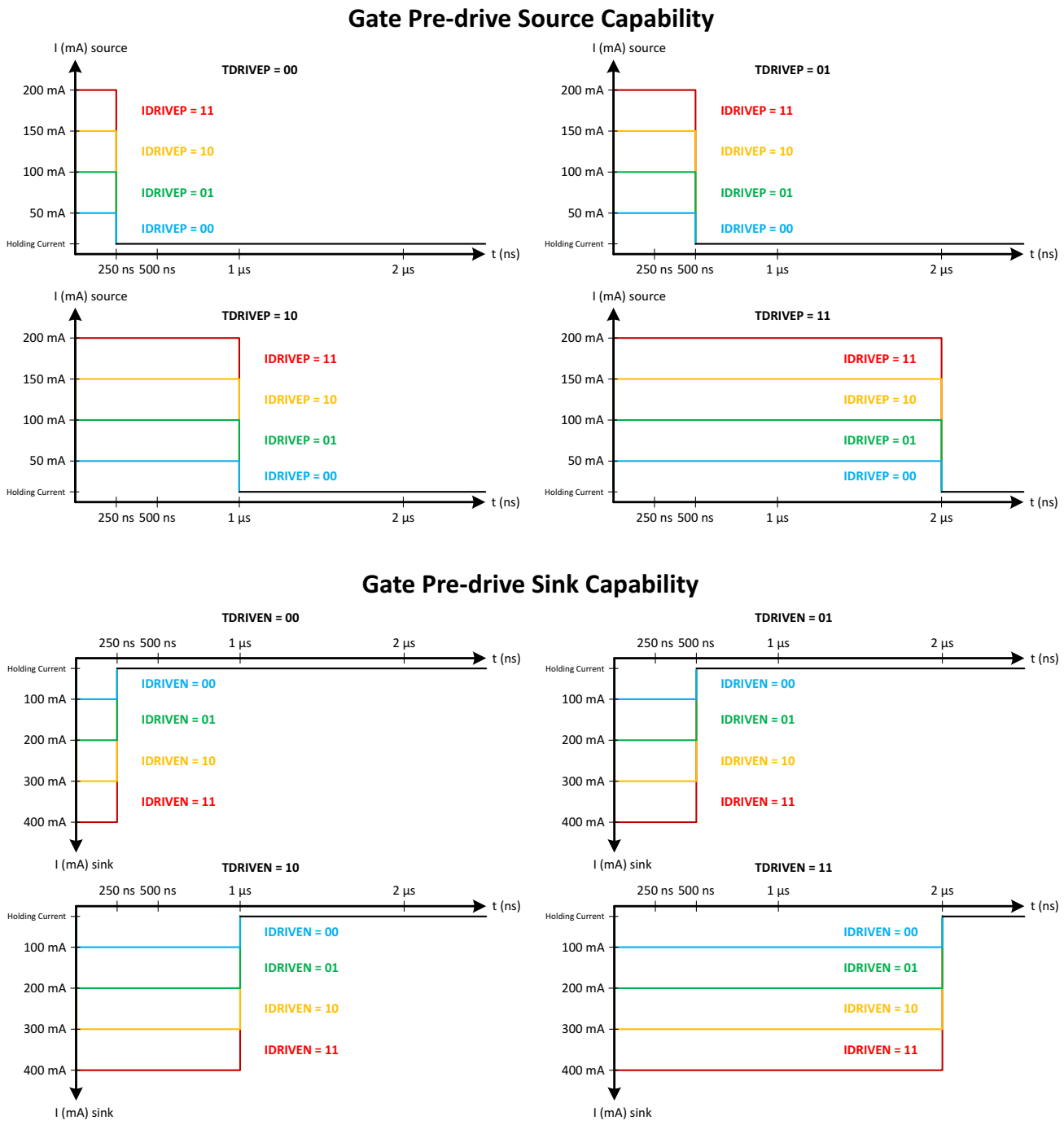


Figure 7. Gate Pre-Drive Source/Sink Capability

Configuring Pre-drivers

IDRIVE and TDRIVE are selected based on the size of external FETs used. These registers need to be configured so that the FET gates are charged completely during TDRIVE. If IDRIVE and TDRIVE are chosen to be too low for a given FET, then the FET may not turn on completely. It is suggested to adjust these values in-system with the required external FETs and stepper motor in order to determine the best possible setting for any application.

Note that TDRIVE will not increase the PWM time or change the PWM chopping frequency.

In a system with capacitor charge Q and desired rise time RT, IDRIVE and TDRIVE can be initially selected based on:

IDRIVE > Q / RT

TDRIVE > 2 x RT

For best results, select the smallest IDRIVE and TDRIVE that meet the above conditions.

Example:

If the gate charge is 15 nC and the desired rise time is 400 ns, then select:

IDRIVEP = 50 mA, IDRIVEN = 100 mA

TDRIVEP = TDRIVEN = 1 µs

External FET Selection

In a typical setup, the DRV8711 can support external FETs over 50 nC each. However, this capacity can be lower or higher based on the device operation. For an accurate calculation of FET driving capacity, use the following equation.

$$Q < \frac{20mA \bullet (2 \bullet DTIME + TBLANK + TOFF)}{4} \quad (3)$$

Example:

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0 (500 ns), then the DRV8711 will support Q < 11.5 nC FETs (please note that this is an absolute worst-case scenario with a PWM frequency ~ 430 kHz).

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x14 (10 µs), then the DRV8711 will support Q < 59 nC FETs (PWM frequency ~ 85 kHz).

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x60 (48 µs), then the DRV8711 will support Q < 249 nC FETs (PWM frequency ~ 20 kHz).

Stall Detection

The DRV8711 implements a back EMF monitoring scheme that is capable of detecting a stall during stepper motor motion. This stall detection is intended to be used to get an indication when a motor is run into a mechanical stop, or when an increased torque load on the motor causes it to stall.

To determine that a stall has occurred, a drop in motor back EMF is detected. The DRV8711 supports two methods of this detection: an automatic internal stall detection circuit, or the ability to use an external microcontroller to monitor back EMF.

During a zero-current step, one side of the H-bridge is placed in a high impedance state, and the opposite low-side FET is turned on for a brief duration defined by TORQUE register SMPLTH bit [10:8]. This allows the current to decay quickly through the low-side FET and the opposite body diode. Which side of the bridge is tri-state and which one is driven low depends on the current direction on the previous step. The bridge with the high side that has been actively PWMed (at the beginning of the PWM cycle during blank time) prior to entering the zero-current step will be held low and the opposite side will be tri-stated.

Back EMF is sampled on the tri-stated output pin at the end of SMPLTH time (TORQUE register bit [10:8]). The back EMF from the selected pin is divided by 4, 8, 16, or 32, depending on the setting of the VDIV bits in the STALL register. The voltage is buffered and held on an external capacitor placed on the BEMF pin. The signal on the BEMF output pin can be further processed by a microcontroller to implement more advanced control and stall detection algorithms.

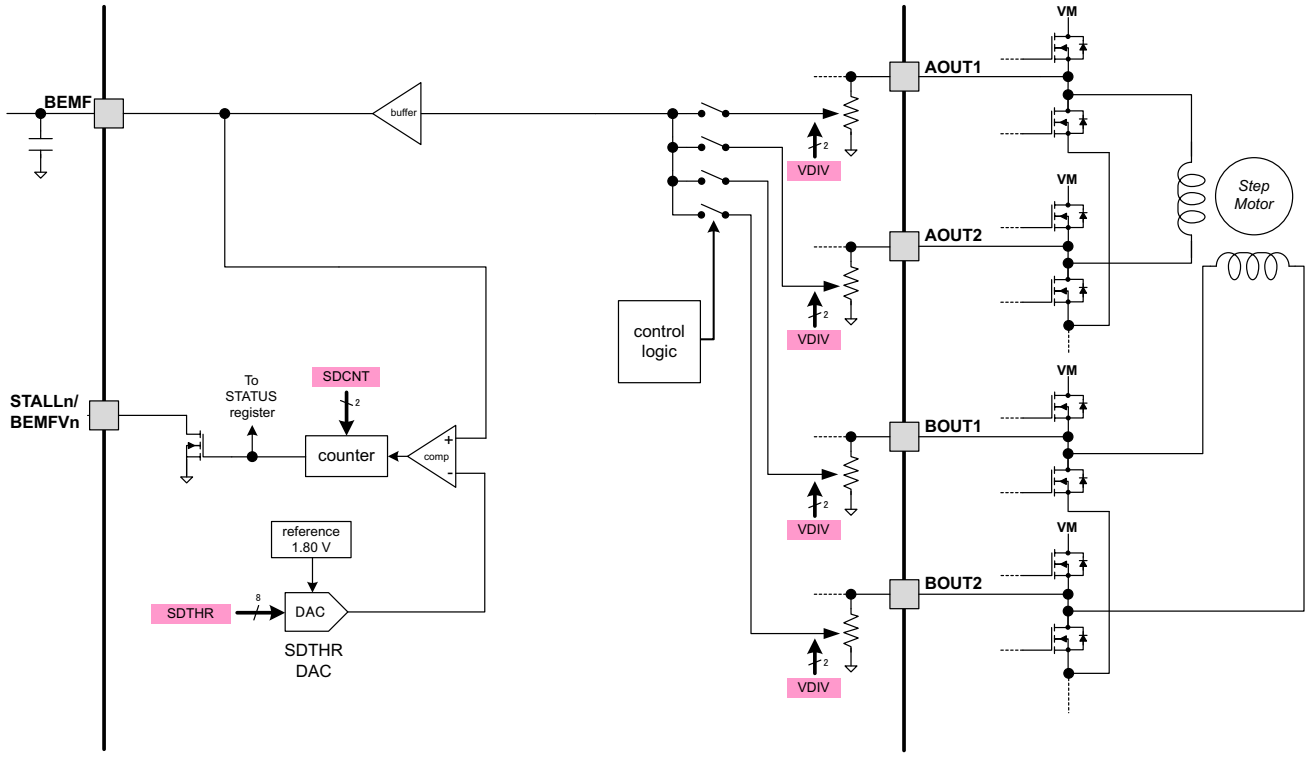


Figure 8. Stall Detection

Internal Stall Detection

To use internal stall detection, the EXSTALL bit in the CTRL register is set to '0'. In this mode, the STALLn/BEMFVn output pin is used to signal a valid stall condition.

Step time, or rate at which step input is applied to DRV8711, has to be greater than SMPLTH time for back EMF sampling.

Using internal stall detection, a stall is detected when the sampled back EMF drops below the value set by the SDTHR bits in the STALL register. A programmable counter circuit allows the assertion of the STALLn output to be delayed until the back EMF has been sampled below the SDTHR value for more than one zero-current step. The counter is programmed by the SDCNT bits in the STALL register, and provides selections of 1, 2, 4, or 8 steps.

When the stall is detected (at the end of a SMPLTH interval), the STALLn/BEMFVn pin is driven active low, and the STD bit and the STDLAT bit in the STATUS register are set. The STALLn/BEMFVn pin will deassert and the STD bit will automatically clear at the next zero-current step if a stall condition is not detected, while the STDLAT bit will remain set until a '0' is written to it. The STDLAT is reset when the STD bit clears after the first zero-cross step that does not detect a stall condition.

This stall detection scheme is only effective when the motor is stalled while running at or above some minimum speed. Since it relies on detecting a drop in motor back EMF, the motor must be rotating with sufficient speed to generate a detectable back EMF. During motor start-up, and at very slow step rates, the stall detection is not reliable.

Since back EMF can only be sampled during a zero-current state, stall detection is not possible in full step mode. During full-step operation, the stall detect circuit is gated off to prevent false signaling of a stall.

The correct setting of the SDTHR bits needs to be determined experimentally. It is dependent on many factors, including the electrical and mechanical characteristics of the load, the peak current setting, and the supply voltage.

External Stall Detection

To use an external microcontroller to manage stall detection, the EXSTALL bit in the CTRL register is set to '1'. In this mode, the STALLn / BEMFVn output pin is used to signal a valid back EMF measurement is ready. In addition, the SDT and SDTLAT bits are also set at this time.

BEMFVn and BEMF are still valid outputs in this mode even if the step time is smaller than SMPLTH time.

When the BEMFVn pin goes active low, it is an indication that a valid back EMF voltage measurement is available. This signal could be used, for example, to trigger an interrupt on a microcontroller. The microcontroller can then sample the voltage present (using an A/D converter) on the BEMF pin.

After sampling the back EMF voltage, the microcontroller writes a '0' to the SDTLAT bit to clear the SDT bit and BEMFVn pin, in preparation for the next back EMF sample. If the SDTLAT bit is not cleared by the microcontroller, it will automatically be cleared in the next zero-current step.

For either internal or external stall detection, at very high motor speeds when the PWM duty cycle approaches 100%, the inductance of the motor and the short duration of each step may cause the time required for current recirculation to exceed the step time. In this case, back EMF will not be correctly sampled, and stall detection cannot function. This condition occurs most at high degrees of micro-stepping, since the zero current step lasts for a shorter duration. It is advisable to run the motor at lower degrees of micro-stepping at higher speeds to allow time for current recirculation if stall detection is needed in this condition.

RESET and SLEEPn Operation

An internal power-up reset circuit monitors the voltage applied to the VM pin. If VM falls below the VM undervoltage lockout voltage, the part is reset, as described below for the case of asserting the RESET pin.

If the RESET pin is asserted, all internal logic including the indexer is reset. All registers are returned to their initial default conditions. The power stage will be disabled, and all inputs, including STEP and the serial interface, are ignored when RESET is active.

On exiting reset state, some time (approximately 1 mS) needs to pass before the part is fully functional.

Applying an active low input to the SLEEPn input pin will place the device into a low power state. In sleep mode, the motor driver circuitry is disabled, the gate drive regulator and charge pump are disabled, and all analog circuitry is placed into a low power state. The digital circuitry in the device still operates, so the device registers can still be accessed via the serial interface.

When SLEEPn is active, the RESET pin does not function. SLEEPn must be exited before RESET will take effect.

When exiting from sleep mode, some time (approximately 1 mS) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize.

Microstepping Drive Current

The following plots are examples of stepper motor current in one of the windings. Since these waveforms are dependent on DRV8711 register settings as well as the external FETs, sense resistor, and stepper motor, they should only be used as a reference.

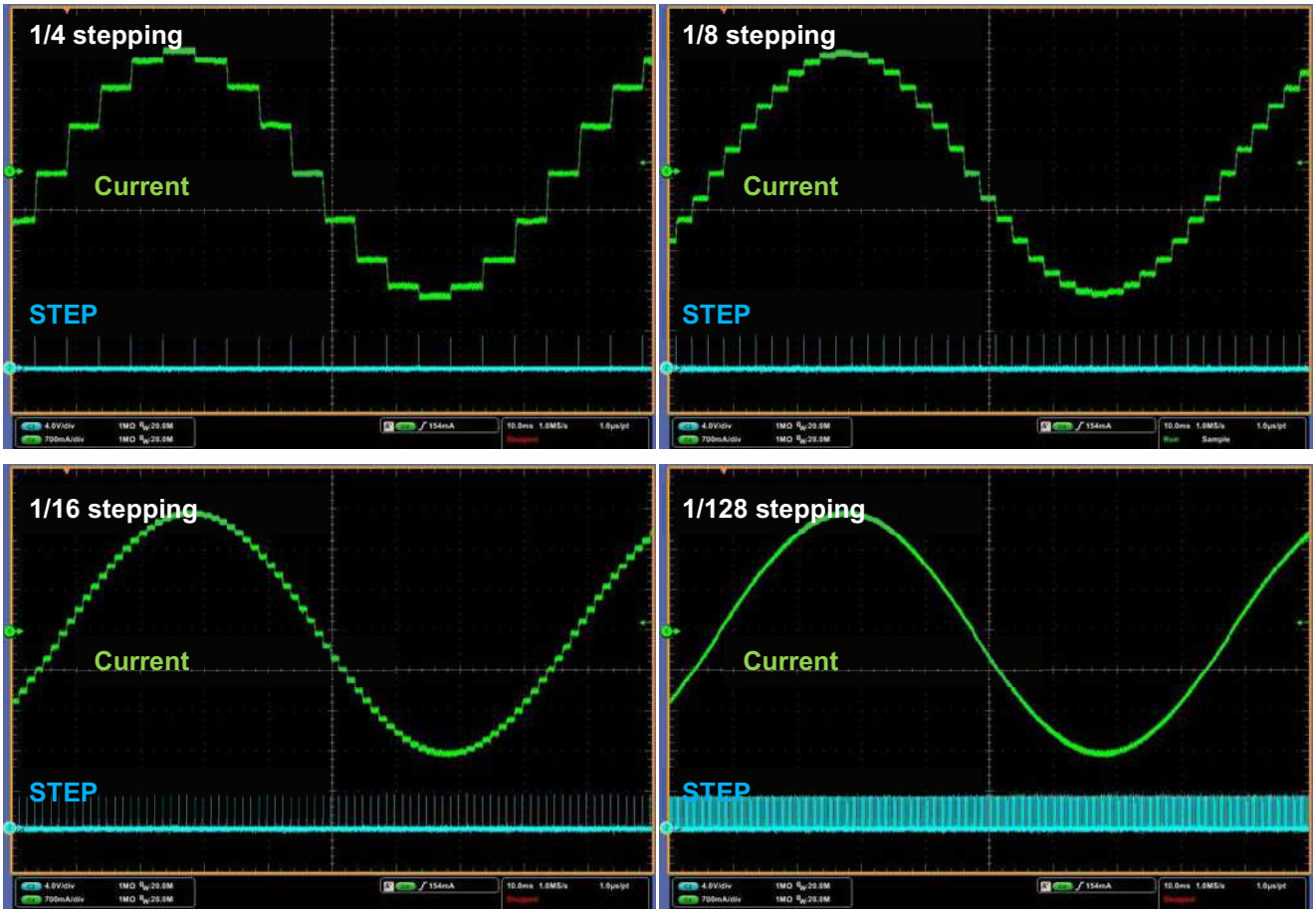


Figure 9. Microstepping Drive Current

Protection Circuits

The DRV8711 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

Overcurrent is sensed by monitoring the voltage drop across the external FETs. If the voltage across a driven FET exceeds the value programmed by the OCPTH bits in the DRIVE register for more than the time period specified by the OCPDEG bits in the DRIVE register, an OCP event is recognized. When operating in direct PWM mode, during an OCP event, the H-bridge experiencing the OCP event is disabled; if operating in indexer mode, both H-bridges will be disabled. In addition, the corresponding xOCP bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge(s) will remain off, and the xOCP bit will remain set, until it is written to 0, or the device is reset.

Pre-Driver Fault

If excessive current is detected on the gate drive outputs (which would be indicative of a failed/shorted output FET or PCB fault), the H-bridge experiencing the fault is disabled, the xPDF bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge will remain off, and the xPDF bit will remain set until it is written to 0, or the device is reset.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled, the OTS bit in the STATUS register will be set, and the FAULTn pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume and the OTS bit will reset. The FAULTn pin will be released after operation has resumed.

Undervoltage Lockout (UVLO)

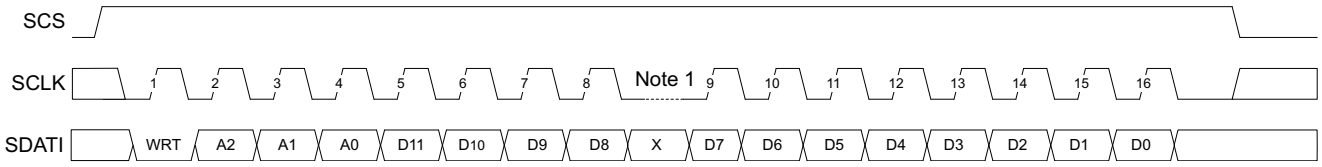
If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the UVLO bit in the STATUS register will be set, and the FAULTn pin will be driven low. Operation will resume and the UVLO bit will reset when VM rises above the UVLO threshold. The FAULTn pin will be released after operat ion has resumed.

During any of these fault conditions, the STEP input pin will be ignored.

Serial Data Format

The serial data consists of a 16-bit serial write, with a read/write bit, 3 address bits and 12 data bits. The three address bits identify one of the registers defined in the register section above.

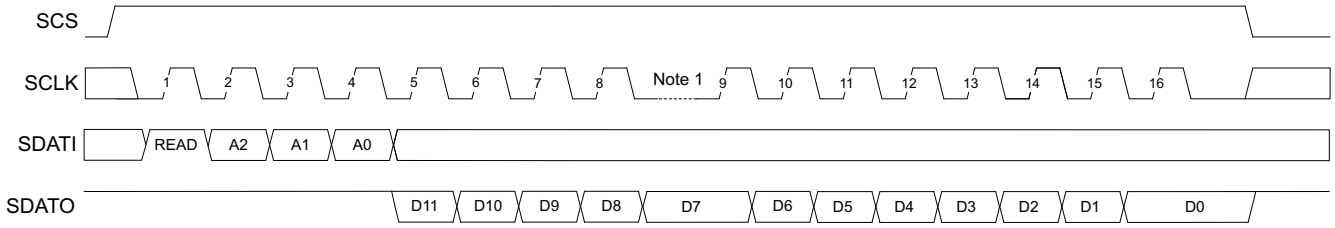
To write to a register, data is shifted in after the address as shown in the timing diagram below:



A. Any amount of time may pass between bits, as long as SCS stays active high. This allows two 8-bit writes to be used.

Figure 10. Write Operation

Data may be read from the registers through the SDATO pin. During a read operation, only the address is used form the SDATI pin; the data bits following are ignored. Reading is enabled by setting the READ bit at the beginning of the access:



(1) Any amount of time may pass between bits, as long as SCS stays active high. This allows two 8-bit writes to be used.

Figure 11. Read Operation

CONTROL REGISTERS

The DRV8711 uses internal registers to control the operation of the motor. The registers are programmed via a serial SPI communications interface. At power-up or reset, the registers will be pre-loaded with default values as shown below.

Following is a map of the DRV8711 registers:

DRV8711 REGISTER MAP

Name	11	10	9	8	7	6	5	4	3	2	1	0		Address Hex
CTRL	DTIME		ISGAIN		EXSTALL	MODE				RSTEP	RDIR	ENBL	RW	00
TORQUE	Reserved	SMPLTH			TORQUE								RW	01
OFF	Reserved			PWMMODE	TOFF								RW	02
BLANK	Reserved			ABT	TBLANK								RW	03
DECAY	Reserved	DECMOD			TDECAY								RW	04
STALL	VDIV		SDCNT		SDTHR								RW	05
DRIVE	IDRIVEP		IDRIVEN		TDRIVEP		TDRIVEN		OCPDEG		OCPTH		RW	06
STATUS	Reserved				STDLAT	STD	UVLO	BPDF	APDF	BOCP	AOCP	OTS	RW	07
Name	11	10	9	8	7	6	5	4	3	2	1	0		Address Hex

Figure 12. DRV8711 Register Map

Individual register contents are defined below.

CTRL Register

Address = 0x00h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	ENBL	1	R/W	0	**0: Disable motor** 1: Enable motor
1	RDIR	1	R/W	0	**0: Direction set by DIR pin** 1: Direction set by inverse of DIR pin
2	RSTEP	1	W	0	0: No action 1: Indexer will advance one step; automatically cleared after write
6-3	MODE	4	R/W	110	0000: Full-step, 71% current 0001: Half step **0010: 1/4 step** 0011: 1/8 step 0100: 1/16 step 0101: 1/32 step 0110: 1/64 step 0111: 1/128 step 1000: 1/256 step 1001 – 1111: Reserved
7	EXSTALL	1	R/W	0	**0: Internal stall detect** 1: External stall detect
9-8	ISGAIN	2	R/W	0	ISENSE amplifier gain set **00: Gain of 5** 01: Gain of 10 10: Gain of 20 11: Gain of 40
11-10	DTIME	2	R/W	11	Dead time set 00: 400 ns dead time 01: 450 ns dead time 10: 650 ns dead time **11: 850 ns dead time**

TORQUE Register

Address = 0x01h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TORQUE	8	R/W	0xFFh	Sets full-scale output current for both H-bridges
10-8	SIMPLTH	3	R/W	1	Back EMF sample threshold 000: 50 µs **001: 100 µs** 010: 200 µs 011: 300 µs 100: 400 µs 101: 600 µs 110: 800 µs 111: 1000 µs
11	Reserved	1	-	-	Reserved

OFF Register

Address = 0x02h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TOFF	8	R/W	0x30h	Sets fixed off time, in increments of 500 ns 0x00h: 500 ns 0xFFh: 128 µs
8	PWMMODE	1	R/W	0	**0: Use internal indexer** 1: Bypass indexer, use xINx inputs to control outputs
11-9	Reserved	3	-	-	Reserved

BLANK Register

Address = 0x03h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 20 ns 0x00h: 1.00 µs … 0x32h: 1.00 µs 0x33h: 1.02 µs … 0xFEh: 5.10 µs 0xFFh: 5.12 µs Also sets minimum on-time of PWM
8	ABT	1	R/W	0	**0: Disable adaptive blanking time** 1: Enable adaptive blanking time
11-9	Reserved	3	-	-	Reserved

DECAY Register

Address = 0x04h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TDECAY	8	R/W	0x10h	Sets mixed decay transition time, in increments of 500 ns
10-8	DECMOD	3	R/W	1	000: Force slow decay at all times **001: Slow decay for increasing current, mixed decay for decreasing current (indexer mode only)** 010: Force fast decay at all times 011: Use mixed decay at all times 100: Slow decay for increasing current, auto mixed decay for decreasing current (indexer mode only) 101: Use auto mixed decay at all times 110 – 111: Reserved
11	Reserved	1	-	-	Reserved

STALL Register

Address = 0x05h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	SDTHR	8	R/W	0x40h	Sets stall detect threshold The correct setting needs to be determined experimentally
10-8	SDCNT	2	R/W	0	**00: STALLn asserted on first step with back EMF below SDTHR** 01: STALLn asserted after 2 steps 10: STALLn asserted after 4 steps 11: STALLn asserted after 8 steps
11	VDIV	2	R/W	0	**00: Back EMF is divided by 32** 01: Back EMF is divided by 16 10: Back EMF is divided by 8 11: Back EMF is divided by 4

DRIVE Register

Address = 0x06h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
1-0	OCPTH	2	R/W	0	OCP threshold **00: 250 mV** 01: 500 mV 10: 750 mV 11: 1000 mV
3-2	OCPDEG	2	R/W	10	OCP deglitch time 00: 1 µs **01: 2 µs** 10: 4 µs 11: 8 µs
5-4	TDRIVEN	2	R/W	1	Low-side gate drive time 00: 250 ns **01: 500 ns** 10: 1 µs 11: 2 µs
7-6	TDRIVEP	2	R/W	1	High-side gate drive time 00: 250 ns **01: 500 ns** 10: 1 µs 11: 2 µs
9-8	IDRIVEN	2	R/W	0	Low-side gate drive peak current **00: 100 mA peak (sink)** 01: 200 mA peak (sink) 10: 300 mA peak (sink) 11: 40 0mA peak (sink)
11-10	IDRIVEP	2	R/W	0	High-side gate drive peak current **00: 50 mA peak (source)** 01: 100 mA peak (source) 10: 150 mA peak (source) 11: 200 mA peak (source)

STATUS Register

Address = 0x07h

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	OTS	1	R	0	0: Normal operation 1: Device has entered overtemperature shutdown OTS bit will clear once temperature has fallen to safe levels
1	AOCP	1	R/W	0	0: Normal operation 1: Channel A overcurrent shutdown Write a '0' to this bit to clear the fault and resume operation
2	BOCP	1	R/W	0	0: Normal operation 1: Channel B overcurrent shutdown Write a '0' to this bit to clear the fault and resume operation
3	UVLO	1	R	0	0: Normal operation 1: Undervoltage lockout UVLO bit will clear after VM has increased over VUVLO
4	APDF	1	R/W	0	0: Normal operation 1: Channel A predriver fault Write a '0' to this bit to clear the fault and resume operation
5	BPDF	1	R/W	0	0: Normal operation 1: Channel B predriver fault Write a '0' to this bit to clear the fault and resume operation
6	STD	1	R	0	0: Normal operation 1: Stall detected
7	STDLAT	1	R/W	0	0: Normal operation 1: Latched stall detect Write a '0' to this bit to clear the fault and resume operation
11-8	Reserved	4	-	-	Reserved

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8711DCP	ACTIVE	HTSSOP	DCP	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8711	Samples
DRV8711DCPR	ACTIVE	HTSSOP	DCP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8711	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

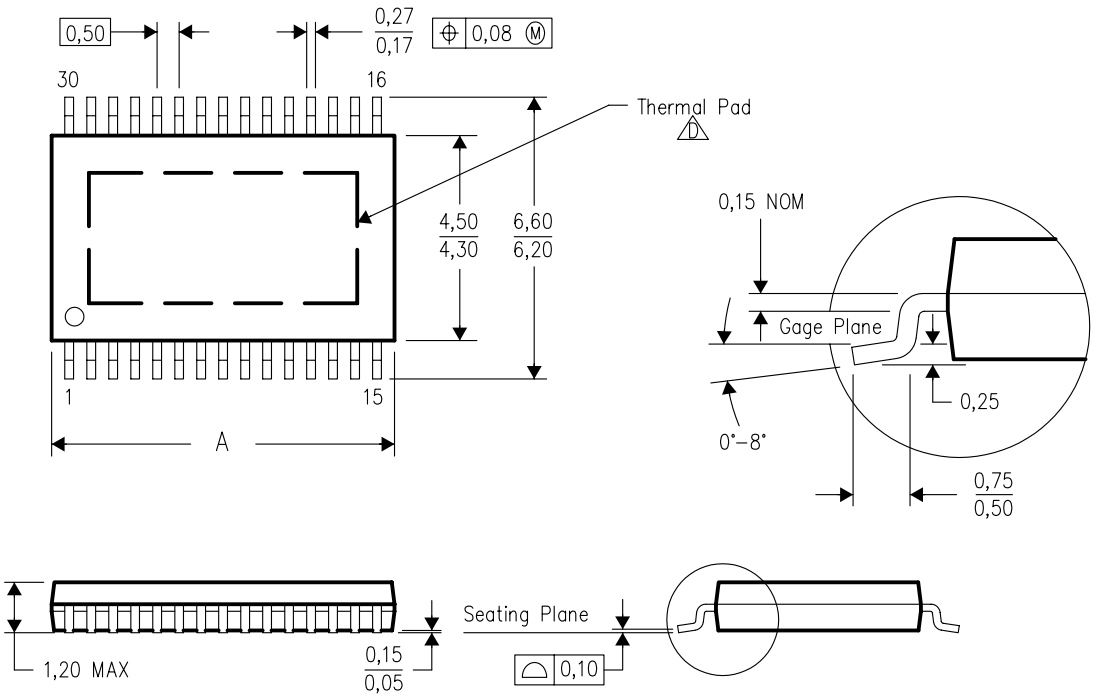
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

DCP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

30 PIN SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,40	12,60
A MIN	7,70	7,70	9,60	11,20	12,40

4073267/C 03/05

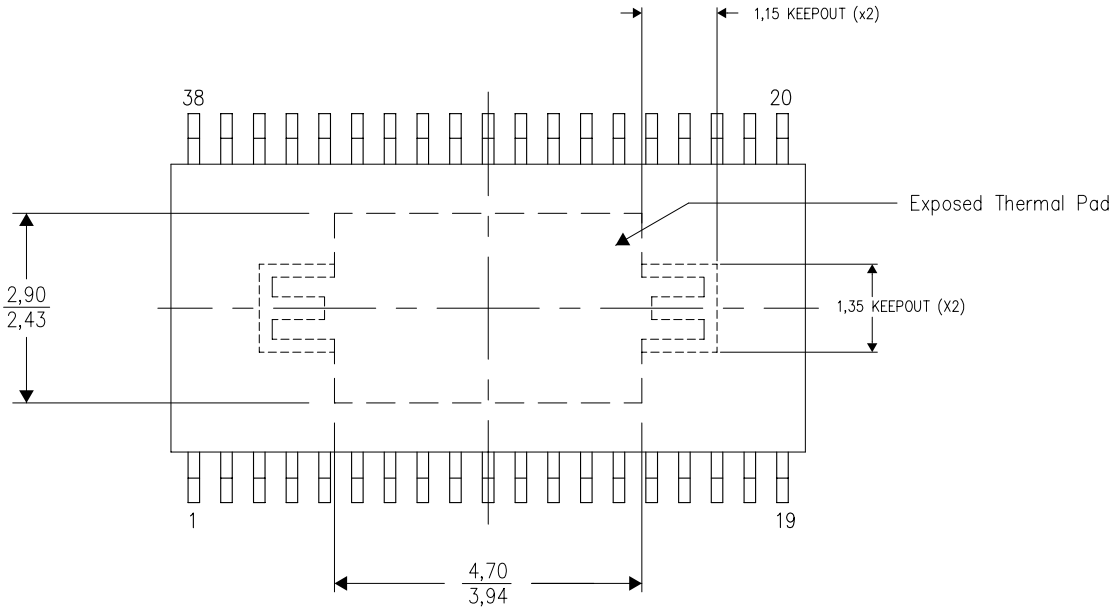
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protusions, mold flash not to exceed 0.15mm.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

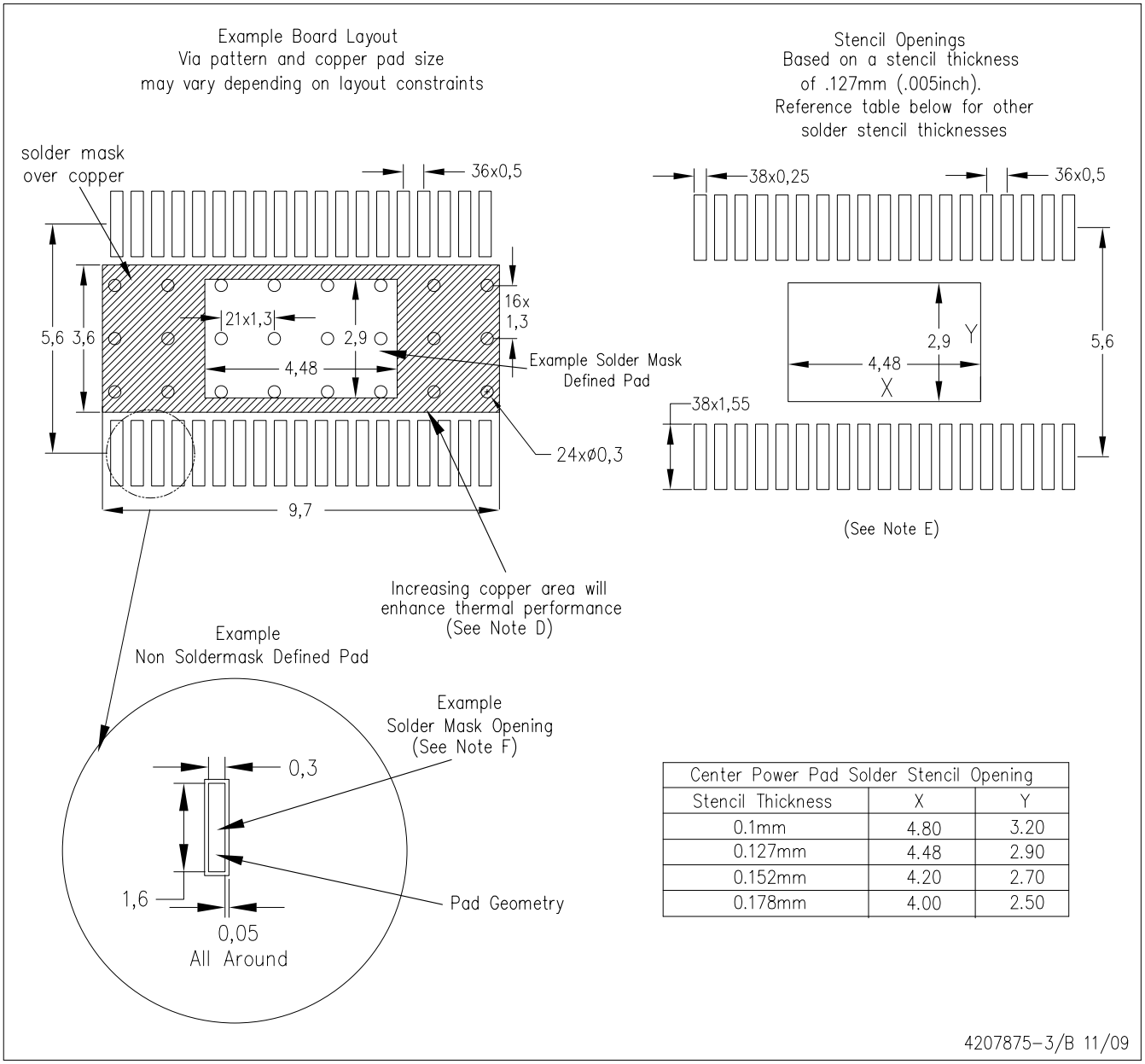


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DCP (R–PDSO–G38) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.80	3.20
0.127mm	4.48	2.90
0.152mm	4.20	2.70
0.178mm	4.00	2.50

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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