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## DRV8702-Q1, DRV8703-Q1

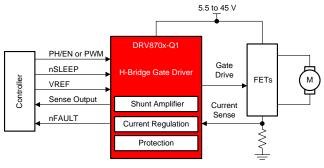
SLVSDR9-OCTOBER 2016

# DRV870x-Q1 Automotive H-Bridge Gate Driver

# 1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
- Single H-Bridge Gate Driver
  - Drives Four External N-Channel MOSFETs
  - Supports 100% PWM Duty Cycle
- 5.5- to 45-V Operating Supply-Voltage Range
- Three Control-Interface Options
  - PH/EN, Independent H-Bridge, and PWM
- Serial Interface for Configuration (DRV8703-Q1)
- Adjustable Gate Drive For Slew-Rate Control
  - 10- to 250-mA Source Current
  - 20- to 500-mA Sink Current
- Independent Control of Each H-Bridge
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Current-Shunt Amplifier
- Integrated PWM Current Regulation
- Low-Power Sleep Mode
- Small Package and Footprint
  - 32-Pin VQFN
  - 5 mm × 5 mm
  - Wettable Flanks Package
- Protection Features
  - Supply Undervoltage Lockout (UVLO)
  - Charge-Pump Undervoltage (CPUV) Lockout
  - Overcurrent Protection (OCP)
  - Gate-Driver Fault (GDF)
  - Thermal Shutdown (TSD)
  - Watchdog Timer (DRV8703-Q1)
  - Fault-Condition Output (nFAULT)

#### Simplified Schematic



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# 2 Applications

- Power Window Lift
- Power Sunroof
- Power Seats
- Power Sliding Door
- Power Folding Roof
- Power Trunk and Tailgate
- Brushed-DC Pumps

# 3 Description

The DRV870x-Q1 family of devices is a single Hbridge gate driver that uses four external N-channel MOSFETs targeted to drive a bidirectional brushed-DC motor.

A PH/EN, independent H-Bridge, or PWM interface allows simple interfacing to controller circuits. An internal sense amplifier provides adjustable current control. The gate driver includes circuitry to regulate the winding current using fixed off-time PWM current chopping.

The DRV870x-Q1 family of devices drives both highside and low-side FETs with a 10.5-V V<sub>GS</sub> gate drive. The gate-drive current for all external FETs is configurable with a single external resistor or through the serial peripheral interface (SPI).

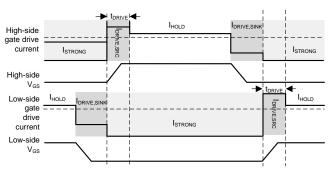
A low-power sleep mode is provided which shuts down internal circuitry to achieve a very-low quiescent-current draw.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)	
DRV8702-Q1		5 00 mm 5 00 mm	
DRV8703-Q1	VQFN (32)	5.00 mm × 5.00 mm	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Gate-Drive Current**



N



## 4 **Description (continued)**

Internal protection functions are provided including: undervoltage lockouts, charge-pump faults, overcurrent shutdown, short-circuit protection, gate-driver faults, and overtemperature. Fault conditions are indicated on the nFAULT pin.

## 5 Device and Documentation Support

### 5.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8702-Q1	Click here	Click here	Click here	Click here	Click here
DRV8703-Q1	Click here	Click here	Click here	Click here	Click here

#### Table 1. Related Links

#### 5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 5.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E<sup>™</sup> Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 5.4 Trademarks

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#### 5.5 Electrostatic Discharge Caution



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 5.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



5-Oct-2016

# PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8702QRHBRQ1	PREVIEW	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	DRV8702	
DRV8702QRHBTQ1	PREVIEW	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	DRV8702	
DRV8703QRHBRQ1	PREVIEW	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	DRV8703	
DRV8703QRHBTQ1	PREVIEW	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	DRV8703	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



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