DRV8428E/P Dual H-Bridge Motor Drivers With Integrated Current Sense and Smart Tune Technology

1 Features

- Dual H-bridge motor driver
  - One bipolar stepper motor
  - Dual bidirectional brushed-DC motors
  - Four unidirectional brushed-DC motors
- Integrated current sense functionality
  - No sense resistors required
  - ±5% Full-scale current accuracy
- 4.2- to 33-V Operating supply voltage range
- Multiple control interface options
  - PHASE/ENABLE
  - PWM
- Smart tune decay technology, and mixed decay options
- 1500 mΩ HS + LS $R_{DS(ON)}$ at 24 V, 25°C
- Current Capacity Per Bridge: 1.7-A peak, 1-A Full-Scale, 0.7-A rms
- Configurable Off-Time PWM Chopping
  - 7, 16 or 32 µs
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Inrush current limiting in brushed-DC applications
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)

2 Applications

- Brushed DC Motors
- Printers and scanners
- Currency counters, and EPOS
- Office and home automation
- Factory automation and robotics
- Small home appliances
- Sewing Machines
- Vacuum, humanoid, and toy robotics
- Smart Meters
- Servo Motors and Actuators

3 Description

The DRV8428E/P devices are dual H-bridge motor drivers for a wide variety of industrial applications. The devices can be used for driving two DC motors, or a bipolar stepper motor. The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges, current sensing and regulation, and protection circuitry. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost. A low-power sleep mode is provided to achieve ultra- low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), output overcurrent (OCP), and device overtemperature (TSD). The DRV8428E/P is capable of driving up to 1-A full scale or 0.7-A rms output current per H-bridge (dependent on PCB design).

Table 1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8428EPWPR	HTSSOP (16)	5mm x 4.4mm
DRV8428ERTER	VQFN (16)	3.0mm x 3.0mm
DRV8428EDYYR	TSOT (16)	4.2mm x 3.26mm
DRV8428PPWPR	HTSSOP (16)	5mm x 4.4mm
DRV8428PRTER	VQFN (16)	3.0mm x 3.0mm
DRV8428PDYYR	TSOT (16)	4.2mm x 3.26mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

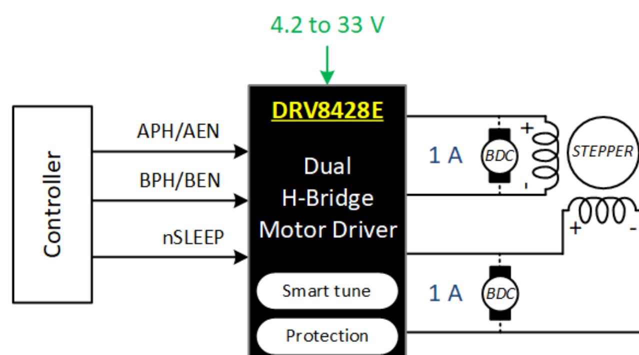

Figure 1. DRV8428E Simplified Schematic

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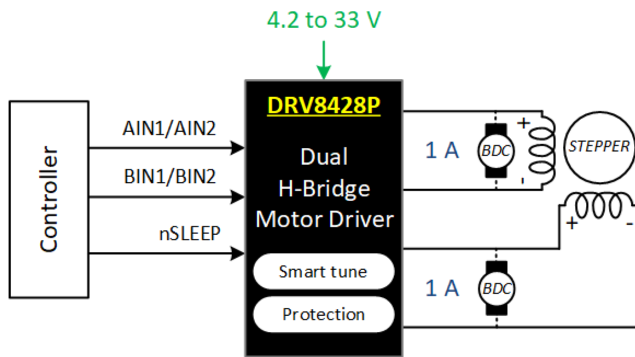

Figure 2. DRV8428P Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	*	Initial release.

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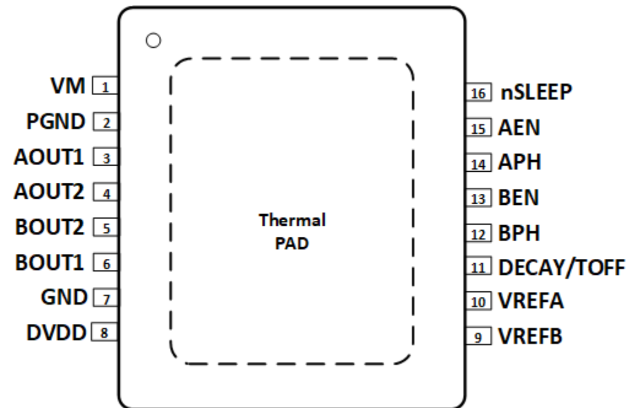
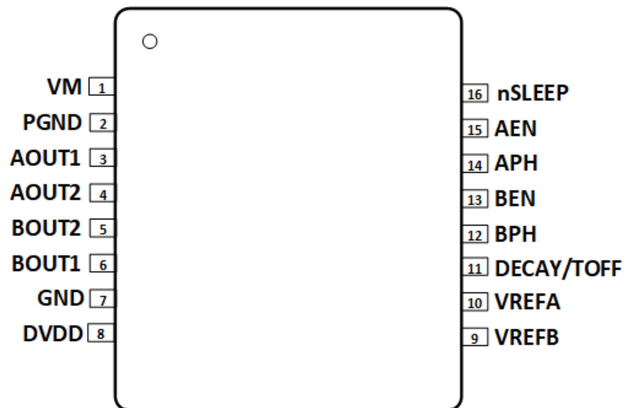
5 Pin Configuration and Functions

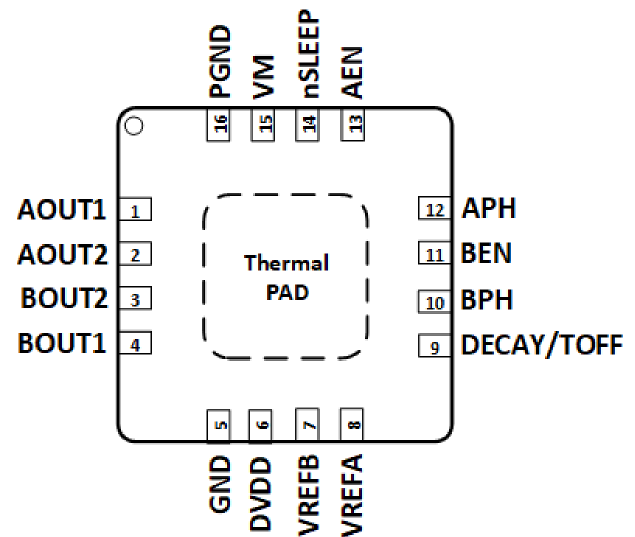
PWP PowerPAD™ Package
16-Pin HTSSOP
Top View DRV8428E



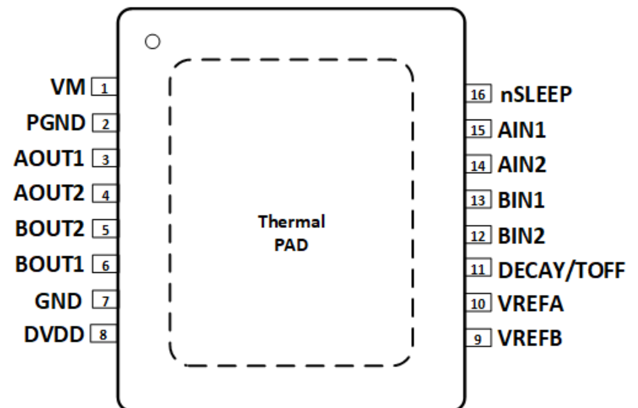
DYY Package
16-Pin TSOT
Top View DRV8428E



RTE Package
16-Pin VQFN with Exposed Thermal PAD
Top View DRV8428E



PWP PowerPAD™ Package
16-Pin HTSSOP
Top View DRV8428P



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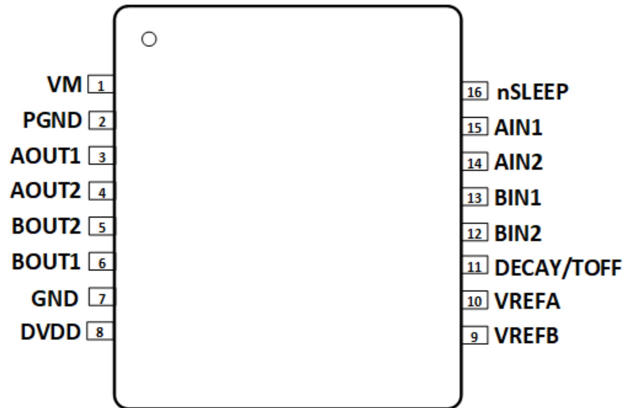
DYY Package
16-Pin TSOT
Top View DRV8428P



RTE Package
16-Pin VQFN with Exposed Thermal PAD
Top View DRV8428P

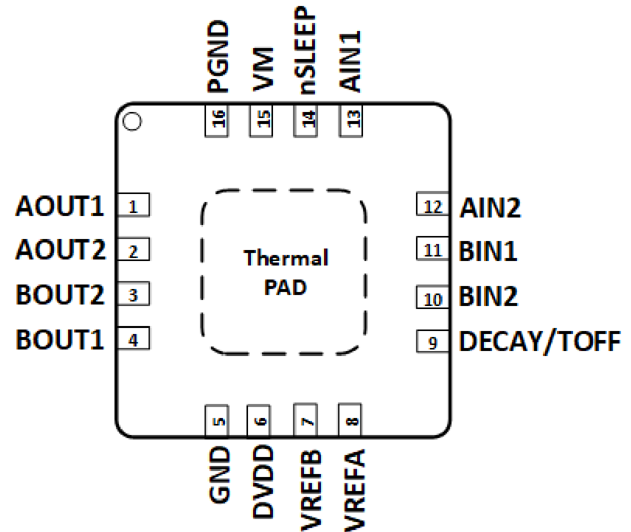


Table 2. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	PWP, DYY		RTE			
	DRV8428E	DRV8428P	DRV8428E	DRV8428P		
DECAY/TOFF	11	11	9	9	I	Decay mode and off-time setting pin. See *Current Regulation, Off-time and Decay Modes* ; seven-level pin.
AEN	15	—	13	—	I	Bridge A enable input. Logic high enables bridge A; logic low disables the bridge Hi-Z.
AIN1	—	15	—	13	I	Bridge A PWM input. Logic controls the state of H-bridge A; internal pulldown.
AIN2	—	14	—	12	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
AOUT1	3	3	1	1	O	Winding A output. Connect to motor winding.
AOUT2	4	4	2	2	O	Winding A output. Connect to motor winding.
APH	14	—	12	—	I	Bridge A phase input. Logic high drives current from AOUT1 to AOUT2.
VREFA	10	10	8	8	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge A.
BEN	13	—	11	—	I	Bridge B enable input. Logic high enables bridge B; logic low disables the bridge Hi-Z.
BIN1	—	13	—	11	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BIN2	—	12	—	10	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BOUT1	6	6	4	4	O	Winding B output. Connect to motor winding.
BOUT2	5	5	3	3	O	Winding B output. Connect to motor winding.
BPH	12	—	10	—	I	Bridge B phase input. Logic high drives current from BOUT1 to BOUT2.
VREFB	9	9	7	7	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge B.
GND	7	7	5	5	PWR	Device ground. Connect to system ground.

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Table 2. Pin Functions (continued)

NAME	PIN				TYPE	DESCRIPTION
	PWP, DYY		RTE			
	DRV8428E	DRV8428P	DRV8428E	DRV8428P		
DVDD	8	8	6	6	PWR	Logic supply voltage. Connect a X7R, 0.47-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VM	1	1	15	15	PWR	Power supply. Connect to motor supply voltage and bypass to GND with a 0.01-µF ceramic capacitor plus a bulk capacitor rated for VM.
PGND	2	2	16	16	PWR	Power ground. Connect to system ground.
nSLEEP	16	16	14	14	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, DECAY/TOFF)	–0.3	5.75	V
Reference input pin voltage (VREFA, VREFB)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 8, 9, and 16)	±750	
			Other pins	±500	

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.2	33	V
V_I	Logic level input voltage	0	5.5	V
V_{REF}	Reference rms voltage range (VREFA, VREFB)	0.05	3	V
f_{PWM}	Applied PWM signal (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2)	0	100	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1	A
I_{rms}	Motor RMS current (xOUTx)	0	0.7	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		PWP (HTSSOP)	DYY (TSOT)	RTE (VQFN)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	88.3	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.2	43.5	57.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.3	26.3	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	1.2	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.2	26.2	23.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	N/A	8.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 33 V	4.5	5	5.5	V
LOGIC-LEVEL INPUTS (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
t_{PD}	Propagation delay	xPH, xEN, xINx input to current change		750		ns
SEVEN-LEVEL INPUT (DECAY/TOFF)						
V_{I1}	Voltage level 1	Tied to GND	0		0.1	V
V_{I2}	Voltage level 2	14.7kΩ ± 1% to GND	0.2		0.35	V
V_{I3}	Voltage level 3	44.2kΩ ± 1% to GND	0.55		0.8	V
V_{I4}	Voltage level 4	100kΩ ± 1% to GND	1		1.25	V
V_{I5}	Voltage level 5	249kΩ ± 1% to GND	1.5		1.75	V
V_{I6}	Voltage level 6	Hi-Z	2.1		2.35	V
V_{I7}	Voltage level 7	Tied to DVDD	3		5.5	V
I_O	Output pull-up current			22.5		µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	V_{VM} = 24 V, T_J = 25 °C, I_O = -0.5 A		750	900	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = -0.5 A		1130	1400	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = -0.5 A		1250	1590	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	V_{VM} = 24 V, T_J = 25 °C, I_O = 0.5 A		750	900	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = 0.5 A		1130	1400	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = 0.5 A		1250	1590	mΩ
t_{SR}	Output slew rate	VM = 24V, I_O = 0.5 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREFA, VREFB)						
K_V	Transimpedance gain	VREF = 3 V	2.85	3	3.15	V/A
t_{OFF}	PWM off-time, mixed 30% decay	DECAY/TOFF = 14.7kΩ to GND		7		µs
		DECAY/TOFF = 44.2kΩ to GND		16		
		DECAY/TOFF = 100kΩ to GND		32		
	PWM off-time, smart tune dynamic decay	DECAY/TOFF = 249kΩ to GND		7		
		DECAY/TOFF = Hi-Z		16		
		DECAY/TOFF = DVDD		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 1 A, 10% to 20% current setting	–15		15	%
		I_O = 1 A, 20% to 67% current setting	–10		10	
		I_O = 1 A, 68% to 100% current setting	-5		5	

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Electrical Characteristics (continued)

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	3.85	3.95	4.05	V
		VM rising, UVLO rising	3.95	4.05	4.15	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
I_{OCP}	Overcurrent protection	Current through any FET	1.7			A
t_{OCP}	Overcurrent deglitch time			1.25		µs
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

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7 Detailed Description

7.1 Overview

The DRV8428E/P are integrated motor driver solutions for bipolar stepper motors or dual brushed-DC motors. The devices integrate two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry. The DRV8428E/P can be powered with a supply voltage between 4.2 and 33 V. The DRV8428E/P are capable of providing an output current up to 1.7-A peak, 1-A full-scale, or 0.7-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8428E/P devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREFA and VREFB pins. These features reduce external component cost, board PCB size, and system power consumption.

A simple PH/**E**N (DRV8428**E**) or **P**WM (DRV8428**P**) interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a smart tune Dynamic Decay, smart tune Ripple Control, or mixed decay. The smart tune decay modes automatically adjust the decay setting to minimize current ripple while still reacting quickly to step changes. This feature greatly simplifies stepper driver integration into a motor drive system. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, or 32 µs.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

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7.2 Functional Block Diagrams

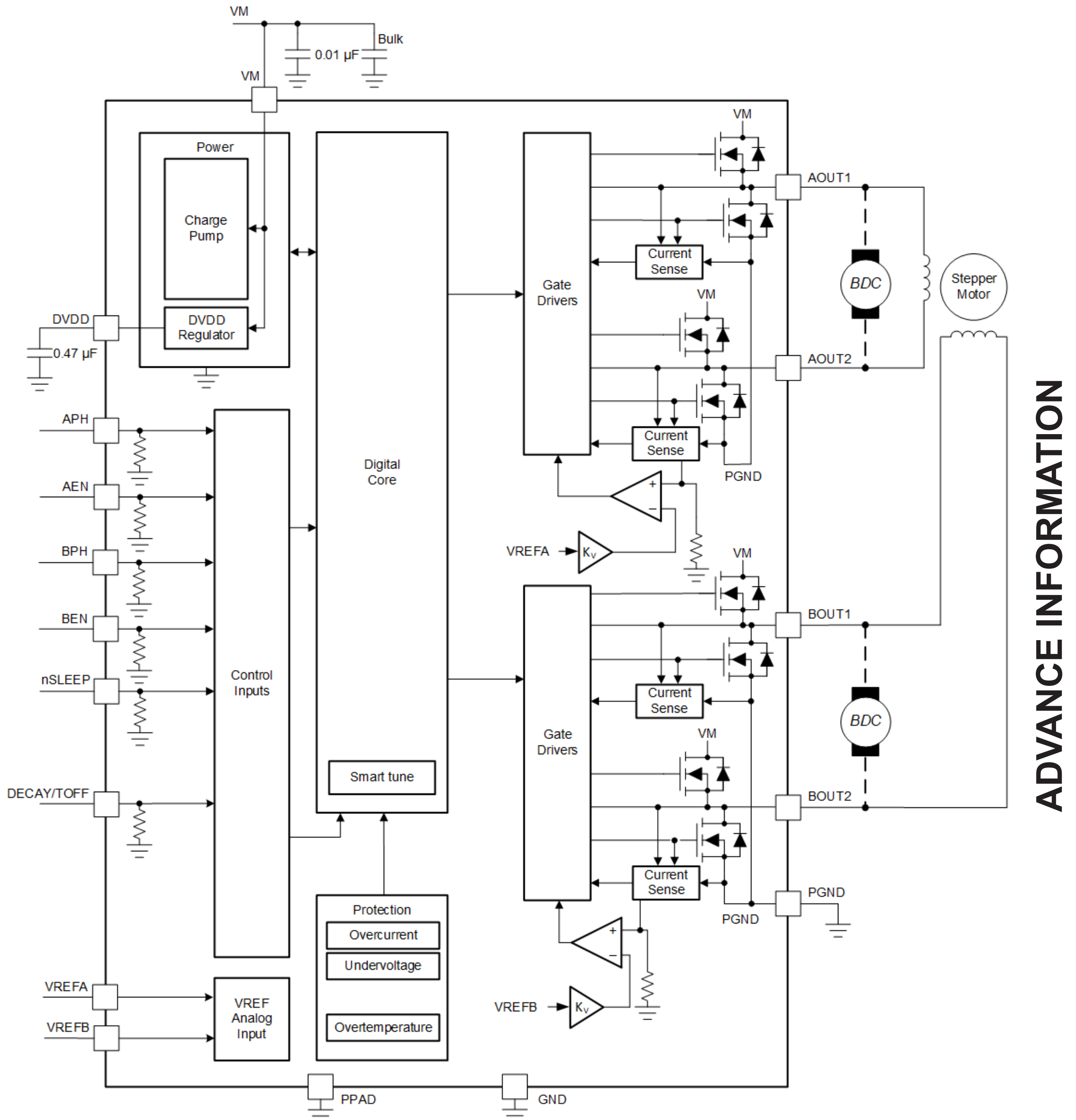

Figure 3. DRV8428E Block Diagram

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Functional Block Diagrams (continued)

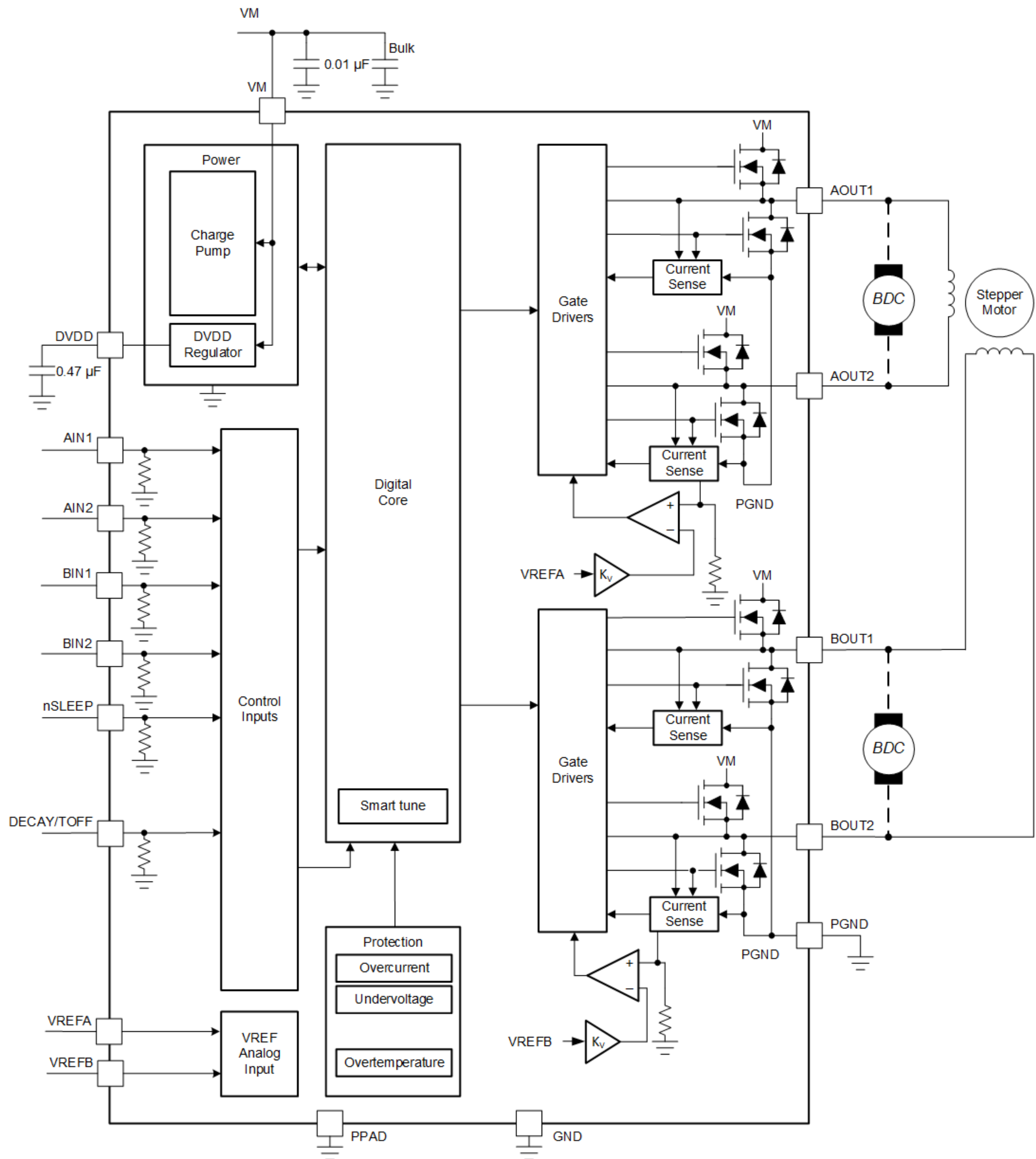

Figure 4. DRV8428P Block Diagram

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7.3 Feature Description

Table 3 shows the recommended values of the external components for the gate driver.

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{REF1}	VREFx	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREFx	GND	

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7.3.1 PWM Motor Drivers

The DRV8428E/P contain drivers for two full H-bridges. Figure 5 shows a block diagram of the circuitry.

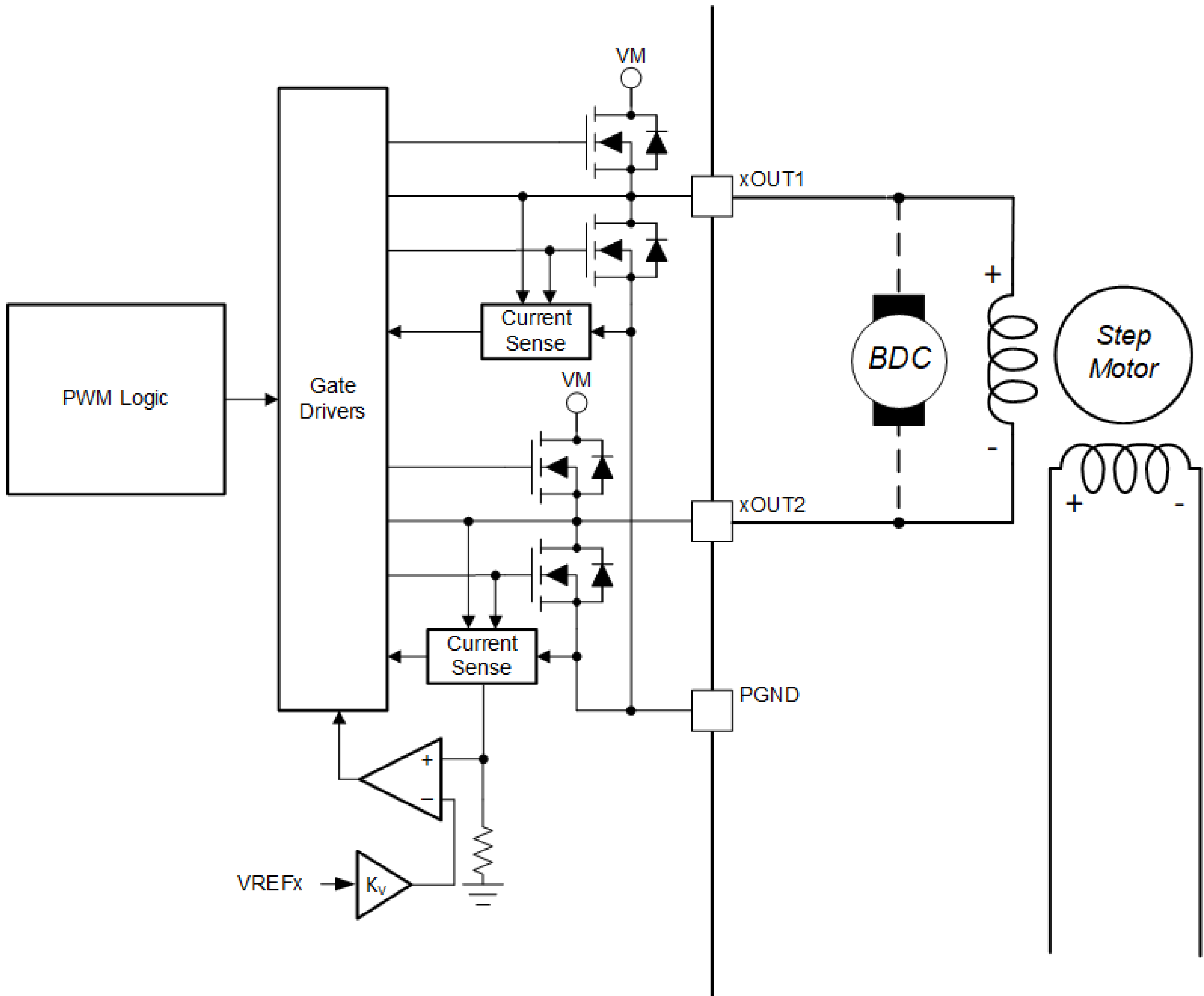

Figure 5. PWM Motor Driver Block Diagram

7.3.2 Bridge Control

The DRV8428E is controlled using a PH/EN interface. Table 4 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8428E. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 4. DRV8428E (PH/EN) Control Interface

nSLEEP	xEN	xPH	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	H-bridge disabled Hi-Z
1	1	0	L	H	Reverse (current xOUT2 to xOUT1)
1	1	1	H	L	Forward (current xOUT1 to xOUT2)

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The DRV8428P is controlled using a PWM interface. Table 5 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8428P. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 5. DRV8428P (PWM) Control Interface

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	L	L	Brake; low-side slow decay
1	0	1	L	H	Reverse (current xOUT2 to xOUT1)
1	1	0	H	L	Forward (current xOUT1 to xOUT2)
1	1	1	H	H	Brake; high-side slow decay

7.3.3 Current Regulation, Off-time and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6, Item 1.

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the seven-level DECAY/TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 6, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6, Item 3.

The PWM chopping current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. To generate the reference voltage for the current chopping comparator, the VREFx input is attenuated by a factor of Kv.

The chopping current (I_{FS}) can be calculated as I_{FS} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 3 (V/A).

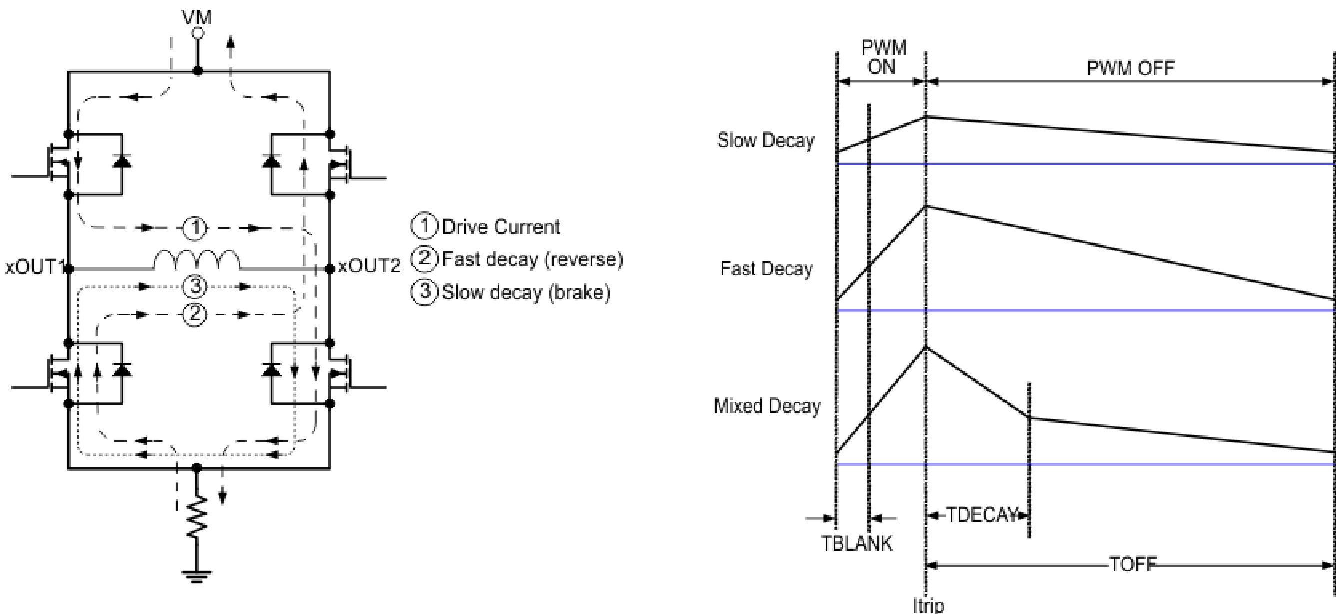

Figure 6. Decay Modes

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The decay mode and off time for each bridge is selected by setting the seven-level DECAY/TOFF pin as shown in Table 6.

Table 6. Decay Mode Settings

DECAY/TOFF	DECAY MODE	OFF TIME
0	Smart tune Ripple Control	-
14.7kΩ to GND	Mixed 30% Decay	7μs
44.2kΩ to GND		16μs
100kΩ to GND		32μs
249kΩ to GND	Smart tune Dynamic Decay	7μs
Hi-Z		16μs
DVDD		32μs

ADVANCE INFORMATION

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7.3.3.1 Mixed Decay

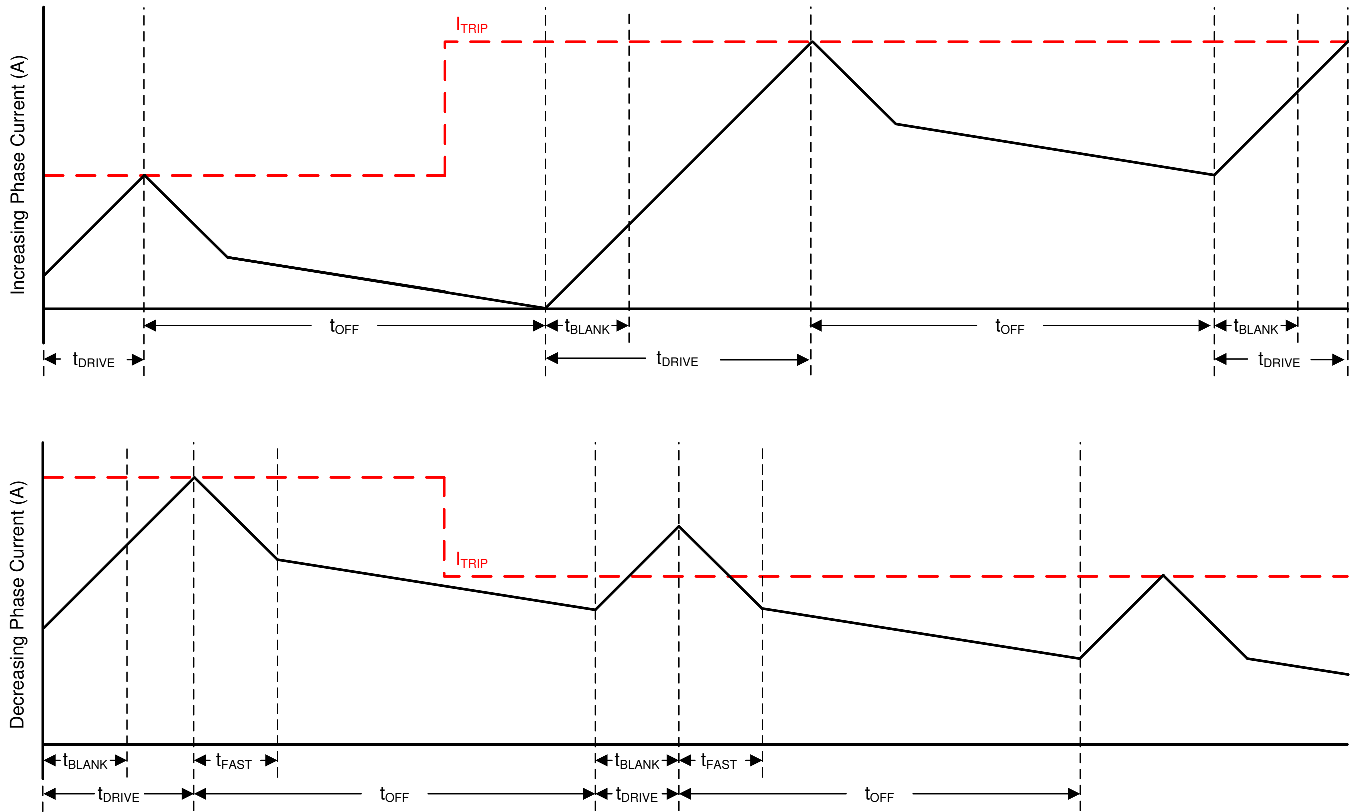

Figure 7. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

ADVANCE INFORMATION

7.3.3.2 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

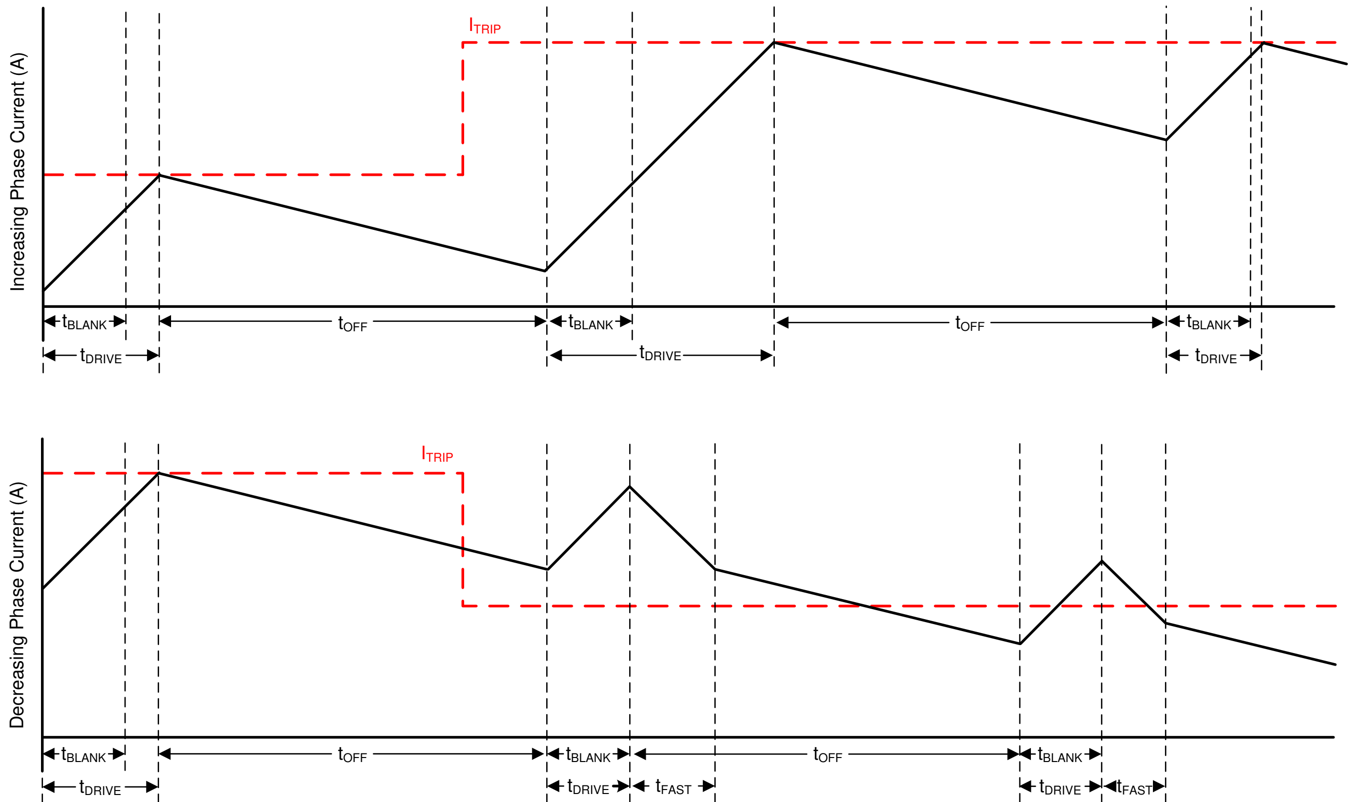

Figure 8. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

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7.3.3.3 Smart tune Ripple Control

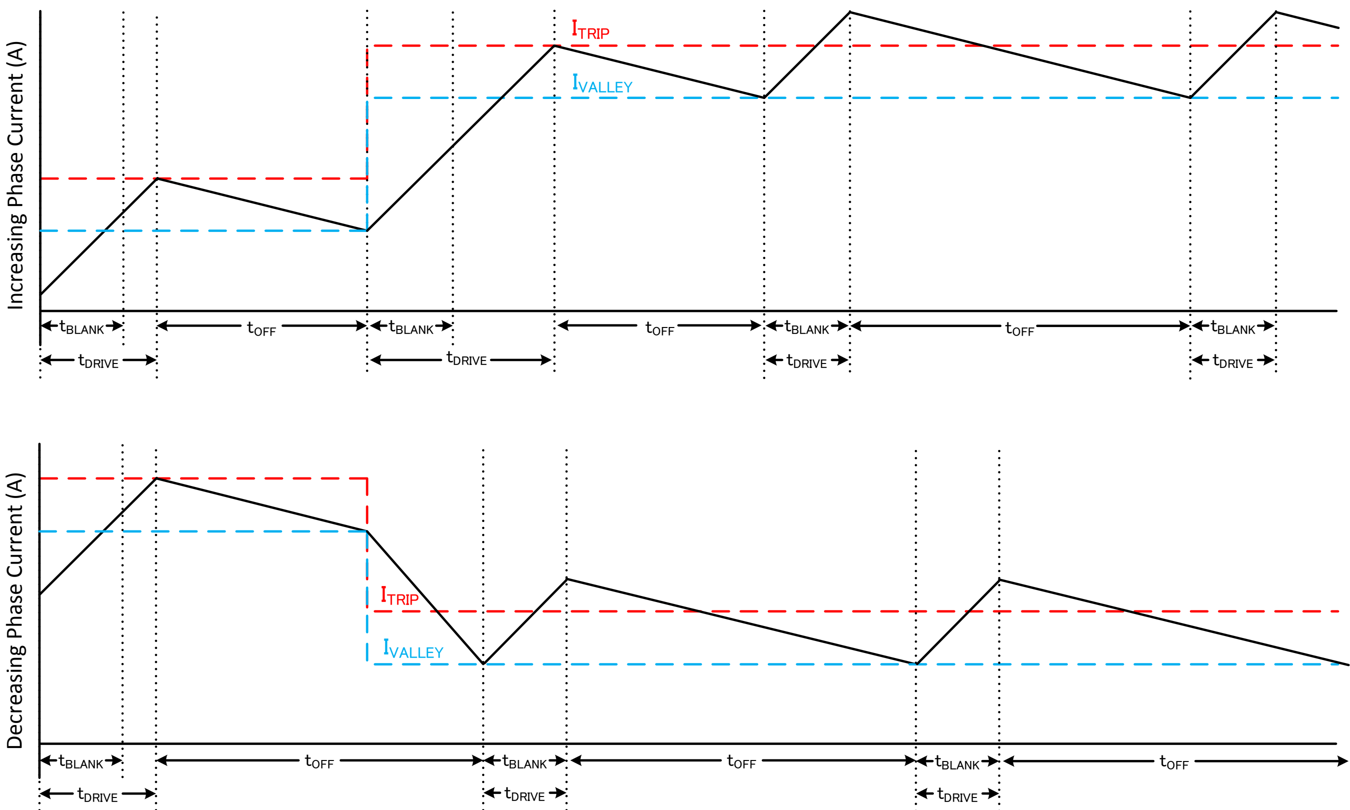

Figure 9. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

The ripple current in this decay mode is 7.5mA + 1% of the ITRIP at a specific microstep level.

7.3.3.4 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

ADVANCE INFORMATION

7.3.4 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

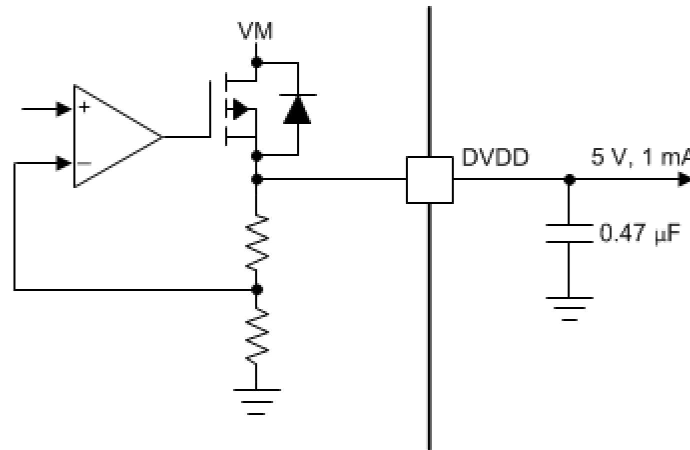

Figure 10. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, DECAY/TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

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7.3.5 Logic and Seven-Level Pin Diagrams

Figure 11 gives the input structure for logic-level pins APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2 and nSLEEP:

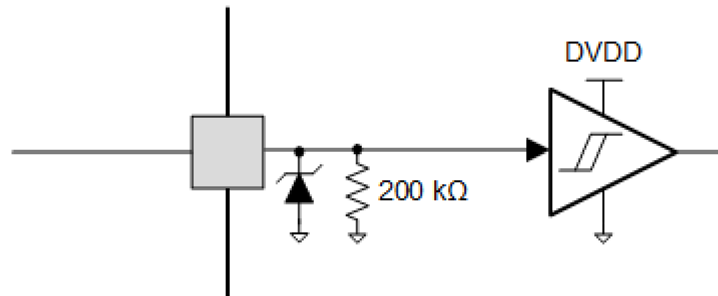

Figure 11. Logic-level Input Pin Diagram

Seven-level logic pin DECAY/TOFF has the following structure as shown in Figure 12.

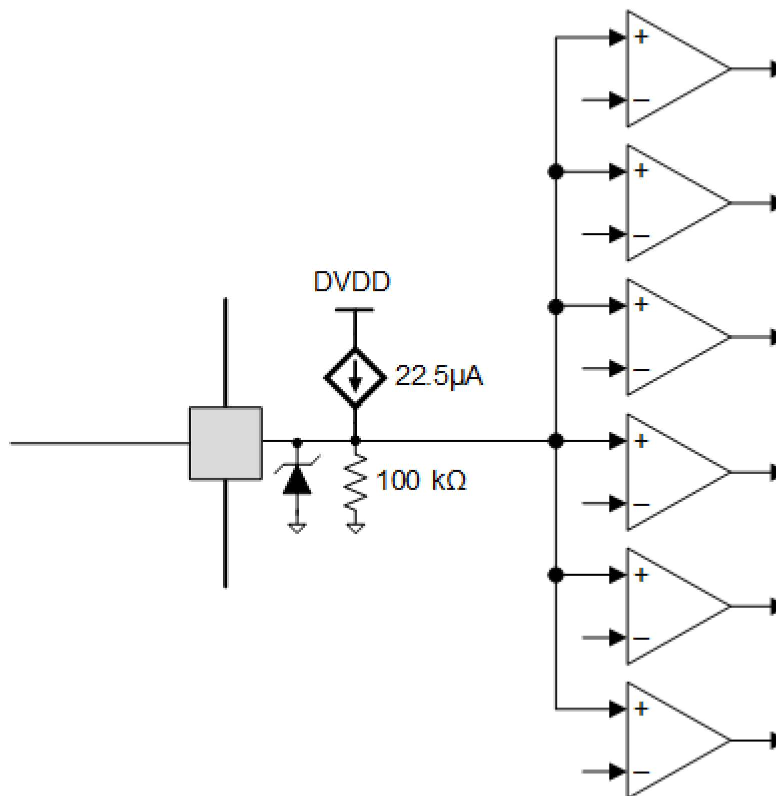

Figure 12. Seven-Level Input Pin Diagram

7.3.6 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.6.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled. Normal operation resumes when the VM undervoltage condition is removed.

ADVANCE INFORMATION

7.3.6.2 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.6.3 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS_OTSD}), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

Table 7. Fault Condition Summary

FAULT	CONDITION	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	Disabled	Reset (V_{DVDD} < 3.6 V)	Automatic: VM > V_{UVLO}
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	Latched
Thermal Shutdown (OTSD)	$T_J > T_{TSD}$	Disabled	Operating	Latched

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 nSLEEP Reset Pulse

A fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 13). This reset pulse does not affect the status of the charge pump or other functional blocks.

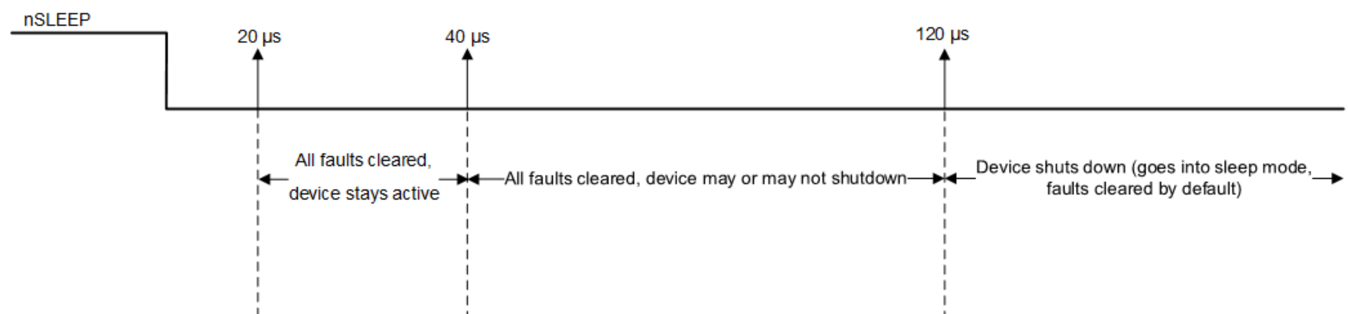

Figure 13. nSLEEP Reset Pulse

Table 8 lists a summary of the functional modes.

Table 8. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	Logic
Sleep mode	4.2 V < VM < 33 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled
Operating	4.2 V < VM < 33 V	nSLEEP pin = 1	Operating	Operating	Operating

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8428E/P is used in stepper or brushed motor control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8428E/P. In this application, the device will be used to drive a stepper motor.

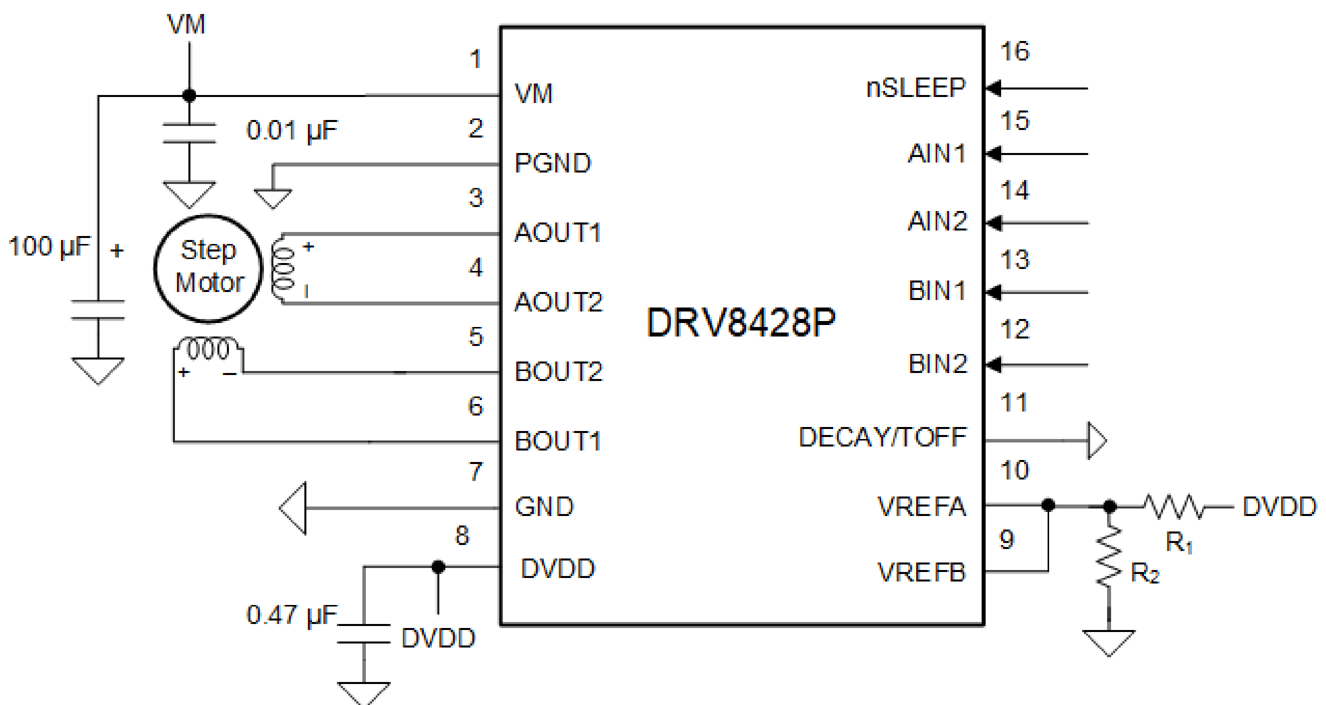

Figure 14. Typical Application Schematic

8.2.1 Design Requirements

Table 9 lists the design input parameters for system design.

Table 9. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	5.6 Ω/phase
Motor winding inductance	L_L	3.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/2 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	500 mA

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8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREFx voltage. The maximum allowable voltage on the VREFx pins is 3 V. DVDD can be used to provide VREFx through a resistor divider.

I_{FS} (A) = V_{REF} (V) / 3 (V/A)

NOTE

The I_{FS} current must also follow Equation 1 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{1}$$

8.2.2.2 Stepper Motor Speed

Next, the driving waveform needs to be planned. In order to command the correct speed, determine the frequency of the input waveform.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (°/rot)}{\theta_{step}\ (°/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \tag{2}$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the device. For the design parameters mentioned in Table 9, f_{step} can be calculated as 800 Hz.

8.2.2.3 Decay Modes

The device supports three different decay modes: mixed decay, smart tune dynamic decay and smart tune ripple control. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

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8.3 Alternate Application

In this application, the device is configured to drive bidirectional currents through two external loads (such as two brushed DC motors) using H-bridge configuration. The H-bridge polarity and duty cycle are controlled from the external controller to the xEN/xIN1 and xPH/xIN2 pins.

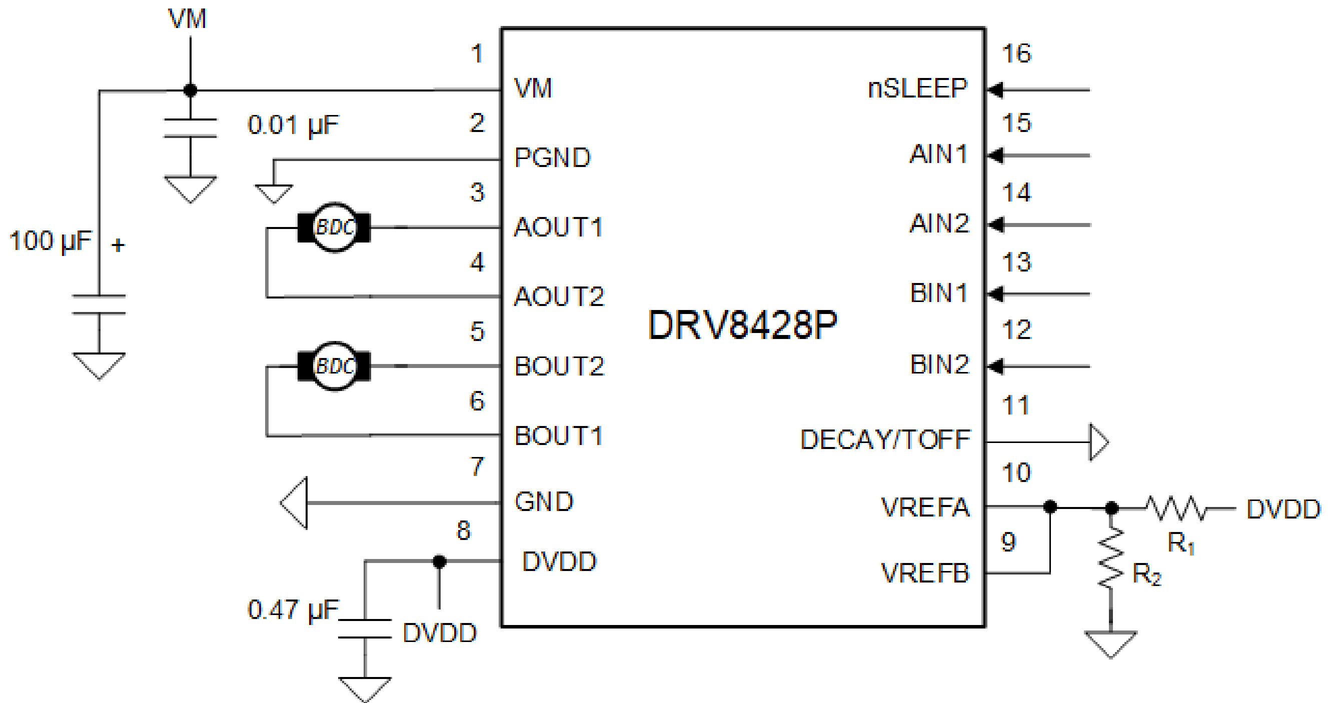

Figure 15. Typical Application Schematic

8.3.1 Design Requirements

Table 10 gives design input parameters for system design.

Table 10. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω
Motor winding inductance	L_L	4.1 mH
f_{PWM}	Switching frequency	20 kHz
Target maximum motor current	I_{TRIP}	500 mA

8.3.2 Detailed Design Procedure

8.3.2.1 Current Regulation

The maximum current (I_{TRIP}) is set by the VREFx analog voltage. When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on startup.

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.2 V to 33 V. A 0.01-µF ceramic capacitor rated for VM must be placed at VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

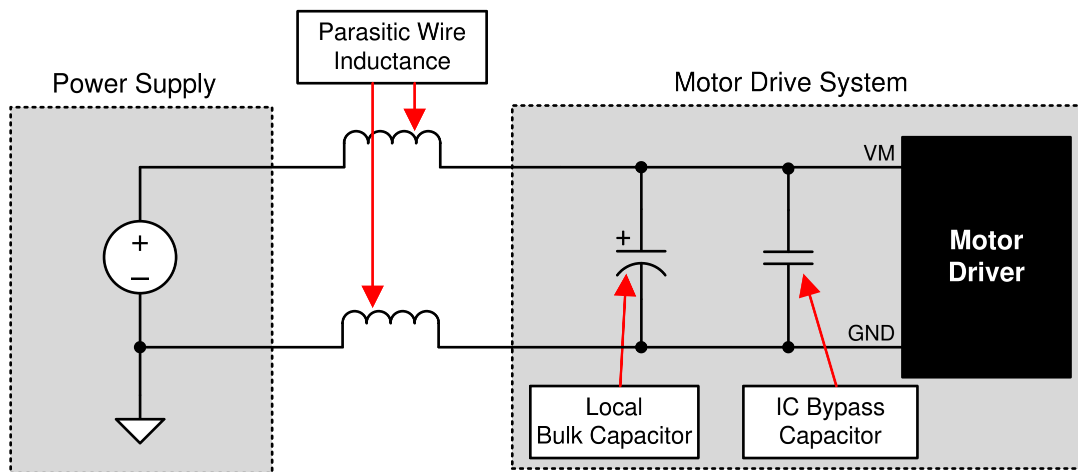

Figure 16. Example Setup of Motor Drive System With External Power Supply

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10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

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11 Device and Documentation Support

11.1 Device Support (Optional)

11.1.1 Development Support (Optional)

11.1.2 Device Nomenclature (Optional)

11.2 Documentation Support (if applicable)

11.2.1 Related Documentation

For related documentation see the following:

-
-

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8428E	Click here	Click here	Click here	Click here	Click here
DRV8428P	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

E2E is a trademark of Texas Instruments.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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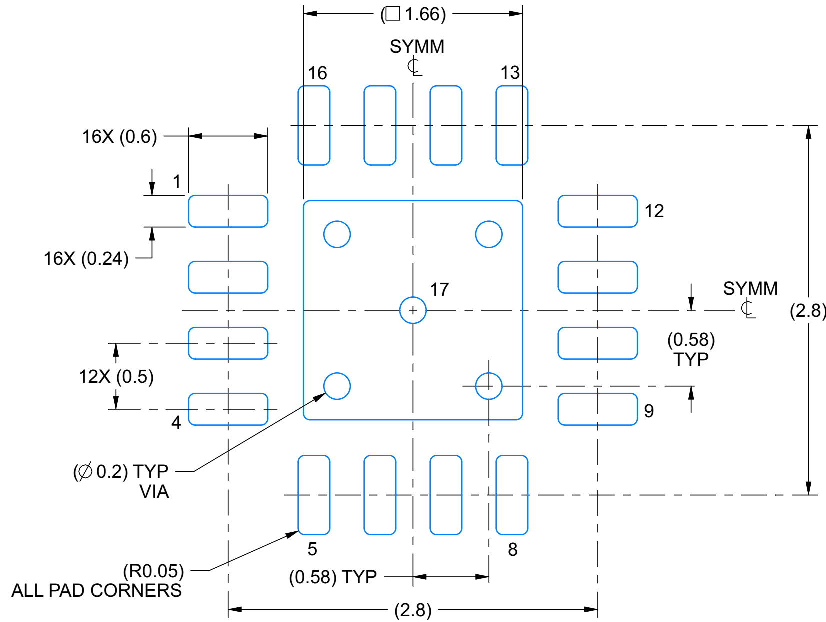
EXAMPLE BOARD LAYOUT

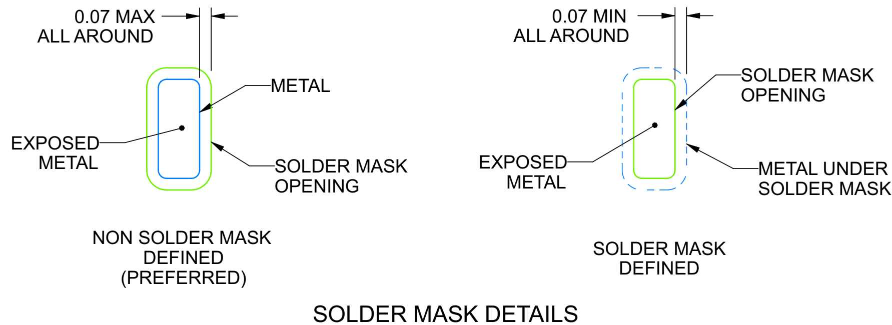
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224278/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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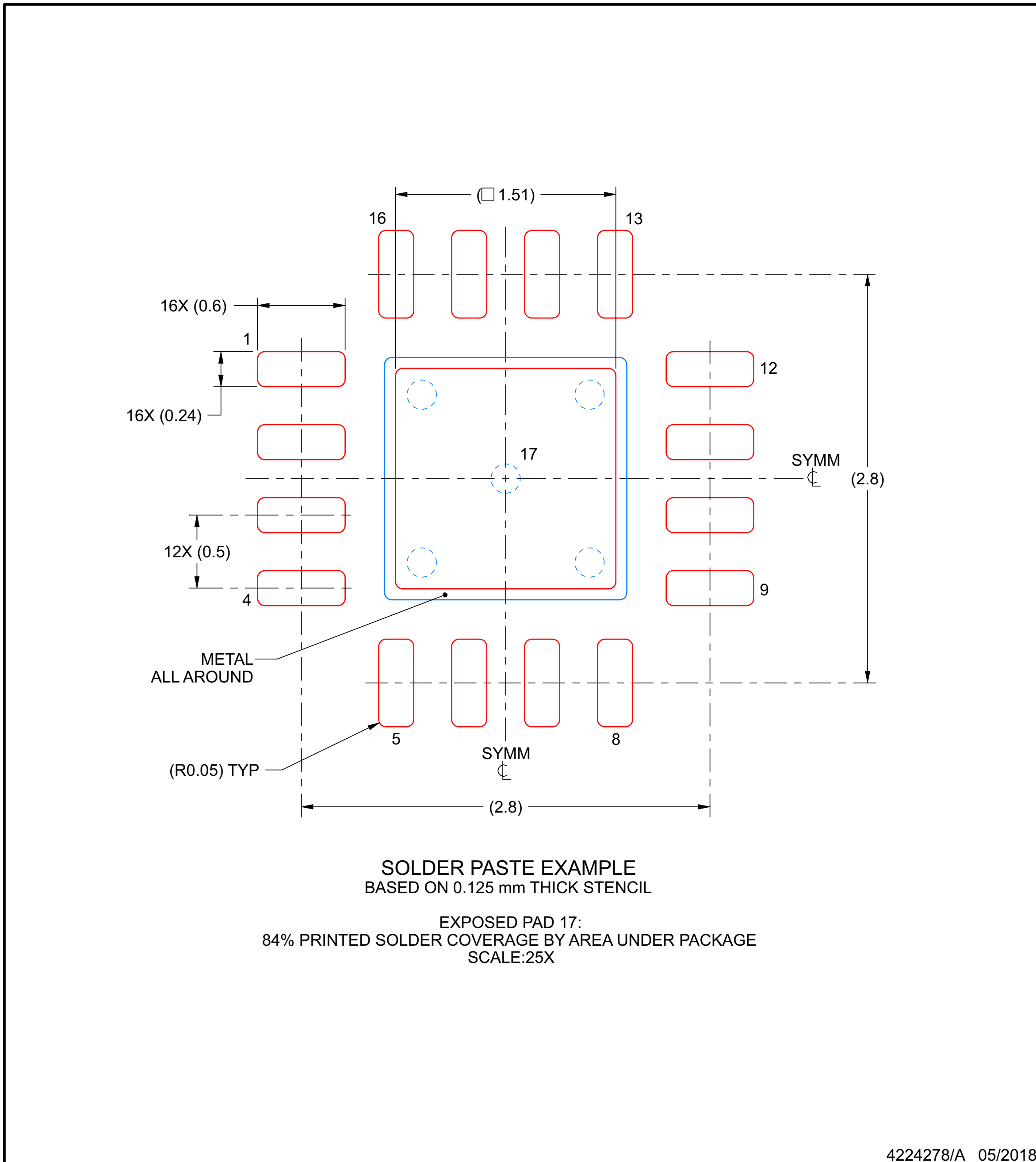
www.ti.com

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RTE0016J **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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PACKAGE OUTLINE

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

A
6.6
6.2 TYP
PIN 1 INDEX
AREA
C
0.1 C
SEATING
PLANE
14X 0.65
16
1
2X
4.55
5.1
4.9
NOTE 3
8
9
B
4.5
4.3
16X 0.30
0.19
0.1 Ⓜ C A B
SEE DETAIL A
(0.15) TYP
2X 0.95 MAX
NOTE 5
4X (0.3)
8
9
2X 0.23 MAX
NOTE 5
2.31
1.75
17
0.25
GAGE PLANE
1.2 MAX
1
16
THERMAL
PAD
2.46
1.75
0° -8°
0.75
0.50
0.15
0.05
DETAIL A
TYPICAL

4224559/B 01/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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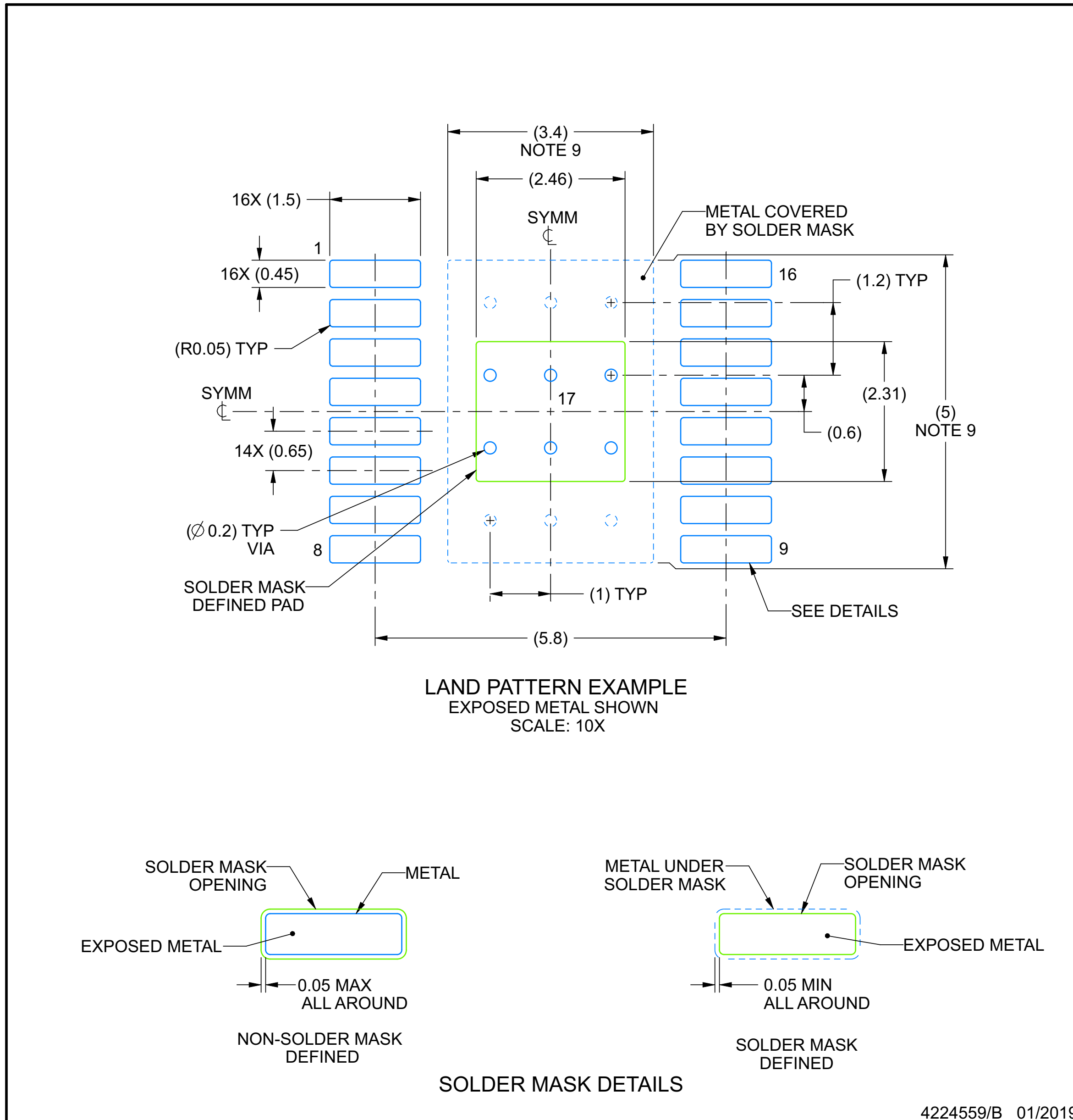
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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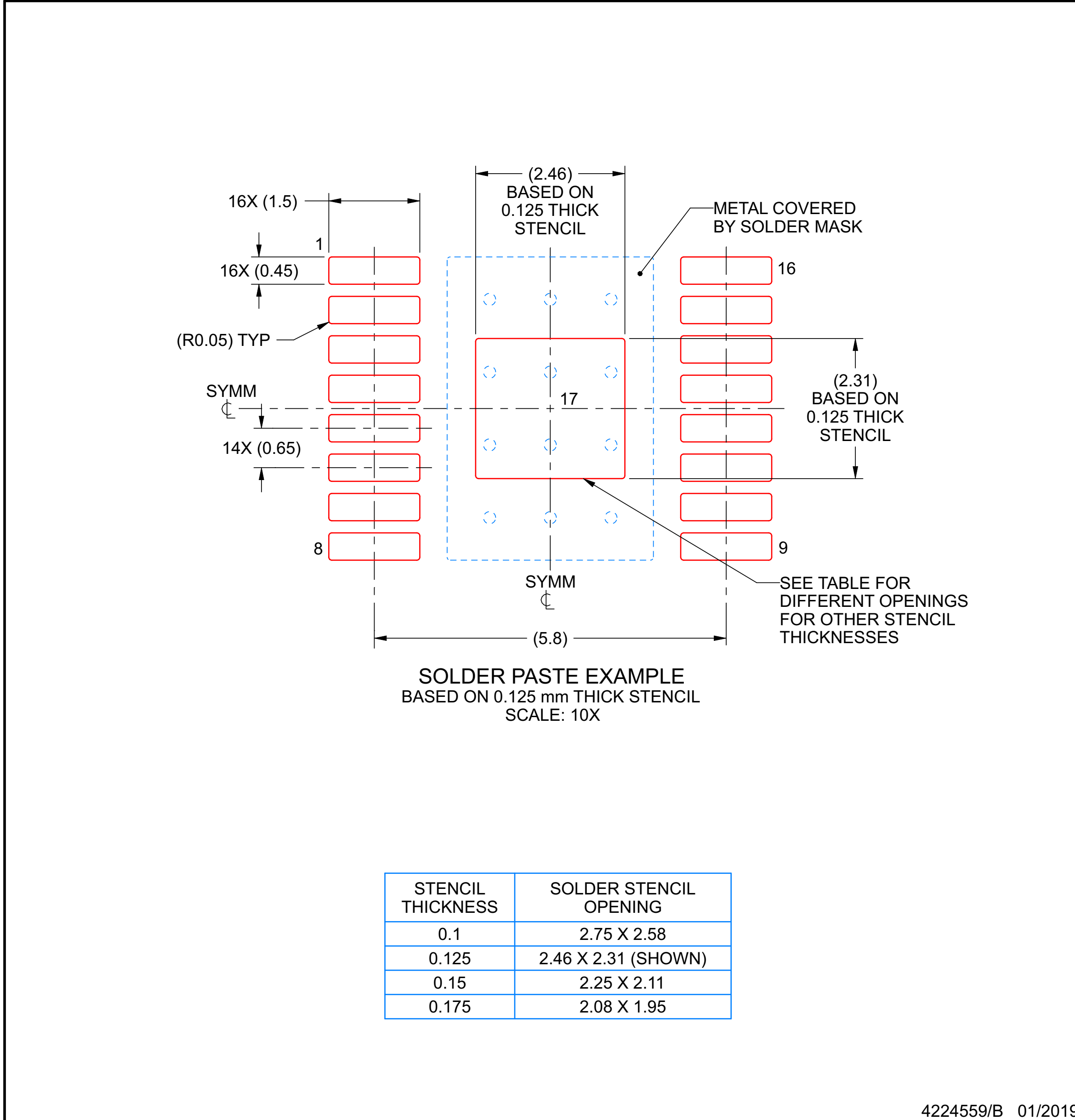
EXAMPLE STENCIL DESIGN

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

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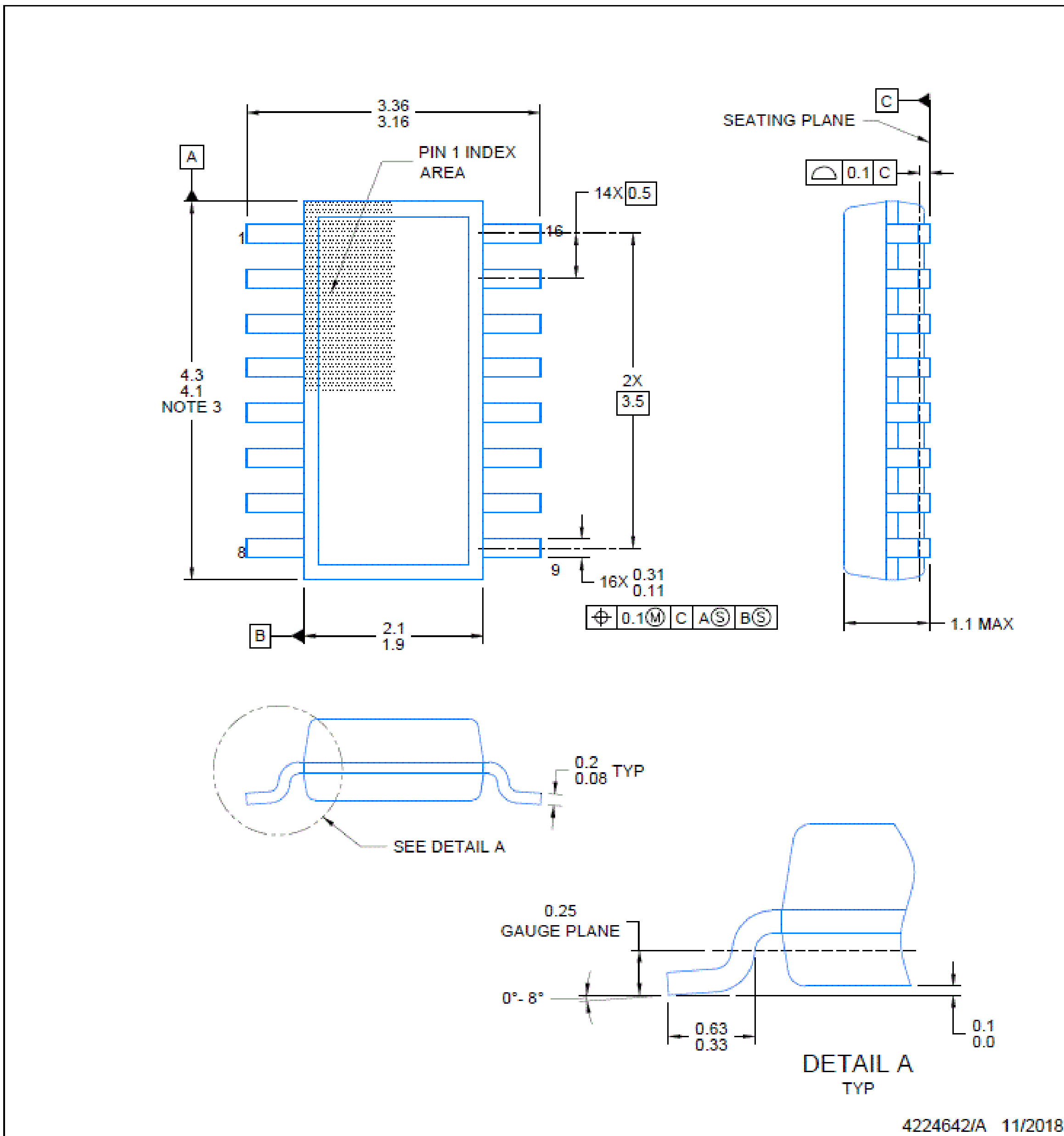
ADVANCE INFORMATION

PACKAGE OUTLINE

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

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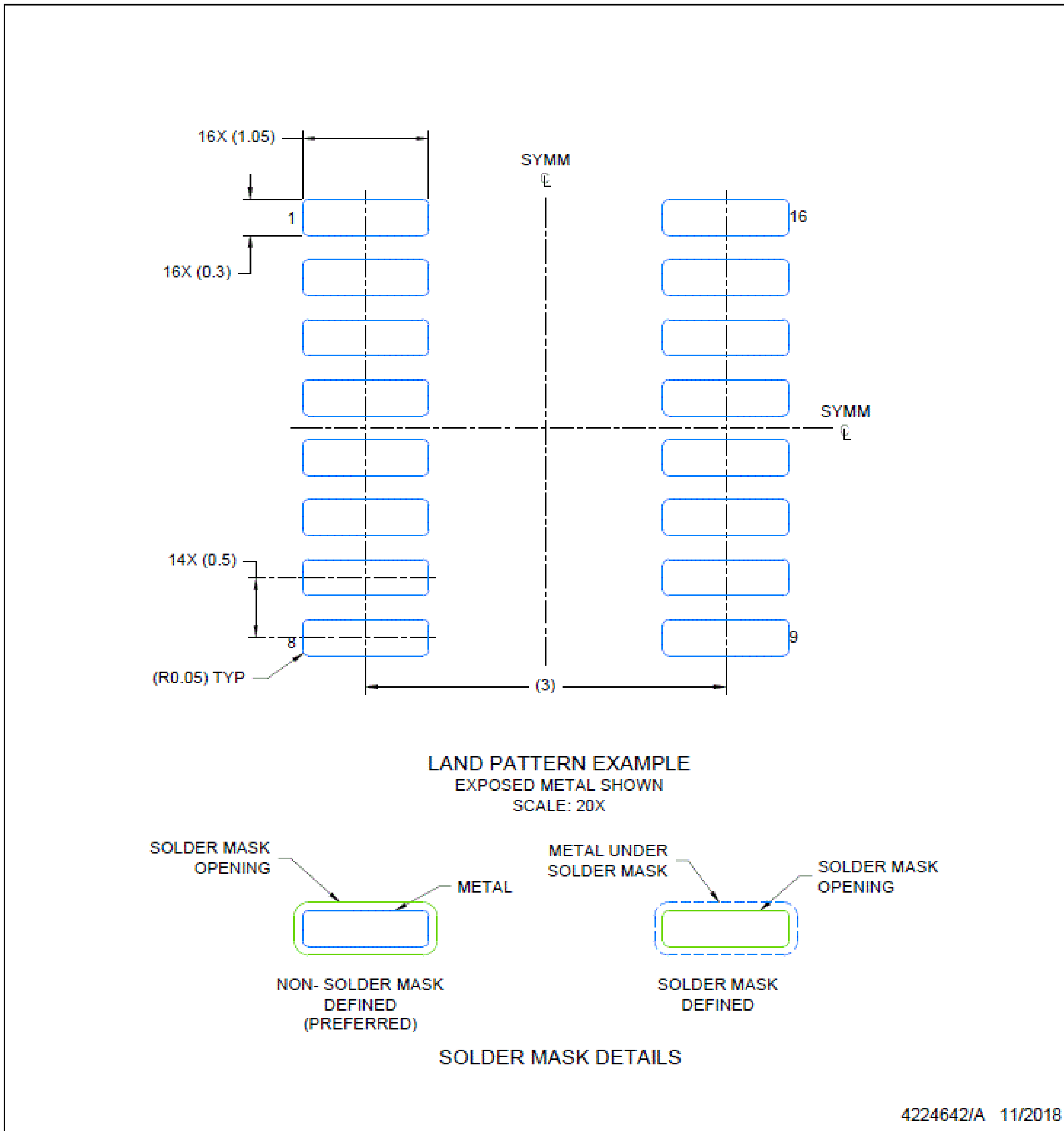

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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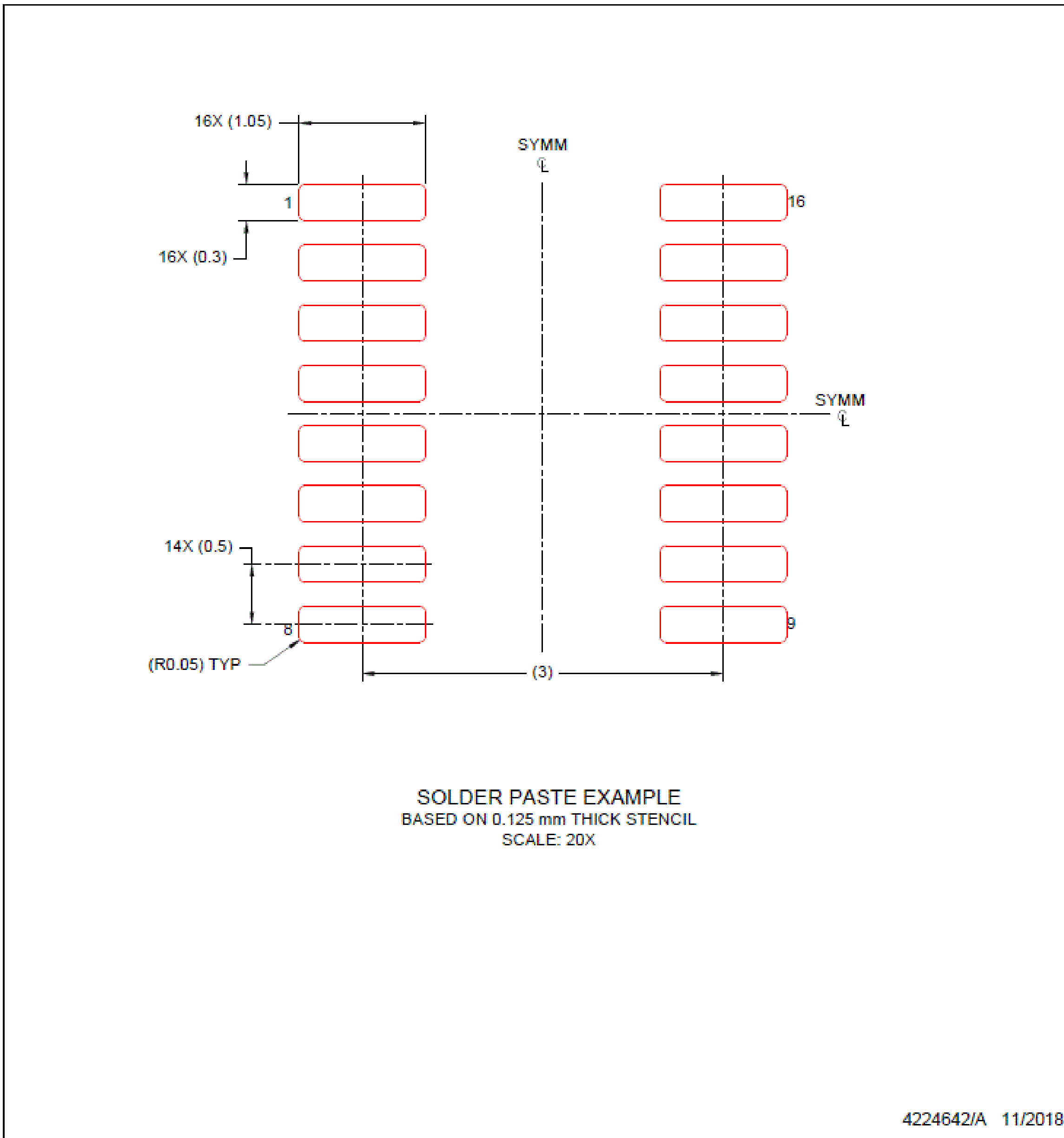
ADVANCE INFORMATION



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8428EDYYR	PREVIEW	SOT-23-THN	DYY	16	3000	TBD	Call TI	Call TI	-40 to 125		
DRV8428EPWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI	-40 to 125		
DRV8428ERTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		
DRV8428PDYYR	PREVIEW	SOT-23-THN	DYY	16	3000	TBD	Call TI	Call TI	-40 to 125		
DRV8428PPWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI	-40 to 125		
DRV8428PRTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		
PDRV8428EDYYR	ACTIVE	SOT-23-THN	DYY	16	1	TBD	Call TI	Call TI	-40 to 125		Samples
PDRV8428EPWPR	PREVIEW	HTSSOP	PWP	16	1	TBD	Call TI	Call TI	-40 to 125		
PDRV8428ERTER	ACTIVE	WQFN	RTE	16	1	TBD	Call TI	Call TI	-40 to 125		Samples
PDRV8428PDYYR	PREVIEW	SOT-23-THN	DYY	16	1	TBD	Call TI	Call TI	-40 to 125		
PDRV8428PPWPR	PREVIEW	HTSSOP	PWP	16	1	TBD	Call TI	Call TI	-40 to 125		
PDRV8428PRTER	PREVIEW	WQFN	RTE	16	1	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

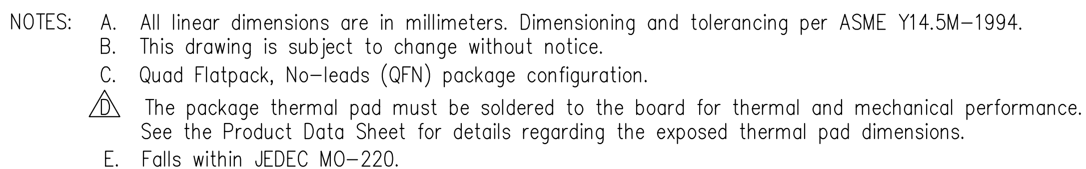
RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

3,15
2,85
A
B
3,15
2,85
16
PIN 1 INDEX AREA
TOP AND BOTTOM
1

0,80
0,70
0,20 REF.
C
SEATING PLANE
0,08
0,05
0,00

16X 0,50
0,30
1
16
EXPOSED THERMAL PAD
D
16X 0,30
0,18
0,10 M C A B
0,05 M C
0,50

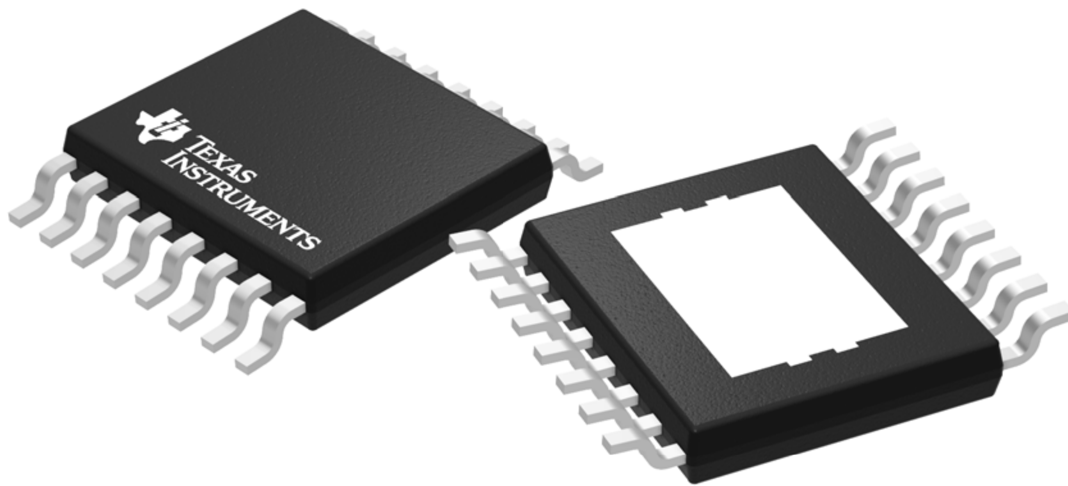
4205254/D 01/11



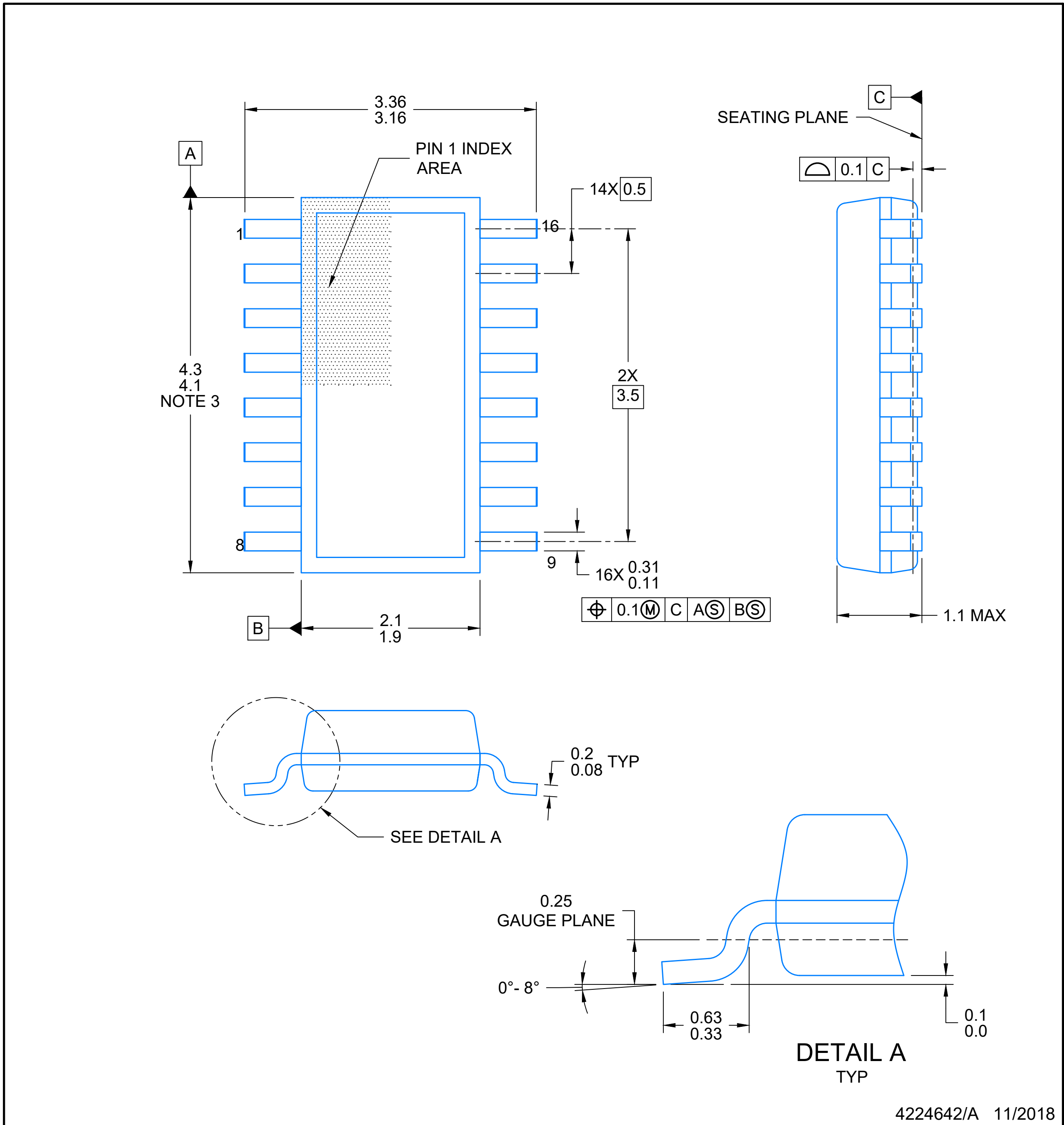
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

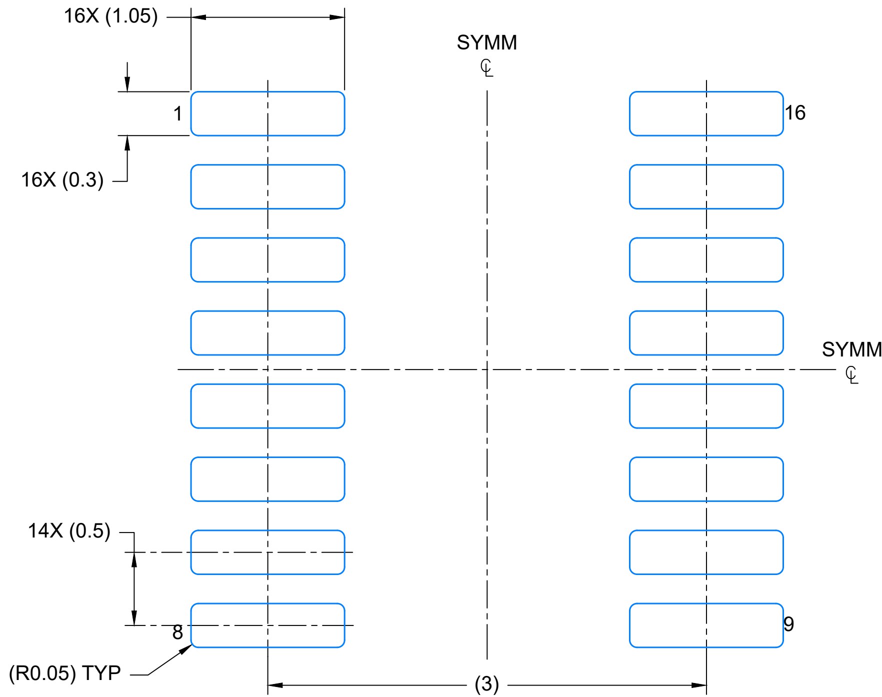


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

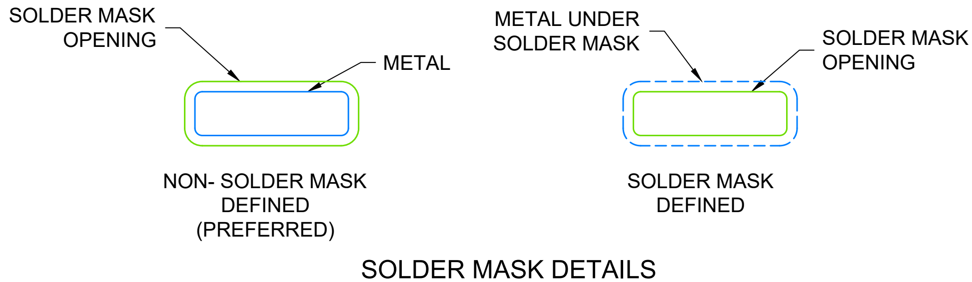


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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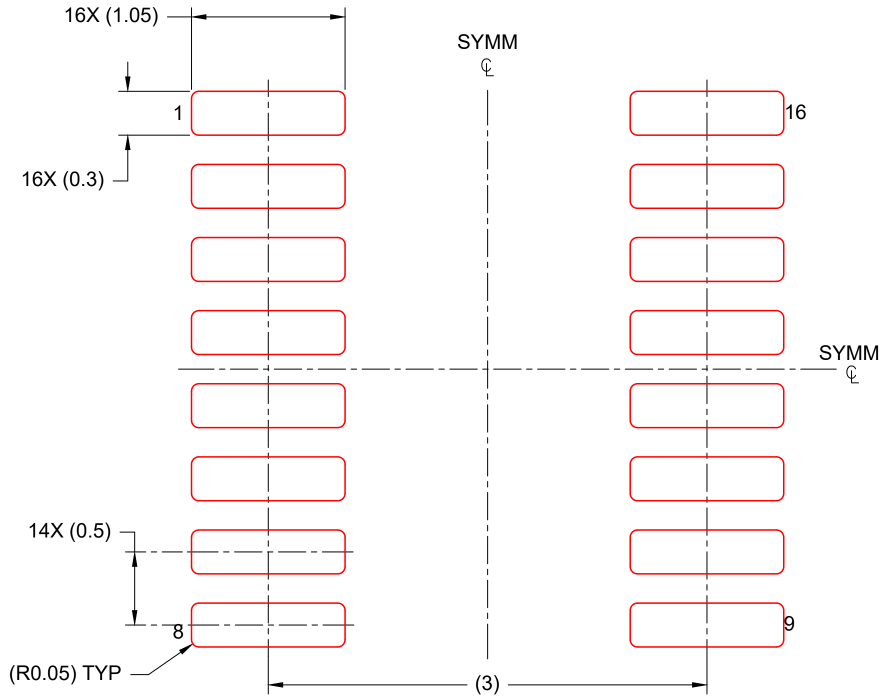
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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