DRV5055-Q1 Automotive Ratiometric Linear Hall Effect Sensor

1 Features

- Ratiometric Linear Hall Effect Magnetic Sensor
- Operates From 3.3-V and 5-V Power Supplies
- Analog Output With V_{CC} / 2 Quiescent Offset
- Magnetic Sensitivity Options (At V_{CC} = 5 V):
  - A1: 100 mV/mT, ±21-mT Range
  - A2: 50 mV/mT, ±42-mT Range
  - A3: 25 mV/mT, ±85-mT Range
  - A4: 12.5 mV/mT, ±169-mT Range
- Fast 20-kHz Sensing Bandwidth
- Low-Noise Output With ±1-mA Drive
- Compensation For Magnet Temperature Drift
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 0: –40°C to 150°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Standard Industry Packages:
  - Surface-Mount SOT-23
  - Through-Hole TO-92

2 Applications

- Automotive Position Sensing
- Brake, Acceleration, Clutch Pedals
- Torque Sensors, Gear Shifters
- Throttle Position, Height Leveling
- Powertrain and Transmission Components
- Absolute Angle Encoding
- Current Sensing

3 Description

The DRV5055-Q1 device is a linear Hall effect sensor that responds proportionally to magnetic flux density. The device can be used for accurate position sensing in a wide range of applications.

The device operates from 3.3-V or 5-V power supplies. When no magnetic field is present, the analog output drives half of V_{CC}. The output changes linearly with the applied magnetic flux density, and four sensitivity options enable maximal output voltage swing based on the needed sensing range. North and south magnetic poles produce unique voltages.

The device senses magnetic flux that is perpendicular to the top of the package, and the two package options provide different sensing directions.

The device uses a ratiometric architecture that can eliminate error from V_{CC} tolerance when the external analog-to-digital converter (ADC) uses the same V_{CC} for its reference. Additionally, the device features magnet temperature compensation to counteract how magnets drift, for linear performance across a wide –40°C to +150°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5055-Q1	SOT-23 (3)	2.92 mm × 1.30 mm
	TO-92 (3)	4.00 mm × 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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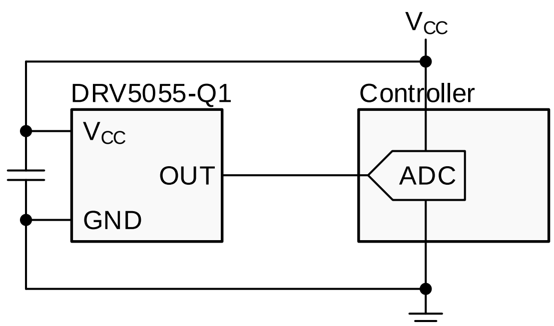
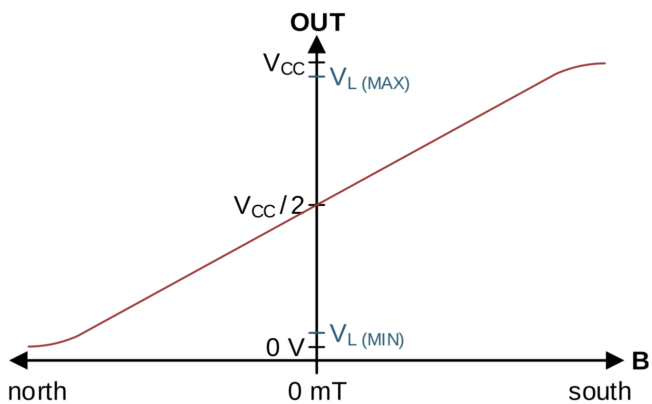
Typical Schematic



Magnetic Response



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2017) to Revision B — **Page**

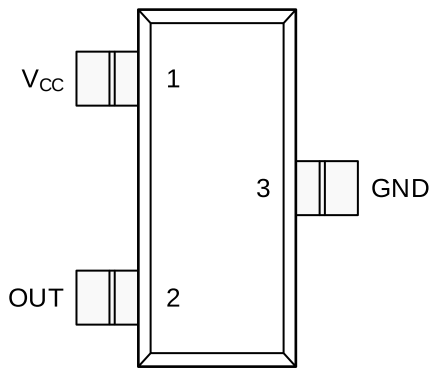
- Changed 5th, 6th, and 7th *Features* bullets ... 1
- Changed B_{ND}, B_N, V_N, and V_Q parameters of Electrical Characteristics table ... 3
- Changed specifications of $V_{Q\Delta T}$ and V_{QRE} parameters in *Electrical Characteristics* table ... 3
- Changed S_{RE} parameter test conditions and specifications in *Electrical Characteristics* table ... 3
- Changed description of V_{OUT} in *Magnetic Response* section ... 7
- Added equations to *Ratiometric Architecture* section ... 8
- Changed description of *Operating V_{CC} Ranges* section for clarity ... 9
- Changed *t_{ON} Definition* figure ... 9

Changes from Original (October 2017) to Revision A — **Page**

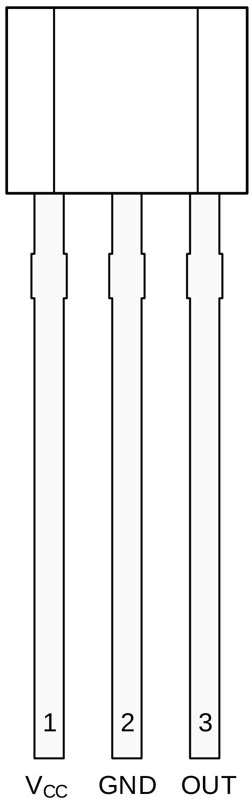
- Changed Applications section: condensed third and fourth bullets together to *Torque Sensors, Gear Shifters* ... 1
- Changed *Electrical Characteristics* table: changed f_{BW} parameter symbol and parameter name and changed V_N specifications, and added B_{ND}, B_N parameters ... 3
- Added footnotes to *Specification* section tables ... 3

5 Pin Configuration and Functions

DBZ Package
4-Pin SOT-23
Top View



LPG Package
3-Pin TO-92
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	TO-92		
V_{CC}	1	1	—	Power supply. TI recommends connecting this pin to a ceramic capacitor to ground with a value of at least 0.01 µF.
OUT	2	3	O	Analog output
GND	3	2	—	Ground reference

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–0.3	7	V
Output voltage	OUT	–0.3	V_{CC} + 0.3	V
Magnetic flux density, B_{MAX}		Unlimited		T
Operating junction temperature, T_J		–40	170	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	±3000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage[(1)]	3	3.63	V
		4.5	5.5	
I_O	Output continuous current	–1	1	mA
T_A	Operating ambient temperature[(2)]	–40	150	°C

(1) There are two isolated operating V_{CC} ranges. For more information see the Operating V_{CC} Ranges section.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC[(1)]		DRV5055-Q1		UNIT
		SOT-23 (DBZ)	TO-92 (LPG)	
		3 PINS	3 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	170	121	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	66	67	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	49	97	°C/W
Y_{JT}	Junction-to-top characterization parameter	1.7	7.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	48	97	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

for V_{CC} = 3 V to 3.63 V and 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[(1)]		MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current				6	10	mA
t_{ON}	Power-on time (see Figure 4)	B = 0 mT, no load on OUT			175	330	µs
f_{BW}	Sensing bandwidth				20		kHz
t_d	Propagation delay time	From change in B to change in OUT			10		µs
B_{ND}	Input-referred RMS noise density	V_{CC} = 5 V			130		$nT/\sqrt{Hz}$
		V_{CC} = 3.3 V			215		
B_N	Input-referred noise	$B_{ND} \times 6.6 \times \sqrt{20\ kHz}$	V_{CC} = 5 V		0.12		mT_{PP}
			V_{CC} = 3.3 V		0.2		
V_N	Output-referred noise[(2)]	$B_N \times S$	DRV5055A1		12		mV_{PP}
			DRV5055A2		6		
			DRV5055A3		3		
			DRV5055A4		1.5		

(1) B is the applied magnetic flux density.
(2) V_N describes voltage noise on the device output. If the full device bandwidth is not needed, noise can be reduced with an RC filter.

6.6 Magnetic Characteristics

for V_{CC} = 3 V to 3.63 V and 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_Q	Quiescent voltage	B = 0 mT, T_A = 25°C	V_{CC} = 5 V	2.43	2.5	2.57	V
			V_{CC} = 3.3 V	1.59	1.65	1.71	
$V_{Q\Delta T}$	Quiescent voltage temperature drift	B = 0 mT, T_A = -40°C to 150°C versus 25°C			±1% × V_{CC}		V
V_{QRE}	Quiescent voltage ratiometry error(2)				±0.1%		
S	Sensitivity	V_{CC} = 5 V, T_A = 25°C	DRV5055A1	95	100	105	mV/mT
			DRV5055A2	47.5	50	52.5	
			DRV5055A3	23.8	25	26.2	
			DRV5055A4	11.9	12.5	13.2	
		V_{CC} = 3.3 V, T_A = 25°C	DRV5055A1	57	60	63	
			DRV5055A2	28.5	30	31.5	
			DRV5055A3	14.3	15	15.8	
			DRV5055A4	7.1	7.5	7.9	
B_L	Linear magnetic sensing range(3)(4)	V_{CC} = 5 V, T_A = 25°C	DRV5055A1	±21			mT
			DRV5055A2	±42			
			DRV5055A3	±85			
			DRV5055A4	±169			
		V_{CC} = 3.3 V, T_A = 25°C	DRV5055A1	±22			
			DRV5055A2	±44			
			DRV5055A3	±88			
			DRV5055A4	±176			
V_L	Linear range of output voltage(4)			0.2		V_{CC} – 0.2	V
S_{TC}	Sensitivity temperature compensation for magnets(5)				0.12		%/°C
S_{LE}	Sensitivity linearity error(4)	V_{OUT} is within V_L			±1%		
S_{SE}	Sensitivity symmetry error(4)	V_{OUT} is within V_L			±1%		
S_{RE}	Sensitivity ratiometry error(2)	T_A = 25°C With respect to V_{CC} = 3.3 V or 5 V		–2.5%		2.5%	

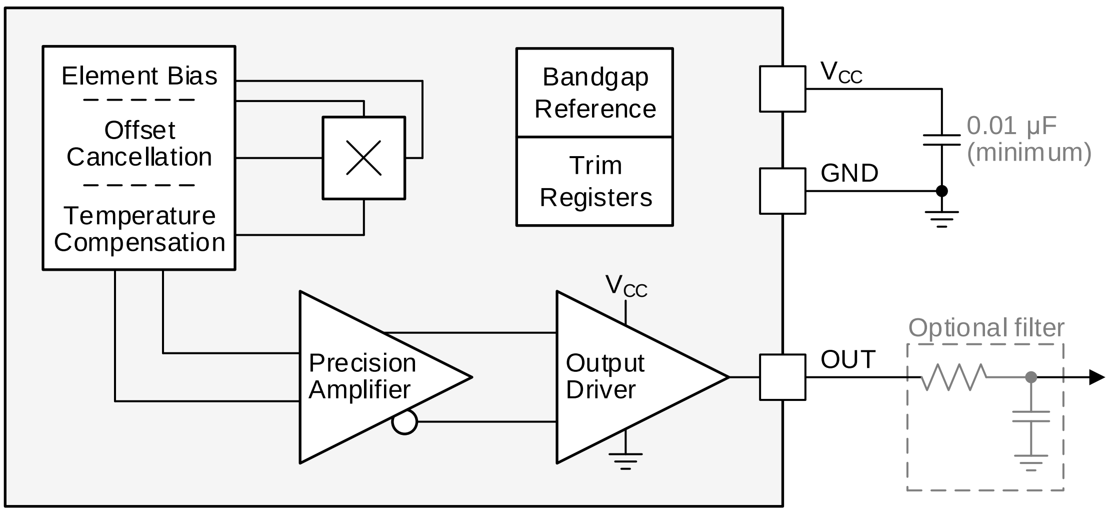
(1) B is the applied magnetic flux density.
(2) See the *Ratiometric Architecture* section.
(3) B_L describes the minimum linear sensing range at 25°C taking into account the maximum V_Q and Sensitivity tolerances.
(4) See the *Sensitivity Linearity* section.
(5) S_{TC} describes the rate the device increases Sensitivity with temperature. For more information, see the *Sensitivity Temperature Compensation For Magnets* section.

7 Detailed Description

7.1 Overview

The DRV5055-Q1 is a 3-pin linear Hall effect sensor with fully integrated signal conditioning, temperature compensation circuits, mechanical stress cancellation, and amplifiers. The device operates from 3.3-V and 5-V (±10%) power supplies, measures magnetic flux density, and outputs a proportional analog voltage that is referenced to V_{CC}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Magnetic Flux Direction

As shown in Figure 1, the DRV5055-Q1 is sensitive to the magnetic field component that is perpendicular to the top of the package.

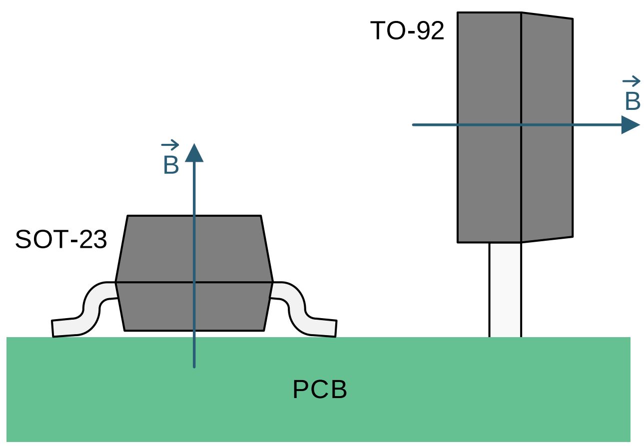


Figure 1. Direction of Sensitivity

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Feature Description (continued)

Magnetic flux that travels from the bottom to the top of the package is considered positive in this document. This condition exists when a south magnetic pole is near the top (marked-side) of the package. Magnetic flux that travels from the top to the bottom of the package results in negative millitesla values.

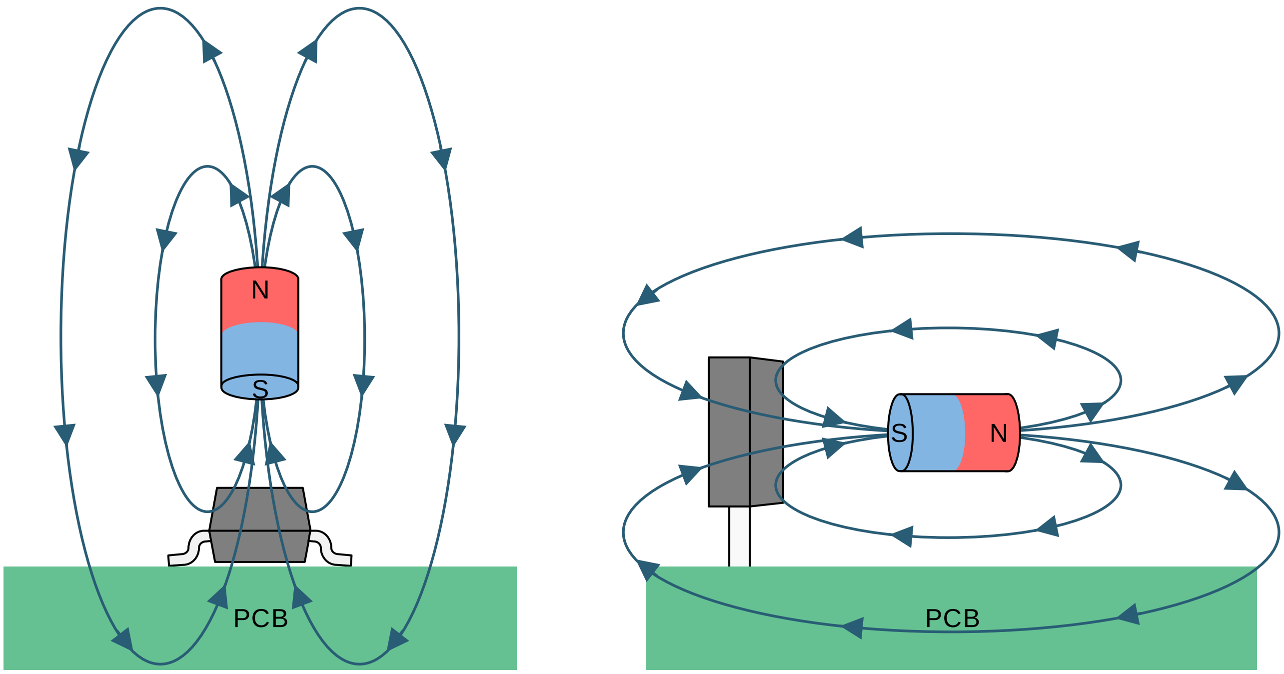

Figure 2. The Flux Direction for Positive B

7.3.2 Magnetic Response

When the DRV5055-Q1 is powered, the DRV5055-Q1 outputs an analog voltage according to Equation 1:

$$V_{OUT} = V_Q + B \times \left(\text{Sensitivity}_{(25°C)} \times (1 + S_{TC} \times (T_A - 25°C))\right)$$

where

- V_Q is typically half of V_{CC}
- B is the applied magnetic flux density
- $\text{Sensitivity}_{(25°C)}$ depends on the device option and V_{CC}
- S_{TC} is typically 0.12%/°C
- T_A is the ambient temperature
- V_{OUT} is within the V_L range (1)

As an example, consider the DRV5055A3 with V_{CC} = 3.3 V, a temperature of 50°C, and 67 mT applied. Excluding tolerances, V_{OUT} = 1650 mV + 67 mT × (15 mV/mT × (1 + 0.0012/°C × (50°C – 25°C))) = 2685 mV.

7.3.3 Sensitivity Linearity

The device produces a linear response when the output voltage is within the specified V_L range. Outside this range, sensitivity is reduced and nonlinear. Figure 3 graphs the magnetic response.

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Feature Description (continued)

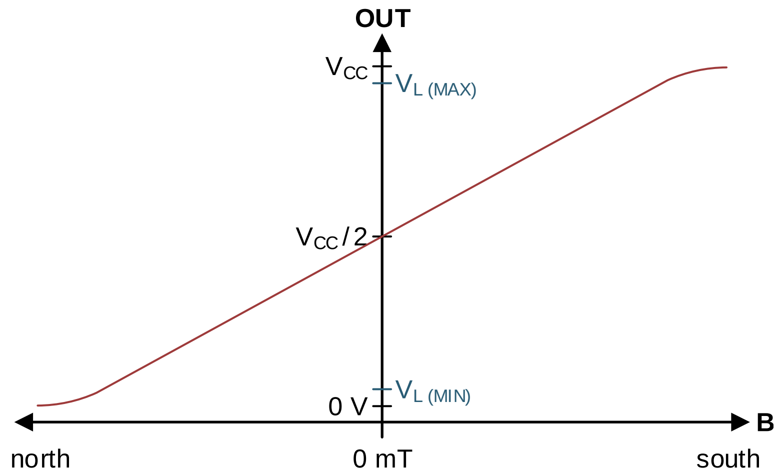

Figure 3. Magnetic Response

Equation 2 calculates parameter B_L, the minimum linear sensing range at 25°C taking into account the maximum quiescent voltage and sensitivity tolerances.

$$B_{L(MIN)} = \frac{V_{L(MAX)} - V_{Q(MAX)}}{S_{(MAX)}} \quad (2)$$

The parameter S_{LE} defines linearity error as the difference in sensitivity between any two positive B values, and any two negative B values, while the output is within the V_L range.

The parameter S_{SE} defines symmetry error as the difference in sensitivity between any positive B value and the negative B value of the same magnitude, while the output voltage is within the V_L range.

7.3.4 Ratiometric Architecture

The DRV5055-Q1 has a ratiometric analog architecture that scales the quiescent voltage and sensitivity linearly with the power-supply voltage. For example, the quiescent voltage and sensitivity are 5% higher when V_{CC} = 5.25 V compared to V_{CC} = 5 V. This behavior enables external ADCs to digitize a consistent value regardless of the power-supply voltage tolerance, when the ADC uses V_{CC} as its reference.

Equation 3 calculates sensitivity ratiometry error:

$$S_{RE} = 1 - \frac{S_{(VCC)} / S_{(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \qquad S_{RE} = 1 - \frac{S_{(VCC)} / S_{(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3 \text{ V to } 3.63 \text{ V}$$

where

- $S_{(VCC)}$ is the sensitivity at the current V_{CC} voltage
- $S_{(5V)}$ or $S_{(3.3V)}$ is the sensitivity when V_{CC} = 5 V or 3.3 V
- V_{CC} is the current V_{CC} voltage (3)

Equation 4 calculates quiescent voltage ratiometry error:

$$V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \qquad V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3 \text{ V to } 3.63 \text{ V}$$

where

- $V_{Q(VCC)}$ is the quiescent voltage at the current V_{CC} voltage
- $V_{Q(5V)}$ or $V_{Q(3.3V)}$ is the quiescent voltage when V_{CC} = 5 V or 3.3 V
- V_{CC} is the current V_{CC} voltage (4)

Feature Description (continued)

7.3.5 Operating V_{CC} Ranges

The DRV5055-Q1 has two recommended operating V_{CC} ranges: 3 V to 3.63 V and 4.5 V to 5.5 V. When V_{CC} is in the middle region between 3.63 V to 4.5 V, the device continues to function, but sensitivity is less known because there is a crossover threshold near 4 V that adjusts device characteristics.

7.3.6 Sensitivity Temperature Compensation For Magnets

Magnets generally produce weaker fields as temperature increases. The DRV5055-Q1 compensates by increasing sensitivity with temperature, as defined by the parameter S_{TC}. The sensitivity at T_A = 125°C is typically 12% higher than at T_A = 25°C.

7.3.7 Power-On Time

After the V_{CC} voltage is applied, the DRV5055-Q1 requires a short initialization time before the output is set. The parameter t_{ON} describes the time from when V_{CC} crosses 3 V until OUT is within 5% of V_Q, with 0 mT applied and no load attached to OUT. Figure 4 shows this timing diagram.

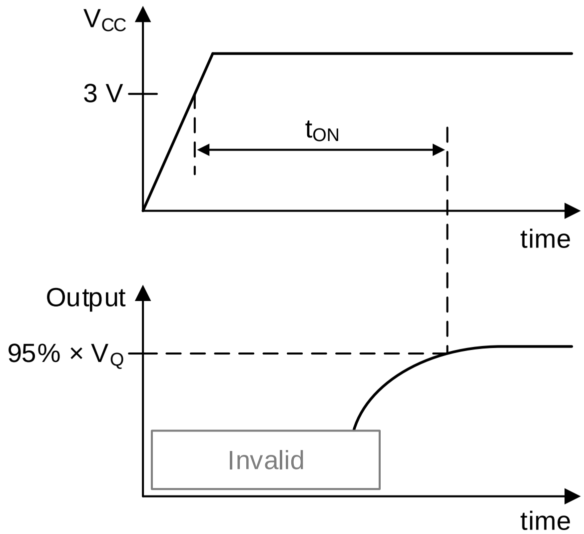

Figure 4. t_{ON} Definition

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Feature Description (continued)

7.3.8 Hall Element Location

Figure 5 shows the location of the sensing element inside each package option.

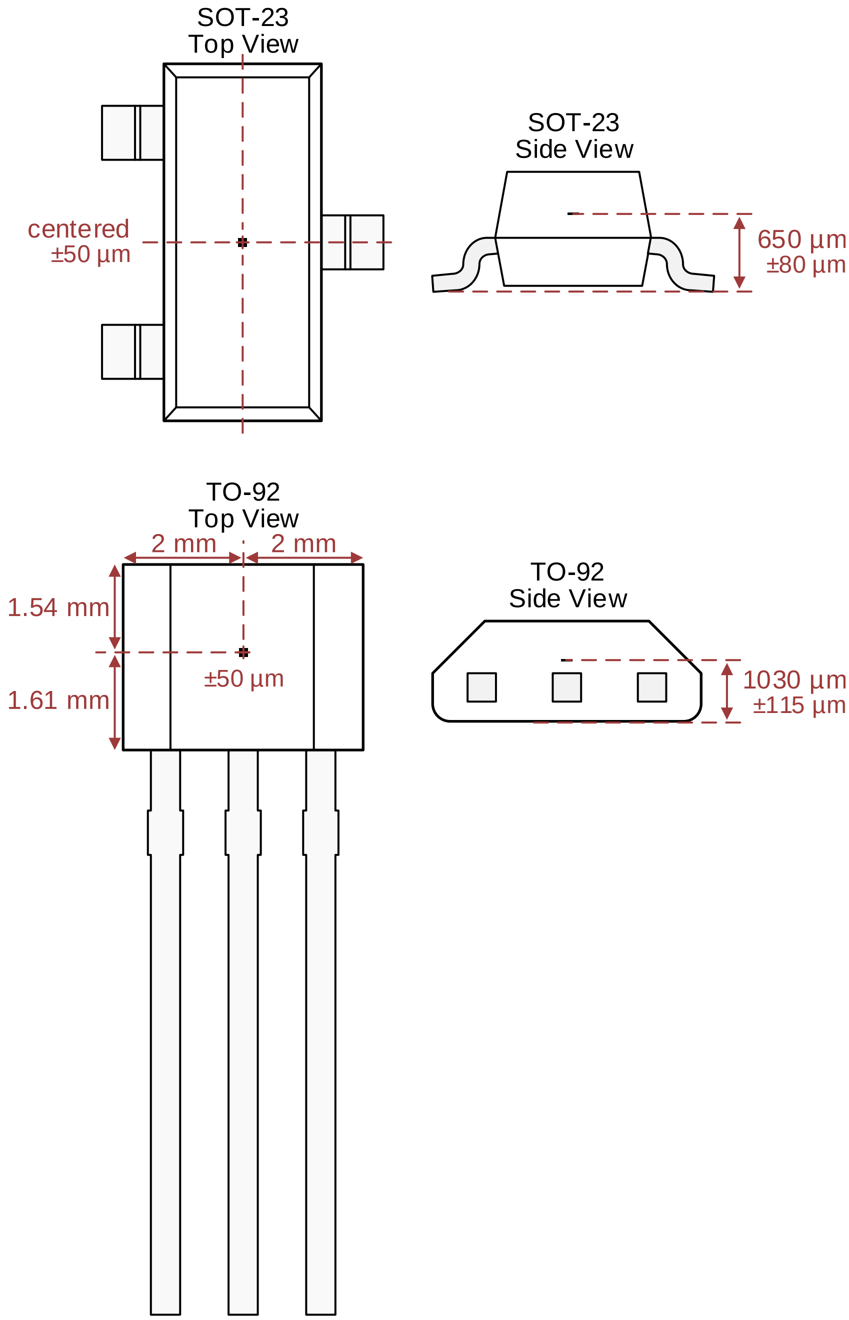

Figure 5. Hall Element Location

7.4 Device Functional Modes

The DRV5055-Q1 has one mode of operation that applies when the *Recommended Operating Conditions* are met.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Selecting the Sensitivity Option

Select the highest DRV5055-Q1 sensitivity option that can measure the required range of magnetic flux density, so that the output voltage swing is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances. This is because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations at http://www.ti.com/product/drv5013.

8.1.2 Temperature Compensation for Magnets

The DRV5055-Q1 temperature compensation is designed to directly compensate the average drift of neodymium (NdFeB) magnets and partially compensate ferrite magnets. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite. When the operating temperature of a system is reduced, temperature drift errors are also reduced.

8.1.3 Adding a Low-Pass Filter

As shown in the *Functional Block Diagram*, an RC low-pass filter can be added to the device output for the purpose of minimizing voltage noise when the full 20-kHz bandwidth is not needed. This filter can improve the signal-to-noise ratio (SNR) and overall accuracy. Do not connect a capacitor directly to the device output without a resistor in between because doing so can make the output unstable.

8.1.4 Designing for Wire Break Detection

Some systems must detect if interconnect wires become open or shorted. The DRV5055-Q1 can support this function.

First, select a sensitivity option that causes the output voltage to stay within the V_L range during normal operation. Second, add a pullup resistor between OUT and V_{CC}. TI recommends a value between 20 kΩ to 100 kΩ, and the current through OUT must not exceed the I_O specification, including current going into an external ADC. Then, if the output voltage is ever measured to be within 150 mV of V_{CC} or GND, a fault condition exists. Figure 6 shows the circuit, and Table 1 describes fault scenarios.

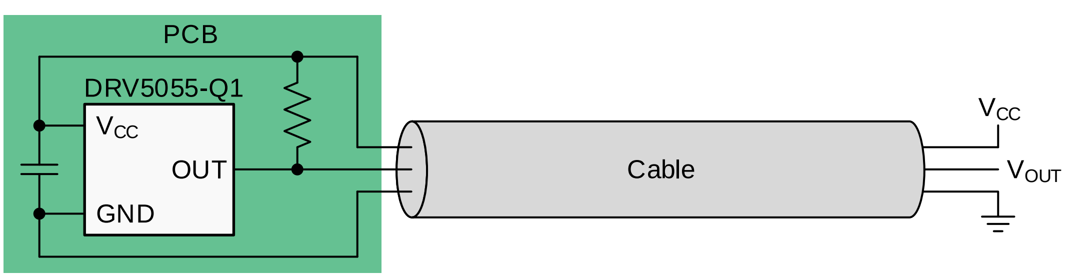

Figure 6. Wire Fault Detection Circuit

Table 1. Fault Scenarios and the Resulting V_{OUT}

FAULT SCENARIO	V_{OUT}
V_{CC} disconnects	Close to GND
GND disconnects	Close to V_{CC}
V_{CC} shorts to OUT	Close to V_{CC}
GND shorts to OUT	Close to GND

8.2 Typical Application

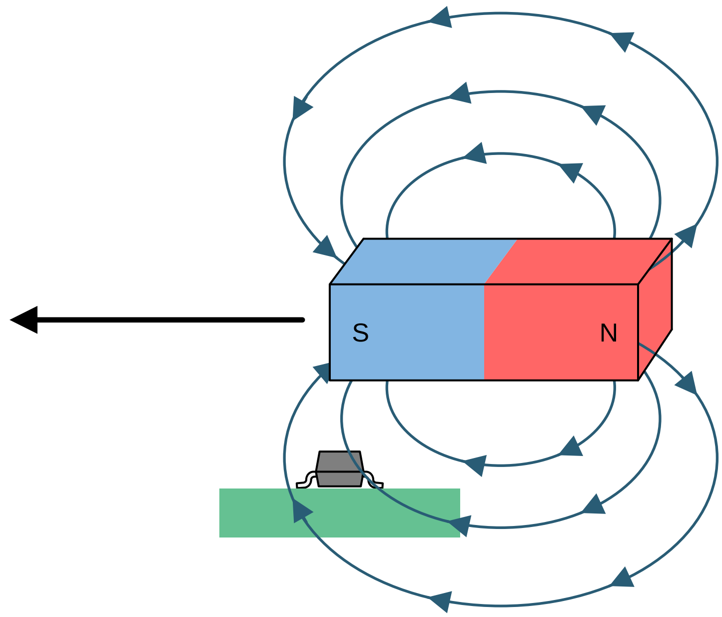

Figure 7. Common Magnet Orientation

8.2.1 Design Requirements

Use the parameters listed in Table 2 for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	5 V
Magnet	15 × 5 × 5 mm NdFeB
Travel distance	12 mm
Maximum B at the sensor at 25°C	±75 mT
Device option	DRV5055A3

8.2.2 Detailed Design Procedure

Linear Hall effect sensors provide flexibility in mechanical design, because many possible magnet orientations and movements produce a usable response from the sensor. Figure 7 shows one of the most common orientations, which uses the full north to south range of the sensor and causes a close-to-linear change in magnetic flux density as the magnet moves across.

To determine the maximum magnetic flux density the sensor will receive, TI recommends using magnetic field simulation software, referring to magnet specifications, and testing.

9 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF.

10 Layout

10.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed-circuit boards, which makes placing the magnet on the opposite side possible.

10.2 Layout Examples

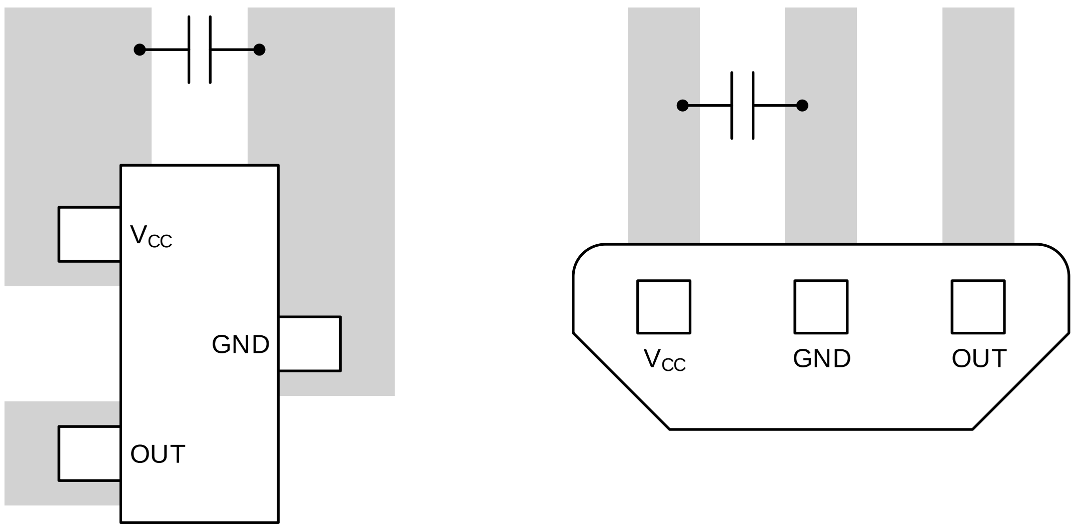

Figure 8. Layout Examples

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5055A1EDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 150	55A1Z	
DRV5055A1ELPGMQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A1ELPGQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A2EDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 150	55A2Z	
DRV5055A2ELPGMQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A2ELPGQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A3EDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 150	55A3Z	
DRV5055A3ELPGMQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A3ELPGQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A4EDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 150	55A4Z	
DRV5055A4ELPGMQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A4ELPGQ1	PREVIEW	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 150		
DRV5055A5EDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 150	55A5Z	
PDRV5055A1EDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A1ELPGQ1	ACTIVE	TO-92	LPG	3	1000	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A2EDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A3EDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A3ELPGQ1	ACTIVE	TO-92	LPG	3	1000	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A4EDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 150		Samples
PDRV5055A4ELPGQ1	ACTIVE	TO-92	LPG	3	1000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DRV5055-Q1 :

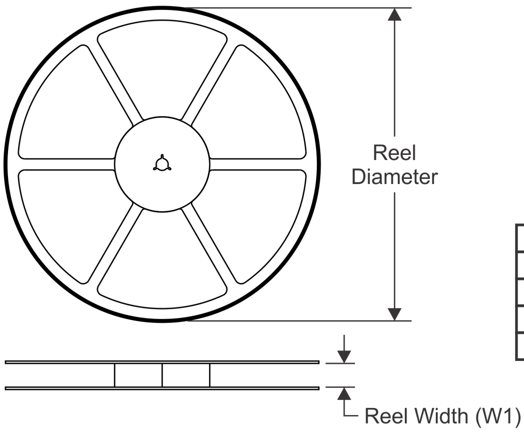
- Catalog: DRV5055

NOTE: Qualified Version Definitions:

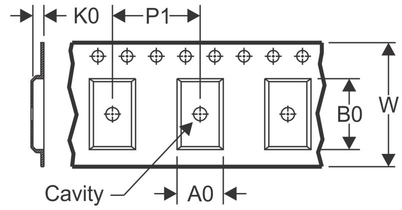
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

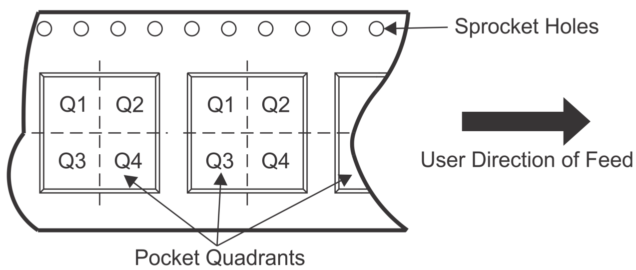


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

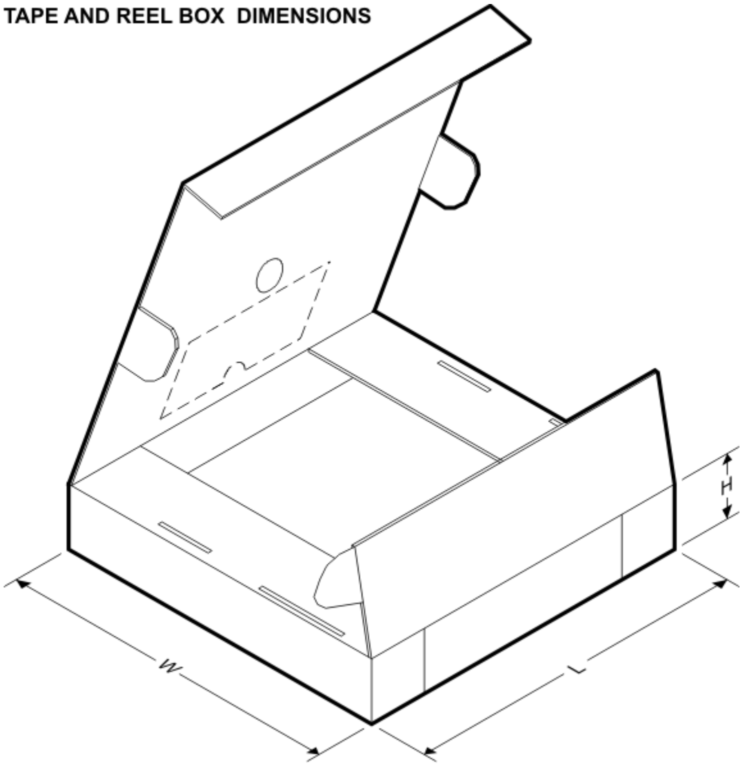
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

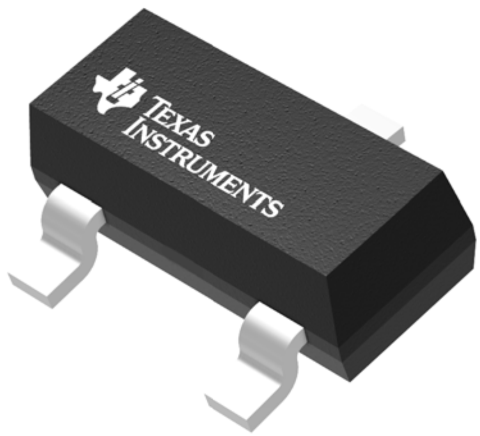
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5055A1EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A2EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A3EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A4EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

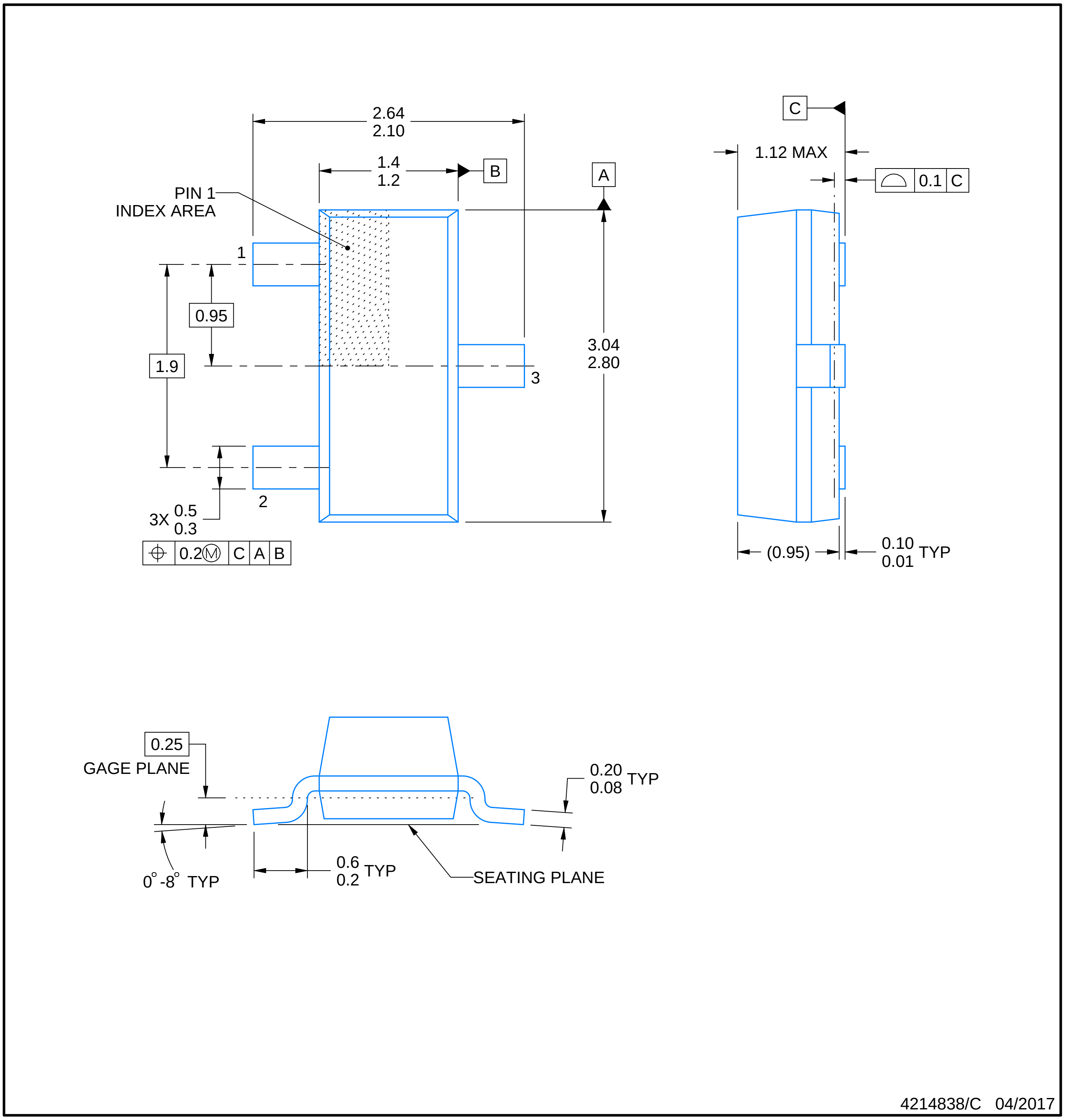


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5055A1EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A2EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A3EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A4EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0

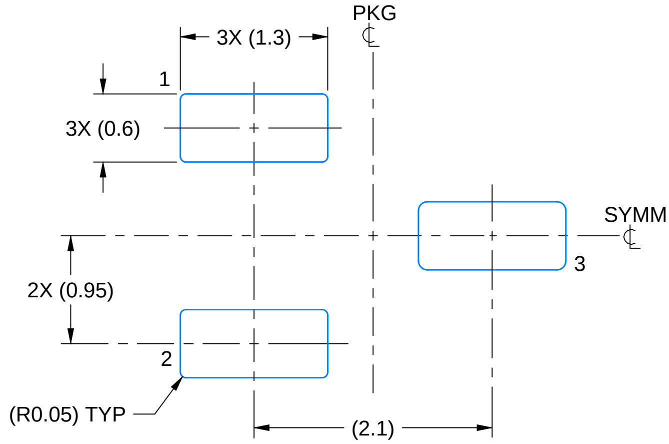


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

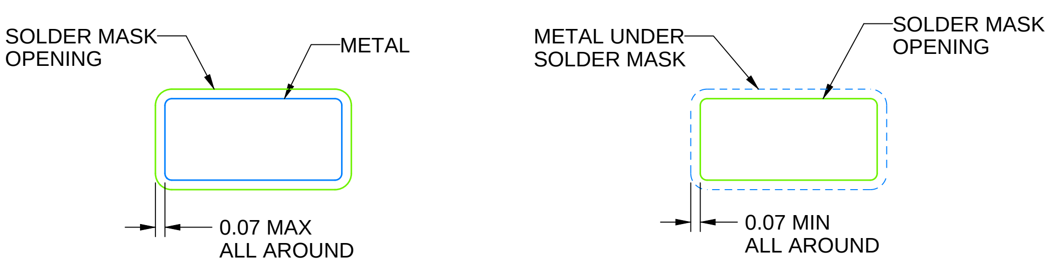


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

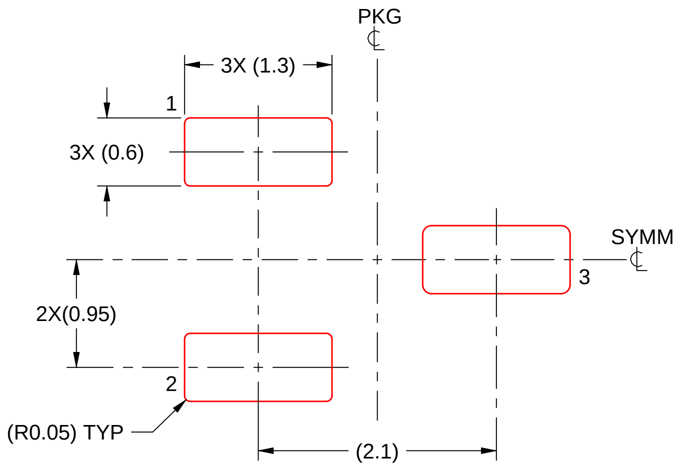
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

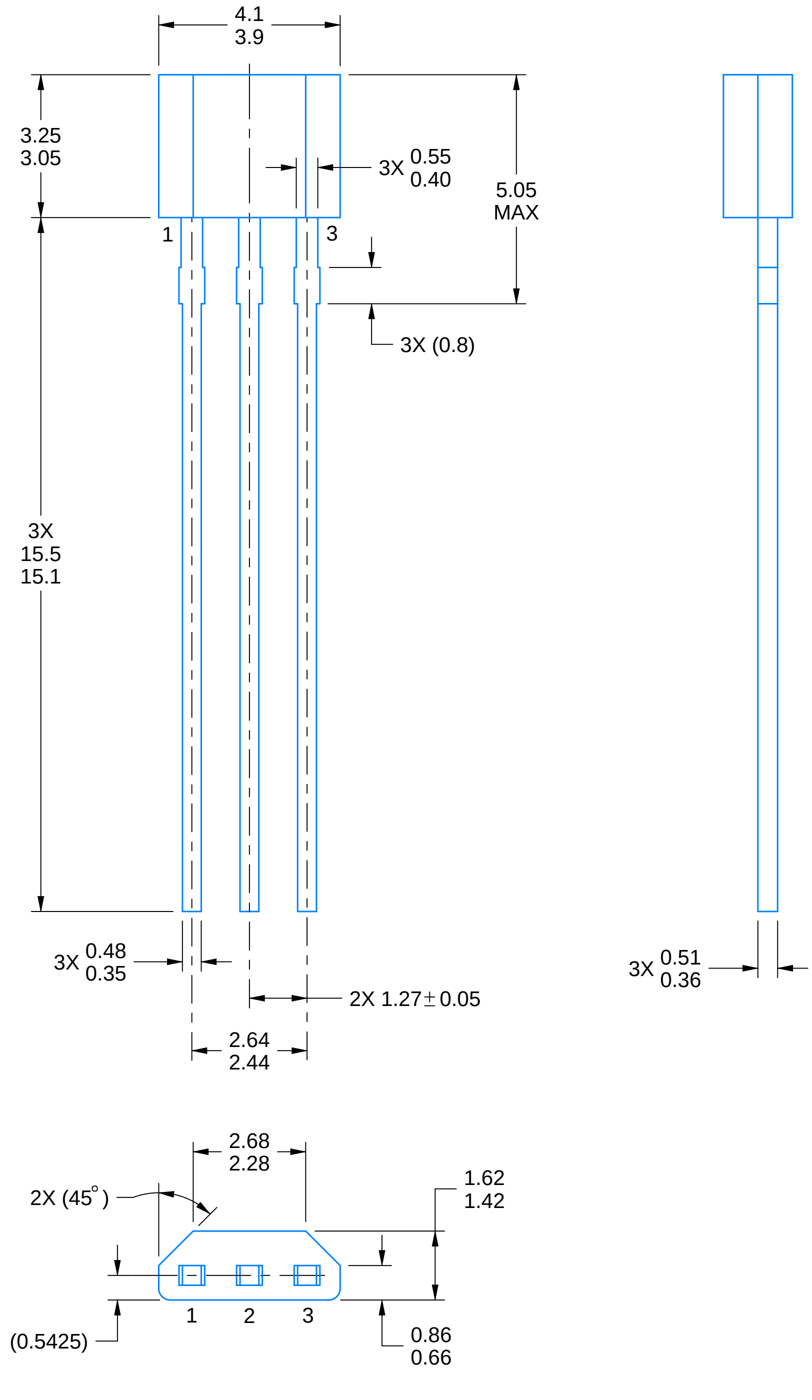


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

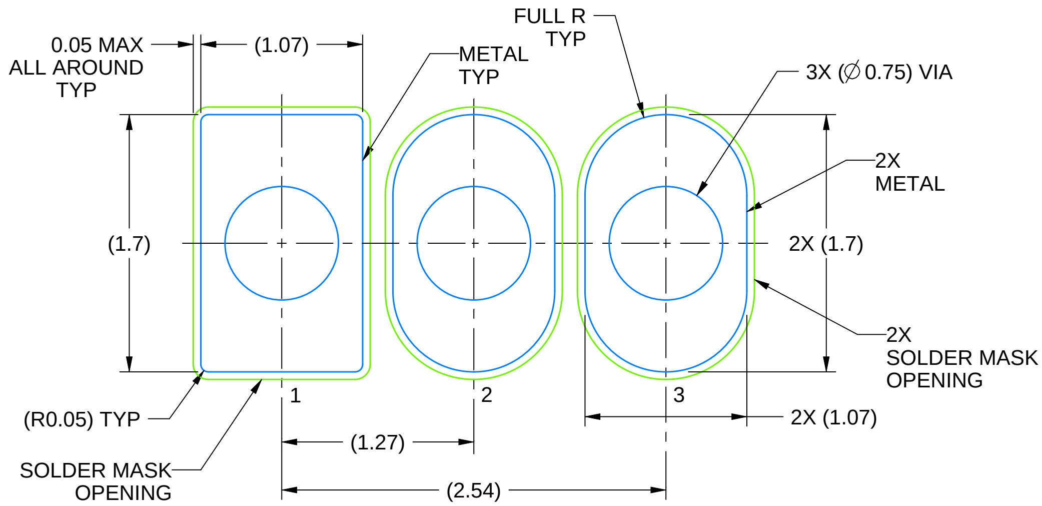
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

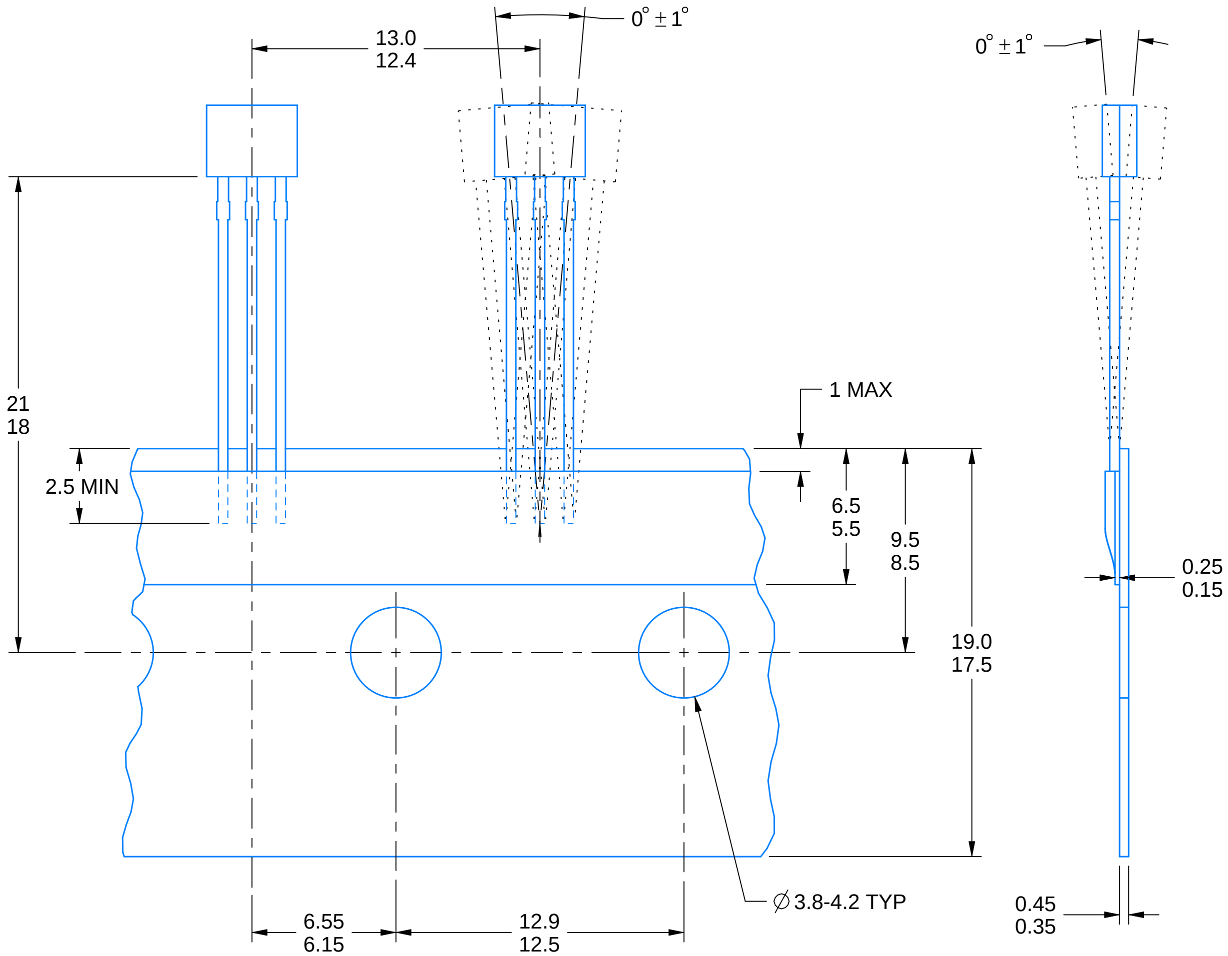


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X



4221343/C 01/2018

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