DP83849I PHYTER DUAL Industrial Temperature With Flexible Port Switching Dual Port 10/100 Mb/s Ethernet Physical Layer Transceiver

1 Device Overview

1.1 Features

- Low-power 3.3-V, 0.18-µm CMOS Technology
- Low power Consumption <600 mW Typical
- 3.3-V MAC Interface
- Auto-MDIX for 10/100 Mb/s
- Energy Detection Mode
- Flexible MII Port Assignment
- Dynamic Integrity Utility
- Dynamic Link Quality Monitoring
- TDR based Cable Diagnostic and Cable Length Detection
- Optimized Latency for Real-Time Ethernet Operation
- Reference Clock Out
- RMII Rev. 1.2 Interface (Configurable)
- SNI Interface (Configurable)
- MII Serial Management Interface (MDC and MDIO)
- IEEE 802.3u MII
- IEEE 802.3u Auto-Negotiation and Parallel Detection
- IEEE 802.3u ENDEC, 10BASE-T Transceivers and Filters
- IEEE 802.3u PCS, 100BASE-TX Transceivers and Filters
- IEEE 1149.1 JTAG
- Integrated ANSI X3.263 Compliant TP-PMD Physical Sub-layer with Adaptive Equalization and Baseline Wander Compensation
- Programmable LED Support for Link, 10/100 Mb/s Mode, Activity, Duplex and Collision Detect
- Single Register Access for Complete PHY Status
- 10/100 Mb/s Packet BIST (Built-In Self Test)
- 80-pin TQFP Package (12-mm × 12-mm)

1.2 Applications

- Medical Instrumentation
- Factory Automation
- Motor and Motion Control
- Wireless Remote Base Station
- General Embedded Applications

1.3 Description

The number of applications requiring Ethernet Connectivity continues to expand. Along with this increased market demand is a change in application requirements. Where single channel Ethernet used to be sufficient, many applications such as wireless remote base stations and industrial networking now require DUAL Port functionality for redundancy or system management.

The DP83849I is a highly reliable, feature rich device perfectly suited for industrial applications enabling Ethernet on the factory floor. The DP83849I features two fully independent 10/100 ports for multi-port applications. The unique port switching capability also allows the two ports to be configured to provide fully integrated range extension, media conversion, hardware based failover and port monitoring.

The DP83849I provides optimum flexibility in MPU selection by supporting both MII and RMII interfaces. In addition this device includes a powerful new diagnostics tool to ensure initial network operation and maintenance.

In addition to the TDR scheme, commonly used for detecting faults during installation, the innovative cable diagnostics provides for real time continuous monitoring of the link quality. This allows the system designer to implement a fault prediction mechanism to detect and warn of changing or deteriorating link conditions.

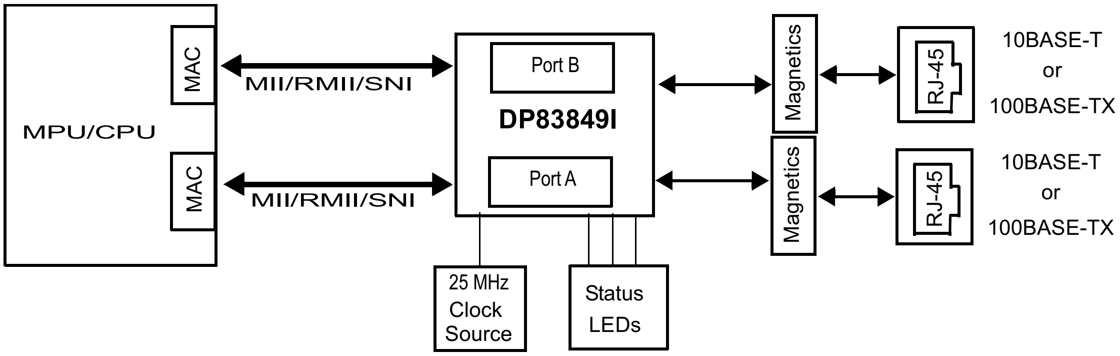
The DP83849I continues to build on its Ethernet expertise and leadership position by providing a powerful combination of features and flexibility, easing Ethernet implementation for the system designer.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
DP83849I	TQFP (80)	12.00 mm × 12.00 mm

(1) For more information, see Section 10, *Mechanical Packaging and Orderable Information*.

1.4 System Diagram



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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2008) to Revision F	Page
• Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

3 Terminal Configuration and Functions

The DP83849I pins are classified into the following interface categories (each interface is described in the sections that follow):

- Serial Management Interface
- MAC Data Interface
- Clock Interface
- LED Interface
- JTAG Interface
- Reset and Power Down
- Strap Options
- 10/100 Mb/s PMD Interface
- Special Connect Pins
- Power and Ground pins

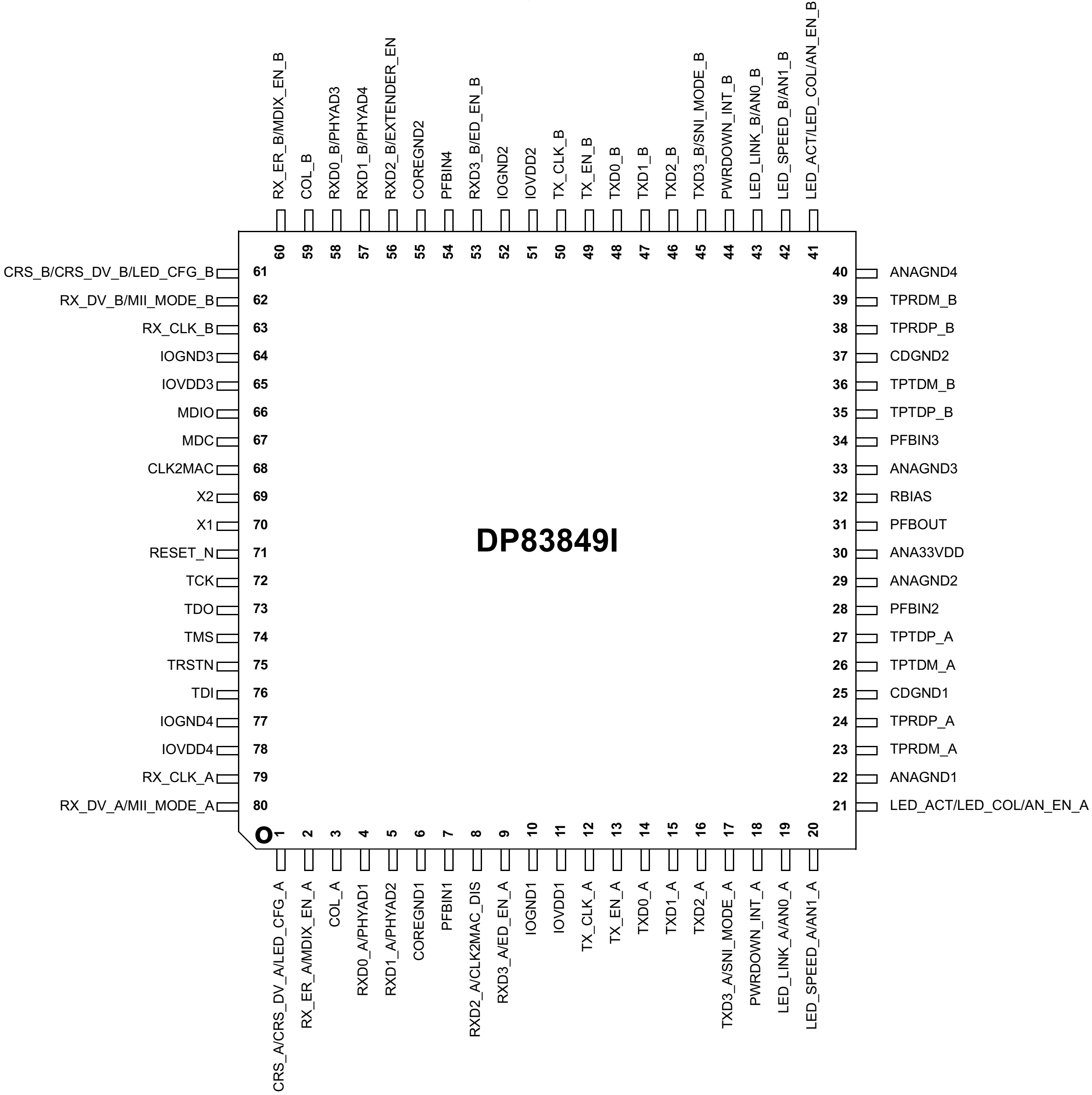
NOTE

Strapping pin option. See *Section 3.2.7* for strap definitions.

All DP83849I signal pins are I/O cells regardless of the particular use. The following definitions define the functionality of the I/O cells for each pin.

Type: I	Input
Type: O	Output
Type: I/O	Input/Output
Type OD	Open Drain
Type: PD, PU	Internal Pulldown/Pullup
Type: S	Strapping Pin (All strap pins have weak internal pullups or pulldowns. If the default strap value is to be changed then an external 2.2-kΩ resistor must be used. See Section 3.2.7 for details.)

PFC Package
80-Pin TQFP
Top View



3.1 Pin Assignments

PIN NO.	NAME		PIN NO.	NAME
1	CRS_A/CRS_DV_A/LED_CFG_A		41	LED_ACT/LED_COL/AN_EN_B
2	RX_ER_A/MDIX_EN_A		42	LED_SPEED_B/AN1_B
3	COL_A		43	LED_LINK_B/AN0_B
4	RXD0_A/PHYAD1		44	PWRDOWN_INT_B
5	RXD1_A/PHYAD2		45	TXD3_B/SNI_MODE_B
6	COREGND1		46	TXD2_B
7	PFBIN1		47	TXD1_B
8	RXD2_A/CLK2MAC_DIS		48	TXD0_B
9	RXD3_A/ED_EN_A		49	TX_EN_B
10	IOGND1		50	TX_CLK_B
11	IOVDD1		51	IOVDD2
12	TX_CLK_A		52	IOGND2
13	TX_EN_A		53	RXD3_B/ED_EN_B
14	TXD0_A		54	PFBIN4
15	TXD1_A		55	COREGND2
16	TXD2_A		56	RXD2_B/EXTENDER_EN
17	TXD3_A/SNI_MODE_A		57	RXD1_B/PHYAD4
18	PWRDOWN_INT_A		58	RXD0_B/PHYAD3
19	LED_LINK_A/AN0_A		59	COL_B
20	LED_SPEED_A/AN1_A		60	RX_ER_B/MDIX_EN_B
21	LED_ACT/LED_COL/AN_EN_A		61	CRS_B/CRS_DV_B/LED_CFG_B
22	ANAGND1		62	RX_DV_B/MII_MODE_B
23	TPRDM_A		63	RX_CLK_B
24	TPRDP_A		64	IOGND3
25	CDGND1		65	IOVDD3
26	TPTDM_A		66	MDIO
27	TPTDP_A		67	MDC
28	PFBIN2		68	CLK2MAC
29	ANAGND2		69	X2
30	ANA33VDD		70	X1
31	PFBOUT		71	RESET_N
32	RBIAS		72	TCK
33	ANAGND3		73	TDO
34	PFBIN3		74	TMS
35	TPTDP_B		75	TRSTN
36	TPTDM_B		76	TDI
37	CDGND2		77	IOGND4
38	TPRDP_B		78	IOVDD4
39	TPRDM_B		79	RX_CLK_A
40	ANAGND4		80	RX_DV_A/MII_MODE_A

3.2 Signal Descriptions

3.2.1 Serial Management Interface

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
MDC	I	67	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 25 MHz with no minimum clock rate.
MDIO	I/O	66	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 1.5-kΩ pullup resistor.

3.2.2 Clock Interface

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
X1	I	70	**CRYSTAL/OSCILLATOR INPUT:** This pin is the primary clock reference input for the DP83849I and must be connected to a 25 MHz 0.005% (+50 ppm) clock source. The DP83849I supports either an external crystal resonator connected across pins X1 and X2, or an external CMOS-level oscillator source connected to pin X1 only. **RMII REFERENCE CLOCK:** This pin is the primary clock reference input for the RMII mode and must be connected to a 50-MHz 0.005% (+50 ppm) CMOS-level oscillator source.
X2	O	69	**CRYSTAL OUTPUT:** This pin is the primary clock reference output to connect to an external 25 MHz crystal resonator device. This pin must be left unconnected if an external CMOS oscillator clock source is used.
CLK2MAC	O	68	**CLOCK TO MAC:** In MII mode, this pin provides a 25-MHz clock output to the system. In RMII mode, this pin provides a 50-MHz clock output to the system. This allows other devices to use the reference clock from the DP83849I without requiring additional clock sources. If the system does not require the CLK2MAC signal, the CLK2MAC output must be disabled through the CLK2MAC disable strap.

3.2.3 MAC Data Interface

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
TX_CLK_A	O	12	**MII TRANSMIT CLOCK:** 25-MHz Transmit clock output in 100-Mb/s mode or 2.5 MHz in 10-Mb/s mode derived from the 25-MHz reference clock. Unused in RMII mode. The device uses the X1 reference clock input as the 50-MHz reference for both transmit and receive. **SNI TRANSMIT CLOCK:** 10-MHz Transmit clock output in 10-Mb/s SNI mode. The MAC must source TX_EN and TXD_0 using this clock.
TX_CLK_B		50	
TX_EN_A	I	13	**MII TRANSMIT ENABLE:** Active high input indicates the presence of valid data inputs on TXD[3:0]. **RMII TRANSMIT ENABLE:** Active high input indicates the presence of valid data on TXD[1:0]. **SNI TRANSMIT ENABLE:** 10-MHz Transmit clock output in 10-Mb/s SNI mode. The MAC must source TX_EN and TXD_0 using this clock.
TX_EN_B		49	
TXD[3:0]_A	I	17, 16, 15, 14	**MII TRANSMIT DATA:** Transmit data MII input pins, TXD[3:0], that accept data synchronous to the TX_CLK (2.5 MHz in 10 Mb/s mode or 25 MHz in 100 Mb/s mode). **RMII TRANSMIT DATA:** Transmit data RMII input pins, TXD[1:0], that accept data synchronous to the 50-MHz reference clock. **SNI TRANSMIT DATA:** Transmit data SNI input pin, TXD_0, that accept data synchronous to the TX_CLK (10 MHz in 10 Mb/s SNI mode).
TXD[3:0]_B		45, 46, 47, 48	
RX_CLK_A	O	79	**MII RECEIVE CLOCK:** Provides the 25-MHz recovered receive clocks for 100 Mb/s mode and 2.5 MHz for 10 Mb/s mode. Unused in RMII mode. The device uses the X1 reference clock input as the 50-MHz reference for both transmit and receive. **SNI RECEIVE CLOCK:** Provides the 10-MHz recovered receive clocks for 10 Mb/s SNI mode.
RX_CLK_B		63	

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
RX_DV_A	O	80	**MII RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on the corresponding RXD[3:0].
RX_DV_B		62	**RMII RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on the corresponding RXD[1:0]. This signal is not required in RMII mode, because CRS_DV includes the RX_DV signal, but is provided to allow simpler recovery of the Receive data. This pin is not used in SNI mode.
RX_ER_A	O	2	**MII RECEIVE ERROR:** Asserted high synchronously to RX_CLK to indicate that an invalid symbol has been detected within a received packet in 100 Mb/s mode.
RX_ER_B		60	**RMII RECEIVE ERROR:** Asserted high synchronously to X1 whenever an invalid symbol is detected, and CRS_DV is asserted in 100 Mb/s mode. This pin is also asserted on detection of a False Carrier event. This pin is not required to be used by a MAC in RMII mode, because the Phy is required to corrupt data on a receive error. This pin is not used in SNI mode.
RXD[3:0]_A	O	9, 8, 5, 4	**MII RECEIVE DATA:** Nibble wide receive data signals driven synchronously to the RX_CLK, 25 MHz for 100 Mb/s mode, 2.5 MHz for 10 Mb/s mode). RXD[3:0] signals contain valid data when RX_DV is asserted.
RXD[3:0]_B		53, 56, 57, 58	**RMII RECEIVE DATA:** 2-bits receive data signals, RXD[1:0], driven synchronously to the X1 clock, 50 MHz. **SNI RECEIVE DATA:** Receive data signal, RXD_0, driven synchronously to the RX_CLK. RXD_0 contains valid data when CRS is asserted. RXD[3:1] are not used in this mode.
CRS_A/CRS_DV_A	O	1	**MII CARRIER SENSE:** Asserted high to indicate the receive medium is non-idle.
CRS_B/CRS_DV_B		61	**RMII CARRIER SENSE/RECEIVE DATA VALID:** This signal combines the RMII Carrier and Receive Data Valid indications. For a detailed description of this signal, see *Section 4.6*. **SNI CARRIER SENSE:** Asserted high to indicate the receive medium is non-idle. It is used to frame valid receive data on the RXD_0 signal.
COL_A	O	3	**MII COLLISION DETECT:** Asserted high to indicate detection of a collision condition (simultaneous transmit and receive activity) in 10 Mb/s and 100 Mb/s Half Duplex Modes.
COL_B		59	While in 10BASE-T Half Duplex mode with heartbeat enabled this pin is also asserted for a duration of approximately 1µs at the end of transmission to indicate heartbeat (SQE test). In Full Duplex Mode, for 10 Mb/s or 100 Mb/s operation, this signal is always logic 0. There is no heartbeat function during 10 Mb/s full duplex operation. **RMII COLLISION DETECT:** Per the RMII Specification, no COL signal is required. The MAC will recover CRS from the CRS_DV signal and use that along with its TX_EN signal to determine collision. **SNI COLLISION DETECT:** Asserted high to indicate detection of a collision condition (simultaneous transmit and receive activity) in 10 Mb/s SNI mode.

3.2.4 LED Interface

The DP83849I supports three configurable LED pins. The LEDs support two operational modes that are selected by the LED mode strap and a third operational mode that is register configurable. The definitions for the LEDs for each mode are detailed in the following table. Because the LEDs are also used as strap options, the polarity of the LED output is dependent on whether the pin is pulled up or down.

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
LED_LINK_A	I/O	19	**LINK LED:** In Mode 1, this pin indicates the status of the LINK. The LED will be ON when Link is good.
LED_LINK_B		43	**LINK/ACT LED:** In Mode 2 and Mode 3, this pin indicates transmit and receive activity in addition to the status of the Link. The LED will be ON when Link is good. It will blink when the transmitter or receiver is active.
LED_SPEED_A	I/O	20	**SPEED LED:** The LED is ON when device is in 100 Mb/s and OFF when in 10 Mb/s. Functionality of this LED is independent of mode selected.
LED_SPEED_B		42	
LED_ACT/LED_COL_A	I/O	21	**ACTIVITY LED:** In Mode 1, this pin is the Activity LED which is ON when activity is present on either Transmit or Receive.
LED_ACT/LED_COL_B		41	**COLLISION/DUPLEX LED:** In Mode 2, this pin by default indicates Collision detection. For Mode 3, this LED output may be programmed to indicate Full-duplex status instead of Collision.

3.2.5 JTAG Interface

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
TCK	I, PU	72	**TEST CLOCK:** This pin has a weak internal pullup.
TDO	O	73	**TEST OUTPUT:**
TMS	I, PU	74	**TEST MODE SELECT: This pin has a weak internal pullup.**
TRSTN	I, PU	75	**TEST RESET Active low test reset.** This pin has a weak internal pullup.
TDI	I, PU	76	**TEST DATA INPUT:** This pin has a weak internal pullup.

3.2.6 Reset and Power Down

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
RESET_N	I, PU	71	**RESET:** Active Low input that initializes or re-initializes the DP83849I. Asserting this pin low for at least 1 µs will force a reset process to occur. All internal registers will re-initialize to their default states as specified for each bit in the Register Block section. All strap options are re-initialized as well.
PWRDOWN_INT_A	I, PU	18	The default function of this pin is POWER DOWN.
PWRDOWN_INT_B		44	**POWER DOWN:** The pin is an active low input in this mode and must be asserted low to put the device in a Power Down mode.
			INTERRUPT: The pin is an open drain output in this mode and will be asserted low when an interrupt condition occurs. Although the pin has a weak internal pullup, some applications may require an external pullup resister. Register access is required for the pin to be used as an interrupt mechanism. See *Section 6.2.4.2* for more details on the interrupt mechanisms.

3.2.7 Strap Options

The DP83849I uses many of the functional pins as strap options. The values of these pins are sampled during reset and used to strap the device into specific modes of operation. The strap option pin assignments are defined below. The functional pin name is indicated in parentheses.

A 2.2-kΩ resistor must be used for pulldown or pullup to change the default strap option. If the default option is required, then there is no need for external pullup or pull down resistors. Because these pins may have alternate functions after reset is deasserted, they must not be connected directly to VCC or GND.

<table>
<tr><th>SIGNAL NAME</th><th>TYPE</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>PHYAD1 (RXD0_A)</td><td rowspan="4">S, O, PD</td><td>4</td><td rowspan="4">PHY ADDRESS [4:1]: The DP83849I provides four PHY address pins, the state of which are latched into the PHYCTRL register at system Hardware-Reset. Phy Address[0] selects between ports A and B.
The DP83849I supports PHY Address strapping for Port A even values 0 (<0000_0>) through 30 (<1111_0>). Port B will be strapped to odd values 1 (<0000_1>) through 31 (<1111_1>).
PHYAD[4:1] pins have weak internal pulldown resistors.</td></tr>
<tr><td>PHYAD2 (RXD1_A)</td><td>5</td></tr>
<tr><td>PHYAD3 (RXD0_B)</td><td>58</td></tr>
<tr><td>PHYAD4 (RXD1_B)</td><td>57</td></tr>
<tr><td>AN_EN (LED_ACT/LED_COL_A)</td><td rowspan="7">S, O, PU</td><td>21</td><td rowspan="7">Auto-Negotiation Enable: When high, this enables Auto-Negotiation with the capability set by AN0 and AN1 pins. When low, this puts the part into Forced Mode with the capability set by AN0 and AN1 pins.
AN0 / AN1: These input pins control the forced or advertised operating mode of the DP83849I according to the following table. The value on these pins is set by connecting the input pins to GND (0) or VCC (1) through 2.2-kΩ resistors. These pins must NEVER be connected directly to GND or VCC.
The value set at this input is latched into the DP83849I at Hardware-Reset.
The float/pulldown status of these pins are latched into the Basic Mode Control Register and the Auto_Negotiation Advertisement Register during Hardware-Reset.
The default is 111 because these pins have internal pullups.
<table>
<tr><th>AN_EN</th><th>AN1</th><th>AN0</th><th>Forced Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>10BASE-T, Half-Duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10BASE-T, Full-Duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100BASE-TX, Half-Duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>100BASE-TX Full-Duplex</td></tr>
<tr><th>AN_EN</th><th>AN1</th><th>AN0</th><th>Advertised Mode</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10BASE-T, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>100BASE-TX, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>10BASE-T, Half-Duplex
100BASE-TX, Half-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>10BASE-T, Half/Full-Duplex
100BASE-TX, Half/Full-Duplex</td></tr>
</table></td></tr>
<tr><td>AN1_A (LED_SPEED_A)</td><td>20</td></tr>
<tr><td>AN0_A (LED_LINK_A)</td><td>19</td></tr>
<tr><td>AN_EN (LED_ACT/LED_COL_B)</td><td>41</td></tr>
<tr><td>AN1_B (LED_SPEED_B)</td><td>42</td></tr>
<tr><td>AN0_B (LED_LINK_B)</td><td>43</td></tr>
<tr><td></td><td></td></tr>
<tr><td>MII_MODE_A (RX_DV_A)</td><td rowspan="5">S, O, PD</td><td>80</td><td rowspan="5">MII MODE SELECT: This strapping option pair determines the operating mode of the MAC Data Interface. Default operation (No pullups) will enable normal MII Mode of operation. Strapping MII_MODE high will cause the device to be in RMII or SNI modes of operation, determined by the status of the SNI_MODE strap. Because the pins include internal pulldowns, the default values are 0. Both MAC Data Interfaces must have their RMII Mode settings the same; that is, both in RMII mode or both not in RMII mode
The following table details the configurations:
<table>
<tr><th>MII_MODE</th><th>SNI_MODE</th><th>MAC Interface Mode</th></tr>
<tr><td>0</td><td>X</td><td>MII Mode</td></tr>
<tr><td>1</td><td>0</td><td>RMII Mode</td></tr>
<tr><td>1</td><td>1</td><td>10-Mb/s SNI mode</td></tr>
</table></td></tr>
<tr><td>SNI_MODE_A (TXD3_A)</td><td>17</td></tr>
<tr><td>MII_MODE_B (RX_DV_B)</td><td>62</td></tr>
<tr><td>SNI_MODE_B (TXD3_B)</td><td>45</td></tr>
<tr><td></td><td></td></tr>
</table>

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
LED_CFG_A (CRS_A/CRS_DV_A)	S, O, PU	1	**LED CONFIGURATION:** This strapping option determines the mode of operation of the LED pins. Default is Mode 1. Mode 1 and Mode 2 can be controlled through the strap option. All modes are configurable through register access. See Table 5-2 for LED Mode Selection.
LED_CFG_B (CRS_B/CRS_DV_B)		61	
MDIX_EN_A (RX_ER_A)	S, O, PU	2	**MDIX ENABLE:** Default is to enable MDIX. This strapping option disables Auto-MDIX. An external pulldown will disable AutoMDIX mode.
MDIX_EN_B (RX_ER_B)		60	
ED_EN_A (RXD3_A)	S, O, PD	9	**Energy Detect ENABLE:** Default is to disable Energy Detect mode. This strapping option enables Energy Detect mode for the port. In Energy Detect mode, the device will initially be in a low-power state until detecting activity on the wire. An external pullup will enable Energy Detect mode.
ED_EN_B (RXD3_B)		53	
CLK2MAC_DIS (RXD2_A)	S, O, PD	8	**Clock to MAC Disable:** This strapping option disables (floats) the CLK2MAC pin. Default is to enable CLK2MAC output. An external pullup will disable (float) the CLK2MAC pin. If the system does not require the CLK2MAC signal, the CLK2MAC output must be disabled through this strap option.
EXTENDER_EN (RXD2_B)	S, O, PD	56	**Extender Mode Enable:** This strapping option enables Extender Mode for both ports. When enabled, the strap will enable Single Clock MII TX and RX modes unless RMII Mode is also strapped. SNI Mode cannot be strapped if Extender Mode is strapped.

3.2.8 PMD Interface for 10 Mb/s and 100 Mb/s

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
TPTDM_A	I/O	26	**10BASE-T or 100BASE-TX Transmit Data** In 10BASE-T or 100BASE-TX: Differential common driver transmit output (PMD Output Pair). These differential outputs are automatically configured to either 10BASE-T or 100BASE-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. These pins require 3.3-V bias for operation.
TPTDP_A		27	
TPTDM_B		36	
TPTDP_B		35	
TPRDM_A	I/O	23	**10BASE-T or 100BASE-TX Receive Data** In 10BASE-T or 100BASE-TX: Differential receive input (PMD Input Pair). These differential inputs are automatically configured to accept either 100BASE-TX or 10BASE-T signaling. In Auto-MDIX mode of operation, this pair can be used as the Transmit Output pair. These pins require 3.3-V bias for operation.
TPRDP_A		24	
TPRDM_B		39	
TPRDP_B		38	

3.2.9 Special Connections

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
RBIAS	I	32	**Bias Resistor Connection:** A 4-87 kΩ 1% resistor must be connected from RBIAS to GND.
PFBOUT	O	31	**Power Feedback Output:** Parallel caps, 10 µF and 0.1 µF, must be placed close to the PFBOUT. Connect this pin to PFBIN1 (pin 13), PFBIN2 (pin 27), PFBIN3 (pin 35), PFBIN4 (pin 49). See *Section 6.2.3* for proper placement pin.
PFBIN1	I	7	**Power Feedback Input:** These pins are fed with power from PFBOUT pin. A small capacitor of 0.1 µF must be connected close to each pin. *Note: Do not supply power to these pins other than from PFBOUT.*
PFBIN2		28	
PFBIN3		34	
PFBIN4		54	

3.2.10 Power Supply Pins

SIGNAL NAME	PIN NO.	DESCRIPTION
IOVDD1, IOVDD2, IOVDD3, IOVDD4	11, 51, 65, 78	I/O 3.3-V Supply
IOGND1, IOGND2, IOGND3, IOGND4	10, 52, 64, 77	I/O Ground
COREGND1, COREGND2	6, 55	Core Ground
CDGND1, CDGND2	25, 37	CD Ground
ANA33VDD	30	Analog 3.3-V Supply
ANAGND1, ANAGND2, ANAGND3, ANAGND4	22, 29, 33, 40	Analog Ground

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	4.2	V
V_{IN}	DC input voltage	–0.5	V_{CC} + 0.5	V
V_{OUT}	DC output voltage	–0.5	V_{CC} + 0.5	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All parameters are specified by test, statistical analysis, or design.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (3)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) R_{ZAP} = 1.5 kΩ, C_{ZAP} = 120 pF
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3		±0.3	V
T_A	Industrial Ambient temperature	–40		85	°C
P_D	Power dissipation			594	mW

4.4 Thermal Information

THERMAL METRIC (1)		DP83849I TQFP 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 DC Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN TYPES	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	Nominal V_{CC}	I, I/O	2.0			V
V_{IL}	Input low voltage		I, I/O			0.8	V
I_{IH}	Input high current	$V_{IN} = V_{CC}$	I, I/O			10	µA
I_{IL}	Input low current	V_{IN} = GND	I, I/O			10	µA
V_{OL}	Output low voltage	I_{OL} = 4 mA	O, I/O			0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA	O, I/O	Vcc – 0.5			V
V_{ledOL}	Output low voltage	I_{OL} = 2.5 mA	LED			0.4	V
V_{ledOH}	Output high voltage	I_{OH} = –2.5 mA	LED	Vcc – 0.5			V
I_{OZ}	Tri-state leakage	$V_{OUT} = V_{CC}$	I/O, O			±10	µA
V_{TPTD_100}	100M Transmit voltage		PMD Output Pair	0.95	1	1.05	V
$V_{TPTDsym}$	100M Transmit voltage symmetry		PMD Output Pair			±2%	
V_{TPTD_10}	10M Transmit voltage		PMD Output Pair	2.2	2.5	2.8	V
C_{IN1}	CMOS Input capacitance		I		8		pF
C_{OUT1}	CMOS Output capacitance		O		8		pF
SD_{THon}	100BASE-TX Signal detect turnon threshold		PMD Input Pair			1000	mV diff pk-pk
SD_{THoff}	100BASE-TX Signal detect turnoff threshold		PMD Input Pair	200			mV diff pk-pk
V_{TH1}	10BASE-T Receive Threshold		PMD Input Pair			585	mV
I_{dd100}	100BASE-TX (Full Duplex)		Supply		180		mA
I_{dd10}	10BASE-T (Full Duplex)		Supply		180		mA
Idd	Power Down Mode	CLK2MAC disabled	Supply		9.5		mA

4.6 AC Timing Requirements

			MIN	NOM	MAX	UNIT
POWER UP TIMING (REFER TO Figure 4-1)(1)						
T2.1.1	Post Power Up Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization. X1 Clock must be stable for a minimum of 167 ms at power up.	167			ms
T2.1.2	Hardware Configuration Latch-in Time from power up	Hardware Configuration Pins are described in the Pin Description section. X1 Clock must be stable for a minimum of 167 ms at power up.	167			ms
T2.1.3	Hardware Configuration pins transition to output drivers			50		ns
RESET TIMING (REFER TO Figure 4-1)(2)						
T2.2.1	Post RESET Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization.		3		µs
T2.2.2	Hardware Configuration Latch-in Time from the Deassertion of RESET (either soft or hard)	Hardware Configuration Pins are described in Pin Description section.		3		µs
T2.2.3	Hardware Configuration pins transition to output drivers			50		ns
T2.2.4	RESET pulse width	X1 Clock must be stable for at minimum of 1 µs during RESET pulse low time.	1			µs
MII SERIAL MANAGEMENT TIMING (REFER TO Figure 4-3)						
T2.3.1	MDC to MDIO (Output) Delay Time		0		30	ns
T2.3.2	MDIO (Input) to MDC Setup Time		10			ns
T2.3.3	MDIO (Input) to MDC Hold Time		10			ns
T2.3.4	MDC Frequency			2.5	25	MHz

(1) In RMII Mode, the minimum Post Power up Stabilization and Hardware Configuration Latch-in times are 84 ms.
(2) It is important to choose pullup and/or pulldown resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.

AC Timing Requirements *(continued)*

			MIN	NOM	MAX	UNIT
100 Mb/s MII TRANSMIT TIMING (REFER TO Figure 4-4)						
T2.4.1	TX_CLK High/Low Time	100 Mb/s Normal mode	16	20	24	ns
T2.4.2	TXD[3:0], TX_EN Data Setup to TX_CLK	100 Mb/s Normal mode	10			ns
T2.4.3	TXD[3:0], TX_EN Data Hold from TX_CLK	100 Mb/s Normal mode	0			ns
100 Mb/s MII RECEIVE TIMING (REFER TO Figure 4-5)(3)						
T2.5.1	RX_CLK High/Low Time	100 Mb/s Normal mode	16	20	24	ns
T2.5.2	RX_CLK to RXD[3:0], RX_DV, RX_ER Delay	100 Mb/s Normal mode	10		30	ns
100BASE-TX TRANSMIT PACKET LATENCY TIMING (REFER TO Figure 4-6)(4)						
T2.6.1	TX_CLK to PMD Output Pair Latency	100 Mb/s Normal mode		5		bits
100BASE-TX TRANSMIT PACKET DEASSERTION TIMING (REFER TO Figure 4-7)(5)						
T2.7.1	TX_CLK to PMD Output Pair Deassertion	100 Mb/s Normal mode		5		bits
100BASE-TX TRANSMIT TIMING ($t_{R/F}$) AND JITTER) (REFER TO Figure 4-8)(6)(7)						
T2.8.1	100 Mb/s PMD Output Pair t_R and t_F		3	4	5	ns
	100 Mb/s t_R and t_F Mismatch				500	ps
T2.8.2	100 Mb/s PMD Output Pair Transmit Jitter				1.4	ns
100BASE-TX RECEIVE PACKET LATENCY TIMING (REFER TO Figure 4-9)(8)(9)						
T2.9.1	Carrier Sense ON Delay	100 Mb/s Normal mode		20		bits
T2.9.2	Receive Data Latency	100 Mb/s Normal mode		24		bits
100BASE-TX MII RECEIVE PACKET DEASSERTION TIMING (REFER TO Figure 4-10)(9)(10)						
T2.10.1	Carrier Sense OFF Delay	100BASE-TX mode		24		bits
10 Mb/s MII TRANSMIT TIMING (REFER TO Figure 4-11)(11)						
T2.11.1	TX_CLK High/Low Time	10 Mb/s MII mode	190	200	210	ns
T2.11.2	TXD[3:0], TX_EN Data Setup to TX_CLK fall	10 Mb/s MII mode	25			ns
T2.11.3	TXD[3:0], TX_EN Data Hold from TX_CLK rise	10 Mb/s MII mode	0			ns
10 Mb/s MII RECEIVE TIMING (REFER TOFigure 4-12)(12)						
T2.12.1	RX_CLK High/Low Time		160	200	240	ns
T2.12.2	RX_CLK to RXD[3:0], RX_DV Delay	10 Mb/s MII mode	100			ns
T2.12.3	RX_CLK rising edge delay from RXD[3:0], RX_DV Valid	10 Mb/s MII mode	100			ns
10 Mb/s SERIAL MODE TRANSMIT TIMING (REFER TO Figure 4-13)						
T2.13.1	TX_CLK High Time	10 Mb/s Serial mode	20	25	30	ns
T2.13.2	TX_CLK Low Time	10 Mb/s Serial mode	70	75	80	ns
T2.13.3	TXD_0, TX_EN Data Setup to TX_CLK rise	10 Mb/s Serial mode	25			ns
T2.13.4	TXD_0, TX_EN Data Hold from TX_CLK rise	10 Mb/s Serial mode	0			ns
10 Mb/s SERIAL MODE RECEIVE TIMING (REFER TO Figure 4-15) (3)						
T2.14.1	RTX_CLK high/low Time		35	50	65	ns
T2.14.2	RX_CLK fall to RXD_0, RX_DV Delay	10 Mb/s Serial mode	–10		10	ns

(3) RX_CLK may be held low or high for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.
(4) For Normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the “J” code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.
(5) Deassertion is determined by measuring the time from the first rising edge of TX_CLK occurring after the deassertion of TX_EN to the first bit of the “T” code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.
(6) Normal Mismatch is the difference between the maximum and minimum of all rise and fall times.
(7) Rise and fall times taken at 10% and 90% of the +1 or –1 amplitude.
(8) Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.
(9) 1 bit time = 10 ns in 100 Mb/s mode.
(10) Carrier Sense Off Delay is determined by measuring the time from the first bit of the “T” code group to the deassertion of Carrier Sense.
(11) An attached Mac must drive the transmit signals using the positive edge of TX_CLK. As shown above, the MII signals are sampled on the falling edge of TX_CLK.
(12) RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

AC Timing Requirements *(continued)*

			MIN	NOM	MAX	UNIT
10BASE-T TRANSMIT TIMING (START OF PACKET) (REFER TO Figure 4-16)(13)						
T2.15.1	Transmit Output Delay from the Falling Edge of TX_CLK	10 Mb/s MII mode		3.5		bits
T2.15.2	Transmit Output Delay from the Rising Edge of TX_CLK	10 Mb/s Serial mode		3.5		bits
10BASE-T TRANSMIT TIMING (END OF PACKET) (REFER TO Figure 4-17)						
T2.16.1	End of Packet High Time (with 0 ending bit)		250	300		ns
T2.16.2	End of Packet High Time (with 1 ending bit)		250	300		ns
10BASE-T RECEIVE TIMING (START OF PACKET) (REFER TO Figure 4-18)(13)(14)						
T2.17.1	Carrier Sense Turnon Delay (PMD Input Pair to CRS)			630	1000	ns
T2.17.2	RX_DV Latency			10		bits
T2.17.3	Receive Data Latency	Measurement shown from SFD		8		bits
10BASE-T RECEIVE TIMING (END OF PACKET) (REFER TO Figure 4-19)						
T2.18.1	Carrier Sense Turn Off Delay				1.0	µs
10Mb/s HEARTBEAT TIMING (REFER TO Figure 4-20)						
T2.19.1	CD Heartbeat Delay	10 Mb/s half-duplex mode		1200		ns
T2.19.2	CD Heartbeat Duration	10 Mb/s half-duplex mode		1000		ns
10 Mb/s JABBER TIMING (REFER TO Figure 4-21)						
T2.20.1	Jabber Activation Time			85		ms
T2.20.2	Jabber Deactivation Time			500		ms
10BASE-T NORMAL LINK PULSE TIMING (REFER TO Figure 4-22)(15)						
T2.21.1	Pulse Width			100		ns
T2.21.2	Pulse Period			16		ms
AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING (REFER TO Figure 4-23)(15)						
T2.22.1	Clock, Data Pulse Width			100		ns
T2.22.2	Clock Pulse to Clock Pulse Period			125		µs
T2.22.3	Clock Pulse to Data Pulse Period	Data = 1		62		µs
T2.22.4	Burst Width			2		ms
T2.22.5	FLP Burst to FLP Burst Period			16		ms
100BASE-TX SIGNAL DETECT TIMING (REFER TO)Figure 4-24						
T2.23.1	SD Internal Turnon Time				1	ms
T2.23.2	SD Internal Turnoff Time				350	µs
100 Mb/s INTERNAL LOOPBACK TIMING (REFER TO Figure 4-25)(16)(17)						
T2.24.1	TX_EN to RX_DV Loopback	100 Mb/s internal loopback mode			240	ns
10 Mb/s INTERNAL LOOPBACK TIMING (REFER TO Figure 4-26)(17)						
T2.25.1	TX_EN to RX_DV Loopback	10 Mb/s internal loopback mode			2	µs
RMII TRANSMIT TIMING (REFER TO Figure 4-27)						
T2.26.1	X1 Clock Period	50-MHz Reference Clock		20		ns
T2.26.2	TXD[1:0], TX_EN, Data Setup to X1 rising		4			ns
T2.26.3	TXD[1:0], TX_EN, Data Hold from X1 rising		2			ns
T2.26.4	X1 Clock to PMD Output Pair Latency	100BASE-TX mode		11		bits

(13) 1 bit time = 100 ns in 10 Mb/s mode.
(14) 10BASE-T RX_DV Latency is measured from first bit of preamble on the wire to the assertion of RX_DV
(15) These specifications represent transmit timings.
(16) Due to the nature of the descrambler function, all 100BASE-TX Loopback modes will cause an initial “dead-time” of up to 550 µs during which time no data will be present at the receive MII outputs. The 100BASE-TX timing specified is based on device delays after the initial 550 µs “dead-time”.
(17) Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

AC Timing Requirements *(continued)*

			MIN	NOM	MAX	UNIT
RMII RECEIVE TIMING (REFER TO Figure 4-28)(18)(19)(20)(21)(22)(23)						
T2.27.1	X1 Clock Period	50-MHz Reference Clock		20		ns
T2.27.2	RXD[1:0], CRS_DV, RX_DV, and RX_ER output delay from X1 rising		2		14	ns
T2.27.3	CRS ON delay (100Mb)	100BASE-TX mode		18.5		bits
T2.27.4	CRS OFF delay (100Mb)	100BASE-TX mode		27		bits
T2.27.5	RXD[1:0] and RX_ER latency (100Mb)	100BASE-TX mode		38		bits
SINGLE CLOCK MII (SMII) TRANSMIT TIMING (REFER TO Figure 4-29)						
T2.28.1	X1 Clock Period	25MHz Reference Clock		40		ns
T2.28.2	TXD[3:0], TX_EN Data Setup	To X1 rising	4			ns
T2.28.3	TXD[3:0], TX_EN Data Hold	From X1 rising	2			ns
T2.28.4	X1 Clock to PMD Output Pair Latency (100Mb)	100BASE-tx MODE		13		bits
SINGLE CLOCK MII (SCMII) RECEIVE TIMING (REFER TO Figure 4-30) (24)(25)(26)(27)(28)(29)						
T2.29.1	1 Clock Period	25MHz Reference Clock		40		ns
T2.29.2	RXD[3:0], RX_DV and RX_ER output delay	From X1 rising	2		18	ns
T2.29.3	CRS ON delay (100Mb)	100BASE-TX mode		19		bits
T2.29.4	CRS OFF delay (100Mb)	100BASE-TX mode		26		bits
T2.29.5	RXD[1:0] and RX_ER latency (100Mb)	100BASE-TX mode		56		bits
ISOLATION TIMING (REFER TO Figure 4-31)						
T2.30.1	From software clear of bit 10 in the BMCR register to the transition from Isolate to Normal Mode				100	µs
CLK2MAC TIMING (REFER TO Figure 4-32) (30)						
T2.31.1	CLK2MAC high/Low Time	MII mode		20		ns
		RMII mode		10	8	ns
T2.31.2	CLK2MAC propagation delay	Relative to X1				ns
100 Mb/s X1 TO TX_CLK TIMING (REFER TO Figure 4-33) (31)						
T2.32.1	X1 to TX_CLK delay	100 Mb/s Normal mode	0		5	ns

(18) Per the RMII Specification, output delays assume a 25-pF load.
(19) CRS_DV is asserted asynchronously in order to minimize latency of control signals through the Phy. CRS_DV may toggle synchronously at the end of the packet to indicate CRS deassertion.
(20) RX_DV is synchronous to X1. While not part of the RMII specification, this signal is provided to simplify recovery of receive data.
(21) CRS ON delay is measured from the first bit of the JK symbol on the PMD Input Pair to initial assertion of CRS_DV.
(22) CRS OFF delay is measured from the first bit of the TR symbol on the PMD Input Pair to initial deassertion of CRS_DV.
(23) Receive Latency is measured from the first bit of the symbol pair on the PMD Input Pair. Typical values are with the Elasticity Buffer set to the default value (01).
(24) Latency measurement is made from the X1 Rising edge to the first bit of symbol.
(25) Output delays assume a 25pF load.
(26) CRS is asserted and deasserted asynchronously relative to the reference clock.
(27) CRS ON delay is measured from the first bit of the JK symbol on the PMD Receive Pair to assertion of CRS_DV
(28) CRS_OFF delay is measured from the first bit of the TR symbol on the PMD Receive Pair to deassertion of CRS_DV.
(29) Receive Latency is measured from the first bit of the symbol pair on the PMD Receive Pair. Typical values are with the Elasticity Buffer set to the default value (01).
(30) CLK2MAC characteristics are dependent upon the X1 input characteristics.
(31) X1 to TX_CLK timing is provided to support devices that use X1 instead of TX_CLK as the reference for transmit MII data.

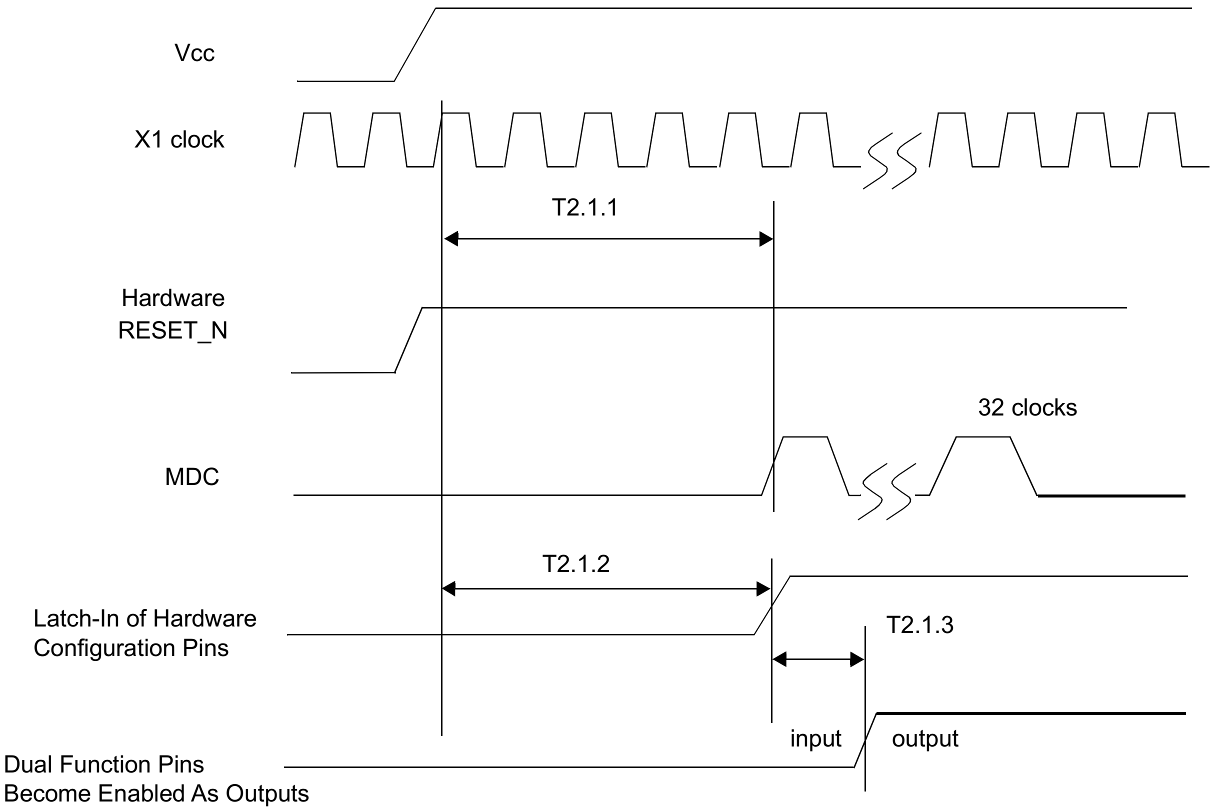


Figure 4-1. Power Up Timing

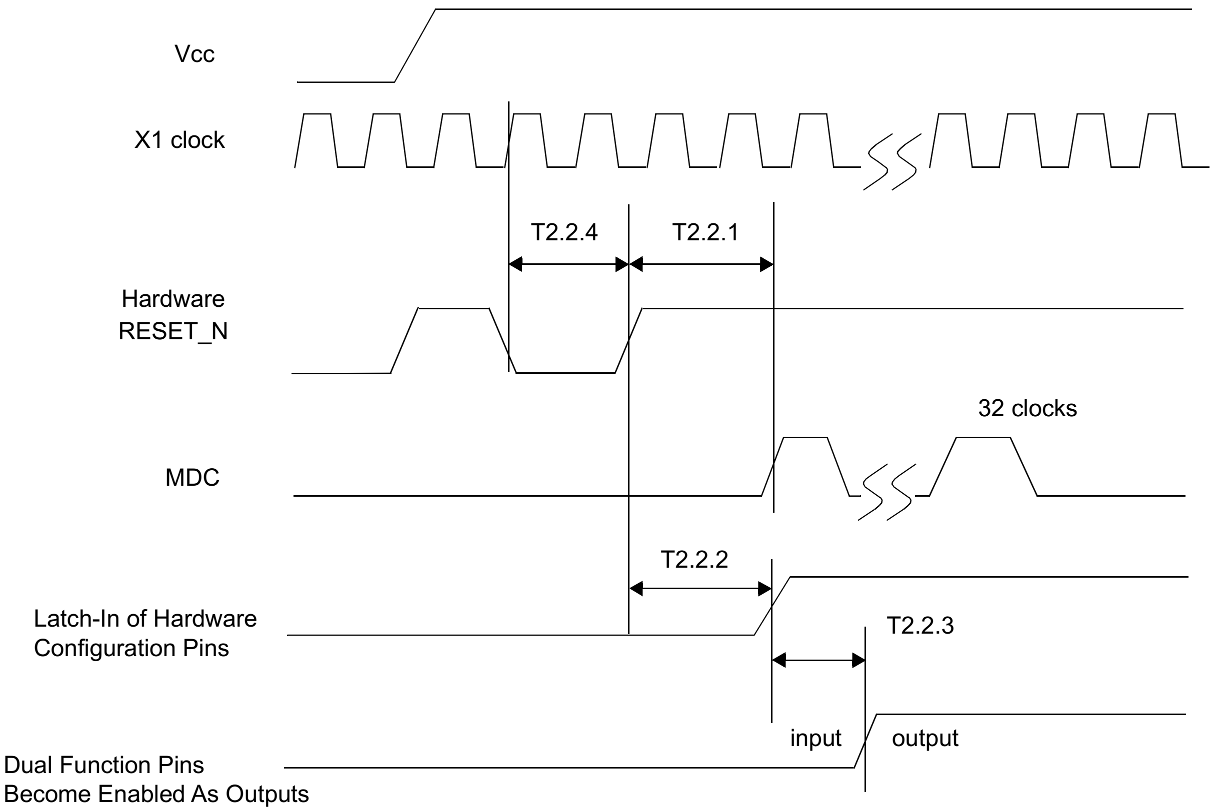


Figure 4-2. Reset Timing

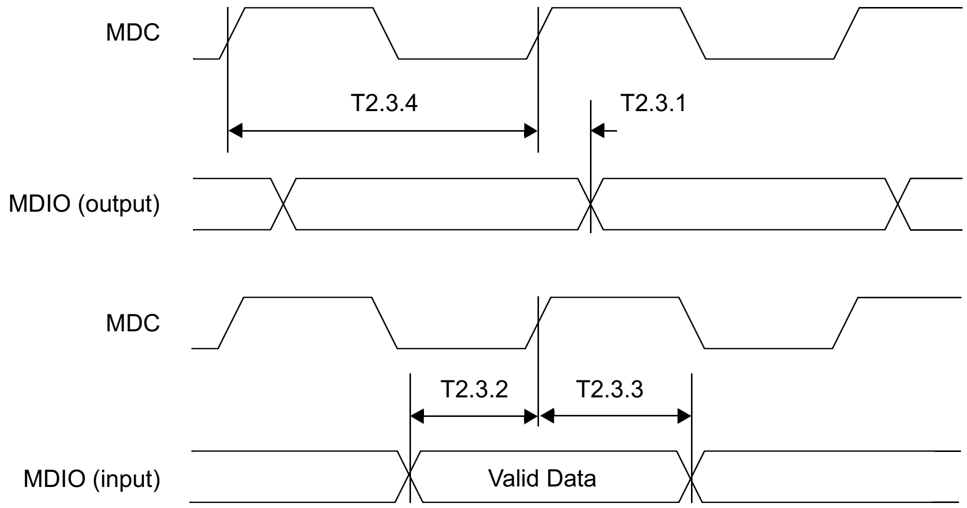


Figure 4-3. MII Serial Management Timing

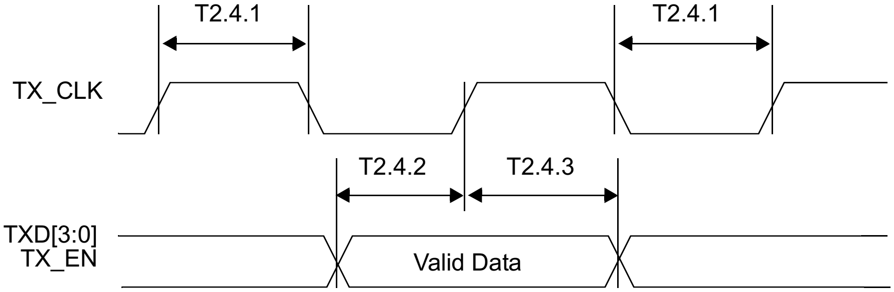


Figure 4-4. 100 Mb/s MII Transmit Timing

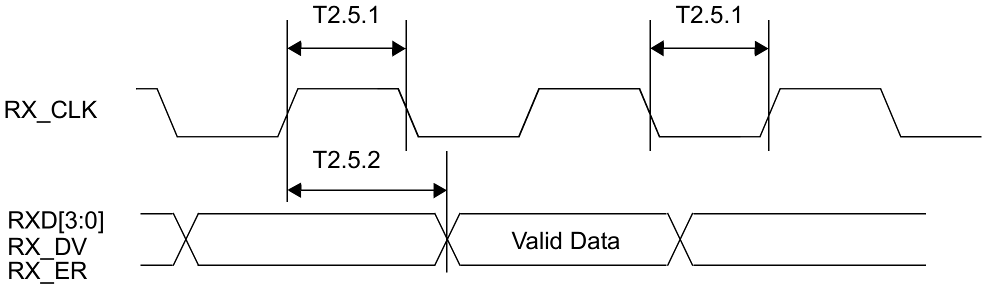


Figure 4-5. 100 Mb/s MII Receive Timing

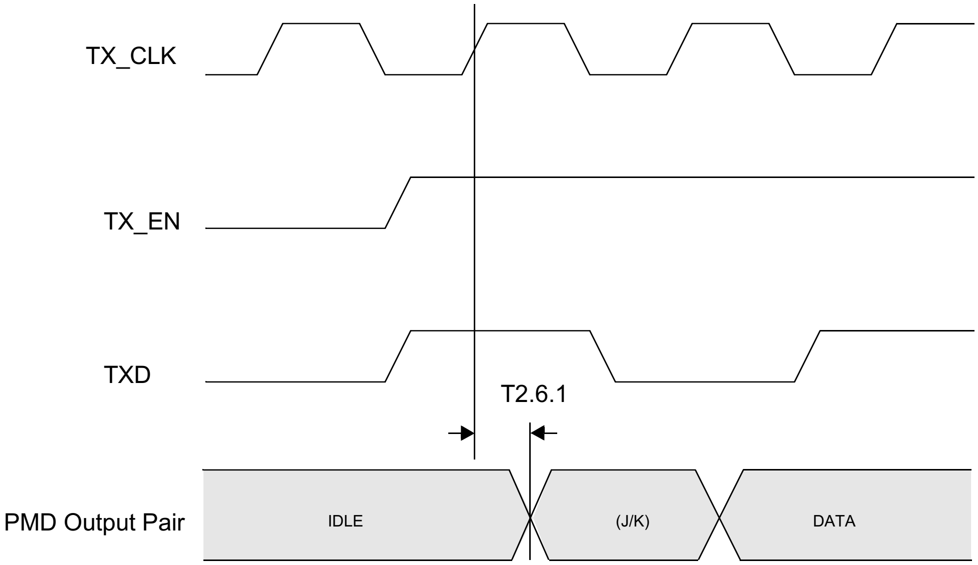


Figure 4-6. 100BASE-TX MII Transmit Packet Latency Timing

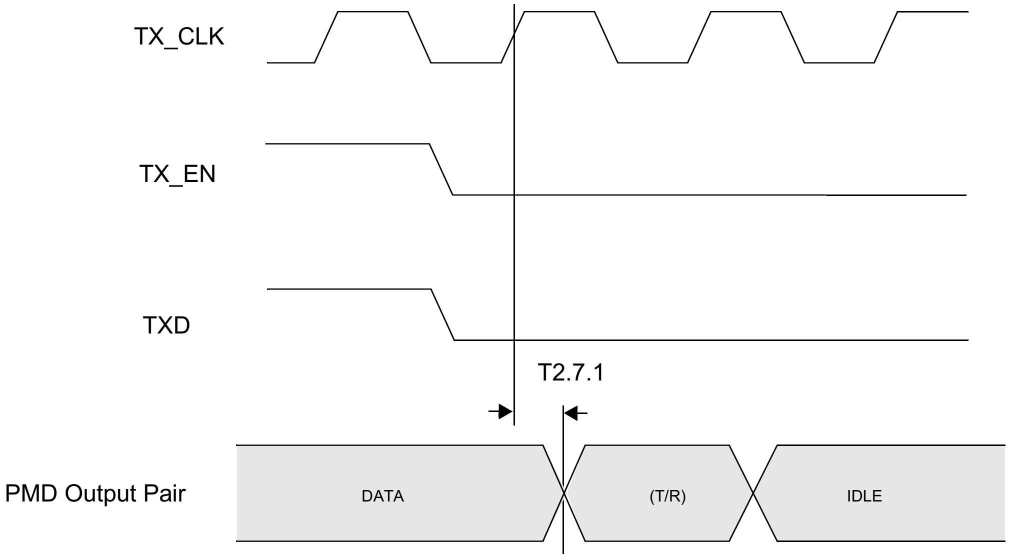


Figure 4-7. 100BASE-TX MII Transmit Packet Deassertion Timing

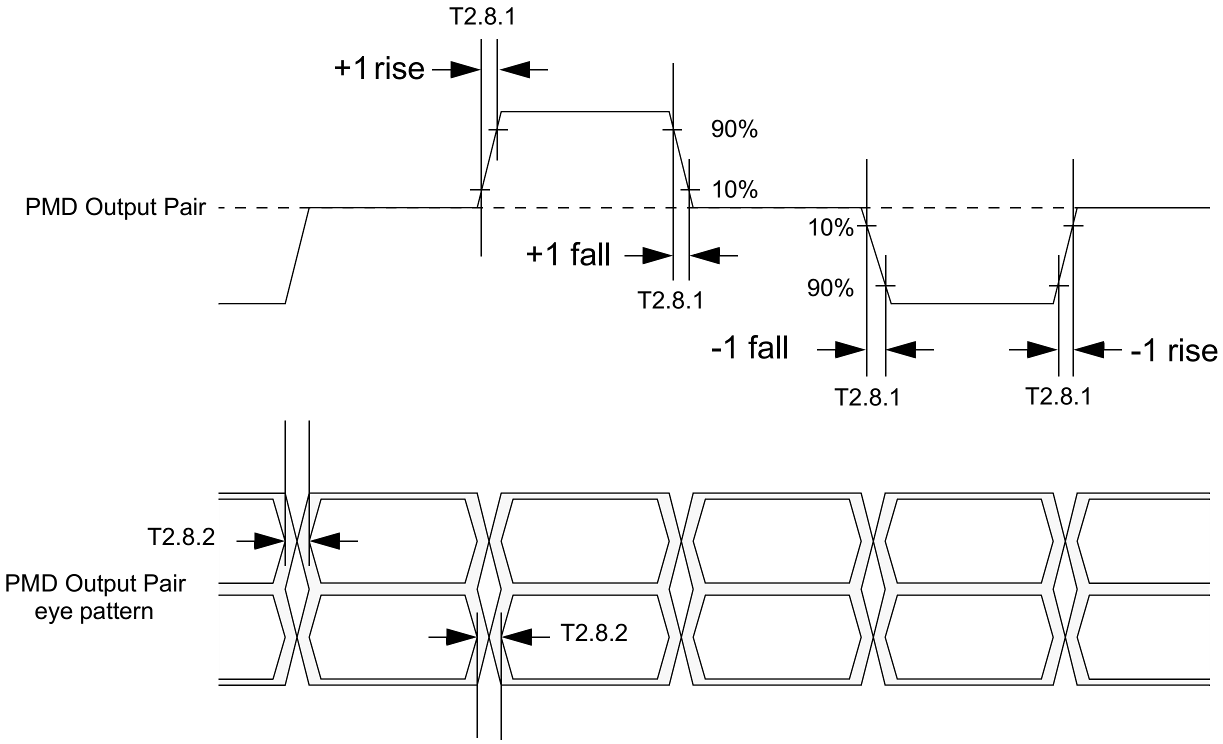


Figure 4-8. 100BASE-TX Transmit Timing ($t_{R/F}$ and Jitter)

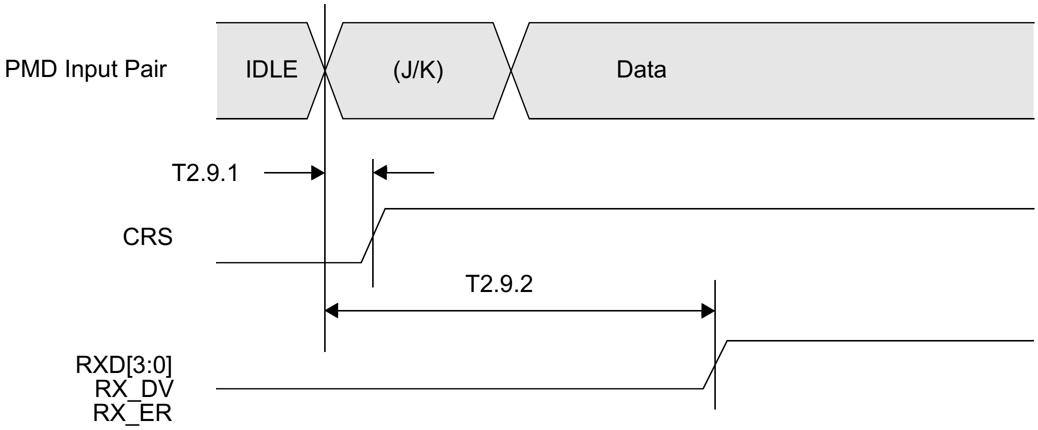


Figure 4-9. 100BASE-TX MII Receive Packet Latency Timing

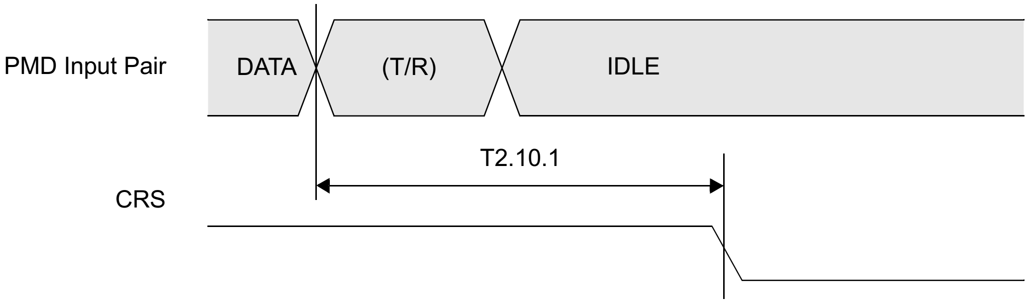


Figure 4-10. 100BASE-TX MII Receive Packet Deassertion Timing

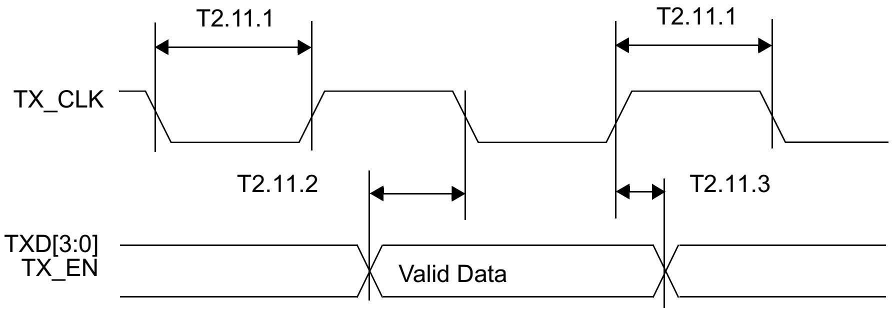


Figure 4-11. 10 Mb/s MII Transmit Timing

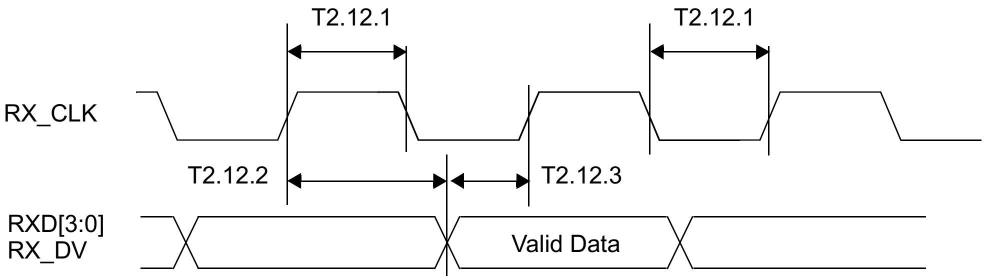


Figure 4-12. 10 Mb/s MII Receive Timing

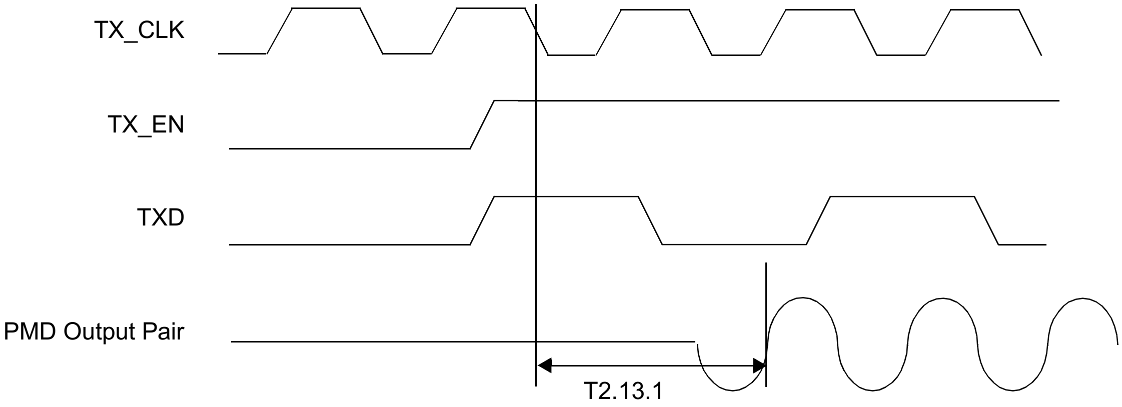


Figure 4-13. 10BASE-T Transmit Timing (Start of Packet)

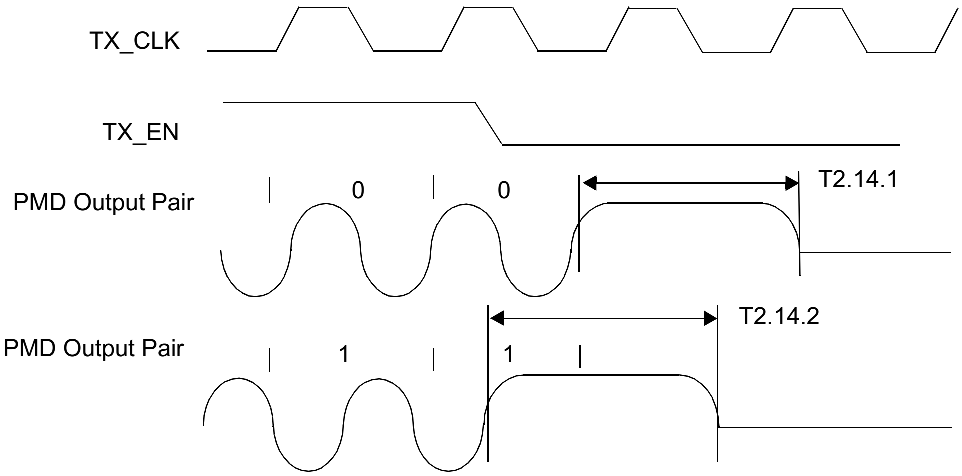


Figure 4-14. 10BASE-T Transmit Timing (End of Packet)

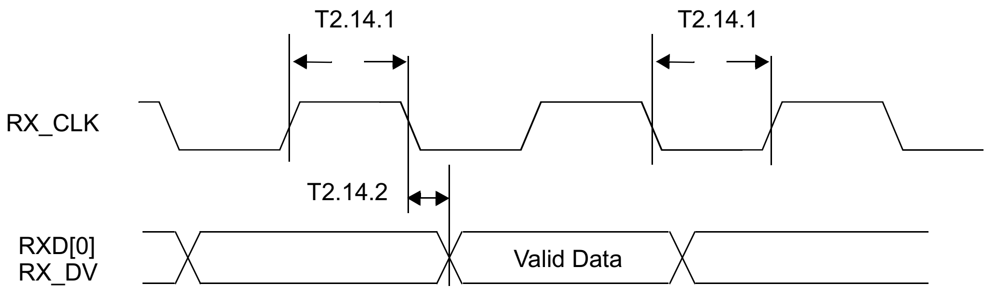


Figure 4-15. 10 Mb/s Serial Mode Receive Timing

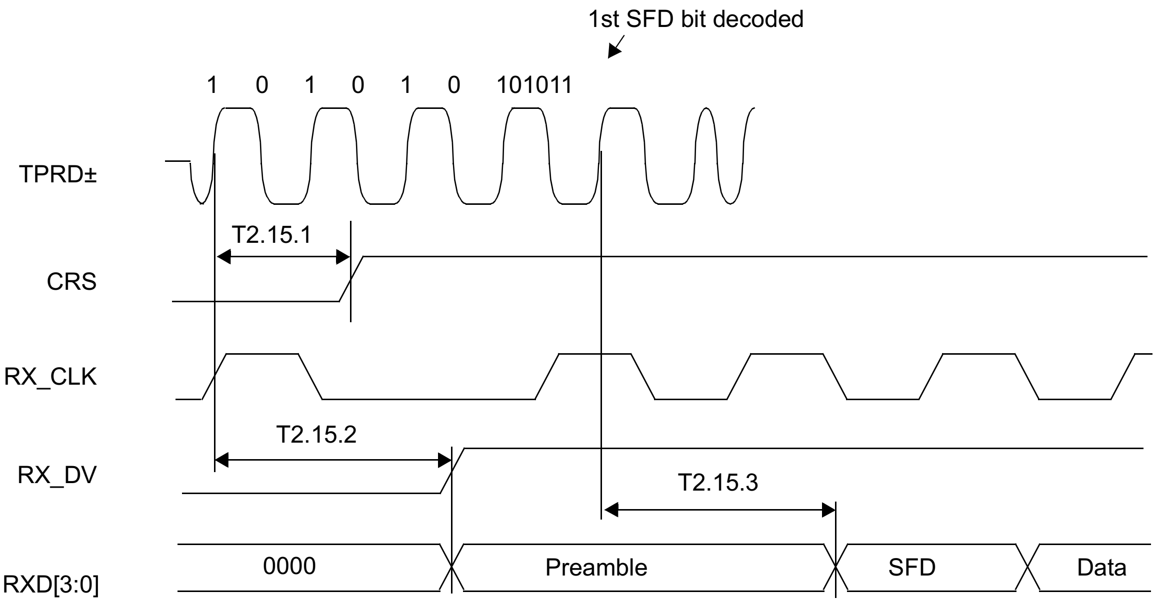


Figure 4-16. 10BASE-T Transmit Timing (Start of Packet)

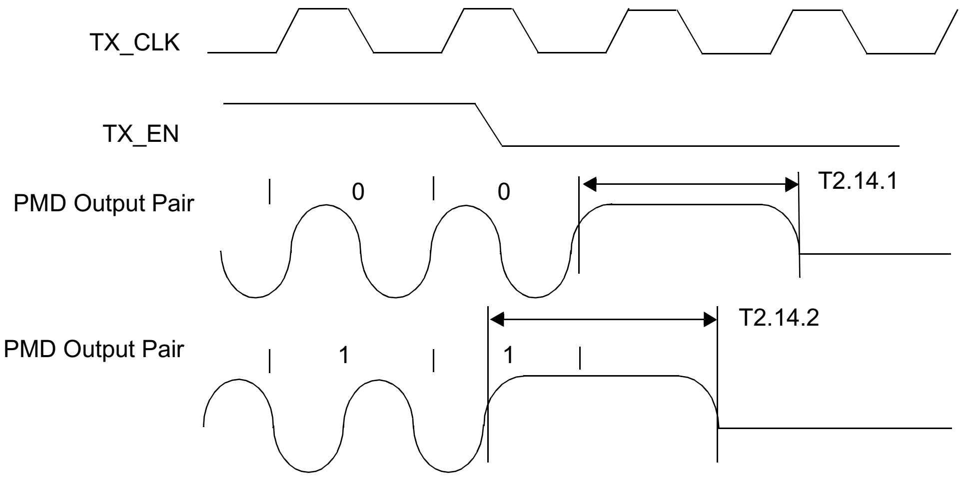


Figure 4-17. 10BASE-T Transmit Timing (End of Packet)

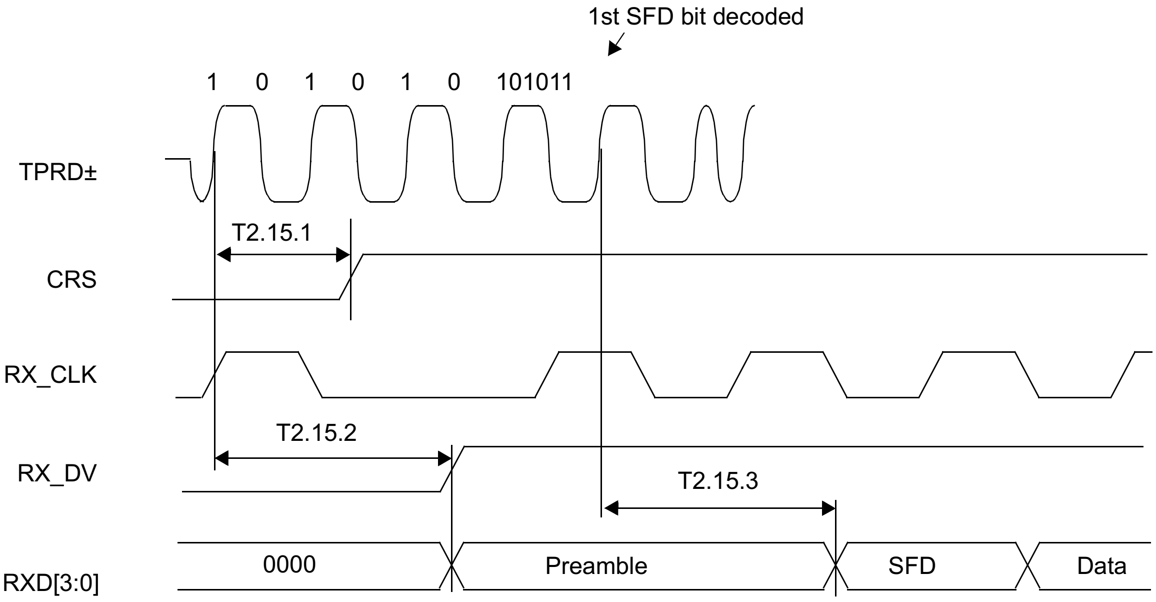


Figure 4-18. 10BASE-T Receive Timing (Start of Packet)

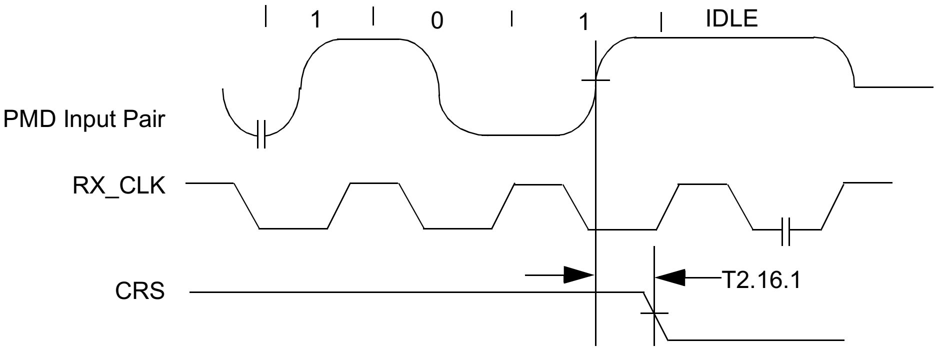


Figure 4-19. 10BASE-T Receive Timing (End of Packet)

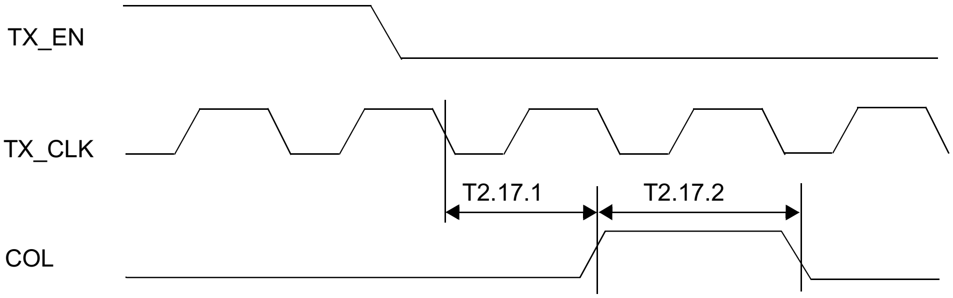


Figure 4-20. 10 Mb/s Heartbeat Timing

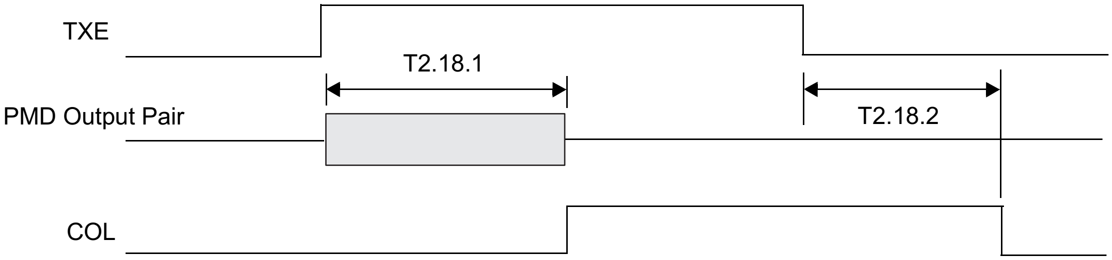


Figure 4-21. 10 Mb/s Jabber Timing

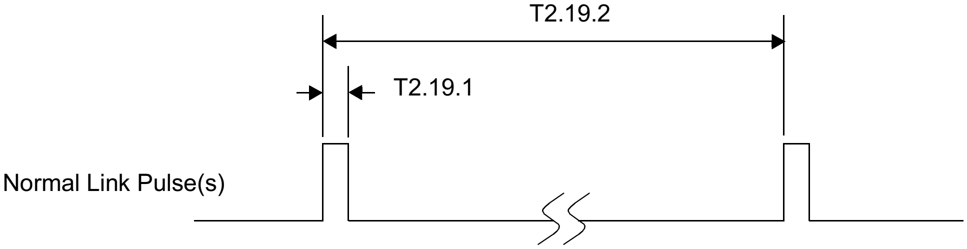


Figure 4-22. 10BASE-T Normal Link Pulse Timing

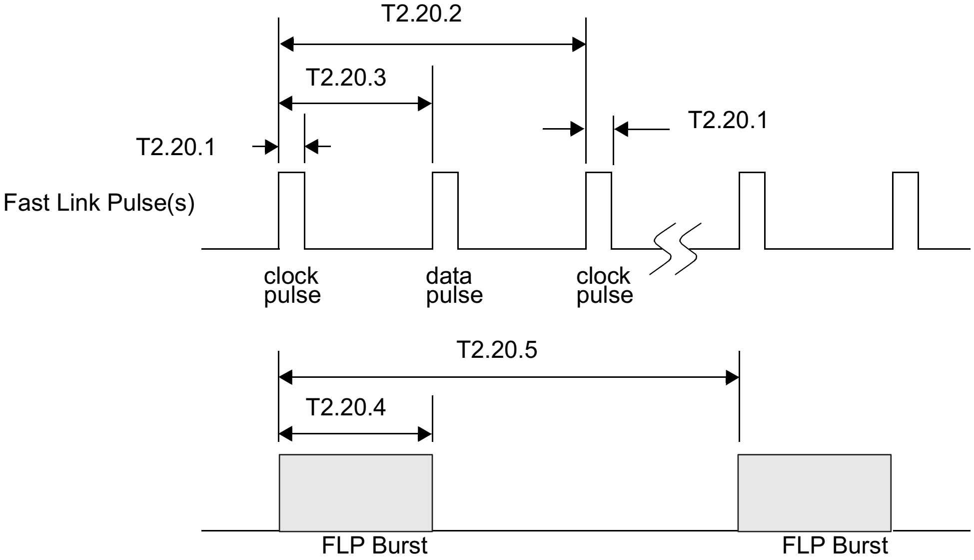


Figure 4-23. Auto-Negotiation Fast Link Pulse (FLP) Timing

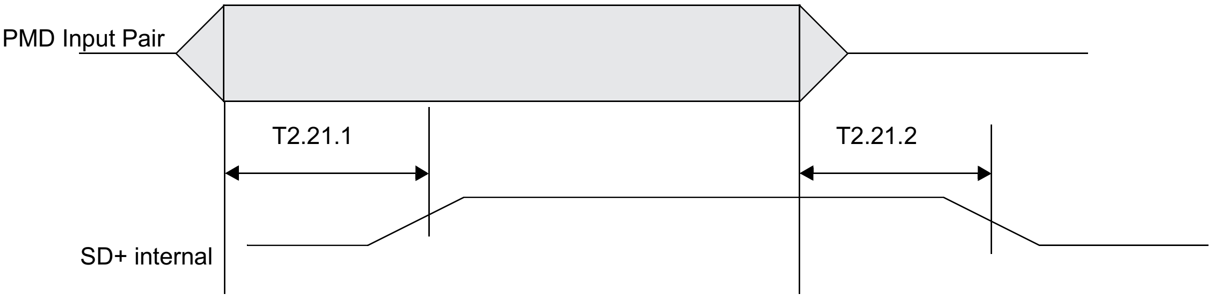


Figure 4-24. 100BASE-TX Signal Detect Timing

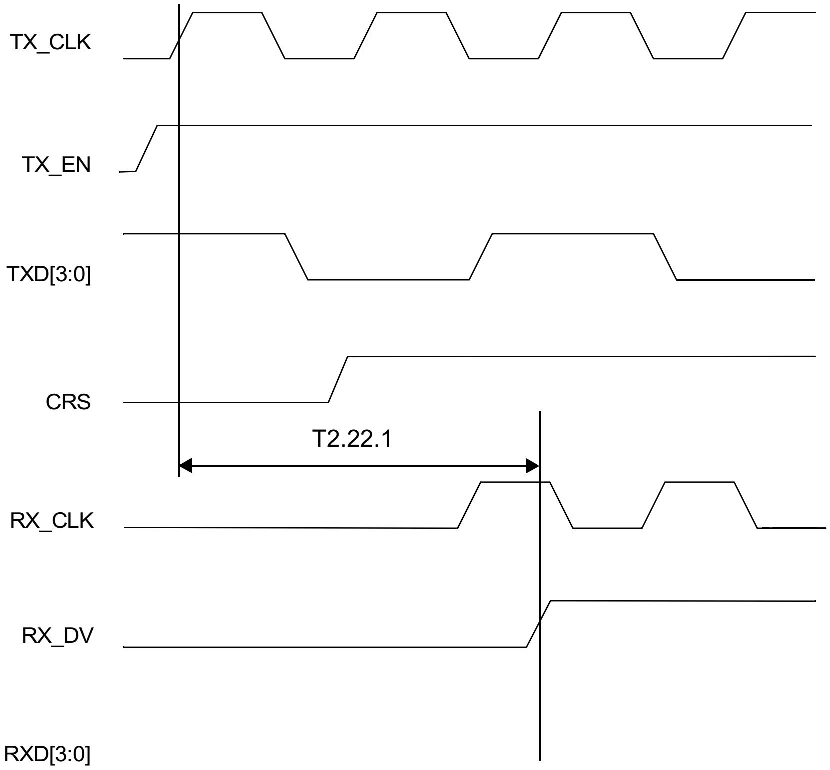


Figure 4-25. 100 Mb/s Internal Loopback Timing

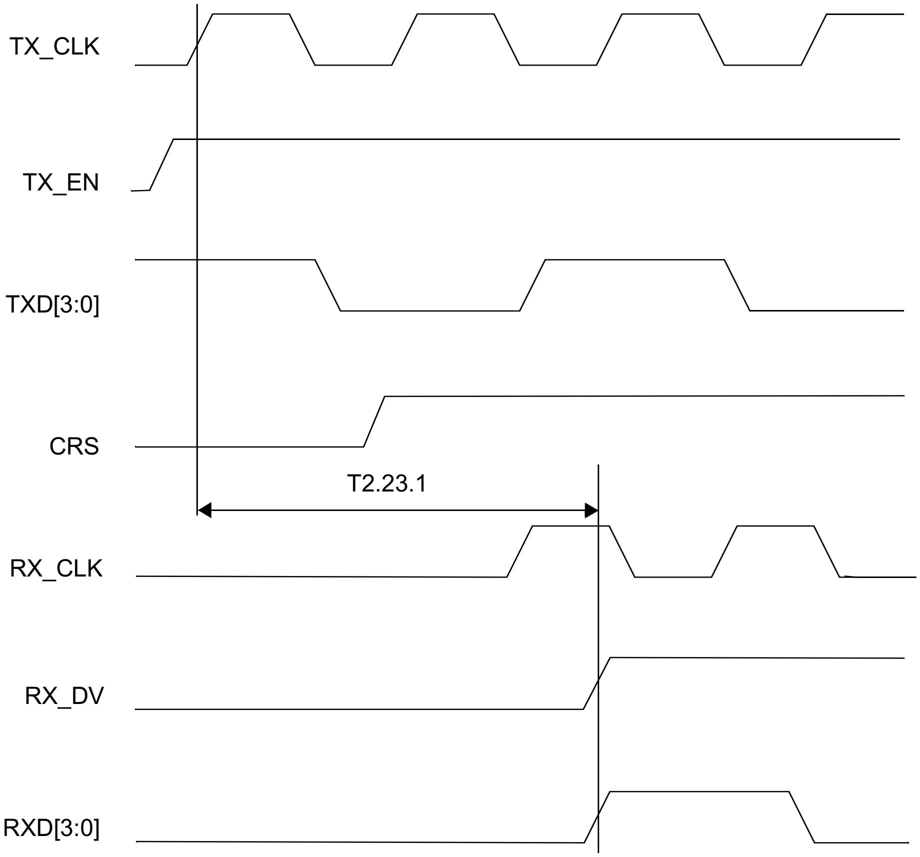


Figure 4-26. 10 Mb/s Internal Loopback Timing

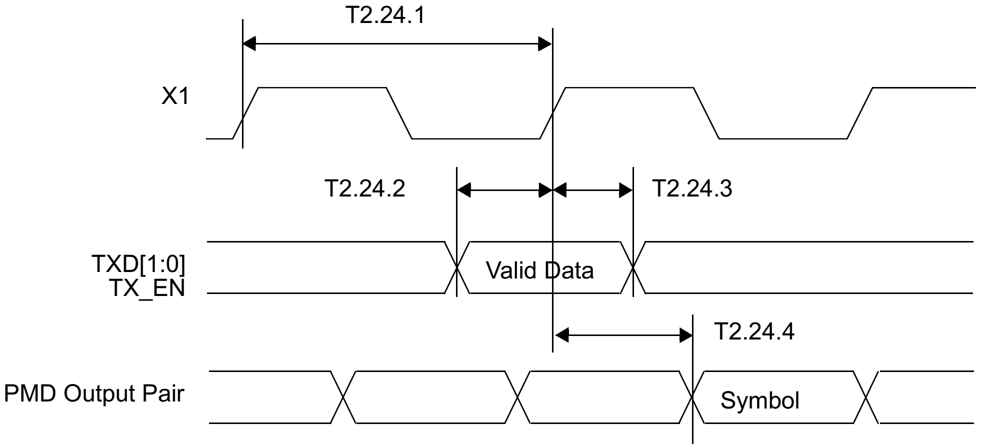


Figure 4-27. RMII Transmit Timing

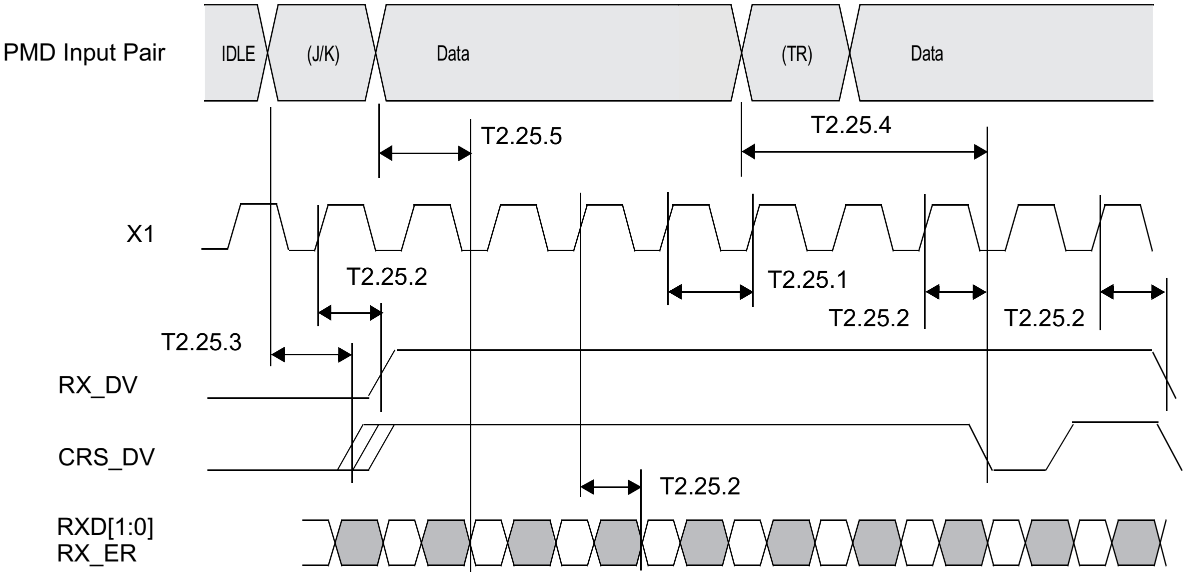


Figure 4-28. RMII Receive Timing

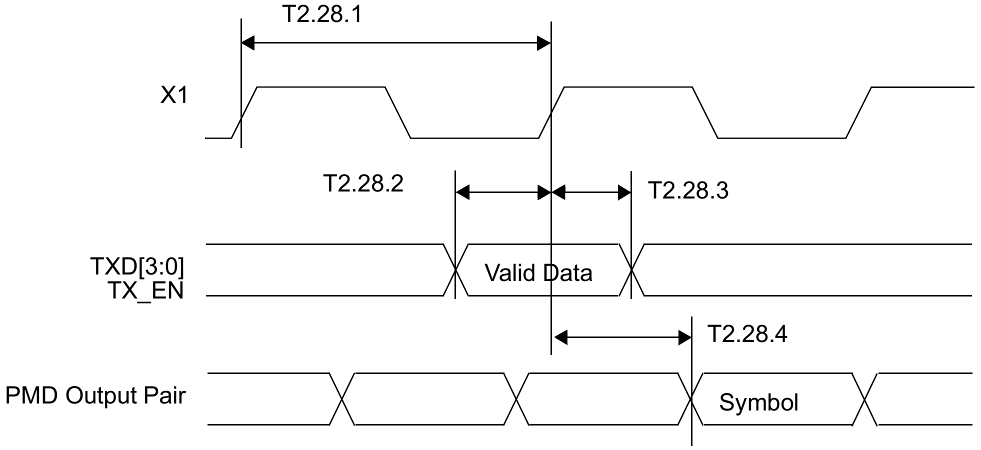


Figure 4-29. Single Clock MII (SCMII) Transmit Timing

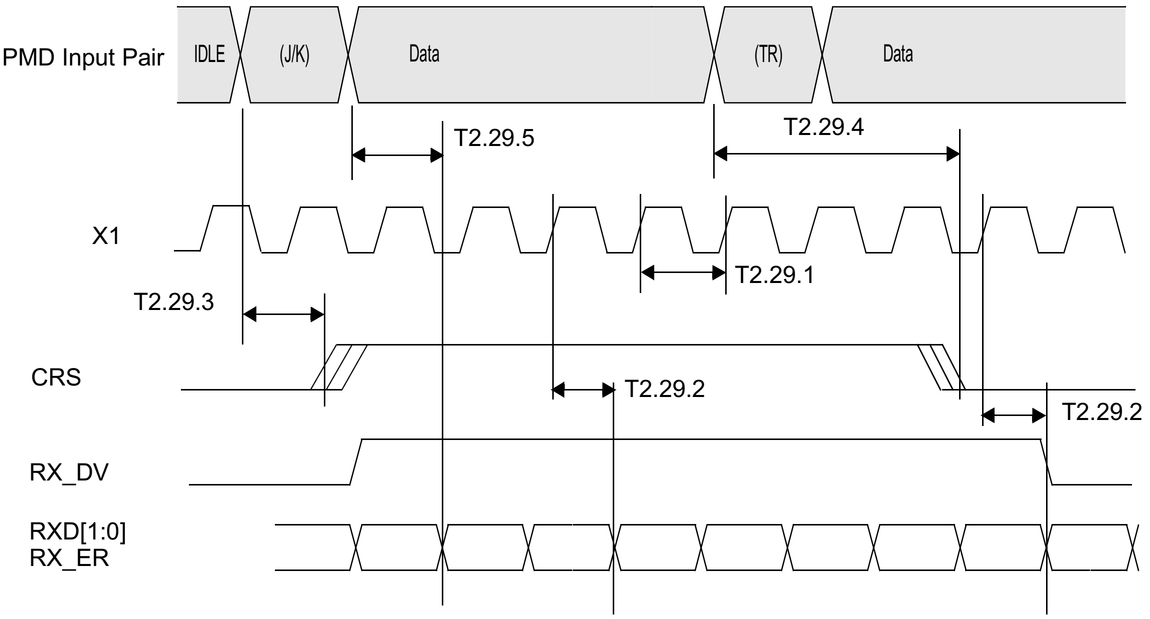


Figure 4-30. Single Clock MII (SCMII) Receive Timing

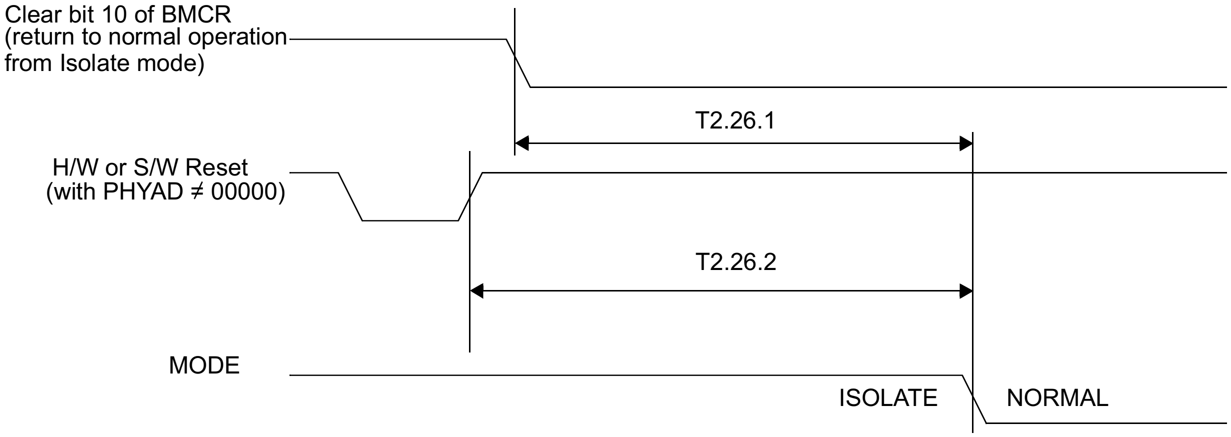


Figure 4-31. Isolation Timing

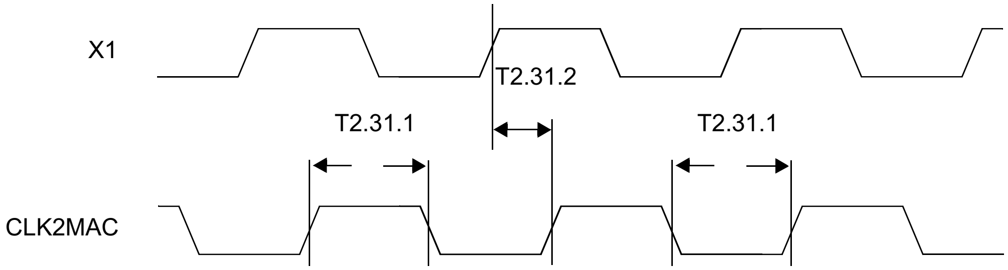


Figure 4-32. CLK2MAC timing

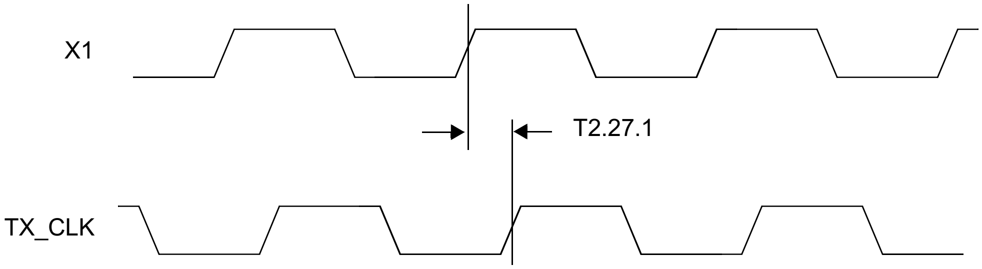


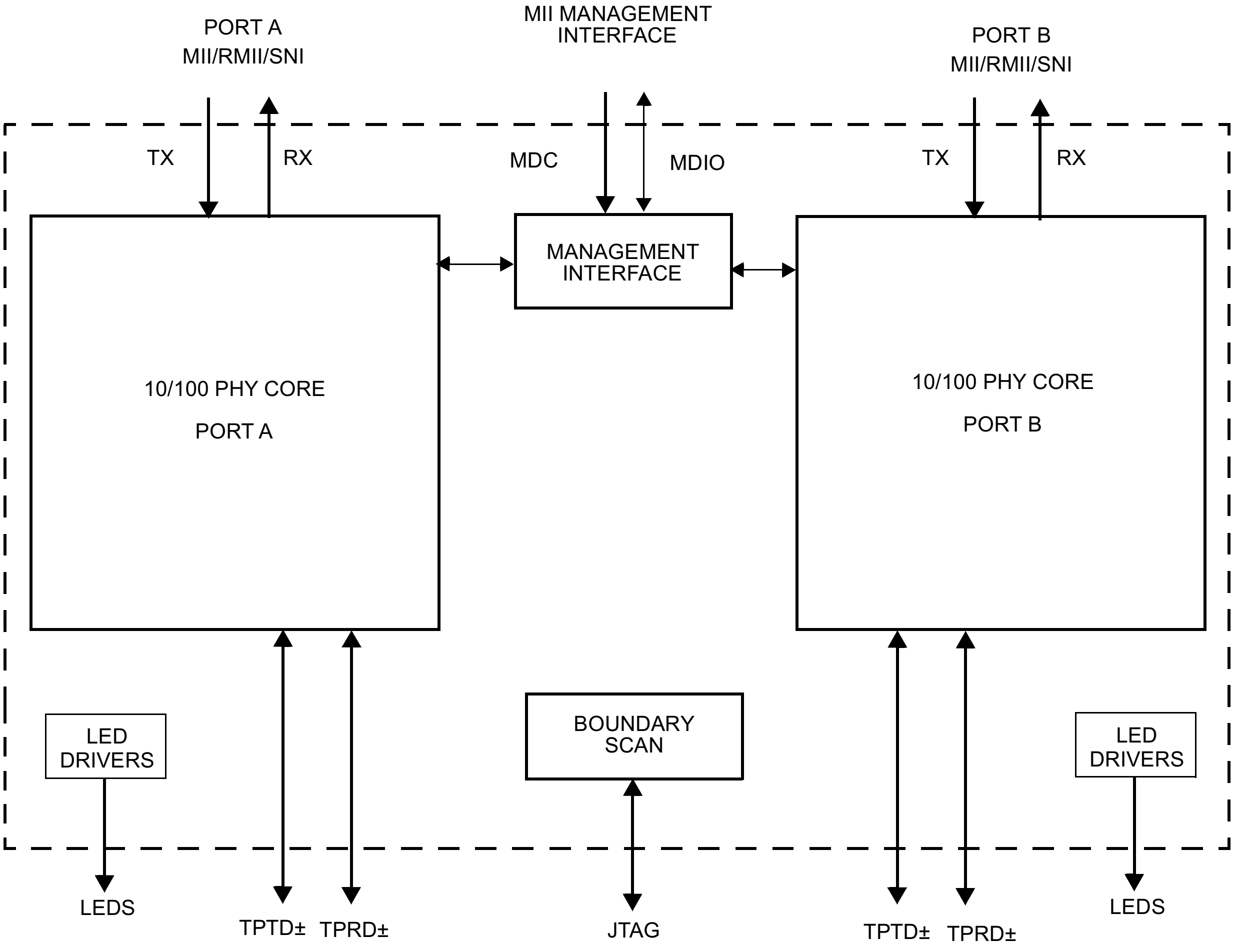
Figure 4-33. 100 Mb/s X1 to TX_CLK Timing

5 Detailed Description

5.1 Overview

The DP83849I is a feature rich, dual 10/100 Mbps Ethernet transceiver. This section discusses in detail features of the DP83849I including: auto-negotiation, auto-mdix, LED interface, internal loopback, BIST operation, energy detection mode, and link cable diagnostics including TDR capability.

5.2 Functional Block Diagram



5.3 Feature Description

This section includes information on the various configuration options available with the DP83849I. The configuration options described in *Section 5.3.1* through *Section 5.3.6* include:

- Auto-Negotiation
- Auto-MDIX
- LED Interface
- Internal Loopback
- BIST
- Energy Detect Mode

5.3.1 Auto-Negotiation

The Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further detail regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DP83849I supports four different Ethernet protocols (10 Mb/s Half Duplex, 10 Mb/s Full Duplex, 100 Mb/s Half Duplex, and 100 Mb/s Full Duplex), so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the Link Partner. The Auto-Negotiation function within the DP83849I can be controlled either by internal register access or by the use of the AN_EN, AN1 and AN0 pins.

5.3.1.1 Auto-Negotiation Pin Control

The state of AN_EN, AN0 and AN1 determines whether the DP83849I is forced into a specific mode or Auto-Negotiation will advertise a specific ability (or set of abilities) as given in Table 5-1. These pins allow configuration options to be selected without requiring internal register access.

The state of AN_EN, AN0 and AN1, upon power-up/reset, determines the state of bits [8:5] of the ANAR register.

The Auto-Negotiation function selected at power-up or reset can be changed at any time by writing to the Basic Mode Control Register (BMCR) at address 00h.

Table 5-1. Auto-Negotiation Modes

AN_EN	**AN1**	**AN0**	**FORCED MODE**
0	0	0	10BASE-T, Half-Duplex
0	0	1	10BASE-T, Full-Duplex
0	1	0	100BASE-TX, Half-Duplex
0	1	1	100BASE-TX, Full-Duplex
AN_EN	AN1	AN0	ADVERTISED MODE
1	0	0	10BASE-T, Half/Full-Duplex
1	0	1	100BASE-TX, Half/Full-Duplex
1	1	0	10BASE-T Half-Duplex 100BASE-TX, Half-Duplex
1	1	1	10BASE-T, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex

5.3.1.2 Auto-Negotiation Register Control

When Auto-Negotiation is enabled, the DP83849I transmits the abilities programmed into the Auto-Negotiation Advertisement register (ANAR) at address 04h through FLP Bursts. Any combination of 10 Mb/s, 100 Mb/s, Half-Duplex, and Full Duplex modes may be selected.

Auto-Negotiation Priority Resolution:

1. 100BASE-TX Full Duplex (Highest Priority)
2. 100BASE-TX Half Duplex
3. 10BASE-T Full Duplex
4. 10BASE-T Half Duplex (Lowest Priority)

The Basic Mode Control Register (BMCR) at address 00h provides control for enabling, disabling, and restarting the Auto-Negotiation process. When Auto-Negotiation is disabled, the Speed Selection bit in the BMCR controls switching between 10 Mb/s or 100 Mb/s operation, and the Duplex Mode bit controls switching between full duplex operation and half duplex operation. The Speed Selection and Duplex Mode bits have no effect on the mode of operation when the Auto-Negotiation Enable bit is set.

The Link Speed can be examined through the PHY Status Register (PHYSTS) at address 10h after a Link is achieved.

The Basic Mode Status Register (BMSR) indicates the set of available abilities for technology types, Auto-Negotiation ability, and Extended Register Capability. These bits are permanently set to indicate the full functionality of the DP83849I (only the 100BASE-T4 bit is not set because the DP83849I does not support that function).

The BMSR also provides status on:

- Whether or not Auto-Negotiation is complete
- Whether or not the Link Partner is advertising that a remote fault has occurred
- Whether or not valid link has been established
- Support for Management Frame Preamble suppression

The Auto-Negotiation Advertisement Register (ANAR) indicates the Auto-Negotiation abilities to be advertised by the DP83849I. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR.

Updating the ANAR to suppress an ability is one way for a management agent to change (restrict) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h is used to receive the base link code word as well as all next page code words during the negotiation. Furthermore, the ANLPAR will be updated to either 0081h or 0021h for parallel detection to either 100 Mb/s or 10 Mb/s respectively.

The Auto-Negotiation Expansion Register (ANER) indicates additional Auto-Negotiation status. The ANER provides status on:

- Whether or not a Parallel Detect Fault has occurred
- Whether or not the Link Partner supports the Next Page function
- Whether or not the DP83849I supports the Next Page function
- Whether or not the current page being exchanged by Auto-Negotiation has been received
- Whether or not the Link Partner supports Auto-Negotiation

5.3.1.3 Auto-Negotiation Parallel Detection

The DP83849I supports the Parallel Detection function as defined in the IEEE 802.3u specification. Parallel Detection requires both the 10 Mb/s and 100 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation but is transmitting link signals that the 100BASE-TX or 10BASE-T PMAs recognize as valid link signals.

If the DP83849I completes Auto-Negotiation as a result of Parallel Detection, bits 5 and 7 within the ANLPAR register will be set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR will also be set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that negotiation completed through Parallel Detection by reading a zero in the Link Partner Auto-Negotiation Able bit once the Auto-Negotiation Complete bit is set. If configured for parallel detect mode and any condition other than a single good link occurs then the parallel detect fault bit will be set.

5.3.1.4 Auto-Negotiation Restart

Once Auto-Negotiation has completed, it may be restarted at any time by setting bit 9 (Restart Auto-Negotiation) of the BMCR to one. If the mode configured by a successful Auto-Negotiation loses a valid link, then the Auto-Negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A renegotiation request from any entity, such as a management agent, will cause the DP83849I to halt any transmit data and link pulse activity until the break_link_timer expires (~1500 ms). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The DP83849I will resume Auto-Negotiation after the break_link_timer has expired by issuing FLP (Fast Link Pulse) bursts.

5.3.1.5 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation take approximately 2-3 seconds to complete. In addition, Auto-Negotiation with next page must take approximately 2-3 seconds to complete, depending on the number of next pages sent. Refer to Clause 28 of the IEEE 802.3u standard for a full description of the individual timers related to Auto-Negotiation.

5.3.1.6 Enabling Auto-Negotiation Through Software

It is important to note that if the DP83849I has been initialized upon power-up as a non-auto-negotiating device (forced technology), and it is then required that Auto-Negotiation or re-Auto-Negotiation be initiated through software, bit 12 (Auto-Negotiation Enable) of the Basic Mode Control Register (BMCR) must first be cleared and then set for any Auto-Negotiation function to take effect.

5.3.2 Auto-MDIX

When enabled, this function utilizes Auto-Negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation. The function uses a random seed to control switching of the crossover circuitry. This implementation complies with the corresponding IEEE 802.3 Auto-Negotiation and Crossover Specifications.

Auto-MDIX is enabled by default and can be configured through strap or through PHYCR (19h) register, bits [15:14].

Neither Auto-Negotiation nor Auto-MDIX is required to be enabled in forcing crossover of the MDI pairs. Forced crossover can be achieved through the FORCE_MDIX bit, bit 14 of PHYCR (19h) register.

NOTE

Auto-MDIX will not work in a forced mode of operation.

5.3.3 LED Interface

The DP83849I supports three configurable Light Emitting Diode (LED) pins for each port.

Several functions can be multiplexed onto the three LEDs using three different modes of operation. The LED operation mode can be selected by writing to the LED_CFG[1:0] register bits in the PHY Control Register (PHYCR) at address 19h, bits [6:5]. In addition, LED_CFG[0] for each port can be set by a strap option on the CRS_A and CRS_B pins. LED_CFG[1] is only controllable through register access and cannot be set by as strap pin.

See Table 5-2 for LED Mode selection.

Table 5-2. LED Mode Select

MODE	LED_CFG[1]	LED_CFG[0]	LED_LINK	LED_SPEED	LED_ACT/LED_COL
1	don't care	1	ON for Good Link OFF for No Link	ON in 100 Mb/s OFF in 10 Mb/s	ON for Activity OFF for No Activity
2	0	0	ON for Good Link BLINK for Activity	ON in 100 Mb/s OFF in 10 Mb/s	ON for Collision OFF for No Collision
3	1	0	ON for Good Link BLINK for Activity	ON in 100 Mb/s OFF in 10 Mb/s	ON for Full Duplex OFF for Half Duplex

The LED_LINK pin in Mode 1 indicates the link status of the port. In 100BASE-T mode, link is established as a result of input receive amplitude compliant with the TPPMD specifications which will result in internal generation of signal detect. A 10 Mb/s Link is established as a result of the reception of at least seven consecutive normal Link Pulses or the reception of a valid 10BASE-T packet. This will cause the assertion of LED_LINK. LED_LINK will deassert in accordance with the Link Loss Timer as specified in the IEEE 802.3 specification.

The LED_LINK pin in Mode 1 will be OFF when no LINK is present.

The LED_LINK pin in Mode 2 and Mode 3 will be ON to indicate Link is good and BLINK to indicate activity is present on activity. The BLINK frequency is defined in BLINK_FREQ, bits [7:6] of register LEDCR (18h).

Activity is defined as configured in LEDACT_RX, bit 8 of register LEDCR (18h). If LEDACT_RX is 0, Activity is signaled for either transmit or receive. If LEDACT_RX is 1, Activity is only signaled for receive.

The LED_SPEED pin indicates 10 or 100 Mb/s data rate of the port. The LED is ON when operating in 100Mb/s mode and OFF when operating in 10Mb/s mode. The functionality of this LED is independent of mode selected.

The LED_ACT/LED_COL pin in Mode 1 indicates the presence of either transmit or receive activity. The LED will be ON for Activity and OFF for No Activity. In Mode 2, this pin indicates the Collision status of the port. The LED will be ON for Collision and OFF for No Collision.

The LED_ACT/LED_COL pin in Mode 3 indicates Duplex status for 10 Mb/s or 100 Mb/s operation. The LED will be ON for Full Duplex and OFF for Half Duplex.

In 10 Mb/s half duplex mode, the collision LED is based on the COL signal.

Because these LED pins are also used as strap options, the polarity of the LED is dependent on whether the pin is pulled up or down.

5.3.3.1 LEDs

Because the Auto-Negotiation (AN) strap options share the LED output pins, the external components required for strapping and LED usage must be considered in order to avoid contention.

Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power-up/reset. For example, if a given AN input is resistively pulled low then the corresponding output will be configured as an active high driver. Conversely, if a given AN input is resistively pulled high, then the corresponding output will be configured as an active low driver.

Refer to Figure 5-1 for an example of AN connections to external components at port A. In this example, the AN strapping results in Auto-Negotiation disabled with 100 Full-Duplex forced.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

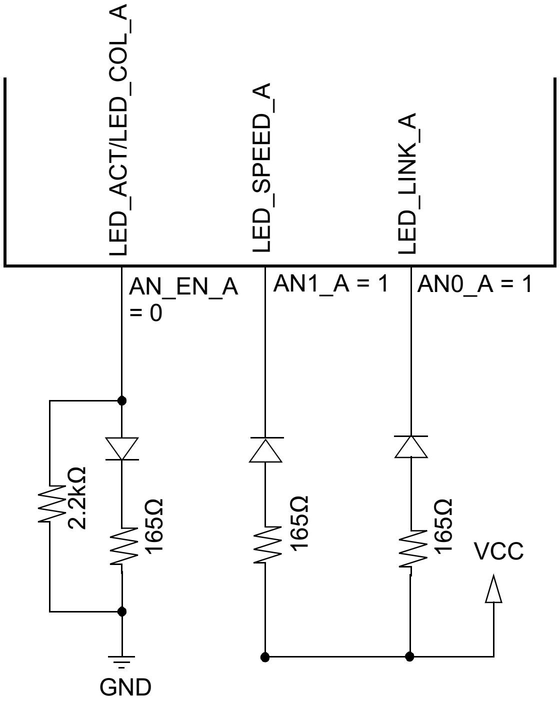


Figure 5-1. AN Strapping and LED Loading Example

5.3.3.2 LED Direct Control

The DP83849I provides another option to directly control any or all LED outputs through the LED Direct Control Register (LEDCR), address 18h. The register does not provide read access to LEDs.

5.3.4 Internal Loopback

The DP83849I includes a Loopback Test mode for facilitating system diagnostics. The Loopback mode is selected through bit 14 (Loopback) of the Basic Mode Control Register (BMCR). Writing 1 to this bit enables MII transmit data to be routed to the MII receive outputs. Loopback status may be checked in bit 3 of the PHY Status Register (PHYSTS). While in Loopback mode the data will not be transmitted onto the media. To ensure that the desired operating mode is maintained, Auto-Negotiation must be disabled before selecting the Loopback mode.

5.3.5 BIST

The DP83849I incorporates an internal Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be utilized to test the integrity of the transmit and receive data paths. BIST testing can be performed with the part in the internal loopback mode or externally looped back using a loopback cable fixture.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo random sequence. The user can select a 9 bit or 15 bit pseudo random sequence from the PSR_15 bit in the PHY Control Register (PHYCR). The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass/fail status.

The pass/fail status of the BIST is stored in the BIST status bit in the PHYCR register. The status bit defaults to 0 (BIST fail) and will transition on a successful comparison. If an error (mis-compare) occurs, the status bit is latched and is cleared upon a subsequent write to the Start/Stop bit.

For transmit VOD testing, the Packet BIST Continuous Mode can be used to allow continuous data transmission, setting BIST_CONT_MODE, bit 5, of CDCTRL1 (1Bh).

The number of BIST errors can be monitored through the BIST Error Count in the CDCTRL1 (1Bh), bits [15:8].

5.3.6 Energy Detect Mode

When Energy Detect is enabled and there is no activity on the cable, the DP83849I will remain in a low power mode while monitoring the transmission line. Activity on the line will cause the DP83849I to go through a normal power up sequence. Regardless of cable activity, the DP83849I will occasionally wake up the transmitter to put ED pulses on the line, but will otherwise draw as little power as possible. Energy detect functionality is controlled through register Energy Detect Control (EDCR), address 1Dh.

5.3.7 Link Diagnostic Capabilities

The DP83849I contains several system diagnostic capabilities for evaluating link quality and detecting potential cabling faults in Twisted Pair cabling. Software configuration is available through the Link Diagnostics Registers – Page 2 which can be selected through Page Select Register (PAGESEL), address 13h. These capabilities include:

- Linked Cable Status
- Link Quality Monitor
- TDR (Time Domain Reflectometry) Cable Diagnostics

5.3.7.1 Linked Cable Status

In an active connection with a valid link status, the following diagnostic capabilities are available:

- Polarity reversal
- Cable swap (MDI vs MDIX) detection
- 100Mb Cable Length Estimation
- Frequency offset relative to link partner
- Cable Signal Quality Estimation

5.3.7.2 Polarity Reversal

The DP83849I detects polarity reversal by detecting negative link pulses. The Polarity indication is available in bit 12 of the PHYSTS (10h) or bit 4 of the 10BTSCR (1Ah). Inverted polarity indicates the positive and negative conductors in the receive pair are swapped. Because polarity is corrected by the receiver, this does not necessarily indicate a functional problem in the cable.

Because the polarity indication is dependent on link pulses from the link partner, polarity indication is only valid in 10Mb modes of operation, or in 100Mb Auto-Negotiated mode. Polarity indication is not available in 100Mb forced mode of operation or in a parallel detected 100Mb mode.

5.3.7.2.1 Cable Swap Indication

As part of Auto-Negotiation, the DP83849I has the ability (using Auto-MDIX) to automatically detect a cable with swapped MDI pairs and select the appropriate pairs for transmitting and receiving data. Normal operation is termed MDI, while crossed operation is MDIX. The MDIX status can be read from bit 14 of the PHYSTS (10h).

5.3.7.2.2 100 MB Cable Length Estimation

The DP83849I provides a method of estimating cable length based on electrical characteristics of the 100Mb Link. This essentially provides an effective cable length rather than a measurement of the physical cable length. The cable length estimation is only available in 100Mb mode of operation with a valid Link status. The cable length estimation is available at the Link Diagnostics Registers – Page 2, register 100Mb Length Detect (LEN100_DET), address 14h.

5.3.7.2.3 Frequency Offset Relative to Link Partner

As part of the 100Mb clock recovery process, the DSP implementation provides a frequency control parameter. This value may be used to indicate the frequency offset of the device relative to the link partner. This operation is only available in 100Mb operation with a valid link status. The frequency offset can be determined using the register 100Mb Frequency Offset Indication (FREQ100), address 15h, of the Link Diagnostics Registers – Page 2.

Two different versions of the Frequency Offset may be monitored through bits [7:0] of register FREQ100 (15h). The first is the long-term Frequency Offset. The second is the current Frequency Control value, which includes short- term phase adjustments and can provide information on the amount of jitter in the system.

5.3.7.2.4 Cable Signal Quality Estimation

The cable signal quality estimator keeps a simple tracking of results of the DSP and can be used to generate an approximate Signal-to-Noise Ratio for the 100Mb receiver. This information is available to software through the Link Diagnostics Registers – Page 2: Variance Control (VAR_CTRL), address 1Ah and Data (VAR_DATA), address 1Bh.

The variance computation times (VAR_TIMER) can be chosen from the set of {2, 4, 6, 8} ms. The 32-bit variance sum can be read by two consecutive reads of the VAR_DATA register. This sum can be used to compute an SNR estimate by software using the following equation: SNR = 10log10((37748736 × VAR_TIMER) / Variance).

5.3.7.2.5 Link Quality Monitor

The Link Quality Monitor allows a method to generate an alarm when the DSP adaption strays from a programmable window. This could occur due to changes in the cable which could indicate a potential problem. Software can program thresholds for the following DSP parameters to be used to interrupt the system:

- Digital Equalizer C1 Coefficient (DEQ C1)
- Digital Adaptive Gain Control (DAGC)
- Digital Base-Line Wander Control (DBLW)
- Recovered Clock Long-Term Frequency Offset (FREQ)
- Recovered Clock Frequency Control (FC)

Software is expected to read initial adapted values and then program the thresholds based on an expected valid range. This mechanism takes advantage of the fact that the DSP adaption must remain in a relatively small range once a valid link has been established.

5.3.7.3 Link Quality Monitor Control and Status

Control of the Link Quality Monitor is done through the Link Quality Monitor Register (LQMR), address 1Dh and the Link Quality Data Register (LQDR), address 1Bh of the Link Diagnostics Registers – Page 2. The LQMR register includes a global enable to enable the Link Quality Monitor function. In addition, it provides warning status from both high and low thresholds for each of the monitored parameters. Note that individual low or high parameter threshold comparisons can be disabled by setting to the minimum or maximum values.

To allow the Link Quality Monitor to interrupt the system, the Interrupt must be enabled through the interrupt control registers, MICR (11h) and MISR (12h).

5.3.7.3.1 Checking Current Parameter Values

Prior to setting Threshold values, it is recommended that software check current adapted values. The thresholds may then be set relative to the adapted values. The current adapted values can be read using the LQDR register by setting the Sample_Param bit [13] of LQDR, address (1Eh).

For example, to read the DBLW current value:

1. Write 2400h to LQDR (1Eh) to set the Sample_Param bit and set the LQ_PARAM_SEL[2:0] to 010.
2. Read LQDR (1Eh). Current DBLW value is returned in the low 8 bits.

5.3.7.3.2 Threshold Control

The LQDR (1Eh) register also provides a method of programming high and low thresholds for each of the four parameters that can be monitored. The register implements an indirect read/write mechanism.

Writes are accomplished by writing data, address, and a write strobe to the register. Reads are accomplished by writing the address to the register, and reading back the value of the selected threshold. Setting thresholds to the maximum or minimum values will disable the threshold comparison because values have to exceed the threshold to generate a warning condition.

Warnings are not generated if the parameter is equal to the threshold. By default, all thresholds are disabled by setting to the min or max values. Table 5-3 shows the four parameters and range of values.

Table 5-3. Link Quality Monitor Parameter Ranges

PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	MIN (2-s comp)	MAX (2-s comp)
DEQ C1	–128	+127	0x80	0x7F
DAGC	0	+255	0x00	0xFF
DBLW	–128	+127	0x80	0x7F
Frequency Offset	–128	+127	0x80	0x7F
Frequency Control	–128	+127	0x80	0x7F

5.3.7.4 TDR Cable Diagnostics

The DP83849I implements a Time Domain Reflectometry (TDR) method of cable length measurement and evaluation which can be used to evaluate a connected twisted pair cable. The TDR implementation involves sending a pulse out on either the Transmit or Receive conductor pair and observing the results on either pair. By observing the types and strength of reflections on each pair, software can determine the following:

- Cable short
- Cable open
- Distance to fault
- Identify which pair has a fault
- Pair skew

The TDR cable diagnostics works best in certain conditions. For example, an unterminated cable provides a good reflection for measuring cable length, while a cable with an ideal termination to an unpowered partner may pro- vide no reflection at all.

5.3.7.4.1 TDR Pulse Generator

The TDR implementation can send two types of TDR pulses. The first option is to send 50-ns or 100-ns link pulses from the 10-Mb Common Driver. The second option is to send pulses from the 100-Mb Common Driver in 8-ns increments up to 56 ns in width. The 100-Mb pulses will alternate between positive and negative pulses. The shorter pulses provide better ability to measure short cable lengths, especially because they will limit overlap between the transmitted pulse and a reflected pulse. The longer pulses may provide better measurements of long cable lengths.

In addition, if the pulse width is programmed to 0, no pulse will be sent, but monitor circuit will still be activated. This allows sampling of background data to provide a baseline for analysis.

5.3.7.4.2 TDR Pulse Monitor

The TDR function monitors data from the Analog to Digital Converter (ADC) to detect both peak values and values above a programmable threshold. It can be programmed to detect maximum or minimum values. In addition, it records the time, in 8-ns intervals, at which the peak or threshold value first occurs.

The TDR monitor implements a timer that starts when the pulse is transmitted. A window may be enabled to qualify incoming data to look for response only in a desired range. This is especially useful for eliminating the transmitted pulse, but also may be used to look for multiple reflections.

5.3.7.4.3 TDR Control Interface

The TDR Control interface is implemented in the Link Diagnostics Registers – Page 2 through TDR Control (TDR_CTRL), address 16h and TDR Window (TDR_WIN), address 17h. The following basic controls are:

- **TDR Enable:** Enable bit 15 of TDR_CTRL (16h) to allow the TDR function. This bypasses normal operation and gives control of the CD10 and CD100 block to the TDR function.
- **TDR Send Pulse:** Enable bit 11 of TDR_CTRL (16h) to send the TDR pulse and starts the TDR Monitor.

The following Transmit mode controls are available:

- **Transmit Mode:** Enables use of 10Mb Link pulses from the 10Mb Common Driver or data pulses from the 100Mb Common Driver by enabling TDR 100Mb, bit 14 of TDR_CRTL (16h)
- **Transmit Pulse Width:** Bits [10:8] of TDR_CTRL (16h) allows sending of 0 to 7 clock width pulses. Actual pulses are dependent on the transmit mode. If Pulse Width is set to 0, then no pulse will be sent.
- **Transmit Channel Select:** The transmitter can send pulses down either the transmit pair or the receive pair by enabling bit 13 of TDR_CTRL (16h). Default value is to select the transmit pair.

The following Receive mode controls are available

- **Min/Max Mode Select:** Bit 7 of TDR_CTRL (16h) controls the TDR Monitor operation. In default mode, the monitor will detect maximum (positive) values. In Min mode, the monitor will detect minimum (negative) values.
- **Receive Channel Select:** The receiver can monitor either the transmit pair or the receive pair by enabling bit 12 of TDR_CTRL (16h). Default value is to select the transmit pair.
- **Receive Window:** The receiver can monitor receive data within a programmable window using the TDR Window Register (TDR_WIN), address 17h. The window is controlled by two register values: TDR Start Window, bits [15:8] of TDR_WIN (17h) and TDR Stop Window, bits [7:0] of TDR_WIN (17h). The TDR Start Window indicates the first clock to start sampling. The TDR Stop Window indicates the last clock to sample. By default, the full window is enabled, with Start set to 0 and Stop set to 255. The window range is in 8ns clock increments, so the maximum window size is 2048 ns.

5.3.7.4.4 TDR Results

The TDR function monitors data from the Analog to Digital Converter (ADC) to detect both peak values and values above a programmable threshold. It can be programmed to detect maximum or minimum values. In addition, it records the time, in 8ns intervals, at which the peak or threshold value first occurs. The results of a TDR peak and threshold measurement are available in the TDR Peak Measurement Register (TDR_PEAK), address 18h and TDR Threshold Measurement Register (TDR_THR), address 19h. The threshold measurement may be a more accurate method of measuring the length for longer cables to provide a better indication of the start of the received pulse, rather than the peak value.

Software utilizing the TDR function must implement an algorithm to send TDR pulses and evaluate results. Multiple runs must be used to best qualify any received pulses as multiple reflections could exist. In addition, when monitoring the transmitting pair, the window feature must be used to disqualify the transmitted pulse. Multiple runs may also be used to average the values providing more accurate results.

Actual distance measurements are dependent on the velocity of propagation of the cable. The delay value is typically on the order of 4.6 to 4.9 ns/m.

5.4 Device Functional Modes

The DP83849I supports several modes of operation using the MII interface pins. The options are defined in the following sections and include:

- MII Mode
- RMII Mode
- 10 Mb Serial Network Interface (SNI)
- Single Clock MII Mode (SCMII)

In addition, the DP83849I supports the standard 802.3u MII Serial Management Interface and a Flexible MII Port Assignment scheme.

The modes of operation can be selected by strap options or register control. For RMII mode, it is required to use the strap option, because it requires a 50-MHz clock instead of the normal 25 MHz.

In each of these modes, the IEEE 802.3 serial management interface is operational for device configuration and status. The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHY(s).

5.4.1 MII Interface

The DP83849I incorporates the Media Independent Interface (MII) as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. This section describes the nibble wide MII data interface.

The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

5.4.1.1 Nibble-wide MII Data Interface

Clause 22 of the IEEE 802.3u specification defines the Media Independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and status signals, allow for the simultaneous exchange of data between the DP83849I and the upper layer agent (MAC).

The receive interface consists of a nibble wide data bus RXD[3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at either 2.5 MHz to support 10 Mb/s operation modes or at 25 MHz to support 100 Mb/s operational modes.

The transmit interface consists of a nibble wide data bus TXD[3:0], a transmit enable control signal TX_EN, and a transmit clock TX_CLK which runs at either 2.5 MHz or 25 MHz.

Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation when both a transmit and receive operation occur simultaneously.

5.4.1.2 Collision Detect

For Half Duplex, a 10BASE-T or 100BASE-TX collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

If the DP83849I is transmitting in 10 Mb/s mode when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision.

If a collision occurs during a receive operation, it is immediately reported by the COL signal.

When heartbeat is enabled (only applicable to 10 Mb/s operation), approximately 1M s after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

5.4.1.3 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity, once valid data is detected through the squelch function during 10 Mb/s operation. During 100 Mb/s operation CRS is asserted when a valid link (SD) and two non-contiguous zeros are detected on the line.

For 10 or 100 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10 or 100 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

5.4.2 Reduced MII Interface

The DP83849I incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification (rev1.2) from the RMII Consortium. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems using a reduced number of pins. In this mode, data is transferred 2-bits at a time using the 50 MHz RMII_REF clock for both transmit and receive. The following pins are used in RMII mode:

- TX_EN
- TXD[1:0]
- RX_ER (optional for Mac)
- CRS_DV
- RXD[1:0]
- X1 (RMII Reference clock is 50 MHz)

In addition, the RMII mode supplies an RX_DV signal which allows for a simpler method of recovering receive data without having to separate RX_DV from the CRS_DV indication. This is especially useful for diagnostic testing where it may be desirable to externally loop Receive MII data directly to the transmitter.

The RX_ER output may be used by the MAC to detect error conditions. It is asserted for symbol errors received during a packet, False Carrier events, and also for FIFO underrun or overrun conditions. Because the Phy is required to corrupt receive data on an error, a MAC is not required to use RX_ER.

It is important to note that because both digital channels in the DP83849I share the X1/RMII_REF input, both channels must have RMII mode enabled or both channels must have RMII mode disabled. Either channel may be in 10Mb or 100Mb mode in RMII or non-RMII mode.

Because the reference clock operates at 10 times the data rate for 10 Mb/s operation, transmit data is sampled every 10 clocks. Likewise, receive data will be generated every 10th clock so that an attached device can sample the data every 10 clocks.

RMII mode requires a 50-MHz oscillator be connected to the device X1 pin. A 50-MHz crystal is not supported.

To tolerate potential frequency differences between the 50-MHz reference clock and the recovered receive clock, the receive RMII function includes a programmable elasticity buffer. The elasticity buffer is programmable to minimize propagation delay based on expected packet size and clock accuracy. This allows for supporting a range of packet sizes including jumbo frames.

The elasticity buffer will force Frame Check Sequence errors for packets which overrun or underrun the FIFO. Underrun and Overrun conditions can be reported in the RMII and Bypass Register (RBR). Table 5-4 indicates how to program the elasticity buffer FIFO (in 4-bit increments) based on expected max packet size and clock accuracy. It assumes both clocks (RMII Reference clock and far-end Transmitter clock) have the same accuracy.

Packet lengths can be scaled linearly based on accuracy (±25 ppm would allows packets twice as large). If the threshold setting must support both 10-Mb and 100-Mb operation, the setting must be made to support both speeds.

Table 5-4. Supported Packet Sizes at ±50 ppm Frequency Accuracy

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE		RECOMMENDED PACKET SIZE AT ±50 ppm	
	100 Mb	10 Mb	100 Mb	10 Mb
01 (default)	2 bits	8 bits	2,400 bytes	9,600 bytes
10	6 bits	4 bits	7,200 bytes	4,800 bytes
11	10 bits	8 bits	12,000 bytes	9,600 bytes
00	14 bits	12 bits	16,800 bytes	14,400 bytes

5.4.3 802.3u MII Serial Management Interface

5.4.3.1 Serial Management Register Access

The serial management MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO. The DP83849I implements all the required MII registers as well as several optional registers. These registers are fully described in *Section 5.6*. A description of the serial management access protocol follows.

In addition, the MDIO pin requires a pullup resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83849I with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pullup resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition 32 MDC clock cycles must be used to re-sync the device if an invalid start, opcode, or turnaround bit is detected.

The DP83849I waits until it has received this preamble sequence before responding to any other transaction. Once the DP83849I serial management port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid Start, invalid Opcode, or invalid turnaround bit has occurred.

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of Turnaround. The addressed DP83849I drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 5-2 shows the timing relationship between MDC and the MDIO as driven/received by the Station (STA) and the DP83849I (PHY) for a typical register read access.

For write transactions, the station management entity writes data to the addressed DP83849I thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 5-3 shows the timing relationship for a typical MII register write access.

Table 5-5. Typical MDIO Frame Format

MII Management Serial Protocol	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

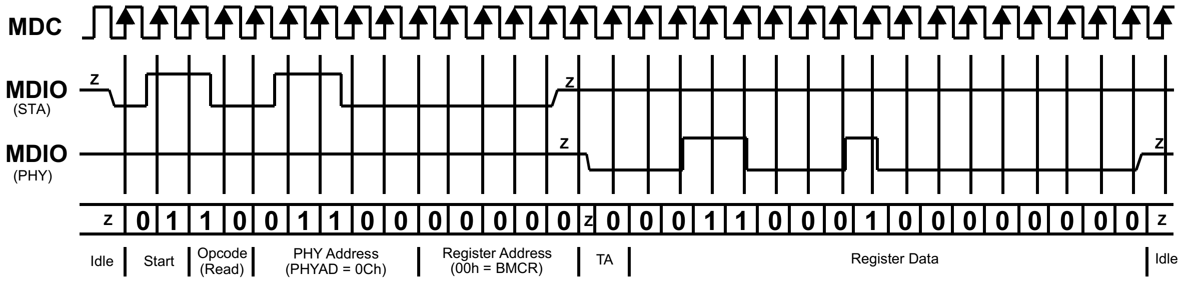


Figure 5-2. Typical MDC/MDIO Read Operation

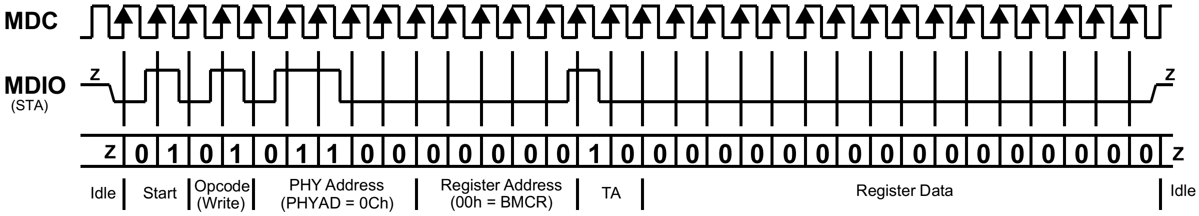


Figure 5-3. Typical MDC/MDIO Write Operation

5.4.3.2 Serial Management Preamble Suppression

The DP83849I supports a Preamble Suppression mode as indicated by a one in bit 6 of the Basic Mode Status Register (BMSR, address 01h.) If the station management entity (that is, MAC or other management controller) determines that all PHYs in the system support Preamble Suppression by returning a one in this bit, then the station management entity need not generate preamble for each management transaction.

The DP83849I requires a single initialization sequence of 32 bits of preamble following hardware/software reset. This requirement is generally met by the mandatory pullup resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether Preamble Suppression is supported.

While the DP83849I requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32-bit sequence between each subsequent transaction. A minimum of one idle bit between management transactions is required as specified in the IEEE 802.3u specification.

5.4.3.3 Simultaneous Register Write

The DP83849I incorporates a mode which allows simultaneous write access to both Port A and B register blocks at the same time. This mode is selected by setting bit 15 of RMII and Bypass Register (RBR, address 17h) in Port A.

As long as this bit remains set, subsequent writes to Port A will write to registers in both ports.

Register reads are unaffected. Each port must still be read individually.

5.4.4 MAC Interface

5.4.4.1 10-Mb Serial Network Interface (SNI)

The DP83849I incorporates a 10-Mb Serial Network Interface (SNI) which allows a simple serial data interface for 10 Mb only devices. This is also referred to as a 7-wire interface. While there is no defined standard for this interface, it is based on early 10-Mb physical layer devices. Data is clocked serially at 10 MHz using separate transmit and receive paths. The following pins are used in SNI mode:

- TX_CLK
- TX_EN
- TXD[0]
- RX_CLK
- RXD[0]
- CRS
- COL

5.4.4.2 Single Clock MII Mode

Single Clock MII (SCMII) Mode allows MII operation using a single 25-MHz reference clock. Normal MII Mode requires three clocks, a reference clock for physical layer functions, a Transmit MII clock, and a Receive MII clock. Similar to RMII mode, Single Clock MII mode requires only the reference clock. In addition to reducing the number of pins required, this mode allows the attached MAC device to use only the reference clock domain. Because the DP83849I has two ports, this actually reduces the number of clocks from 6 to 1. A/C Timing requirements for SCMII operation are similar to the RMII timing requirements.

For 10-Mb operation, as in RMII mode, data is sampled and driven every 10 clocks because the reference clock is at 10x the data rate.

Separate control bits allow enabling the Transmit and Receive Single Clock modes separately, allowing just transmit or receive to operate in this mode. Control of Single Clock MII mode is through the RBR register.

Single Clock MII mode incorporates the use of the RMII elasticity buffer, which is required to tolerate potential frequency differences between the 25-MHz reference clock and the recovered receive clock. Settings for the Elasticity Buffer for SCMII mode are detailed in Table 5-6.

Table 5-6. Supported SCMII Packet Sizes at ±50 ppm Frequency Accuracy

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE		RECOMMENDED PACKET SIZE AT ±50 ppm	
	100 Mb	10 Mb	100 Mb	10 Mb
01 (default)	4 bits	8 bits	4,000 bytes	9,600 bytes
10	4 bits	8 bits	4,000 bytes	9,600 bytes
11	12 bits	8 bits	96,00 bytes	9,600 bytes
00	12 bits	8 bits	96,00 bytes	9,600 bytes

5.4.4.3 Flexible MII Port Assignment

The DP83849I supports a flexible assignment scheme for each of the channels to the MII/RMII interface. Either of the MII ports may be assigned to the internal channels A/B. These values are controlled by the RMII and Bypass Register (RBR), address 17h. Transmit assignments and Receive assignments can be made separately to allow even more flexibility (that is, both channels could transmit from MII A while still allowing separate receive paths for the channels).

In addition, the opposite receive channel may be used as the transmit source for each channel. As shown in Figure 5-4, Channel A receive data may be used as the Channel B transmit data source while Channel B receive data may be used as the Channel A transmit data source. For proper clock synchronization, this function requires the device be in RMII mode or Single Clock MII mode of operation. A configuration strap is provided on pin 56, RXD2_B/EXTENDER_EN to enable this mode.

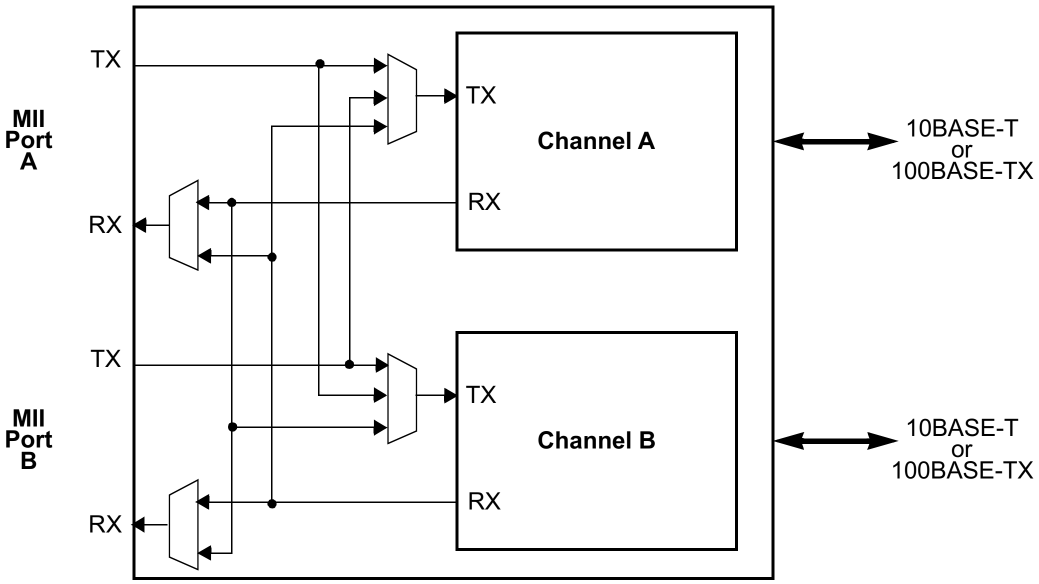


Figure 5-4. MII Port Mapping

5.4.4.3.1 RX MII Port Mapping

Note that Channel A is the master of MII Port A, and Channel B is the master of MII Port B. This means that in order for Channel B to control MII Port A, Channel A must be configured to either control MII Port B or be Disabled; the reverse is also true.

RX MII Port Mapping controls and configurations are shown in Table 5-7 and Table 5-8:

Table 5-7. RX MII Port Mapping Controls

RBR[12:11]	Desired RX Channel Destination
00	Normal Port
01	Opposite Port
10	Both Ports
11	Disabled

Table 5-8. RX MII Port Mapping Configurations

Channel A RBR[12:11]	Channel B RBR[12:11]	RX MII Port A Source	RX MII Port B Source
00	00	Channel A	Channel B
00	01	Channel A	Channel B
00	10	Channel A	Channel B
00	11	Channel A	Disabled
01	00	Channel A	Channel B
01	01	Channel B	Channel A
01	10	Channel B	Channel A
01	11	Disabled	Channel A
10	00	Channel A	Channel B
10	01	Channel B	Channel A
10	10	Channel A	Channel B
10	11	Channel A	Channel A
11	00	Disabled	Channel B
11	01	Channel B	Disabled

Table 5-8. RX MII Port Mapping Configurations (continued)

Channel A RBR[12:11]	Channel B RBR[12:11]	RX MII Port A Source	RX MII Port B Source
11	10	Channel B	Channel B
11	11	Disabled	Disabled

5.4.4.3.2 *TX MII Port Mapping*

TX MII Port Mapping controls and configurations are shown in Table 5-9 and Table 5-10:

Table 5-9. TX MII Port Mapping Controls

RBR[12:11]	Desired RX Channel Destination
00	Normal Port
01	Opposite Port
10	Opposite RX Port
11	Disabled

Table 5-10. TX MII Port Mapping Configurations

Channel A RBR[10:9]	Port A TX Source	Channel B RBR[10:9]	Port B TX Source
00	MII Port A	00	MII Port B
01	MII Port B	01	MII Port A
10	RX Channel B	10	RX Channel A
11	Disabled	11	Disabled

5.4.4.3.3 *Common Flexible MII Port Configurations*

Table 5-11. Common Flexible MII Port Configurations

Mode	Channel A RBR[12:9]	Channel B RBR[12:9]	Description
Normal	0	0	MII port A assigned to Channel A, MII Port B assigned to Channel B
Full Port Swap	101	101	MII port A assigned to Channel B, MII Port B assigned to Channel A
Extender	1110	1110	MII RX disabled, Channel A transmits from Channel B RX data, Channel B transmits from Channel A RX data
Broadcast TX MII Port A	xx00	xx01	Both Channels transmit from TX MII Port A
Broadcast TX MII Port B	xx01	xx00	Both Channels transmit from TX MII Port B
Mirror RX Channel A	10xx	11xx	Channel A RX traffic appears on both Ports.
Mirror RX Channel B	11xx	10xx	Channel B RX traffic appears on both Ports.
Disable Port A	1111	xxxx	MII Port A is disabled
Disable Port B	xxxx	1111	MII Port B is disabled

5.4.4.4 Strapped Extender Mode

The DP83849I provides a simple strap option to automatically configure both channels for Extender Mode with no device register configuration necessary. The EXTENDER_EN Strap can be used in conjunction with the Auto-Negotiation Straps (AN_EN, AN0, AN1), the RMII Mode Strap to allow many possible configurations. If Extender Mode is strapped but RMII Mode is not, both channels will automatically be configured for Single Clock MII Receive and Transmit Modes. The optional use of RMII Mode in conjunction with Extender Mode allows flexibility in the system design.

Several common configurations are shown in Table 5-12.

Table 5-12. Common Strapped Extender Mode Configurations

Mode	Auto-Negotiation Straps
100-Mb Copper Extender	Both channels are forced to 100-Mb Full Duplex
10-Mb Copper Extender	Both channels are forced to 10-Mb Full Duplex

5.4.4.5 Notes and Restrictions

- **Extender:** Both channels must be operating at the same speed (10-Mb or 100-Mb). This can be accomplished using straps or channel register controls. Both channels must be in Full Duplex mode. Both channels must either be in RMII Mode (RBR:RMII_EN = 1) or full Single Clock MII Mode (RBR:SCMII_RX = 1 and RBR:SCMII_TX = 1) to ensure synchronous operation. If only one RX to TX path is enabled, SCMII_RX in the RX channel (RBR register 17h bit 7) and SCMII_TX in the TX channel (RBR register 17h bit 6) must be set to 1.
- **Broadcast TX MII Port Mode:** To ensure synchronous operation, both channels must be in RMII Mode (RBR register 17h bit 5 = 1) or in Single Clock TX MII Mode (RBR register 17h bit 6 = 1). Both channels must be operating at the same speed (10 or 100Mb). Both channels must be in Full Duplex mode to ensure no collisions are seen. This is because in Single Clock TX MII Mode, a collision on one PHY channel would cause both channels to send the Jam pattern.
- **RMII Mode:** Both Channels must have RMII Mode enabled or disabled concurrently due to the internal reference clocking scheme. In Full Port Swap Mode, Channels are not required to have a common speed.
- **10Base-T Serial Mode:** This MAC-side mode, also known as Serial Network Interface (SNI), may not be used when both channels share data connections (Extender or Broadcast TX MII Port). This is due to the requirement of synchronous operation between channels, which is not supported in SNI Mode.
- **CRS Assignment:** When a channel is not in RMII Mode, its associated CRS pin is sourced from the transmitter and controlled by the TX MII Port Assignment, bits [10:9] of RBR (17h). When a channel is in RMII Mode, the associated CRS pin is sourced from the receiver and controlled by the RX MII Port Assignment, bits [12:11] of RBR (17h).
- **Output Enables:** Flexible MII Port Assignment does not control signal output enables.
- **Test Modes:** Test modes are not designed to be compatible with Flexible MII Port Selection, which assumes default MII pin directions.
- **LED Assignment:** LEDs are associated with their respective digital channels, and therefore do not get mapped to alternate channels. For example, assertion of LED_LINK_A indicates valid link status for Channel A independent of the MII Port Assignment.
- **Straps:** Strap pins are always associated with their respective channel, that is, a strap on RX_ER_A is used by Channel A.
- **Port Isolate Mode:** Each MII port's Isolate function, bit 10 of BMCR (00h) is always associated with its respective channel, that is, the Isolate function for Port A is always controlled by Channel A's BMCR (00h). Due to the various possible combinations of TX and RX port selection, it may not be advisable to place a port in Isolate mode.
- **Energy Detect and Powerdown Modes:** The output enables for each MII port are always controlled by the respective channel Energy Detect and Powerdown functions. These functions must be disabled whenever an MII port is in use but not assigned to its default channel. Note that Extender/Media Converter modes allow the use of Energy Detect and Powerdown modes if the RX MII ports are not in use.

5.4.5 PHY Address

The 4 PHY address inputs pins are shown in Table 5-13.

Table 5-13. PHY Address Mapping

PIN NO.	PHYAD FUNCTION	RXD FUNCTION
4	PHYAD1	RXD0_A
5	PHYAD2	RXD1_A
58	PHYAD3	RXD0_B
57	PHYAD4	RXD1_B

The DP83849I provides four address strap pins for determining the PHY addresses for ports A and B of the device. The 4 address strap pins provide the upper four bits of the PHY address. The lowest bit of the PHY address is dependent on the port. Port A has a value of 0 for the PHY address bit 0 while port B has a value of 1. The PHY address strap input pins are shown in Table 5-13.

The PHY address strap information is latched into the PHYCR register (address 19h, bits [4:0]) at device power-up and hardware reset. The PHY Address pins are shared with the RXD pins. Each DP83849I or port sharing an MDIO bus in a system must have a unique physical address.

The DP83849I supports PHY Address strapping of Port A to even values 0 (<0000_0>) through 30 (<1111_0>). Port B is strapped to odd values 1 (<0000_1>) through 31 (<1111_1>). Note that Port B address is always 1 greater than Port A address.

For further detail relating to the latch-in timing requirements of the PHY Address pins, as well as the other hardware configuration pins, refer to the Reset summary in *Section 5.4.7*.

Refer to Figure 5-5 for an example of a PHYAD connection to external components. In this example, the PHYAD strapping results in address 00010 (02h) for Port A and address 00011 (03h) for Port B.

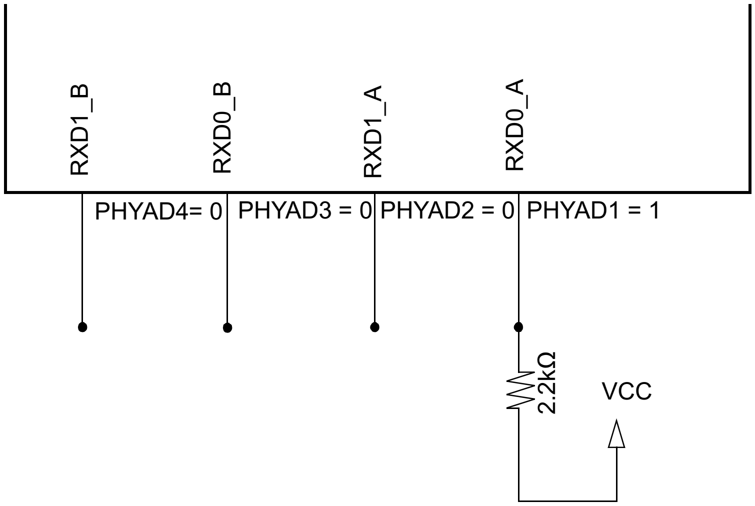


Figure 5-5. PHYAD Strapping Example

5.4.5.1 MII Isolate Mode

TThe DP83849I can be put into MII Isolate mode by writing to bit 10 of the BMCR register.

When in the MII isolate mode, the DP83849I does not respond to packet data present at TXD[3:0], TX_EN inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. When in Isolate mode, the DP83849I will continue to respond to all management transactions.

While in Isolate mode, the PMD output pair will not transmit packet data but will continue to source 100BASE-TX scrambled idles or 10BASE-T normal link pulses.

The DP83849I can Auto-Negotiate or parallel detect to a specific technology depending on the receive signal at the PMD input pair. A valid link can be established for the receiver even when the DP83849I is in Isolate mode.

5.4.6 Half Duplex vs Full Duplex

The DP83849I supports both half and full duplex operation at both 10-Mb/s and 100-Mb/s speeds.

Half-duplex relies on the CSMA/CD protocol to handle collisions and network access. In Half-Duplex mode, CRS responds to both transmit and receive activity in order to maintain compliance with the IEEE 802.3 specification.

Because the DP83849I is designed to support simultaneous transmit and receive activity it is capable of supporting full-duplex switched applications with a throughput of up to 200 Mb/s per port when operating in 100BASE-TX. Because the CSMA/CD protocol does not apply to full-duplex operation, the DP83849I disables its own internal collision sensing and reporting functions and modifies the behavior of Carrier Sense (CRS) such that it indicates only receive activity. This allows a full-duplex capable MAC to operate properly.

All modes of operation (100BASE-TX, 10BASE-T) can run either half-duplex or full-duplex. Additionally, other than CRS and Collision reporting, all remaining MII signaling remains the same regardless of the selected duplex mode.

It is important to understand that while Auto-Negotiation with the use of Fast Link Pulse code words can interpret and configure to full-duplex operation, parallel detection can not recognize the difference between full and half-duplex from a fixed 10-Mb/s or 100-Mb/s link partner over twisted pair. As specified in the 802.3u specification, if a far-end link partner is configured to a forced full duplex 100BASE-TX ability, the parallel detection state machine in the partner would be unable to detect the full duplex capability of the far-end link partner. This link segment would negotiate to a half duplex 100BASE-TX configuration (same scenario for 10Mb/s). It is important to understand that while Auto-Negotiation with the use of Fast Link Pulse code words can interpret and configure to full-duplex operation, parallel detection can not recognize the difference between full and half-duplex from a fixed 10-Mb/s or 100-Mb/s link partner over twisted pair. As specified in the 802.3u specification, if a far-end link partner is configured to a forced full duplex 100BASE-TX ability, the parallel detection state machine in the partner would be unable to detect the full duplex capability of the far-end link partner. This link segment would negotiate to a half duplex 100BASE-TX configuration (same scenario for 10 Mb/s).

5.4.7 Reset Operation

The DP83849I includes an internal power-on reset (POR) function and does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

5.4.7.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to the RESET_N pin. This will reset the device such that all registers will be reinitialized to default values and the hardware configuration values will be re-latched into the device (similar to the power-up/reset operation).

5.4.7.2 Full Software Reset

A full-chip software reset is accomplished by setting the reset bit (bit 15) of the Basic Mode Control Register (BMCR). The period from the point in time when the reset bit is set to the point in time when software reset has concluded is approximately 1 µs.

The software reset will reset the device such that all registers will be reset to default values and the hardware configuration values will be maintained. Software driver code must wait 3 µs following a software reset before allowing further serial MII operations with the DP83849I.

5.4.7.3 Soft Reset

A partial software reset can be initiated by setting the Soft Reset bit (bit 9) in the PHYCR2 Register. Setting this bit will reset all transmit and receive operations, but will not reset the register space. All register configurations will be pReserved. Register space will remain available following a Soft Reset.

5.5 Programming

5.5.1 Architecture

This section describes the operations within each transceiver module, 100BASE-TX and 10BASE-T. Each operation consists of several functional blocks and described in the following:

- 100BASE-TX Transmitter
- 100BASE-TX Receiver
- 10BASE-T Transceiver Module

5.5.1.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mb/s serial data stream. Because the 100BASE-TX TP-PMD is integrated, the differential output pins, PMD Output Pair, can be directly routed to the magnetics

The block diagram in Figure 5-6. provides an overview of each functional block within the 100BASE-TX transmit section.

The Transmitter section consists of the following functional blocks:

- Code-group Encoder and Injection block
- Scrambler block (bypass option)
- NRZ to NRZI encoder block
- Binary to MLT-3 converter / Common Driver

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83849I implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

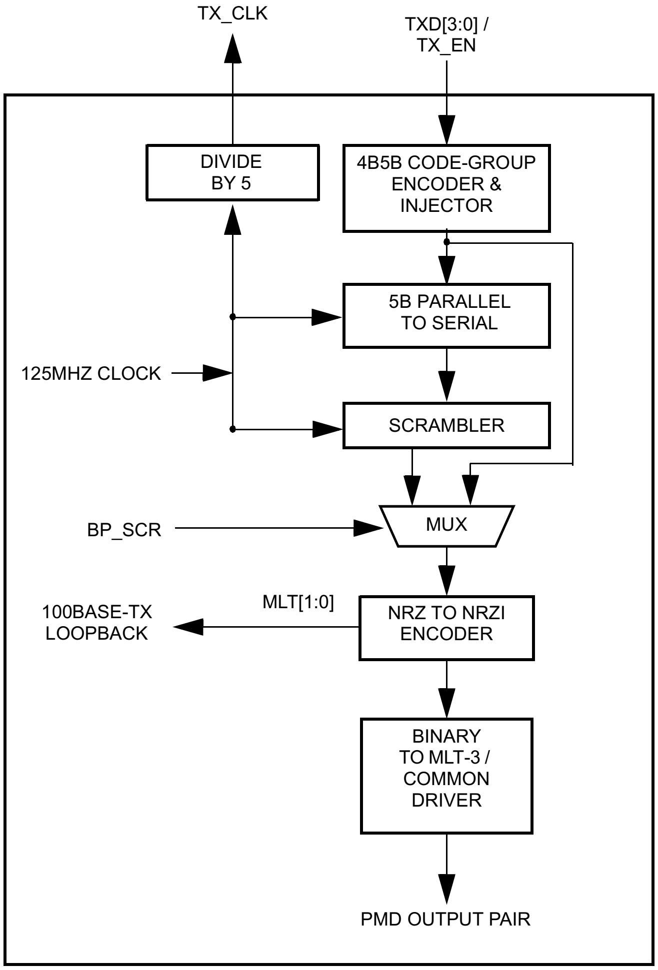


Figure 5-6. 100BASE-TX Transmit Block Diagram

Table 5-14. 4B5B Code-Group Encoding/Decoding

DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111

Table 5-14. 4B5B Code-Group Encoding/Decoding (continued)

DATA CODES		
IDLE AND CONTROL CODES		
H	00100	HALT code-group Error code
I	11111	Inter-Packet IDLE - 0000 (1)
J	11000	First Start of Packet - 0101 (1)
K	10001	Second Start of Packet - 0101 (1)
T	01101	First End of Packet - 0000 (1)
R	00111	Second End of Packet - 0000 (1)
INVALID CODES		
V	00000	
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

5.5.1.1.1 Code-group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 5-14 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of Transmit Enable signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of Transmit Enable).

5.5.1.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB. The DP83849I uses the PHY_ID (pins PHYAD [4:1]) to set a unique seed value.

5.5.1.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 Unshielded twisted pair cable.

5.5.1.1.4 Binary to MLT-3 Convertor

The Binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD Output Pair common driver is slew rate controlled. This must be considered when selecting AC coupling magnetics to ensure TP-PMD Standard compliant transition times (3 ns < Tr < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83849I is capable of sourcing only MLT-3 encoded data. Binary output from the PMD Output Pair is not possible in 100 Mb/s mode.

5.5.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII. Because the 100BASE-TX TP-PMD is integrated, the differential input pins, RD±, can be directly routed from the AC coupling magnetics.

See Figure 5-7 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.

The Receive section consists of the following functional blocks

- Analog Front End
- Digital Signal Processor
- Signal Detect
- MLT-3 to Binary Decoder
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B/5B Decoder
- Link Integrity Monitor
- Bad SSD Detection

5.5.3 Analog Front End

In addition to the Digital Equalization and Gain Control, the DP83849I includes Analog Equalization and Gain Control in the Analog Front End. The Analog Equalization reduces the amount of Digital Equalization required in the DSP.

5.5.3.1 Digital Signal Processor

The Digital Signal Processor includes Adaptive Equalization with Gain Control and Base Line Wander Compensation.

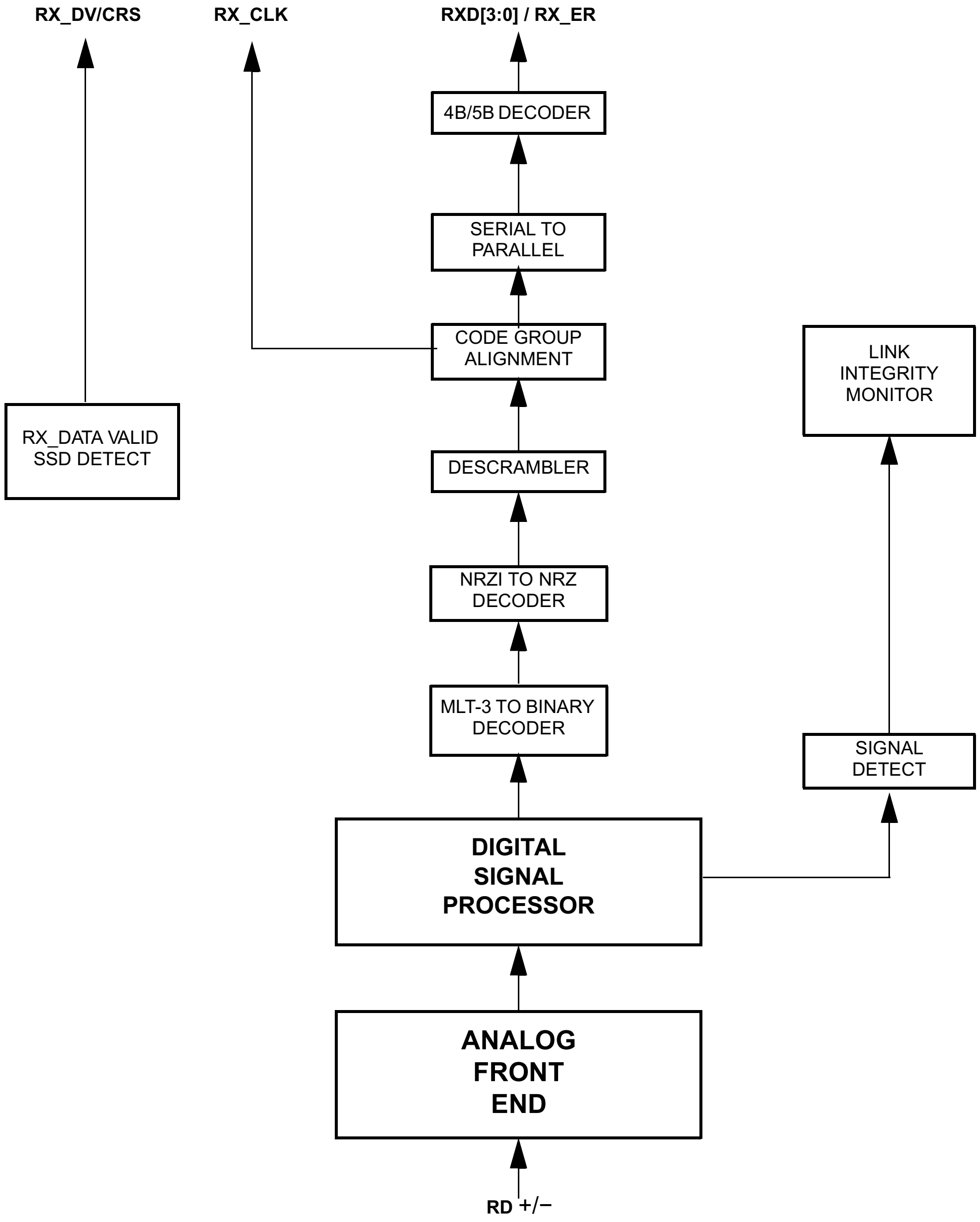


Figure 5-7. 100BASE-TX Receive Block Diagram

5.5.3.2 Digital Adaptive Equalization and Gain Control

When transmitting data at high speeds over copper twisted pair cable, frequency dependent attenuation becomes a concern. In high-speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated to ensure the integrity of the transmission.

In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will over-compensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. The compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

The DP83849I utilizes an extremely robust equalization scheme referred as *Digital Adaptive Equalization*.

The Digital Equalizer removes inter-symbol interference (ISI) from the receive data stream by continuously adapting to provide a filter with the inverse frequency response of the channel. Equalization is combined with an adaptive gain control stage. This enables the receive *eye pattern* to be opened sufficiently to allow very reliable data recovery.

The curves given in Figure 5-8 illustrate attenuation at certain frequencies for given cable lengths. This is derived from the worst case frequency versus attenuation figures as specified in the EIA/TIA Bulletin TSB-36. These curves indicate the significant variations in signal attenuation that must be compensated for by the receive adaptive equalization circuit.

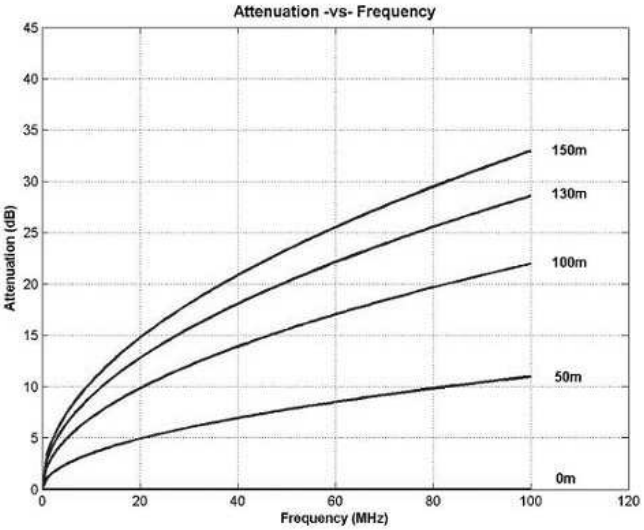


Figure 5-8. EIA/TIA Attenuation vs Frequency for 0, 50, 100, 130 and 150 Meters of CAT 5 Cable

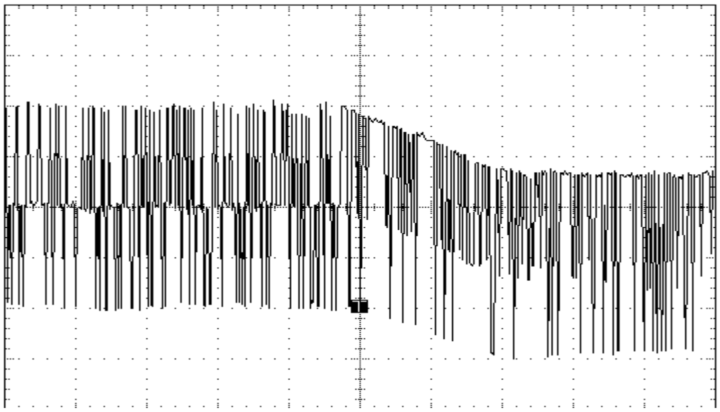


Figure 5-9. 100BASE-TX BLW Event

The DP83849I is completely ANSI TP-PMD compliant and includes Base Line Wander (BLW) compensation. The BLW compensation block can successfully recover the TP-PMD defined *killer* pattern.

BLW can generally be defined as the change in the average DC content, relatively short period over time, of an AC coupled digital transmission over a given transmission medium. (that is, copper wire).

BLW results from the interaction between the low frequency components of a transmitted bit stream and the frequency response of the AC coupling component(s) within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformers then the droop characteristics of the transformers will dominate resulting in potentially serious BLW.

The digital oscilloscope plot provided in Figure 5-9 illustrates the severity of the BLW event that can theoretically be generated during 100BASE-TX packet transmission. This event consists of approximately 800 mV of DC offset for a period of 120 µs. Left uncompensated, events such as this can cause packet loss.

5.5.3.3 Signal Detect

The signal detect function of the DP83849I is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

Note that the reception of normal 10BASE-T link pulses and fast link pulses per IEEE 802.3u Auto-Negotiation by the 100BASE-TX receiver do not cause the DP83849I to assert signal detect.

5.5.3.4 MLT-3 to NRZI Decoder

The DP83849I decodes the MLT-3 information from the Digital Adaptive Equalizer block to binary NRZI data.

5.5.3.5 NRZI to NRZ

In a typical application, the NRZI to NRZ decoder is required in order to present NRZ formatted data to the descrambler.

5.5.3.6 Serial to Parallel

The 100BASE-TX receiver includes a Serial to Parallel converter which supplies 5-bit wide data symbols to the PCS Rx state machine.

5.5.3.7 Descrambler

A serial descrambler is used to de-scramble the received NRZ data. The descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = (UD \oplus N) \tag{1}$$

$$UD = (SD \oplus N) \tag{2}$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized 12 consecutive IDLE code-groups, where an unscrambled IDLE code-group in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B code-groups.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722-µs countdown. Upon detection of sufficient IDLE code-groups (58 bit times) within the 722-µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE code-groups within the 722-µs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to reacquire synchronization.

5.5.3.8 Code-Group Alignment

The code-group alignment module operates on unaligned 5-bit data from the descrambler (or, if the descrambler is bypassed, directly from the NRZI/NRZ decoder) and converts it into 5B code-group data (5 bits). Code-group alignment occurs after the J/K code-group pair is detected. Once the J/K code-group pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

5.5.3.9 4B/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5B code-groups into 4B nibbles. The code-group decoder first detects the J/K code-group pair preceded by IDLE code-groups and replaces the J/K with MAC preamble. Specifically, the J/K 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5B code-groups are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R code-group pair denoting the End of Stream Delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

5.5.3.10 100BASE-TX Link Integrity Monitor

The 100Base TX Link monitor ensures that a valid and stable link is established before enabling both the Transmit and Receive PCS layer.

Signal detect must be valid for 395 µs to allow the link monitor to enter the *Link Up* state, and enable the transmit and receive functions.

5.5.3.11 BAD SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K.

If this condition is detected, the DP83849I will assert RX_ER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the False Carrier Sense Counter register (FCSCR) will be incremented by one.

Once at least two IDLE code groups are detected, RX_ER and CRS become de-asserted.

5.5.4 10BASE-T Transceiver Module

The 10BASE-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard. An external filter is not required on the 10BASE-T interface because this is integrated inside the DP83849I. This section focuses on the general 10BASE-T system level operation.

5.5.4.1 Operational Modes

The DP83849I has two basic 10BASE-T operational modes:

- Half Duplex mode
- Full Duplex mode

Half Duplex Mode: In Half Duplex mode the DP83849I functions as a standard IEEE 802.3 10BASE-T transceiver supporting the CSMA/CD protocol.

Full Duplex Mode: In Full Duplex mode the DP83849I is capable of simultaneously transmitting and receiving without asserting the collision signal. The DP83849I's 10-Mb/s ENDEC is designed to encode and decode simultaneously.

5.5.4.2 Smart Squelch

The smart squelch is responsible for determining when valid data is present on the differential receive inputs. The DP83849I implements an intelligent receive squelch to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. Smart squelch operation is independent of the 10BASE-T operational mode.

The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BSE-T standard) to determine the validity of data on the twisted pair inputs (refer to Figure 5-10).

The signal at the start of a packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally the signal must again exceed the original squelch level within 150 ns to ensure that the input waveform will not be rejected. This checking procedure results in the loss of typically three preamble bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 150 ns, indicating the End of Packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise causing premature End of Packet detection.

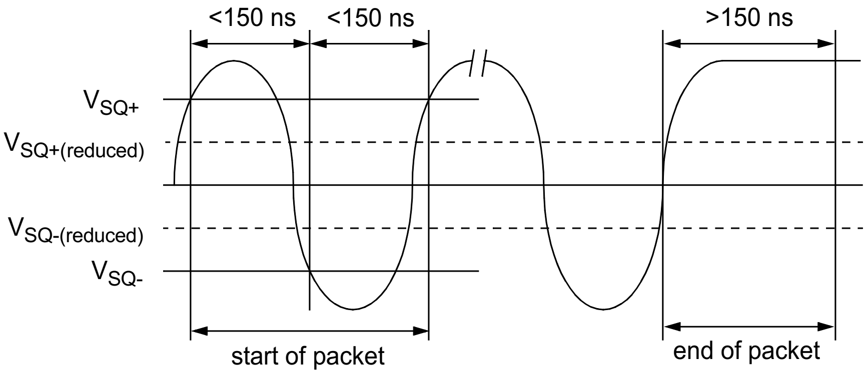


Figure 5-10. 10BASE-T Twisted Pair Smart Squelch Operation

5.5.4.3 Collision Detection and SQE

When in Half Duplex, a 10BASE-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. Collisions are also reported when a jabber condition is detected.

The COL signal remains set for the duration of the collision. If the PHY is receiving when a collision is detected it is reported immediately (through the COL pin).

When heartbeat is enabled, approximately 1 µs after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10-bit times is generated to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

The SQE test is inhibited when the PHY is set in full duplex mode. SQE can also be inhibited by setting the HEARTBEAT_DIS bit in the 10BTSCR register.

5.5.4.4 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected through the squelch function.

For 10-Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10-Mb/s Full Duplex operation, CRS is asserted only during receive activity.

CRS is deasserted following an end of packet.

5.5.4.5 Normal Link Pulse Detection/Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-T standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data.

Link pulses are used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10BASE-T twisted pair transmitter, receiver and collision detection functions.

When the link integrity function is disabled (FORCE_LINK_10 of the 10BTSCR register), a good link is forced and the 10BASE-T transceiver will operate regardless of the presence of link pulses.

5.5.4.6 Jabber Function

The jabber function monitors the DP83849I's output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 85 ms.

Once disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal has to be de-asserted for approximately 500 ms (the *unjab* time) before the Jabber function re-enables the transmit outputs.

The Jabber function is only relevant in 10BASE-T mode.

5.5.4.7 Automatic Link Polarity Detection and Correction

The DP83849I's 10BASE-T transceiver module incorporates an automatic link polarity detection circuit. When three consecutive inverted link pulses are received, bad polarity is reported.

A polarity reversal can be caused by a wiring error at either end of the cable, usually at the Main Distribution Frame (MDF) or patch panel in the wiring closet.

The bad polarity condition is latched in the 10BTSCR register. The DP83849I's 10BASE-T transceiver module corrects for this error internally and will continue to decode received data correctly. This eliminates the need to correct the wiring error immediately.

5.5.4.8 Transmit and Receive Filtering

External 10BASE-T filters are not required when using the DP83849I, as the required signal conditioning is integrated into the device.

Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

5.5.4.9 Transmitter

The encoder begins operation when the Transmit Enable input (TX_EN) goes high and converts NRZ data to pre-emphasized Manchester data for the transceiver. For the duration of TX_EN, the serialized Transmit Data (TXD) is encoded for the transmit-driver pair (PMD Output Pair). TXD must be valid on the rising edge of Transmit Clock (TX_CLK). Transmission ends when TX_EN deasserts. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

5.5.4.10 Receiver

The decoder detects the end of a frame when no additional mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for five more bit times after CRS goes low, to ensure the receive timings of the controller.

5.6 Register Block

Table 5-15. Register Map

OFFSET		ACCESS	TAG	DESCRIPTION
HEX	DECIMAL			
00h	0	RW	BMCR	Basic Mode Control Register
01h	1	RO	BMSR	Basic Mode Status Register
02h	2	RO	PHYIDR1	PHY Identifier Register #1
03h	3	RO	PHYIDR2	PHY Identifier Register #2
04h	4	RW	ANAR	Auto-Negotiation Advertisement Register
05h	5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register (Base Page)
05h	5	RW	ANLPARNP	Auto-Negotiation Link Partner Ability Register (Next Page)
06h	6	RW	ANER	Auto-Negotiation Expansion Register
07h	7	RW	ANNPTR	Auto-Negotiation Next Page TX
08h-Fh	8-15	RW	RESERVED	RESERVED
10h	16	RO	PHYSTS	PHY Status Register
11h	17	RW	MICR	MII Interrupt Control Register
12h	18	RW	MISR	MII Interrupt Status Register
13h	19	RW	PAGSEL	Page Select Register
EXTENDED REGISTERS – PAGE 0				
14h	20	RO	FCSCR	False Carrier Sense Counter Register
15h	21	RO	RECR	Receive Error Counter Register
16h	22	RW	PCSR	PCS Sub-Layer Configuration and Status Register
17h	23	RW	RBR	RMII and Bypass Register
18h	24	RW	LEDCR	LED Direct Control Register
19h	25	RW	PHYCR	PHY Control Register
1Ah	26	RW	10BTSCR	10Base-T Status/Control Register
1Bh	27	RW	CDCTRL1	CD Test Control Register and BIST Extensions Register
1Ch	28	RW	PHYCR2	Phy Control Register 2
1Dh	29	RW	EDCR	Energy Detect Control Register
1Eh-1Fh	30-31		RESERVED	RESERVED
RESERVED REGISTERS				
14h-1Fh	30-31		RESERVED	RESERVED
LINK DIAGNOSTICS REGISTERS - PAGE 2				
14h	20	RO	LEN100_DET	100Mb Length Detect Register
15h	21	RW	FREQ100	100Mb Frequency Offset Indication Register
16h	22	RW	TDR_CTRL	TDR Control Register
17h	23	RW	TDR_WIN	TDR Window Register
18h	24	RO	TDR_PEAK	TDR Peak Measurement Register
19h	25	RO	TDR_THR	TDR Threshold Measurement Register
1Ah	26	RW	VAR_CTRL	Variance Control Register
1Bh	27	RO	VAR_DAT	Variance Data Register
1Ch	28		RESERVED	RESERVED
1Dh	29	RW	LQMR	Link Quality Monitor Register
1Eh	30	RW	LQDR	Link Quality Data Register
1Fh	31		RESERVED	RESERVED

Table 5-16. Register Table

REGISTER NAME	ADDR	TAG	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Basic Mode Control Register	00h	BMCR	Reset	Loopback	Speed Selection	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Duplex Mode	Collision Test	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Basic Mode Status Register	01h	BMSR	100Base-T4	100Base - TX FDX	100Base - TX HDX	10Base-TFDX	10Base-THDX	Reserved	Reserved	Reserved	Reserved	MF Pre-amble Sup-press	Auto- Neg Com- plete	Remote Fault	Auto- Neg Ability	Link Status	Jabber Detect	Extended Capability
PHY Identifier Register 1	02h	PHYIDR1	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB
PHY Identifier Register 2	03h	PHYIDR2	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	MDL_ REV	MDL_ REV	MDL_ REV	MDL_ REV
Auto-Negotiation Advertisement Register	04h	ANAR	Next Page Ind	Reserved	Remote Fault	Reserved	ASM_DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register (Base Page)	05h	ANLPAR	Next Page Ind	ACK	Remote Fault	Reserved	ASM_DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register Next Page	05h	AN-LPARNP	Next Page Ind	ACK	Message Page	ACK2	Toggle	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code
Auto-Negotiation Expansion Register	06h	ANER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDF	LP_NP_ ABLE	NP_ ABLE	PAGE_ RX	LP_AN_ ABLE
Auto-Negotiation Next Page TX Register	07h	ANNPTR	Next Page Ind	Reserved	Message Page	ACK2	TOG_TX	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE
RESERVED	08-0fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
PHY Status Register	10h	PHYSTS	Reserved	MDI-X mode	Rx Err Latch	Polarity Status	False Carrier Sense	Signal Detect	Descram Lock	Page Receive	Reserved	Remote Fault	Jabber Detect	Auto-Neg Complete	Loopback Status	Duplex Status	Speed Status	Link Status
MII Interrupt Control Register	11h	MICR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TINT	INTEN	RINT
MII Interrupt Status and Misc. Control Register	12h	MISR	LQ_INT	ED_INT	LINK_INT	SPD_INT	DUP_INT	ANC_INT	FHF_INT	RHF_INT	LQ_INT_ EN	ED_INT_ EN	LINK_ IN T_EN	SPED_ I NT_EN	DUP_ IN T_EN	ANC_ IN T_EN	FHF_INT _EN	RHF_IN T_EN
Page Select Register	13h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Page_Se l Bit	Page_Se l Bit
EXTENDED REGISTERS																		
False Carrier Sense Counter Register	14h	FCSCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT
Receive Error Counter Register	15h	RECR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT
PCS Sub-Layer Configuration and Status Register	16h	PCSR	Reserved	Reserved	Reserved	Reserved	FREE_CLK	TQ_EN	SD_FOR CE_PMA	SD_ OPTION	DESC_ T IME	Reserved	FORCE_ 100_OK	Reserved	Reserved	NRZI_ BYPASS	Reserved	Reserved
RMII and Bypass Register	17h	RBR	SIM_ WRITE	Reserved	DIS_TX_ OPT	RX_POR T	RX_POR T	TX_SOU RCE	TX_SOU RCE	PMD_LO OP	SCMII_R X	SCMII_T X	RMII_ M ODE	RMII_RE V1_0	RX_OVF _STS	RX_UNF _STS	ELAST_ BUF	ELAST_ BUF
LED Direct Control Register	18h	LEDCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LEDACT _RX	BLINK_F REQ	BLINK_F REQ	DRV_SP DLED	DRV_LN KLED	DRV_AC TLED	SPDLED	LNKLED	ACTLED
PHY Control Register	19h	PHYCR	MDIX_E N	FORCE_ MDIX	PAUSE_ RX	PAUSE_ TX	BIST_FE	PSR_15	BIST_ STATUS	BIST_ST ART	BP_STR ETCH	Reserved	LED_ CNFG[1]	LED_ CNFG[0]	PHY ADDR	PHY ADDR	PHY ADDR	PHY ADDR
10Base-T Status/Control Register	1Ah	10BT_ SERIAL	Reserved	Reserved	Reserved	Reserved	SQUELCH	SQUELCH	SQUELCH	LOOPBA CK_10_ DIS	LP_DIS	FORC_ LINK_10	Reserved	POLARITY	Reserved	Reserved	HEARBEA T_ DIS	JABBER _DIS

Table 5-16. Register Table (continued)

REGISTER NAME	ADDR	TAG	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CD Test Control and BIST Extensions Register	1Bh	CDCTRL1	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	BIST_ERROR_C OUNT	Reserved	Reserved	BIST_CONT_MODE	CDPatEN_10	Reserved	10Meg_Patt_Gap	CDPatt-Sel	CDPatt-Sel
Phy Control Register 2	1Ch	PHYCR2	Reserved	Reserved	Reserved	Reserved	Reserved	SOFT_RESET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Energy Detect Control Register	1Dh	EDCR	ED_EN	ED_AUTO_UP	ED_AUTO_DOW N	ED_MAN	ED_BURST_DIS	ED_PWR_STATE	ED_ERR_MET	ED_DATA_MET	ED_ERR_COUNT	ED_ERR_COUNT	ED_ERR_COUNT	ED_ERR_COUNT	ED_DATA_COUNT	ED_DATA_COUNT	ED_DATA_COUNT	ED_DATA_COUNT
RESERVED	1Eh-1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RESERVED REGISTERS																		
RESERVED	14h-1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
LINK DIAGNOSTICS REGISTERS - PAGE 2																		
100Mb Length Detect Register	14h	LEN100_DET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN	CABLE_LEN
100Mb Frequency Offset Indication Register	15h	FREQ100	SAMPLE_FREQ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_FC	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET	FREQ_OFFSET
TDR Control Register	16h	TDR_CTRL	TDR_ENABLE	TDR_100Mb	TX_CHANNEL	RX_CHANNEL	SEND_TDR	TDR_WIDTH	TDR_WIDTH	TDR_WIDTH	TDR_MIN_MODE	Reserved	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD	RX_THRESHOLD
TDR Window Register	17h	TDR_WIN	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_START	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOP	TDR_STOPP
TDR Peak Register	18h	TDR_PEAK	Reserved	Reserved	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR_PEAK_TIME	TDR PEAK_TIME
TDR Threshold Register	19h	TDR_THR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TDR_ THR_MET	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME	TDR-THR_TIME
Variance Control Register	1Ah	VAR_CTRL	VAR_RDY	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VAR_ FREEZE	VAR_ TIMER	VAR_ TIMER	VAR_ TIMER
Variance Data Register	1Bh	VAR_DATA	VAR_DATA	VAR_DATAT	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATAT	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATAT	VAR_DATA	VAR_DATA	VAR_DATA	VAR_DATAT	VAR_DATA	VAR_DATA
RESERVED	1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Link Quality Monitor Register	1Dh	LQMR	LQM_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	FC_HI_WARN	FC_LO_WARN	FREQ_HI_WARN	FREQ_LO_WARN	DBLW_HI_WARN	DBLW_LO_WARN	DAGC_HI_WARN	DAGC_LO_WARN	C1_HI_WARN	C1_LO_WARN
Link Quality Data Register	1Eh	LQDR	Reserved	Reserved	SAMPLE_PARAM	WRITE_LQ_THR	LQ_PARAM_SEL	LQ_PARAM_SEL	LQ_PARAM_SEL	LQ_THR_SEL	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA	LQ_THR_DATA
RESERVED	1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

5.6.1 Register Definition

In the register definitions under the *Default* heading, the following definitions hold true:

- **RW** = **R**ead **W**rite access
- **SC** = Register sets on event occurrence and **S**elf-**C**lears when event ends
- **RW/SC** = **R**ead **W**rite access/**S**elf **C**learing bit
- **RO** = **R**ead **O**nly access
- **COR** = **C**lear **o**n **R**ead
- **RO/COR** = **R**ead **O**nly, **C**lear **o**n **R**ead
- **RO/P** = **R**ead **O**nly, **P**ermanently set to a default value
- **LL** = **L**atched **L**ow and held until read, based upon the occurrence of the corresponding event
- **LH** = **L**atched **H**igh and held until read, based upon the occurrence of the corresponding event

5.6.1.1 Basic Mode Control Register (BMCR)

Table 5-17. Basic Mode Control Register (BMCR), address 00h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESET	0, RW/SC	**Reset:** 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. This bit, which is self-clearing, returns a value of one until the reset process is complete. The configuration is re-strapped.
14	LOOPBACK	0, RW	**Loopback:** 1 = Loopback enabled. 0 = Normal operation. The loopback function enables MII transmit data to be routed to the MII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500 µs *dead time* before any valid data will appear at the MII receive outputs.
13	SPEED SELECTION	Strap, RW	**Speed Select:** When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 1 = 100 Mb/s. 0 = 10 Mb/s.
12	AUTO-NEGOTIATION ENABLE	0, RW	**Auto-Negotiation Enable:** Strap controls initial value at reset. 1 = Auto-Negotiation Enabled - bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 8 and 13 determine the port speed and duplex mode.
11	POWER DOWN	0, RW	**Power Down:** 1 = Power down. 0 = Normal operation. Setting this bit powers down the PHY. Only the register block is enabled during a power-down condition. This bit is OR'd with the input from the PWRDOWN_INT pin. When the active low PWRDOWN_INT pin is asserted, this bit will be set.
10	ISOLATE	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management. 0 = Normal operation.
9	RESTART AUTO-NEGOTIATION	0, RW/SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation.
8	DUPLEX MODE	Strap, RW	**Duplex Mode:** When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full Duplex operation. 0 = Half Duplex operation.

Table 5-17. Basic Mode Control Register (BMCR), address 00h (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
7	COLLISION TEST	0, RW	**Collision Test:** 1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be deasserted within 4-bit times in response to the deassertion of TX_EN.
6:0	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.

5.6.1.2 Basic Mode Status Register (BMSR)

Table 5-18. Basic Mode Status Register (BMSR), address 01h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	**100BASE-T4 Capable:** 0 = Device not able to perform 100BASE-T4 mode.
14	100BASE-TX FULL DUPLEX	1, RO/P	**100BASE-TX Full Duplex Capable:** 1 = Device able to perform 100BASE-TX in full duplex mode.
13	100BASE-TX HALF DUPLEX	1, RO/P	**100BASE-TX Half Duplex Capable:** 1 = Device able to perform 100BASE-TX in half duplex mode.
12	10BASE-T FULL DUPLEX	1, RO/P	**10BASE-T Full Duplex Capable:** 1 = Device able to perform 10BASE-T in full duplex mode.
11	10BASE-T HALF DUPLEX	1, RO/P	**10BASE-T Half Duplex Capable:** 1 = Device able to perform 10BASE-T in half duplex mode.
10:7	RESERVED	0, RO	**RESERVED:** Write as 0, read as 0.
6	MF PREAMBLE SUPPRESSION	1, RO/P	**Preamble suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation.
5	AUTO-NEGOTIATION COMPLETE	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete.
4	REMOTE FAULT	0, RO/LH	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	AUTO-NEGOTIATION ABILITY	1, RO/P	**Auto Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	LINK STATUS	0, RO/LL	**Link Status:** 1 = Valid link established (for either 10 or 100 Mb/s operation). 0 = Link not established. The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read through the management interface.
1	JABBER DETECT	0, RO/LH	**Jabber Detect:** This bit only has meaning in 10-Mb/s mode. 1 = Jabber condition detected. 0 = No Jabber. This bit is implemented with a latching function, such that the occurrence of a jabber condition causes it to set until it is cleared by a read to this register by the management interface or by a reset.
0	EXTENDED CAPABILITY	1, RO/P	**Extended Capability:** 1 = Extended register capabilities. 0 = Basic register set capabilities only.

The PHY Identifier Register 1 and Register 2 together form a unique identifier for the DP83849I. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. Texas Instrument's IEEE assigned OUI is 080017h.

5.6.1.3 PHY Identifier Register #1 (PHYIDR1)

Table 5-19. PHY Identifier Register #1 (PHYIDR1), address 02h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	OUI_MSB	<0010 0000 0000 0000>, RO/P	**OUI Most Significant Bits:** Bits 3 to 18 of the OUI (080017h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

5.6.1.4 PHY Identifier Register #2 (PHYIDR2)

Table 5-20. PHY Identifier Register #2 (PHYIDR2), address 03h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	<0101 11>, RO/P	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080017h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<00 1001>, RO/P	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0000>, RO/P	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

5.6.1.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation. Any writes to this register prior to completion of Auto-Negotiation (as indicated in the Basic Mode Status Register (address 01h) Auto-Negotiation Complete bit, BMSR[5]) must be followed by a renegotiation. This will ensure that the new values are properly used in the Auto-Negotiation.

Table 5-21. Auto-Negotiation Advertisement Register (ANAR), address 04h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.
14	RESERVED	0, RO/P	**RESERVED by IEEE:** Writes ignored, Read as 0.
13	RF	0, RW	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	RESERVED	0, RW	**RESERVED for Future IEEE use:** Write as 0, Read as 0
11	ASM_DIR	0, RW	**Asymmetric PAUSE Support for Full Duplex Links:** The ASM_DIR bit indicates that asymmetric PAUSE is supported. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full duplex flow control.

Table 5-21. Auto-Negotiation Advertisement Register (ANAR), address 04h (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
10	PAUSE	0, RW	**PAUSE Support for Full Duplex Links:** The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full duplex flow control.
9	T4	0, RO/P	**100BASE-T4 Support:** 1= 100BASE-T4 is supported by the local device. 0 = 100BASE-T4 not supported.
8	TX_FD	Strap, RW	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported.
7	TX	Strap, RW	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the local device. 0 = 100BASE-TX not supported.
6	10_FD	RW	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the local device. 0 = 10BASE-T Full Duplex not supported.
5	10	RW	**10BASE-T Support:** 1 = 10BASE-T is supported by the local device. 0 = 10BASE-T not supported.
4:0	SELECTOR	<00001>, RW	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3u.

5.6.1.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful auto-negotiation if Next-pages are supported.

Table 5-22. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), address 05h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	RESERVED	0, RO	**RESERVED for Future IEEE use:** Write as 0, read as 0.
11	ASM_DIR	0, RO	**ASYMMETRIC PAUSE:** 1 = Asymmetric pause is supported by the Link Partner. 0 = Asymmetric pause is not supported by the Link Partner.
10	PAUSE	0, RO	**PAUSE:** 1 = Pause function is supported by the Link Partner. 0 = Pause function is not supported by the Link Partner.
9	T4	0, RO	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 not supported by the Link Partner.

Table 5-22. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), address 05h (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
8	TX_FD	0, RO	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex not supported by the Link Partner.
7	TX	0, RO	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX not supported by the Link Partner.
6	10_FD	0, RO	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the Link Partner. 0 = 10BASE-T Full Duplex not supported by the Link Partner.
5	10	0, RO	**10BASE-T Support:** 1 = 10BASE-T is supported by the Link Partner. 0 = 10BASE-T not supported by the Link Partner.
4:0	SELECTOR	<0 0000>, RO	**Protocol Selection Bits:** Link Partner’s binary encoded protocol selector.

5.6.1.7 Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page)

Table 5-23. Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page), address 05h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 1 = Link Partner desires Next Page Transfer. 0 = Link Partner does not desire Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts. Software must not attempt to write to this bit.
13	MP	0, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge 2:** 1 = Link Partner does have the ability to comply to next page message. 0 = Link Partner does not have the ability to comply to next page message.
11	TOGGLE	0, RO	**Toggle:** 1 = Previous value of the transmitted Link Code word equaled 0. 0 = Previous value of the transmitted Link Code word equaled 1.
10:0	CODE	<000 0000 0000>, RO	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a “Message Page,” as defined in annex 28C of Clause 28. Otherwise, the code shall be interpreted as an “Unformatted Page,” and the interpretation is application specific.

5.6.1.8 Auto-Negotiate Expansion Register (ANER)

This register contains additional Local Device and Link Partner status information.

Table 5-24. Auto-Negotiate Expansion Register (ANER), address 06h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = A fault has been detected through the Parallel Detection function. 0 = A fault has not been detected.
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page. 0 = Link Partner does not support Next Page.
2	NP_ABLE	1, RO/P	**Next Page Able:** 1 = Indicates local device is able to send additional “Next Pages”.
1	PAGE_RX	0, RO/COR	**Link Code Word Page Received:** 1 = Link Code Word has been received, cleared on a read. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = indicates that the Link Partner supports Auto-Negotiation. 0 = indicates that the Link Partner does not support Auto-Negotiation.

5.6.1.9 Auto-Negotiation Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 5-25. Auto-Negotiation Next Page Transmit Register (ANNPTR), address 07h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
13	MP	1, RW	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RW	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000 0000 0001>, RW	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page”, as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page”, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

5.6.1.10 PHY Status Register (PHYSTS)

This register provides a single location within the register set for quick access to commonly accessed information.

Table 5-26. PHY Status Register (PHYSTS), address 10h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.
14	MDIX MODE	0, RO	**MDI-X mode as reported by the Auto-Negotiation logic:** This bit will be affected by the settings of the MDIX_EN and FORCE_MDIX bits in the PHYCR register. When MDIX is enabled, but not forced, this bit will update dynamically as the Auto-MDIX algorithm swaps between MDI and MDI-X configurations. 1 = MDI pairs swapped (Receive on TPTD pair, Transmit on TPRD pair) 0 = MDI pairs normal (Receive on TRD pair, Transmit on TPTD pair)
13	RECEIVE ERROR LATCH	0, RO/LH	**Receive Error Latch**: This bit will be cleared upon a read of the RECR register. 1 = Receive error event has occurred because last read of RXERCNT (address 0x15, Page 0). 0 = No receive error event has occurred.
12	POLARITY STATUS	0, RO	**Polarity Status:** This bit is a duplication of bit 4 in the 10BTSCR register. This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 1 = Inverted Polarity detected. 0 = Correct Polarity detected.
11	FALSE CARRIER SENSE LATCH	0, RO/LH	**False Carrier Sense Latch:** This bit will be cleared upon a read of the FCSR register. 1 = False Carrier event has occurred because last read of FCSCR (address 0x14). 0 = No False Carrier event has occurred.
10	SIGNAL DETECT	0, RO/LL	**100Base-TX unconditional Signal Detect from PMD.** This is the SD that goes into the link monitor. It is the AND of raw SD and descrambler lock, when address 16h, bit 8 (page 0) is set. When this bit is cleared, it will be equivalent to the raw SD from the PMD.
9	DESCRAMBLER LOCK	0, RO/LL	100Base-TX Descrambler Lock from PMD.
8	PAGE RECEIVED	0, RO	**Link Code Word Page Received:** This is a duplicate of the Page Received bit in the ANER register, but this bit will not be cleared upon a read of the PHYSTS register. 1 = A new Link Code Word Page has been received. Cleared on read of the ANER (address 0x06, bit 1). 0 = Link Code Word Page has not been received.
7	MII INTERRUPT	0, RO	**MII Interrupt Pending:** 1 = Indicates that an internal interrupt is pending. Interrupt source can be determined by reading the MISR Register (12h). Reading the MISR will clear the Interrupt. 0 = No interrupt pending.
6	REMOTE FAULT	0, RO	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read of BMSR (address 01h) register or by reset). Fault criteria: notification from Link Partner of Remote Fault through Auto-Negotiation. 0 = No remote fault condition detected.
5	JABBER DETECT	0, RO	**Jabber Detect:** This bit only has meaning in 10-Mb/s mode This bit is a duplicate of the Jabber Detect bit in the BMSR register, except that it is not cleared upon a read of the PHYSTS register. 1 = Jabber condition detected. 0 = No Jabber.
4	AUTO-NEG COMPLETE	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation complete. 0 = Auto-Negotiation not complete.

Table 5-26. PHY Status Register (PHYSTS), address 10h (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
3	LOOPBACK STATUS	0, RO	**Loopback:** 1 = Loopback enabled. 0 = Normal operation.
2	DUPLEX STATUS	0, RO	**Duplex:** This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. 1 = Full duplex mode. 0 = Half duplex mode. Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
1	SPEED STATUS	0, RO	**Speed10:** This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. 1 = 10-Mb/s mode. 0 = 100 Mb/s mode. Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
0	LINK STATUS	0, RO	**Link Status:** This bit is a duplicate of the Link Status bit in the BMSR register, except that it will not be cleared upon a read of the PHYSTS register. 1 = Valid link established (for either 10 or 100 Mb/s operation) 0 = Link not established.

5.6.1.11 MII Interrupt Control Register (MICR)

This register implements the MII Interrupt PHY Specific Control register. Sources for interrupt generation include: Energy Detect State Change, Link State Change, Speed Status Change, Duplex Status Change, Auto-Negotiation Complete or any of the counters becoming half-full. The individual interrupt events must be enabled by setting bits in the MII Interrupt Status and Event Control Register (MISR).

Table 5-27. MII Interrupt Control Register (MICR) address 11h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:03	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
2	TINT	0, RW	**Test Interrupt:** Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 1 = Generate an interrupt 0 = Do not generate interrupt
1	INTEN	0, RW	**Interrupt Enable:** Enable interrupt dependent on the event enables in the MISR register. 1 = Enable event based interrupts 0 = Disable event based interrupts
0	INT_OE	0, RW	**Interrupt Output Enable:** Enable interrupt events to signal through the PWRDOWN_INT pin by configuring the PWRDOWN_INT pin as an output. 1 = PWRDOWN_INT is an Interrupt Output 0 = PWRDOWN_INT is a Power Down Input

5.6.1.12 MII Interrupt Status and Miscellaneous Control Register (MICR)

This counter provides information required to implement the *False Carriers* attribute within the MAU managed object class of Clause 30 of the IEEE 802.3u specification.

Table 5-28. MII Interrupt Status and Miscellaneous Control Register (MICR) address 12h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	LQ_INT	0, RO/COR	**Link Quality interrupt:** 1 = Link Quality interrupt is pending and is cleared by the current read. 0 = No Link Quality interrupt pending.
14	ED_INT	0, RO/COR	**Energy Detect interrupt:** 1 = Energy detect interrupt is pending and is cleared by the current read. 0 = No energy detect interrupt pending.
13	LINK_INT	0, RO/COR	**Change of Link Status interrupt:** 1 = Change of link status interrupt is pending and is cleared by the current read. 0 = No change of link status interrupt pending.
12	SPD_INT	0, RO/COR	**Change of speed status interrupt:** 1 = Speed status change interrupt is pending and is cleared by the current read. 0 = No speed status change interrupt pending.
11	DUP_INT	0, RO/COR	**Change of duplex status interrupt:** 1 = Duplex status change interrupt is pending and is cleared by the current read. 0 = No duplex status change interrupt pending.
10	ANC_INT	0, RO/COR	**Auto-Negotiation Complete interrupt:** 1 = Auto-negotiation complete interrupt is pending and is cleared by the current read. 0 = No Auto-negotiation complete interrupt pending.
9	FHF_INT	0, RO/COR	**False Carrier Counter half-full interrupt:** 1 = False carrier counter half-full interrupt is pending and is cleared by the current read. 0 = No false carrier counter half-full interrupt pending.
8	RHF_INT	0, RO/COR	**Receive Error Counter half-full interrupt:** 1 = Receive error counter half-full interrupt is pending and is cleared by the current read. 0 = No receive error carrier counter half-full interrupt pending.
7	LQ_INT_EN	0, RW	Enable Interrupt on Link Quality Monitor event
6	ED_INT_EN	0, RW	Enable Interrupt on energy detect event
5	LINK_INT_EN	0, RW	Enable Interrupt on change of link status
4	SPD_INT_EN	0, RW	Enable Interrupt on change of speed status
3	DUP_INT_EN	0, RW	Enable Interrupt on change of duplex status
2	ANC_INT_EN	0, RW	Enable Interrupt on Auto-negotiation complete event
1	FHF_INT_EN	0, RW	Enable Interrupt on False Carrier Counter Register half-full event
0	RHF_INT_EN	0, RW	Enable Interrupt on Receive Error Counter Register half-full event

5.6.1.13 Page Select Register (PAGESEL)

This register is used to enable access to the Link Diagnostics Registers.

Table 5-29. Page Select Register (PAGESEL), address 13h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:02	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0
1:00	PAGE_SEL	0, RW	**Page_Sel Bit:** Selects between paged registers for address 14h to 1Fh. 0 = Extended Registers Page 0 1 = Test Mode Register Page 1 2 = Link Diagnostics Registers Page 2

5.6.2 *Extended Registers - Page 0*

5.6.2.1 False Carrier Sense Counter Register (FCSCR)

This counter provides information required to implement the *False Carriers* attribute within the MAU managed object class of Clause 30 of the IEEE 802.3 specification.

Table 5-30. False Carrier Sense Counter Register (FCSCR), address 14h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0
7:0	FCSCNT[7:0]	0, RO / COR	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter sticks when it reaches its max count (FFh).

5.6.2.2 Receiver Error Counter Register (RECR)

This counter provides information required to implement the “Symbol Error During Carrier” attribute within the PHY managed object class of Clause 30 of the IEEE 802.3 specification.

Table 5-31. Receiver Error Counter Register (RECR), address 15h

Bit	Bit Name	Default	Description
15:8	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0
7:0	RXERCNT[7:0]	0, RO / COR	**RX_ER Counter:** When a valid carrier is present and there is at least one occurrence of an invalid data symbol, this 8-bit counter increments for each receive error detected. This event can increment only once per valid carrier event. If a collision is present, the attribute will not increment. The counter sticks when it reaches its max count.

5.6.2.3 100 Mb/s PCS Configuration and Status Register (PCSR)

This register contains control and status information for the 100BASE Physical Coding Sublayer.

Table 5-32. 100 Mb/s PCS Configuration and Status Register (PCSR), address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	<00>, RO	**RESERVED:** Writes ignored, Read as 0.
11	FREE_CLK	0, RW	**Receive Clock:** 1 = RX_CLK is free-running 0 = RX_CLK phase adjusted based on alignment
10	TQ_EN	0, RW	**100Mbs True Quiet Mode Enable:** 1 = Transmit True Quiet Mode. 0 = Normal Transmit Mode.
9	SD FORCE PMA	0, RW	**Signal Detect Force PMA:** 1 = Forces Signal Detection in PMA. 0 = Normal SD operation.
8	SD_OPTION	1, RW	**Signal Detect Option:** 1 = Default operation. Link will be asserted following detection of valid signal level and Descrambler Lock. Link will be maintained as long as signal level is valid. A loss of Descrambler Lock will not cause Link Status to drop. 0 = Modified signal detect algorithm. Link will be asserted following detection of valid signal level and Descrambler Lock. Link will be maintained as long as signal level is valid and Descrambler remains locked.
7	DESC_TIME	0, RW	**Descrambler Timeout:** Increase the descrambler timeout. When set this must allow the device to receive larger packets (>9k bytes) without loss of synchronization. 1 = 2ms 0 = 722µs (per ANSI X3.263: 1995 (TP-PMD) 7.2.3.3e)
6	RESERVED	0	**RESERVED:** Must be zero.

Table 5-32. 100 Mb/s PCS Configuration and Status Register (PCSR), address 0x16 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
5	FORCE_100_OK	0, RW	**Force 100Mb/s Good Link:** 1 = Forces 100Mb/s Good Link. 0 = Normal 100Mb/s operation.
4:3	RESERVED	0	**RESERVED:** Must be zero.
2	NRZI_BYPASS	0, RW	**NRZI Bypass Enable:** 1 = NRZI Bypass Enabled. 0 = NRZI Bypass Disabled.
1:0	RESERVED	0	**RESERVED:** Must be zero.

5.6.2.4 RMII and Bypass Register (RBR)

This register configures the RMII Mode of operation. When RMII mode is disabled, the RMII functionality is bypassed.

Table 5-33. RMII and Bypass Register (RBR), addresses 17h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	SIM_WRITE	0, RO	**Simultaneous Write:** Setting this bit in port A register space enables simultaneous write to Phy registers in both ports. Subsequent writes to port A registers will write to registers in both ports A and B. 1 = Simultaneous writes to both ports 0 = Per-port write
14	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0
13	DIS_TX_OPT	0, RW	**Disable RMII TX Latency Optimization:** Normally the RMII Transmitter will minimize the transmit latency by realigning the transmit clock with the Reference clock phase at the start of a packet transmission. Setting this bit will disable Phase realignment and ensure that IDLE bits will always be sent in multiples of the symbol size. This will result in a larger uncertainty in RMII transmit latency.
12:11	RX_PORT	00, RW	**Receive Port:** See *Section 5.4.4.3* for more information on Flexible Port Switching.
10:9	TX_SOURCE	Strap, RW	Transmit Source: See *Section 5.4.4.3* for more information on Flexible Port Switching. 00 = Not strapped for Extender Mode 10 = Strapped for Extender Mode
8	PMD_LOOP	0, RW	**PMD Loopback:** 0= Normal Operation 1= Remote (PMD) Loopback Setting this bit will cause the device to Loopback data received from the Physical Layer. The loopback is done prior to the MII or RMII interface. Data received at the internal MII or RMII interface will be applied to the transmitter. This mode must only be used if RMII mode or Single Clock MII mode is enabled.
7	SCMII_RX	Strap, RW	**Single Clock RX MII Mode:** 0= Standard MII mode 1= Single Clock RX MII Mode Setting this bit will cause the device to generate receive data (RX_DV, RX_ER, RXD[3:0]) synchronous to the X1 Reference clock. RX_CLK is not used in this mode. This mode uses the RMII elasticity buffer to tolerate variations in clock frequencies. This bit cannot be set if RMII_MODE is set to a 1. This bit is strapped to 1 if EXTENDER_EN is 1 and RMII Mode is not strapped at hard reset.
6	SCMII_TX	Strap, RW	**Single Clock TX MII Mode:** 0= Standard MII mode 1= Single Clock TX MII Mode Setting this bit will cause the device to sample transmit data (TX_EN, TXD[3:0]) synchronous to the X1 Reference clock. TX_CLK is not used in this mode. This bit cannot be set if RMII_MODE is set to a 1. This bit is strapped to 1 if EXTENDER_EN is 1 and RMII Mode is not strapped at hard reset.
5	RMII_MODE	Strap, RW	**Reduced MII Mode:** 0 = Standard MII Mode 1 = Reduced MII Mode
4	RMII_REV1_0	0, RW	**Reduce MII Revision 1.0:** 0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate deassertion of CRS. 1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet.
3	RX_OVF_STS	0, RO	**RX FIFO Over Flow Status:** 0 = Normal 1 = Overflow detected

Table 5-33. RMII and Bypass Register (RBR), addresses 17h (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	RX_UNF_STS	0, RO	**RX FIFO Under Flow Status:** 0 = Normal 1 = Underflow detected
1:0	ELAST_BUF[1:0]	01, RW	**Receive Elasticity Buffer.** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. See *Section 5.4.2* for more information on Elasticity Buffer settings in RMII mode. See *Section 5.4.4.2* for more information on Elasticity Buffer settings in SCMII mode.

5.6.2.5 LED Direct Control Register (LEDCR)

This register provides the ability to directly control the LED outputs. It does not provide read access to the LEDs. In addition, it provides control for the Activity source and blinking LED frequency.

Table 5-34. LED Direct Control Register (LEDCR), address 18h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:9	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
8	LEDACT_RX	0, RW	1 = Activity is only indicated for Receive traffic 0 = Activity is indicated for Transmit or Receive traffic
7:6	B;O;ML_FREQ	00, RW	**LED Blink Frequency:** These bits control the blink frequency of the LED_LINK output when blinking on activity is enabled. 0 = 6Hz 1 = 12Hz 2 = 24Hz 3 = 48Hz
5	DRV_SPDLED	0, RW	1 = Drive value of SPDLED bit onto LED_SPEED output 0 = Normal operation
4	DRV_LNKLED	0, RW	1 = Drive value of LNKLED bit onto LED_LINK output 0 = Normal operation
3	DRV_ACTLED	0, RW	1 = Drive value of ACTLED bit onto LED_ACT/LED_COL output 0 = Normal operation
2	SPDLED	0, RW	Value to force on LED_SPEED output
1	LNKLED	0, RW	Value to force on LED_LINK output
0	ACTLED	0, RW	Value to force on LED_ACT/LED_COL output

5.6.2.6 PHY Control Register (PHYCR)

This register provides control for Phy functions such as MDIX, BIST, LED configuration, and Phy address. It also provides Pause Negotiation status.

Table 5-35. PHY Control Register (PHYCR), address 19h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	MDIX_EN	Strap, RW	**Auto-MDIX Enable:** 1 = Enable Auto-neg Auto-MDIX capability. 0 = Disable Auto-neg Auto-MDIX capability. The Auto-MDIX algorithm requires that the Auto-Negotiation Enable bit in the BMCR register to be set. If Auto-Negotiation is not enabled, Auto-MDIX must be disabled as well.
14	FORCE_MDIX	0, RW	**Force MDIX:** 1 = Force MDI pairs to cross. (Receive on TPTD pair, Transmit on TPRD pair) 0 = Normal operation.

Table 5-35. PHY Control Register (PHYCR), address 19h (continued)

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>13</td><td>PAUSE_RX</td><td>0, RO</td><td>Pause Receive Negotiated:
Indicates that pause receive must be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings.
This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.</td></tr>
<tr><td>12</td><td>PAUSE_TX</td><td>0, RO</td><td>Pause Transmit Negotiated:
Indicates that pause transmit must be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings.
This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.</td></tr>
<tr><td>11</td><td>BIST_FE</td><td>0, RW/SC</td><td>BIST Force Error:
1 = Force BIST Error.
0 = Normal operation.
This bit forces a single error, and is self clearing.</td></tr>
<tr><td>10</td><td>PSR_15</td><td>0, RW</td><td>BIST Sequence select:
1 = PSR15 selected.
0 = PSR9 selected.</td></tr>
<tr><td>9</td><td>BIST_STATUS</td><td>0, LL/RO</td><td>BIST Test Status:
1 = BIST pass.
0 = BIST fail. Latched, cleared when BIST is stopped.
For a count number of BIST errors, see <i>Section 5.6.2.8</i> for the BIST Error Count in the CDCTRL1 register.</td></tr>
<tr><td>8</td><td>BIST_START</td><td>0, RW</td><td>BIST Start:
1 = BIST start.
0 = BIST stop.</td></tr>
<tr><td>7</td><td>BP_STRETCH</td><td>0, RW</td><td>Bypass LED Stretching:
This will bypass the LED stretching and the LEDs will reflect the internal value.
1 = Bypass LED stretching.
0 = Normal operation.</td></tr>
<tr><td>6
5</td><td>LED_CONFG[1]
LED_CNFG[0]</td><td>0, RW
Strap, RW</td><td>LED Configuration
<table>
<tr><th>LED_ CNFG[1]</th><th>LED_ CNFG[0]</th><th>MODE DESCRIPTION</th></tr>
<tr><td>Don't care</td><td>1</td><td>Mode 1</td></tr>
<tr><td>0</td><td>0</td><td>Mode 2</td></tr>
<tr><td>1</td><td>0</td><td>Mode 3</td></tr>
</table>
In Mode 1, LEDs are configured as follows:
LED_LINK = ON for Good Link, OFF for No Link
LED_SPEED = ON in 100Mb/s, OFF in 10Mb/s
LED_ACT/LED_COL = ON for Activity, OFF for No Activity
In Mode 2, LEDs are configured as follows:
LED_LINK = ON for good Link, BLINK for Activity
LED_SPEED = ON in 100Mb/s, OFF in 10Mb/s
LED_ACT/LED_COL = ON for Collision, OFF for No Collision
Full Duplex, OFF for Half Duplex
In Mode 3, LEDs are configured as follows:
LED_LINK = ON for Good Link, BLINK for Activity
LED_SPEED = ON in 100 Mb/s, OFF in 10-Mb/s
LED_ACT/LED_COL = ON for Full Duplex, OFF for Half Duplex</td></tr>
<tr><td>4:0</td><td>PHYADDR[4:0]</td><td>Strap, RW</td><td>PHY Address: PHY address for port.</td></tr>
</table>

5.6.2.7 10BASE-T Status/Control Register (10BTSCR)

This register is used for control and status for 10BASE-T device operation.

Table 5-36. 10BASE-T Status/Control Register (10BTSCR), address 1Ah

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	10BT_SERIAL	Strap, RW	**10Base-T Serial Mode (SNI)** 1 = Enables 10Base-T Serial Mode 0 = Normal Operation Places 10-Mb/s transmit and receive functions in Serial Network Interface (SNI) Mode of operation. Has no effect on 100-Mb/s operation.
14:12	RESERVED	0, RW	**RESERVED:** Must be zero.
11:9	SQUELCH	100, RW	**Squelch Configuration:** Used to set the Squelch 'ON' threshold for the receiver. Default Squelch ON is 330-mV peak.
8	LOOPBACK_10_DIS	0, RW	**10Base-T Loopback Disable:** In half-duplex mode, default 10BASE-T operation loops Transmit data to the Receive data in addition to transmitting the data on the physical medium. This is for consistency with earlier 10BASE2 and 10BASE5 implementations which used a shared medium. Setting this bit disables the loopback function. This bit does not affect loopback due to setting BMCR[14].
7	LP_DIS	0, RW	**Normal Link Pulse Disable:** 1 = Transmission of NLPs is disabled. 0 = Transmission of NLPs is enabled.
6	FORCE_LINK_10	0, RW	**Force 10Mb Good Link:** 1 = Forced Good 10-Mb Link. 0 = Normal Link Status.
5	RESERVED	0, RW	**RESERVED:** Must be zero.
4	POLARITY	RO/LH	**10Mb Polarity Status:** This bit is a duplication of bit 12 in the PHYSTS register. Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 1 = Inverted Polarity detected. 0 = Correct Polarity detected.
3	RESERVED	0, RW	**RESERVED:** Must be zero.
2	RESERVED	1, RW	**RESERVED:** Must be set to one.
1	HEARTBEAT_DIS	0, RW	**Heartbeat Disable:** This bit only has influence in half-duplex 10Mb mode. 1 = Heartbeat function disabled. 0 = Heartbeat function enabled. **When the device is operating at 100 Mb or configured for full duplex operation, this bit will be ignored - the heartbeat function is disabled.**
0	JABBER_DIS	0, RW	**Jabber Disable:** Applicable only in 10BASE-T. 1 = Jabber function disabled. 0 = Jabber function enabled.

5.6.2.8 CD Test and BIST Extensions Register (CDCTRL1)

This register controls test modes for the 10BASE-T Common Driver. In addition it contains extended control and status for the packet BIST function.

Table 5-37. CD Test and BIST Extensions Register (CDCTRL1), address 1Bh

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BIST_ERROR_COUNT	0, RO	**BIST ERROR Counter:** Counts number of errored data nibbles during Packet BIST. This value will reset when Packet BIST is restarted. The counter sticks when it reaches its max count.
7:6	RESERVED	0, RW	**RESERVED:** Must be zero.
5	BIST_CONT_MODE	0, RW	**Packet BIST Continuous Mode:** Allows continuous pseudo random data transmission without any break in transmission. This can be used for transmit VOD testing. This is used in conjunction with the BIST controls in the PHYCR Register (19h). For 10-Mb operation, jabber function must be disabled, bit 0 of the 10BTSCR (1Ah), JABBER_DIS = 1.
4	CDPATTEN_10	0, RW	**CD Pattern Enable for 10Mb:** 1 = Enabled. 0 = Disabled.
3	RESERVED	0, RW	**RESERVED:** Must be zero.
2	10MEG_PATT_GAP	0, RW	**Defines gap between data or NLP test sequences:** 1 = 15 µs. 0 = 10 µs.
1:0	CDPATTSEL[1:0]	00, RW	**CD Pattern Select[1:0]:** If CDPATTEN_10 = 1: 00 = Data, EOP0 sequence 01 = Data, EOP1 sequence 10 = NLPs 11 = Constant Manchester 1s (10-MHz sine wave) for harmonic distortion testing.

5.6.2.9 Phy Control Register 2 (PHYCR2)

This register provides additional general control.

Table 5-38. Phy Control Register 2 (PHYCR2), address 1Ch

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	RESERVED	0, RO	**RESERVED:** writes ignored, read as 0.
9	SOFT_RESET	0, W/SC	**Soft Reset:** Resets the entire device minus the registers – all configuration is preserved 1 = Reset, self-clearing.
8:0	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.

5.6.2.10 Energy Detect Control (EDCR)

This register provides control and status for the Energy Detect function.

Table 5-39. Energy Detect Control (EDCR), address 1Dh

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	ED_EN	Strap, RW	**Energy Detect Enable:** Allow Energy Detect Mode. When Energy Detect is enabled and Auto-Negotiation is disabled through the BMCR register, Auto-MDIX must be disabled through the PHYCR register.
14	ED_AUTO_UP	1, RW	**Energy Detect Automatic Power Up:** Automatically begin power-up sequence when Energy Detect Data Threshold value (EDCR[3:0]) is reached. Alternatively, device could be powered up manually using the ED_MAN bit (ECDR[12]).
13	ED_AUTO_DOWN	1, RW	**Energy Detect Automatic Power Down:** Automatically begin power-down sequence when no energy is detected. Alternatively, device could be powered down using the ED_MAN bit (EDCR[12]).
12	ED_MAN	0, RW/SC	**Energy Detect Manual Power Up/Down:** Begin power-up/down sequence when this bit is asserted. When set, the Energy Detect algorithm will initiate a change of Energy Detect state regardless of threshold (error or data) and timer values. In managed applications, this bit can be set after clearing the Energy Detect interrupt to control the timing of changing the power state.
11	ED_BURST_DIS	0, RW	**Energy Detect Bust Disable:** Disable bursting of energy detect data pulses. By default, Energy Detect (ED) transmits a burst of 4 ED data pulses each time the CD is powered up. When bursting is disabled, only a single ED data pulse will be send each time the CD is powered up.
10	ED_PWR_STATE	0, RO	**Energy Detect Power State:** Indicates current Energy Detect Power state. When set, Energy Detect is in the powered up state. When cleared, Energy Detect is in the powered down state. This bit is invalid when Energy Detect is not enabled.
9	ED_ERR_MET	0, RO/COR	**Energy Detect Error Threshold Met:** No action is automatically taken upon receipt of error events. This bit is informational only and would be cleared on a read.
8	ED_DATA_MET	0, RO/COR	**Energy Detect Data Threshold Met:** The number of data events that occurred met or surpassed the Energy Detect Data Threshold. This bit is cleared on a read.
7:4	ED_ERR_COUNT	0001, RW	**Energy Detect Error Threshold:** Threshold to determine the number of energy detect error events that must cause the device to take action. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.
3:0	ED_DATA_COUNT	0001, RW	**Energy Detect Data Threshold:** Threshold to determine the number of energy detect events that must cause the device to take actions. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.

5.6.3 Link Diagnostics Registers - Page 2

Page 2 Link Diagnostics Registers are accessible by setting bits [1:0] = 10 of PAGESEL (13h).

5.6.3.1 100Mb Length Detect Register (LEN100_DET), Page 2, address 14h

This register contains linked cable length estimation in 100-Mb operation. The cable length is an estimation of the effective cable length based on the characteristics of the recovered signal. The cable length is valid only during 100-Mb operation with a valid Link status indication.

Table 5-40. 100Mb Length Detect Register (LEN100_DET), address 14h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	ARESERVED	0, RO	**RESERVED:** writes ignored, read as 0.
7:0	CABLE_LEN	0, RO	**Cable Length Estimate:** Indicates an estimate of effective cable length in meters. A value of FF indicates cable length cannot be determined.

5.6.3.2 100Mb Frequency Offset Indication Register (FREQ100), Page 2, address 15h

This register returns an indication of clock frequency offset relative to the link partner. Two values can be read, the long term Frequency Offset, or a short term Frequency Control value. The Frequency Control value includes short term phase correction. The variance between the Frequency Control value and the Frequency Offset can be used as an indication of the amount of jitter in the system.

Table 5-41.

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	SAMPLE_FREQ	0, RW	**Sample Frequency Offset:** If Sel_FC is set to a 0, then setting this bit to a 1 will poll the DSP for the long-term Frequency Offset value. The value will be avail- able in the Freq_Offset bits of this register. If Sel_FC is set to a 1, then setting this bit to a 1 will poll the DSP for the current Frequency Control value. The value will be available in the Freq_Offset bits of this register. This register bit will always read back as 0.
14:9	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
8	SEL_FC	0, RW	**Select Frequency Control:** Setting this bit to a 1 will select the current Frequency Control value instead of the Frequency Offset. This value contains Frequency Offset plus the short term phase correction and can be used to indicate amount of jitter in the system. The value will be available in the Freq_Offset bits of this register.
7:0	FREQ_OFFSET	0, RO	**Frequency Offset:** Frequency offset value loaded from the DSP following assertion of the Sample_Freq control bit. The Frequency Offset or Frequency Control value is a 2s-complement signed value in units of approximately 5.1562ppm. The range is as follows: 0x7F = +655ppm 0x00 = 0ppm 0x80 = -660ppm

5.6.3.3 TDR Control Register (TDR_CTRL), Page 2, address 16h

This register contains control for the Time Domain Reflectometry (TDR) cable diagnostics. The TDR cable diagnostics sends pulses down the cable and captures reflection data to be used to estimate cable length and detect certain cabling faults.

Table 5-42. TDR Control Register (TDR_CTRL), address 16h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	TDR_ENABLE	0, RW	**TDR Enable:** Enable TDR mode. This forces powerup state to correct operating condition for sending and receiving TDR pulses.
14	TDR_100Mb	0, RW	**TDR 100Mb:** Sets TDR controller to use the 100-Mb Transmitter. This allows for sending pulse widths in multiples of 8 ns. Pulses in 100-Mb mode will alternate between positive pulses and negative pulses. Default operation uses the 10-Mb Link Pulse generator. Pulses may include just the 50-ns pre-emphasis portion of the pulse or the 100-ns full link pulse (as controlled by setting TDR Width).
13	TX_CHANNEL	0, RW	**Transmit Channel Select:** Select transmit channel for sending pulses. Pulse can be sent on the Transmit or Receive pair. 0 : Transmit channel 1 : Receive channel
12	RX_CHANNEL	0, RW	**Receive Channel Select:** Select receive channel for detecting pulses. Pulse can be monitored on the Transmit or Receive pair. 0 : Transmit channel 1 : Receive channel
11	SEND_TDR	0, RW/SC	**Send TDR Pulse:** Setting this bit will send a TDR pulse and enable the monitor circuit to capture the response. This bit will automatically clear when the capture is complete.
10:8	TDR_WIDTH	0, RW	**TDR Pulse Width:** Pulse width in clocks for the transmitted pulse. In 100-Mb mode, pulses are in 8-ns increments. In 10-Mb mode, pulses are in 50-ns increments, but only 50-ns or 100-ns pulses can be sent. Sending a pulse of 0 width will not transmit a pulse, but allows for baseline testing.
7	TDR_MIN_MODE	0, RW	**Min/Max Mode control:** This bit controls direction of the pulse to be detected. Default looks for a positive peak. Threshold and peak values will be interpreted appropriately based on this bit. 0 : Max Mode, detect positive peak 1 : Min Mode, detect negative peak
6	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
5:0	RX_THRESHOLD	<10_000>, RW	**RX Threshold:** This value provides a threshold for measurement to the start of a peak. If Min Mode is set to 0, data must be greater than this value to trigger a capture. If Min Mode is 1, data must be less than this value to trigger a capture. Data ranges from 0x00 to 0x3F, with 0x20 as the midpoint. Positive data is greater than 0x20, negative data is less than 0x20.

5.6.3.4 TDR Window Register (TDR_WIN), Page 2, address 17h

This register contains sample window control for the Time Domain Reflectometry (TDR) cable diagnostics. The two values contained in this register specify the beginning and end times for the window to monitor the response to the transmitted pulse. Time values are in 8ns increments. This provides a method to search for multiple responses and also to screen out the initial outgoing pulse.

Table 5-43. TDR Window Register (TDR_WIN), address 17h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_START	0, RW	**TDR Start Window:** Specifies start time for monitoring TDR response.
7:0	TDR_STOP	0xFF, RW	**TDR Stop Window:** Specifies stop time for monitoring TDR response. The Stop Window must be set to a value greater than or equal to the Start Window.

5.6.3.5 TDR Peak Register (TDR_PEAK), Page 2, address 18h

This register contains the results of the TDR Peak Detection. Results are valid if the TDR_CTRL[11] is clear following sending the TDR pulse.

Table 5-44. TDR Peak Register (TDR_PEAK), address 18h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
13:8	TDR_PEAK	0, RO	**TDR Peak Value:** This register contains the peak value measured during the TDR sample window. If Min Mode control (TDR_CTRL[7]) is 0, this contains the maximum detected value. If Min Mode control is 1, this contains the minimum detected value.
7:0	TDR_PEAK_TIME	0, RO	**TDR Peak Time:** Specifies the time for the first occurrence of the peak value.

5.6.3.6 TDR Threshold Register (TDR_THR), Page 2, address 19h

This register contains the results of the TDR Threshold Detection. Results are valid if the TDR_CTRL[11] is clear following sending the TDR pulse.

Table 5-45. TDR Threshold Register (TDR_THR), address 19h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:9	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
8	TDR_THR_MET	0, RO	**TDR Threshold Met:** This bit indicates the TDR threshold was met during the sample window. A value of 0 indicates the threshold was not met.
7:0	TDR_THR_TIME	0, RO	**TDR Threshold Time:** Specifies the time for the first data that met the TDR threshold. This field is only valid if the threshold was met.

5.6.3.7 Variance Control Register (VAR_CTRL), Page 2, address 1Ah

The Variance Control and Data Registers provide control and status for the Cable Signal Quality Estimation function. The Cable Signal Quality Estimation allows a simple method of determining an approximate Signal-to-Noise Ratio for the 100-Mb receiver. This register contains the programmable controls and status bits for the variance computation, which can be used to make a simple Signal-to-Noise Ratio estimation.

Table 5-46. Variance Control Register (VAR_CTRL), address 1Ah

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	VAR_RDY	0, RO	**Variance Data Ready Status:** Indicates new data is available in the Variance data register. This bit will be automatically cleared after two consecutive reads ot VAR_DATA.
14:4	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
3	VAR_FREEZE	0, RW	**Freeze Variance Registers:** Freeze VAR_DATA register. This bit is ensures that VAR_DATA register is frozen for software reads. This bit is automatically cleared after two consecutive reads of VAR_DATA.
2:1	VAR_TIMER	0, RW	**Variance Computation Timer (in ms):** Selects the Variance computation timer period. After a new value is written, computation is automatically restarted. New variance register values are loaded after the timer elapses.. Var_Timer = 0 => 2 ms timer (default) Var_Timer = 1 => 4 ms timer Var_Timer = 2 => 6 ms timer Var_Timer = 3 => 8 ms timer Time units are actually 2^{17} cycles of an 8ns clock, or 1.048576ms
0	VAR_ENABLE	0, RW	**Variance Enable:** Enable Variance computation. Off by default.

5.6.3.8 Variance Data Register (VAR_DATA), Page 2, address 1Bh

This register contains the 32-bit Variance Sum. The contents of the data are valid only when VAR_RDY is asserted in the VAR_CTRL register. Upon detection of VAR_RDY asserted, software must set the VAR_FREEZE bit in the VAR_CTRL register to prevent loading of a new value into the VAR_DATA register. Because the Variance-Data value is 32-bits, two reads of this register are required to get the full value.

Table 5-47. Variance Data Register (VAR_DATA), address 1Bh

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	VAR_DATA	0, RO	**Variance Data:** Two reads are required to return the full 32-bit Variance Sum value. Following setting the VAR_FREEZE control, the first read of this register will return the low 16 bits of the Variance data. A second read will return the high 16 bits of Variance data.

5.6.3.9 Link Quality Monitor Register (LQMR), Page 2, address 1Dh

This register contains the controls for the Link Quality Monitor function. The Link Quality Monitor provides a mechanism for programming a set of thresholds for DSP parameters. If the thresholds are violated, an interrupt will be asserted if enabled in the MISR. Monitor control and status are available in this register, while the LQDR register controls read/write access to threshold values and current parameter values. Reading of LQMR register clears warning bits and re-arms the interrupt generation. In addition, this register provides a mechanims for allowing automatic reset of the 100-Mb link based on the Link Quality Monitor status.

Table 5-48. Link Quality Monitor Register (LQMR), address 1Dh

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	LQM_ENABLE	0, RW	**Link Quality Monitor Enable:** Enables the Link Quality Monitor. The enable is qualified by having a valid 100Mb link. In addition, the individual thresholds can be dis- abled by setting to the max or min values.
14:10	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
9	FC_HI_WARN	0, RO/COR	**Frequency Control High Warning:** This bit indicates the Frequency Control High Threshold was exceeded. This register bit will be cleared on read.
8	FC_LO_WARN	0, RO/COR	**Frequency Control Low Warning:** This bit indicates the Frequency Control Low Threshold was exceeded. This register bit will be cleared on read.
7	FREQ_HI_WARN	0, RO/COR	**Frequency Offset High Warning:** This bit indicates the Frequency Offset High Threshold was exceeded. This register bit will be cleared on read.
6	FREQ_LO_WARN	0, RO/COR	**Frequency Offset Low Warning:** . This bit indicates the Frequency Offset Low Threshold was exceeded. This register bit will be cleared on read
5	DBLW_HI_WARN	0, RO/COR	**DBLW High Warning:** This bit indicates the DBLW High Threshold was exceeded. This register bit will be cleared on read.
4	DBLW_LO_WARN	0, RO/COR	**DBLW Low Warning:** This bit indicates the DBLW Low Threshold was exceeded. This register bit will be cleared on read.
3	DAGC_HI_WARN	0, RO/COR	**DAGC High Warning:** This bit indicates the DAGC High Threshold was exceeded. This register bit will be cleared on read.
2	DAGC_LO_WARN	0, RO/COR	**DAGC Low Warning:** This bit indicates the DAGC Low Threshold was exceeded. This register bit will be cleared on read.
1	C1_HI_WARN	0, RO/COR	**C1 High Warning:** This bit indicates the DEQ C1 High Threshold was exceeded. This register bit will be cleared on read.
0	C1_LO_WARN	0, RO/COR	**C1 Low Warning:** This bit indicates the DEQ C1 Low Threshold was exceeded. This register bit will be cleared on read.

5.6.3.10 Link Quality Data Register (LQDR), Page 2

This register provides read/write control of thresholds for the 100Mb Link Quality Monitor function. The register also provides a mechanism for reading current adapted parameter values. Threshold values may not be written if the device is powered-down.

Table 5-49. Link Quality Data Register (LQDR), address 1Eh

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
13	SAMPLE_PARAM	0, RW	**Sample DSP Parameter:** Setting this bit to a 1 enables reading of current parameter values and initiates sampling of the parameter value. The parameter to be read is selected by the LQ_PARAM_SEL bits.
12	WRITE_LQ_THR	0, RW	**Write Link Quality Threshold:** Setting this bit will cause a write to the Threshold register selected by LQ_PARAM_SEL and LQ_THR_SEL. The data written is contained in LQ_THR_DATA. This bit will always read back as 0.
11:9	LQ_PARAM_SEL	0, RW	**Link Quality Parameter Select:** This 3-bit field selects the Link Quality Parameter. This field is used for sampling current parameter values as well as for reads/writes to Threshold values. The following encodings are available: 000: DEQ_C1 001: DAGC 010: DBLW 011: Frequency Offset 100: Frequency Control
8	LQ_THR_SEL	0, RW	**Link Quality Threshold Select:** This bit selects the Link Quality Threshold to be read or written. A 0 selects the Low threshold, while a 1 selects the high threshold. When combined with the LQ_PARAM_SEL field, the following encodings are available {LQ_PARAM_SEL, LQ_THR_SEL}: 000,0: DEQ_C1 Low 000,1: DEQ_C1 High 001,0: DAGC Low 001,1: DAGC High 010,0: DBLW Low 010,1: DBLW High 011,0: Frequency Offset Low 011,1: Frequency Offset High 100,0: Frequency Control Low 100,1: Frequency Control High
7:0	LQ_THR_DATA	0, RW	**Link Quality Threshold Data:** The operation of this field is dependent on the value of the Sample_Param bit. **If Sample_Param = 0:** On a write, this value contains the data to be written to the selected Link Quality Threshold register. On a read, this value contains the current data in the selected Link Quality Threshold register. **If Sample_Param = 1:** On a read, this value contains the sampled parameter value. This value will remain unchanged until a new read sequence is started

6 Applications, Implementation, and Layout

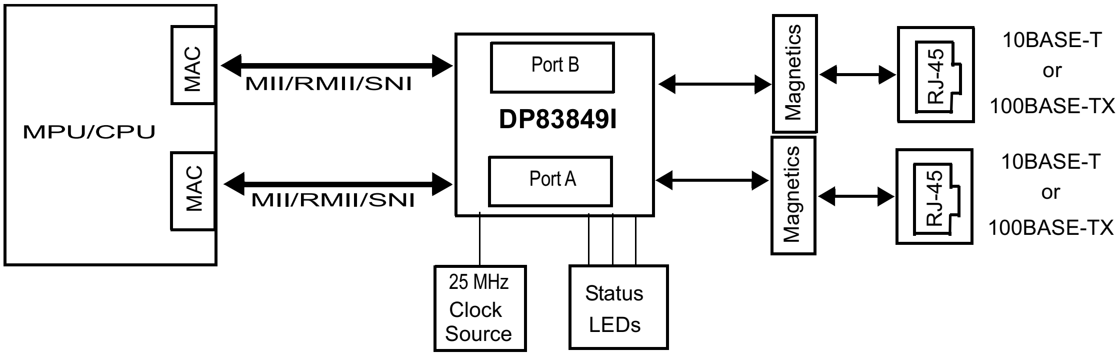
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The DP83849I is a dual port physical layer Ethernet transceiver. When using the device for Ethernet application, it is necessary to meet certain requirements for normal operation of the device. The following typical application and design requirements can be used for selecting appropriate component values for DP83849.

6.2 Typical Application



6.2.1 Design Requirements

For this design example, use the parameters listed in Table 6-1 as the input parameters.

Table 6-1. Design Parameters

PARAMETER	EXAMPLE VALUE
VIN	3.3 V
VOUT	VCC – 0.5 V
Clock Input	25 MHz for MII and 50 MHz for RMII

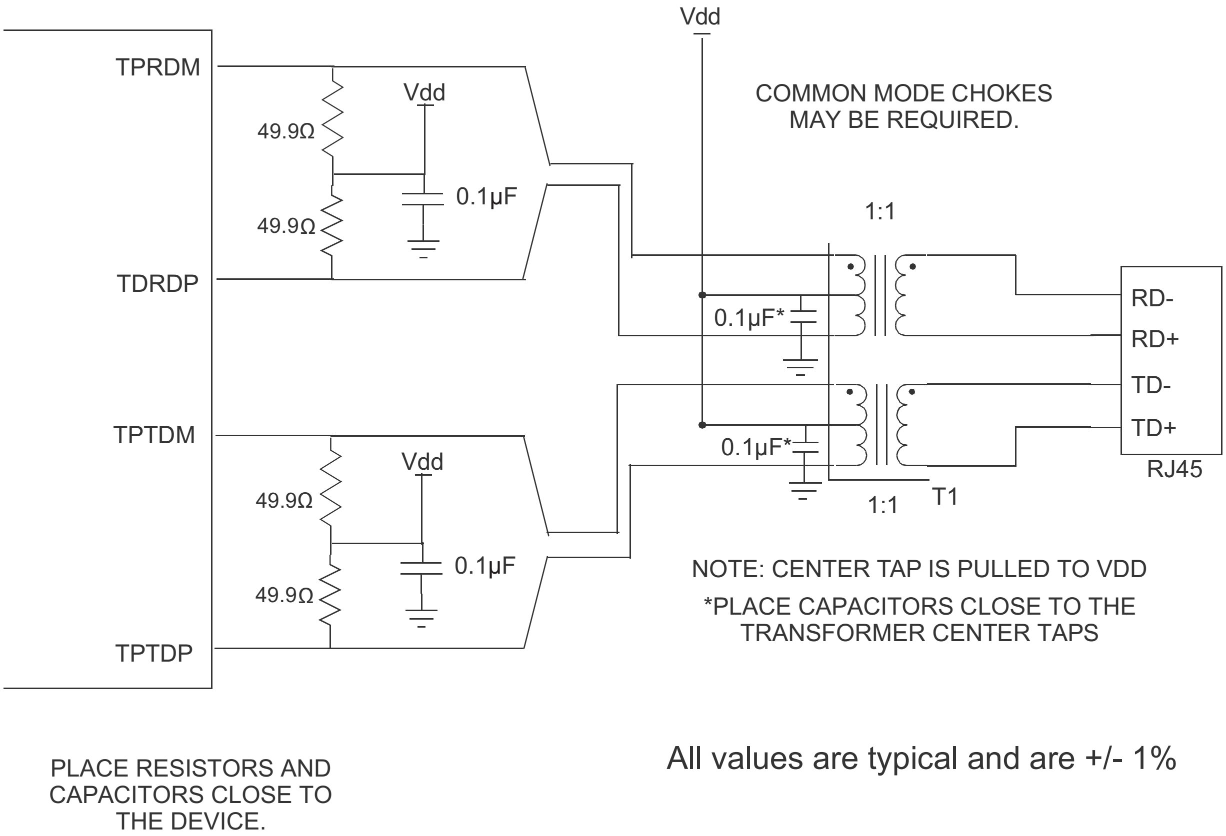
6.2.2 Detailed Design Procedure

6.2.2.1 TPI Network Circuit

Figure 6-1 shows the recommended circuit for a 10/100 Mb/s twisted pair interface.

Below is a partial list of recommended transformers. It is important that the user realize that variations with PCB and component characteristics requires that the application be tested to ensure that the circuit meets the requirements of the intended application.

- Pulse H1102
- Pulse H2019
- Belfuse S558-5999-U7
- Halo TG110-S050N2RL



COMMON MODE CHOKES MAY BE REQUIRED.

NOTE: CENTER TAP IS PULLED TO VDD

*PLACE CAPACITORS CLOSE TO THE TRANSFORMER CENTER TAPS

PLACE RESISTORS AND CAPACITORS CLOSE TO THE DEVICE.

All values are typical and are +/- 1%

Figure 6-1. 10/100 Mb/s Twisted Pair Interface

6.2.2.2 Clock In (X1) Requirements

The DP83849I supports an external CMOS level oscillator source or a crystal resonator device.

6.2.2.2.1 Oscillator

If an external clock source is used, X1 must be tied to the clock source and X2 must be left floating.

Specifications for CMOS oscillators: 25 MHz in MII Mode and 50 MHz in RMII Mode are listed in Table 6-2 and Table 6-3.

6.2.2.2.2 Crystal

A 25 MHz, parallel, 20-pF load crystal resonator must be used if a crystal source is desired. Figure 6-2 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads. The oscillator circuit is designed to drive a parallel resonance AT cut crystal with a minimum drive level of 100 µW and a maximum of 500 µW. If a crystal is specified for a lower drive level, a current limiting resistor must be placed in series between X2 and the crystal.

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, C_{L1} and C_{L2} must be set at 33 pF, and R1 must be set at 0 Ω.

Specification for 25-MHz crystal are listed in Table 6-4.

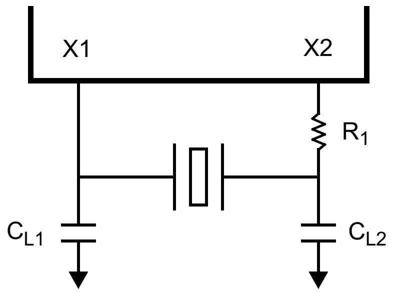


Figure 6-2. Crystal Oscillator Circuit

Table 6-2. 25-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			50	ppm
Frequency Stability	1 year aging			50	ppm
Rise / Fall Time	20%–80%			6	nsec
Jitter	Short term			800 (1)	psec
Jitter	Long term			800 (1)	psec
Symmetry	Duty Cycle	40%		60%	

(1) This limit is provided as a guideline for component selection and **not** guaranteed by production testing. Refer to SNLA076, *PHYTER 100 Base-TX Reference Clock Jitter Tolerance*, for details on jitter performance.

Table 6-3. 50-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			50		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	Operational Temperature			±50	ppm
Rise / Fall Time	20%–80%			6	nsec
Jitter	Short term			800 (1)	psec
Jitter	Long term			800 (1)	psec
Symmetry	Duty Cycle	40%		60%	

(1) This limit is provided as a guideline for component selection and **not** guaranteed by production testing. Refer to SNLA076, *PHYTER 100 Base-TX Reference Clock Jitter Tolerance*, for details on jitter performance.

Table 6-4. 25-MHz Crystal Specification

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Load Capacitance		25		40	pF

6.2.3 Power Feedback Circuit

To ensure correct operation for the DP83849I, parallel caps with values of 10 µF and 0.1 µF must be placed close to pin 31 (**PFBOUT**) of the device. Pin 7 (**PFBIN1**), pin 28 (**PFBIN2**), pin 34 (**PFBIN3**) and pin 54 (**PFBIN4**) must be connected to pin 31 (**PFBOUT**), each pin requires a small capacitor (0.1 µF). See Figure 6-3 for proper connections.

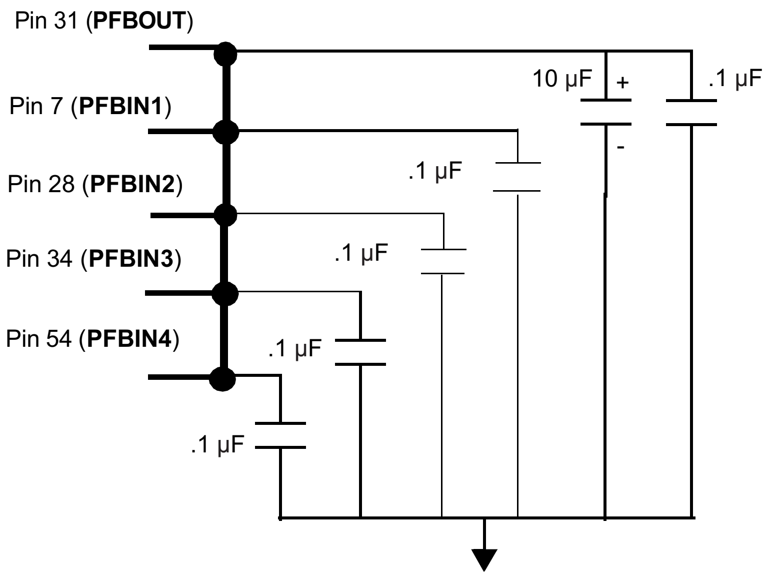


Figure 6-3. Power Feedback Connections

6.2.4 *Power Down/Interrupt*

The Power Down and Interrupt functions are multiplexed on pin 18 and pin 44 of the device. By default, this pin functions as a power down input and the interrupt function is disabled. Setting bit 0 (INT_OE) of MICR (11h) will configure the pin as an active low interrupt output. Ports A and B can be powered down individually, using the separate PWRDOWN_INT_A and PWRDOWN_INT_B pins.

6.2.4.1 Power Down Control Mode

The PWRDOWN_INT pins can be asserted low to put the device in a Power Down mode. This is equivalent to setting bit 11 (Power Down) in the Basic Mode Control Register, BMCR (00h). An external control signal can be used to drive the pin low, overcoming the weak internal pullup resistor. Alternatively, the device can be configured to initialize into a Power Down state by use of an external pulldown resistor on the PWRDOWN_INT pin. Because the device will still respond to management register accesses, setting the INT_OE bit in the MICR register will disable the PWRDOWN_INT input, allowing the device to exit the Power Down state

6.2.4.2 Interrupt Mechanisms

Because each port has a separate interrupt pin, the interrupts can be connected individually or may be combined in a wired-OR fashion. If the interrupts share a single connection, each port status must be checked following an interrupt.

The interrupt function is controlled through register access. All interrupt sources are disabled by default. Setting bit 1 (INTEN) of MICR (11h) will enable interrupts to be output, dependent on the interrupt mask set in the lower byte of the MISR (12h). The PWRDOWN_INT pin is asynchronously asserted low when an interrupt condition occurs. The source of the interrupt can be determined by reading the upper byte of the MISR. One or more bits in the MISR will be set, denoting all currently pending interrupts. Reading of the MISR clears ALL pending interrupts.

Example: To generate an interrupt on a change of link status or on a change of energy detect power state, the steps would be:

- Write 0003h to MICR to set INTEN and INT_OE
- Write 0060h to MISR to set ED_INT_EN and LINK_INT_EN
- Monitor PWRDOWN_INT pin

When PWRDOWN_INT pin asserts low, the user would read the MISR register to see if the ED_INT or LINK_INT bits are set; that is, which source caused the interrupt. After reading the MISR, the interrupt bits must clear and the PWRDOWN_INT pin will deassert.

6.2.5 Application Curves

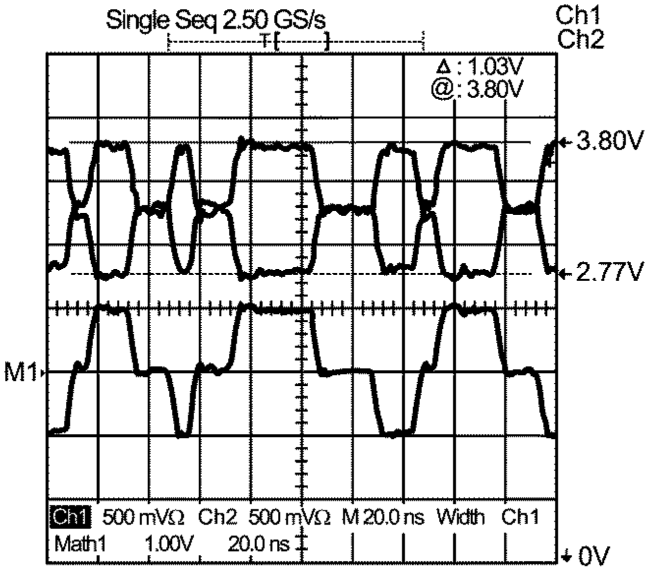


Figure 6-4. Sample 100-Mb/s Waveform (MLT-3)

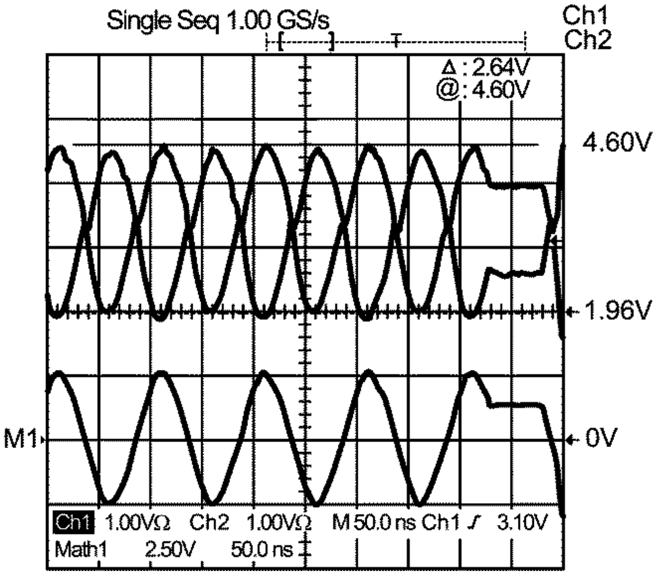


Figure 6-5. Sample 10-Mb/s Waveform

7 Power Supply Recommendations

The device V_{DD} supply pins must be bypassed with low-impedance 0.1-µF surface mount capacitors. To reduce EMI, the capacitors must be places as close as possible to the component V_{DD} supply pins, preferably between the supply pins and the vias connecting to the power plane. In some systems it may be desirable to add 0-Ω resistors in series with supply pins, as the resistor pads provide flexibility if adding EMI beads becomes necessary to meet system level certification testing requirements. (See Figure 7-1) It is recommended the PCB have at least one solid ground plane and one solid V_{DD} plane to provide a low impedance power source to the component. This also provides a low impedance return path for non-differential digital MII and clock signals. A 10.0-µF capacitor must also be placed near the PHY component for local bulk bypassing between the V_{DD} and ground planes.

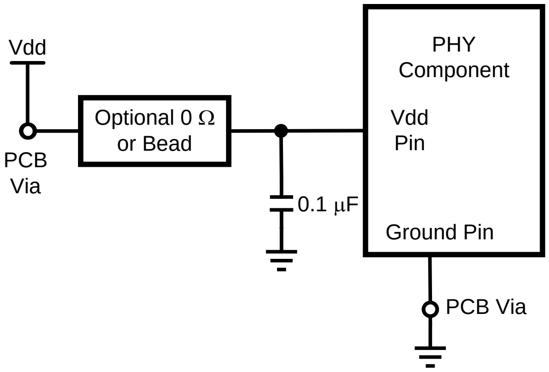


Figure 7-1. V_{DD} Bypass Layout

8 Layout

8.1 Layout Guidelines

Place the 49.9-Ω,1% resistors, and 0.1-µF decoupling capacitor near the PHYTER TD± and RD± pins and through directly to the V_{DD} plane.

Stubs must be avoided on all signal traces, especially the differential signal pairs. See Figure 8-1. Within the pairs (for example, TD+ and TD-) the trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and increased EMI. See Figure 8-1.

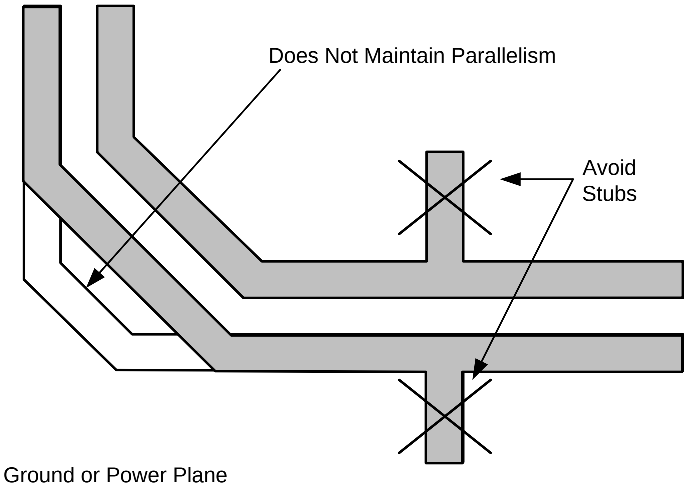


Figure 8-1. Differential Signal Pair - Stubs

Ideally, there must be no crossover or through on the signal paths. Vias present impedance discontinuities and must be minimized. Route an entire trace pair on a single layer if possible. PCB trace lengths must be kept as short as possible.

Signal traces must not be run such that they cross a plane split. See Figure 8-2. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.

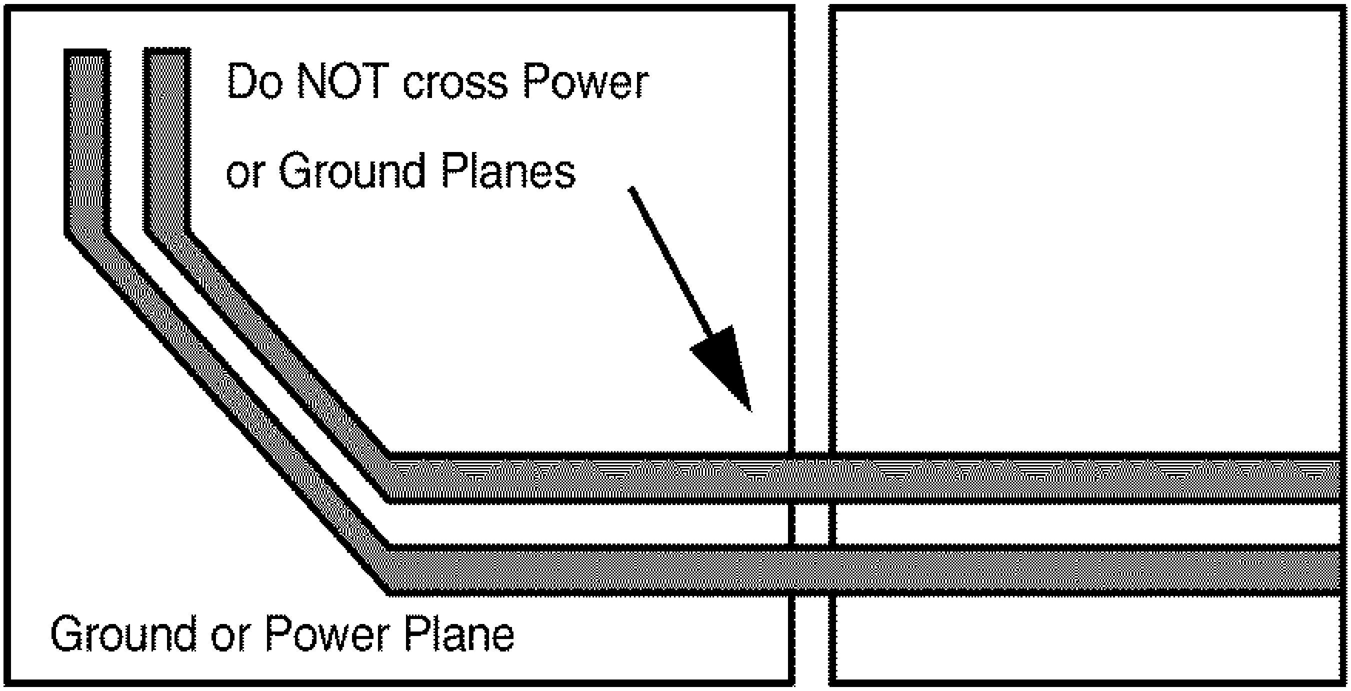


Figure 8-2. Differential Signal Pair-Plane Crossing

MDI signal traces must have 50 Ω to ground or 100-Ω differential controlled impedance. Many tools are available online to calculate this.

8.1.1 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a 4-layer PCB is recommended for implementing PHYTER components in end user systems. The following layer stack-ups are recommended for four, six, and eight-layer boards, although other options are possible.

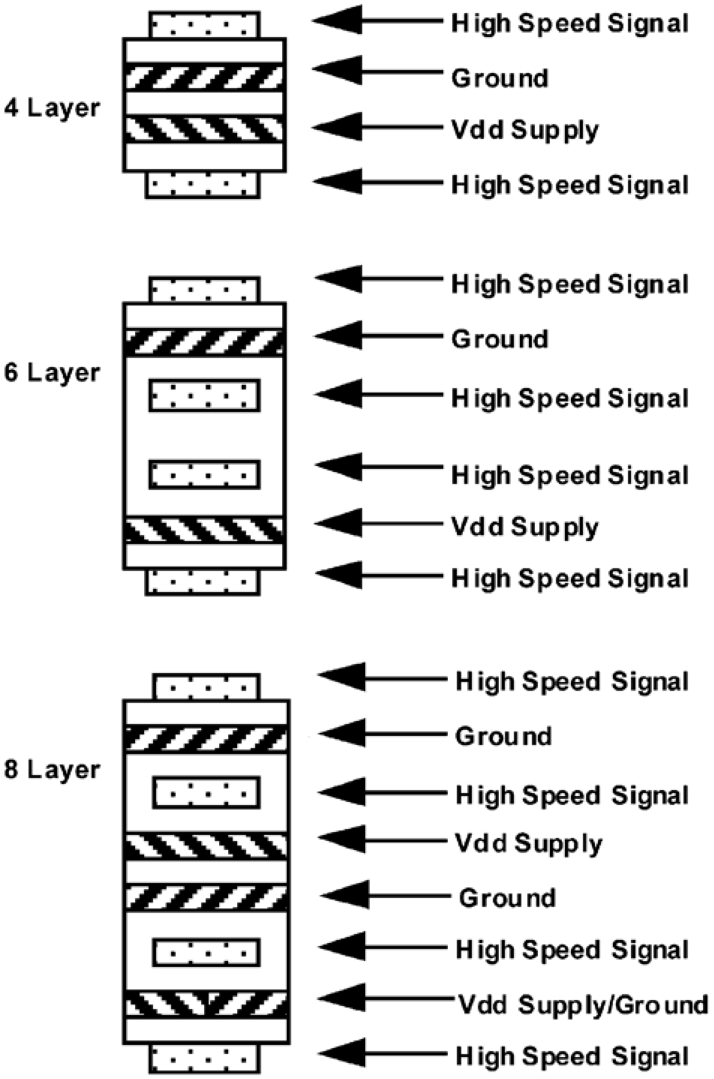


Figure 8-3. PCB Stripline Layer Stacking

Within a PCB it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. Figure 8-4 illustrates alternative PCB stacking options.

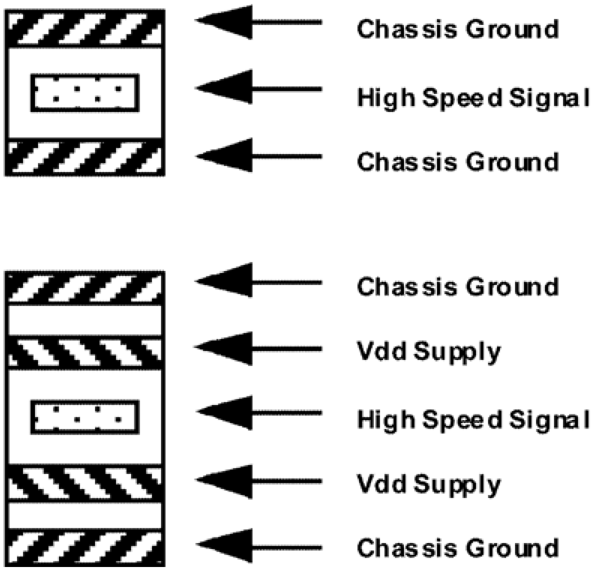


Figure 8-4. Alternative PCB Stripline Layer Stacking

8.2 Layout Example

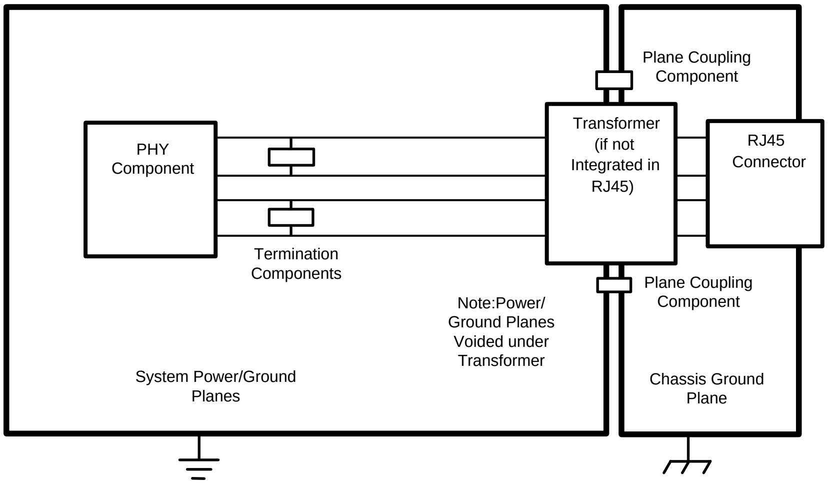


Figure 8-5. Layout Example

9 Device and Documentation Support

9.1 Community Resources

9.1.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.2 Trademarks

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9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical Packaging and Orderable Information

10.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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