DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY

1 Features

- Low and deterministic latency
  - TX latency: 40 ns, RX latency: 170 ns
  - Deterministic latency over power cycles < ±2 ns
  - Fixed phase XI to TX_CLK relationship < ±2 ns
- Robust and small system solution
  - Integrated circuitry for enhanced EMC
  - IEC 61000-4-2 ESD: ±8 kV contact, ±15 kV air
  - IEC 61000-4-4 EFT: ±4 kV @ 5 kHz, 100 kHz
  - CISPR 22 conducted emissions Class B
  - CISPR 22 radiated emissions Class B
  - Fast link-drop < 10 µs
  - Cable reach > 150 meters
  - Voltage mode line driver
  - Integrated terminations on MAC interface
  - Voltage tolerance: ±10%
- Two selectable pin modes in single device
  - ENHANCED mode for additional features
  - BASIC mode for common Ethernet pinout
- Low power consumption < 160 mW
- MAC interfaces: MII, RMII
- Programmable energy-saving modes
  - Active sleep
  - Deep power down
  - Wake-on-LAN (WoL)
- Diagnostic tools: cable diagnostics, built-in self-test (BIST), loopback modes
- Single, 3.3-V power supply
- I/O voltages: 1.8 V or 3.3 V
- RMII back-to-back repeater mode
- DP83826E operating temperature range: –40°C to 105°C
- DP83826I operating temperature range: –40°C to 85°C
- IEEE 802.3 compliant: 10BASE-Te, 100BASE-TX

2 Applications

- Factory automation, robotics and motion control
- Motor drives
- Grid infrastructure
- Building automation
- Industrial Ethernet fieldbus

3 Description

The DP83826 offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems.

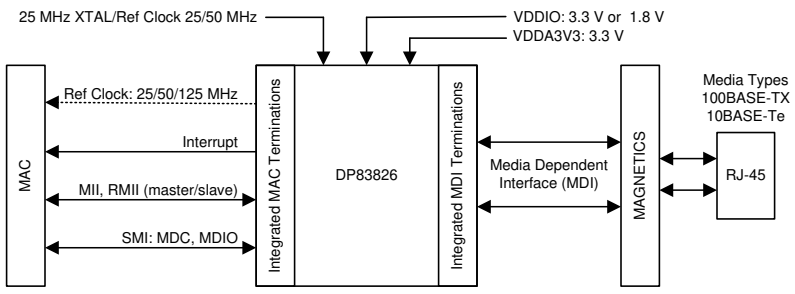
The two configurable modes are BASIC standard Ethernet mode that uses a common Ethernet pinout, and ENHANCED Ethernet mode which supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with the additional features and hardware bootstraps configuration.

Device Family Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)	ATTRIBUTES
DP83826E/I	VQFN (32)	5.00 mm × 5.00 mm	Lowest latency, common pinout
DP83825I	WQFN (24)	3.00 mm × 3.00 mm	Small size, optimized solution cost
DP83822HF/IF/H/I	VQFN (32)	5.00 mm × 5.00 mm	Wide temperature range, fiber, and RGMII support

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2020) to Revision B — **Page**

- Added DP83826I temperature range in Electrical Section also ... 1
- Added DP83826I to Device Family Information table ... 1

Changes from Original (January 2020) to Revision A — **Page**

- Added link to DP83826EVM User's Guide ... 1
- Deleted pin 18 from Table 2 ... 3
- Changed ENHANCED Mode pin map and pin functions table to match pin names ... 4
- Changed BASIC Mode pin map and pin functions table to match pin names ... 7
- Deleted "This pin can be configured to RX_DV in RMII mode to enable RMII Repeater Mode." from Pin Functions (BASIC Mode) ... 8
- Added the *100BASE-TX Transmit Latency Timing* graphic ... 22
- Added the *100BASE-TX Receive Latency Timing* graphic ... 23
- Added steps to disable CLKOUT via register configuration in Clock Output ... 30
- Deleted mentions of "clause 45" from Serial Management Interface and Extended Register Space Access ... 34
- Deleted "Analog Loopback requires 100-Ω terminations across pins #1 and #2 as well as 100-Ω terminations across pins #3 and #6 at the RJ45." from Analog Loopback ... 42
- Added row for RMII slave mode configuration in Table 16 ... 48
- Added register descriptions for 0x0459 and 0x045A ... 49
- Changed register description for 0x0460 ... 49

5 Mode Comparison Tables

The DP83826 operates in two different modes: ENHANCED mode and BASIC mode. ENHANCED mode allows the DP83826 to support real-time Ethernet applications in addition to the standard Ethernet applications. BASIC mode also allows the DP83826 to support all the standard Ethernet applications, additionally the DP83826 in this mode, matches a common pinout configuration used in many applications.

Table 1. Selecting EHANCED Mode or BASIC Mode

ENHANCED Mode	BASIC Mode
Connect ModeSelect (Pin 1) to VDDIO through pullup resistor	Short ModeSelect (Pin 1) to GND

Table 2. Pin Map Difference Between ENHANCED Mode and BASIC Mode

PIN NO.	ENHANCED MODE	BASIC MODE	DESCRIPTION
31	CLKOUT/LED1	TX_ER/LED1	Offers reference clockout 25 MHz at POR. Clock is not interrupted by RST_N
21	PWRDN/INT	INT	Offers *power down* as default pin function

Table 3. Hardware Bootstraps Difference Between ENHANCED Mode and BASIC Mode

HARDWARE BOOTSTRAPS	ENHANCED Mode(1)	BASIC Mode
Fast link-drop enable and disable(2)	Yes	No
Auto-MDIX enable and disable(2)	Yes	No
Force MDI/MDIX selection(2)	Yes	No
RMII back-to-back repeater mode configuration(3)	Yes	No
MII or RMII selection	Yes	Yes
Speed selection (10 M or 100 M)	No	Yes
MII isolate enable and disable	No	Yes
Auto-negotiation enable and disable	Yes	Yes
Number of PHY addresses available	8	8
Half or full duplex selection	No	Yes
CLKOUT in place of LED1	Yes	No

(1) ENHANCED mode includes all the modes of operation BASIC mode can be configured to. The difference is, in these modes of operation, ENHANCED mode may require register configuration.
(2) These pin bootstraps enable the ENHANCED mode DP83826 to meet the stringent requirements of real-time Ethernet applications.
(3) This pin bootstrap enables the ENHANCED mode DP83826 to function as an RMII repeater.

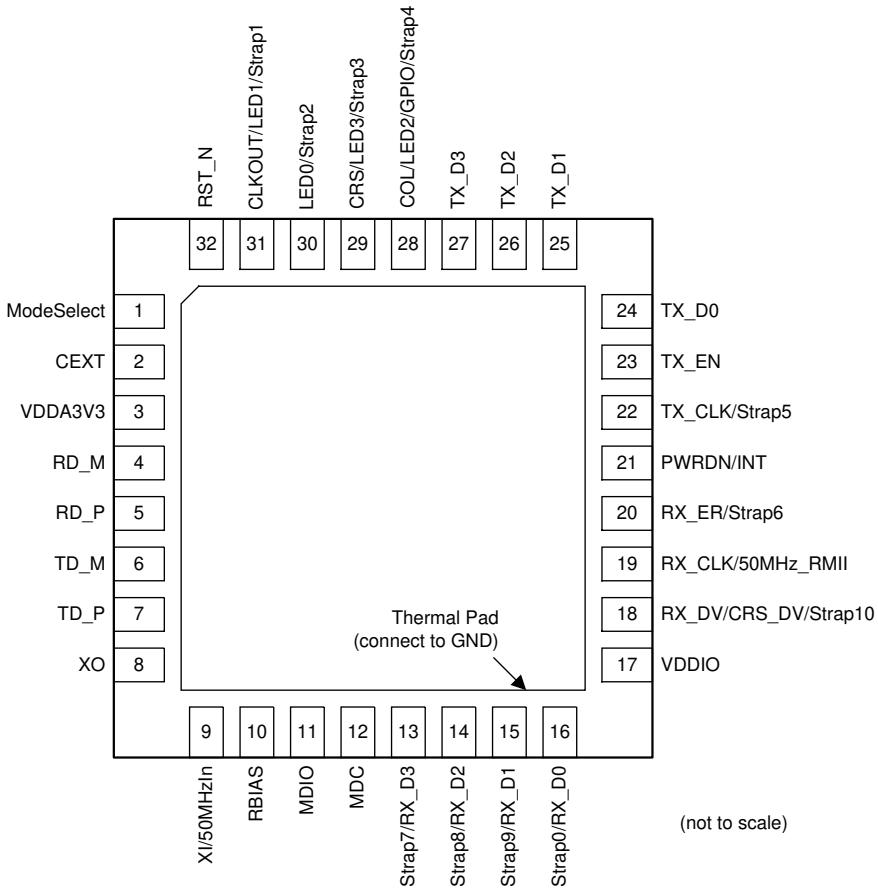
NOTE

For standardized list of Ethernet related acronyms, refer to *Chinese and English Definitions of Acronyms Related to Ethernet Products*.

6 Pin Configuration and Functions (ENHANCED Mode)

The ENHANCED mode is one of two modes that the DP83826 can be configured in at start-up. This mode allows the DP83826 to support real-time Ethernet applications in addition to the standard Ethernet applications. To configure the DP83826 to ENHANCED mode, leave ModeSelect (pin 1) unconnected or pull up with a resistor to VDDIO.

RHB Package
32-Pin QFN
(Top View)



Pin Functions (ENHANCED Mode)

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
ModeSelect	1	Reset: I, PU Active: I, PU	This pin selects the DP83826 operating mode: BASIC mode or ENHANCED mode. For ENHANCED mode, this pin shall be left NC or pulled-up with a resistor to VDDIO. For BASIC mode, this pin shall be shorted to GND.
CEXT	2	A	External capacitor: Connect the CEXT pin through a 2-nF capacitor to GND.
VDDA3V3	3	Power	Input analog supply: 3V3. For decoupling capacitor requirements, refer to Figure 30 section of data sheet.
RD_M	4	A	Differential receive input (physical media dependent: PMD): These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX specific signaling mode.
RD_P	5	A	
TD_M	6	A	Differential transmit output (PMD): These differential outputs are configured to either 10BASE-Te or 100BASE-TX signaling mode based on configuration chosen for PHY.
TD_P	7	A	
XO	8	A	Crystal output: Reference clock output. XO pin is used for crystal only. Leave this pin floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	9	A	Crystal or oscillator input clock: MII mode, RMII master mode: 25-MHz ±50 ppm-tolerance crystal or oscillator clock. RMII slave mode: 50-MHz ±50 ppm-tolerance CMOS-level oscillator clock.
RBIAS	10	A	RBIAS (Bias resistor) value 6.49 kΩ with 1% precision connected to ground.
MDIO	11	Reset: I, PU Active: I/O, PU	Management data I/O: Bi-directional management data signal that may be sourced by the management station or the PHY. This pin has internal pullup resistor of 10 kΩ. An external pullup resistor can be added if needed.
MDC	12	Reset: I, PD Active: I, PD	Management data clock: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz. There is no minimum clock rate.
RX_D3	13	Reset: I, PD Active: O Strap7	Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII mode. 2-bits RX_D[1:0] is received in RMII mode.
RX_D2	14	Reset: I, PD Active: O Strap8	
RX_D1	15	Reset: I, PD Active: O Strap9	
RX_D0	16	Reset: I, PD Active: O Strap0	
VDDIO	17	Power	I/O supply voltage: 3.3 V/1.8 V. For decoupling capacitor requirements, refer to Figure 30 section of data sheet.
RX_DV/ CRS_DV	18	Reset: I, PD Active: O Strap10	Receive data valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] in RMII mode. In MII mode, this pin acts as RX_DV. In RMII mode, this pin acts as CRS_DV and combines the RMII Carrier and Receive Data Valid indications. This pin can be configured to RX_DV in RMII mode to enable RMII Repeater Mode.
RX_CLK/ 50MHz_RMII	19	Reset: I, PD Active: O	MII receive clock: MII Receive Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the received data stream. In RMII Master mode, this provides 50-MHz reference clock. In RMII Slave mode, this pin is not used and remains Input, pulldown.
RX_ER	20	Reset: I, PD Active: O Strap6	Receive error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. RX_ER is asserted high for every reception error, including errors during Idle.

(1) I = Input, O = Output, I/O = Input/Ouput, A = Analog, PU or PD = Internal pullup or pulldown: Hardware bootstrap configuration

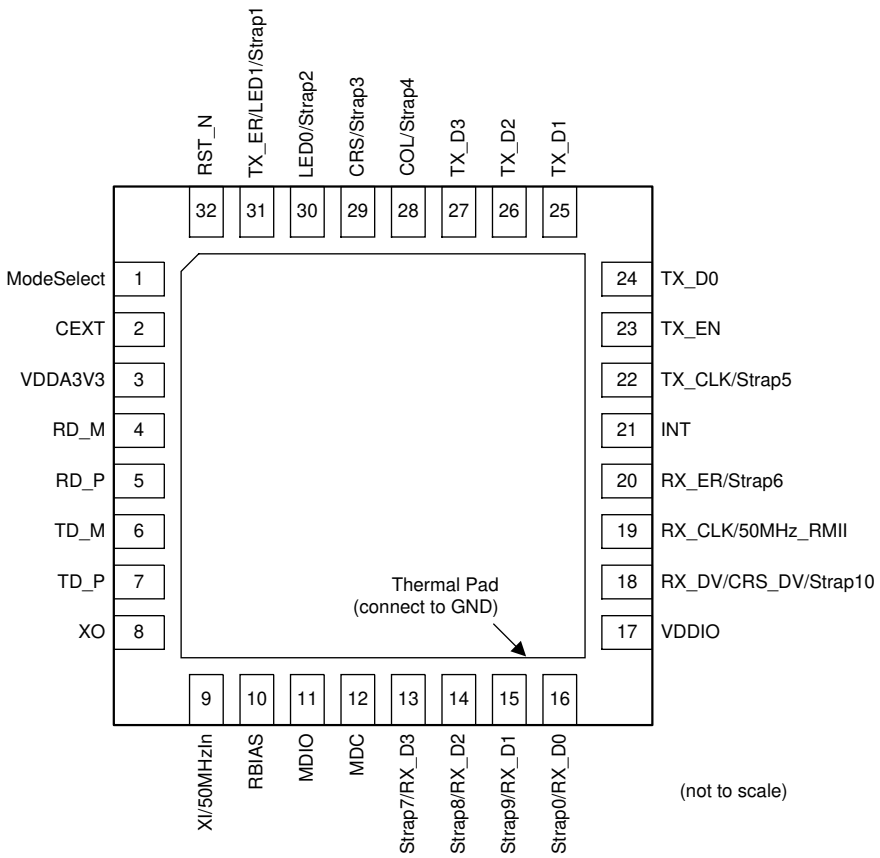
Pin Functions (ENHANCED Mode) (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
PWRDN/INT	21	Reset: I, PU Active: I, PU	Power down (default), interrupt: The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup resistor (9.5 kΩ). Some applications may require an external PU resistor.
TX_CLK	22	Reset: I, PD Active: O Strap5	MII transmit clock: MII transmit clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. Note that in MII mode, this clock has constant phase referenced to the input clock. Unused in RMII Mode.
TX_EN	23	Reset: I, PD Active: I, PD	Transmit enable: TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal.
TX_D0	24	Reset: I, PD Active: I, PD	Transmit data: In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock.
TX_D1	25	Reset: I, PD Active: I, PD	
TX_D2	26	Reset: I, PD Active: I, PD	
TX_D3	27	Reset: I, PD Active: I, PD	
COL/LED2/ GPIO	28	Reset: I, PD Active: O Strap4	Collision detect: In MII mode: For Full-Duplex mode, this pin is always LOW. In Half Duplex mode, this pin is asserted HIGH only when both transmit and receive media are non-idle. This pin can be configured as a second additional LED driver (LED2) or general purpose I/O (GPIO) through register configurations. In RMII mode, this pin acts as LED2 by default.
CRS/LED3	29	Reset: I, PD Active: O Strap3	Carrier sense: In MII mode this pin is asserted high when the receive or transmit medium is non-idle. Carrier sense and receive data valid. This pin can be configured as third LED (LED3) through register configuration. In RMII mode, it is configured as LED3 by default.
LED0	30	Reset: I, PD Active: O Strap2	LED0: This LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active.
CLKOUT/ LED1	31	Reset: I, PD Active: O Strap1	This pin provides 25-MHz reference clock from XI as default to clock. The output is not affected by Resets allowing Application to reset PHY without impacting other system getting impacted. The output clock switches off only by IEEE Power Down. The pin can be configured to act as LED1 using strap or register configuration. The LED is ON when link is 100 M. LED remains OFF if Link is 10 M or no Link.
RST_N	32	Reset: I, PU Active: I, PU	Reset low: RST_N pin is an active low reset input. Asserting this pin low for at least 25 μs forces a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.

7 Pin Configuration and Functions (BASIC Mode)

The BASIC mode is one of two modes that the DP83826 can be configured in at start-up. This mode allows the DP83826 to support all the standard Ethernet applications and matches a common pinout configuration used in many of today's applications. To configure the DP83826 to BASIC mode, ModeSelect (pin 1) should be shorted to GND.

RHB Package
32-Pin QFN
(Top View)



Pin Functions (BASIC Mode)

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
ModeSelect	1	Reset: I, PU Active: I, PU	This pin selects the operating mode: BASIC mode or ENHANCED mode. This pin shall be shorted to GND to configure DP83826 in BASIC mode. For ENHANCED mode, this pin shall be left NC or pulled-up with a resistor to VDDIO.
CEXT	2	A	External capacitor: Connect the CEXT pin through a 2-nF capacitor to GND.
VDDA3V3	3	Power	Input analog power supply pin: This pin shall be connected with 3.3 V. For decoupling capacitor requirements, refer to section of datasheet.
RD_M	4	A	Differential receive input (PMD): These differential inputs are automatically configured to accept either 10BASE-Te or 100BASE-TX specific signaling mode.
RD_P	5	A	
TD_M	6	A	Differential transmit output (PMD): These differential outputs are configured to either 10BASE-Te or 100BASE-TX signaling mode based on the configuration chosen for the PHY.
TD_P	7	A	
XO	8	A	Crystal output: reference clock output. XO pin is used for crystal only. Leave this pin floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	9	A	Crystal or oscillator input clock: MII mode or RMII master mode: 25-MHz ±50 ppm-tolerance crystal or oscillator clock. RMII slave mode: 50-MHz ±50 ppm-tolerance CMOS-level oscillator clock.
RBIAS	10	A	Bias resistance: R_{BIAS} value 6.49 kΩ 1% precision connected to ground.
MDIO	11	Reset: I, PU Active: I/O, PU	Management data I/O: Bi-directional management data signal that may be sourced by the management station or the PHY. This pin has internal pullup resistor of 10 kΩ. An external pullup resistor can be added if needed.
MDC	12	Reset: I, PD Active: I, PD	Management data clock: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz. There is no minimum clock rate.
RX_D3	13	Reset: I, PD Active: O Strap7	Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII mode. 2-bits RX_D[1:0] is received in RMII mode.
RX_D2	14	Reset: I, PD Active: O Strap8	
RX_D1	15	Reset: I, PD Active: O Strap9	
RX_D0	16	Reset: I, PD Active: O Strap0	
VDDIO	17	Power	I/O supply voltage: 3.3 V or 1.8 V. For decoupling capacitor requirements, refer to section of datasheet.
RX_DV/ CRS_DV	18	Reset: I, PD Active: O Strap10	Receive data valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] in RMII mode. In MII mode, this pin acts as RX_DV. In RMII mode, this pin acts as CRS_DV and combines the RMII carrier and receive data valid indications.
RX_CLK/ 50MHz_RMII	19	Reset: I, PD Active: O	MII receive clock: MII receive clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the received data stream. In RMII master mode, this provides 50-MHz reference clock. In RMII slave mode, this pin is not used and remains Input/PD.
RX_ER	20	Reset: I, PD Active: O Strap6	Receive Error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. RX_ER is asserted high for every reception error, including errors during Idle.

(1) I = Input, O = Output, I/O = Input/Ouput, A = Analog, PU or PD = Internal pullup or pulldown: Hardware bootstrap configuration

Pin Functions (BASIC Mode) (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
INT	21	Reset: I, PU; Active: I, PU	Interrupt: The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup resistor (9.5 kΩ). Some applications may require an external PU resistor.
TX_CLK	22	Reset: I, PD Active: O Strap5	MII transmit clock: MII Transmit Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. Note that in MII mode, this clock has constant phase referenced to the reference clock. Applications requiring such constant phase may use this feature. Unused in RMII Mode.
TX_EN	23	Reset: I, PD Active: I, PD	Transmit enable: TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal.
TX_D0	24	Reset: I, PD Active: I, PD	Transmit data: In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock.
TX_D1	25	Reset: I, PD Active: I, PD	
TX_D2	26	Reset: I, PD Active: I, PD	
TX_D3	27	Reset: I, PD Active: I, PD	
COL	28	Reset: I, PD Active: O Strap4	Collision detect: In MII mode: For Full-Duplex mode, this pin is always LOW. In Half Duplex mode, this pin is asserted HIGH only when both transmit and receive media are non-idle. In RMII mode, this pin is not used.
CRS	29	Reset: I, PD Active: O Strap3	Carrier sense: In MII mode this pin is asserted high when the receive or transmit medium is non-idle. carrier sense or receive data valid. In RMII mode, this pin is not used.
LED0	30	Reset: I, PD Active: O Strap2	LED0: This LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active.
TX_ER/LED1	31	Reset: I, PD Active: O Strap1	Transmit errors: The pin acts as TX_ER as default. This pin can be configured to LED1 thru register configuration. The LED is ON when link is 100 M. LED remains OFF if the Link is 10 M, or there is no Link.
RST_N	32	Reset: I, PU Active: I, PU	Reset low: RST_N pin is an active low reset input. Asserting this pin low for at least 25 μs forces a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Analog supply voltage	VDDA3V3	–0.3	4	V
IO supply voltage	VDDIO3V3	–0.3	4	V
IO supply voltage	VDDIO1V8	–0.3	2.1	V
Storage Temperature	Tstg	–65	150	°C
MDI pins		-0.6	4	V
MAC interface pins		-0.3	4	V
MDIO, MDC interface pins		-0.3	4	V
XI		-0.3	4	V
Reset		-0.3	4	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
ESD (HBM)(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) MDI (Media Dependent Interface) pins	+/- 5	kV
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) All pins except MDI	+/- 2	kV
ESD (CDM)(2)	Charged device model (CDM) per JEDEC specification JESD22-C101, all pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500-V HBM is possible with the necessary precautions. Pins listed as ±5 kV and/or ± 4 kV may actually have higherperformance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	VDDA3V3	3	3.3	3.6	V
IO supply voltage	VDDIO3V3	3	3.3	3.6	V
	VDDIO1V8	1.62	1.8	1.98	V
Operating Free Air Temperature (DP83826E)	Ta	–40	25	105	C
Operating Free Air Temperature (DP83826I)	Ta	–40	25	85	C
VDDIO: 1.8v	TX_EN, TX_D0, TX_D1, TX_D2, TX_D3, TX_CLK, RX_D0, RX_D1, RX_D2, RX_D3 RX_DV, RX_ER, MDIO, MDC, COL/LED2, CRS, CLKOUT/LED1, INT/PWDN, RESET	1.62	1.8	1.98	V
	XI Osclliator Input	1.62	1.8	1.98	V
	LED0	1.62	1.8	1.98	V
VDDIO: 3.3v	TX_EN, TX_D0, TX_D1, TX_D2, TX_D3, TX_CLK, RX_D0, RX_D1, RX_D2, RX_D3 RX_DV, RX_ER, MDIO, MDC, COL/LED2, CRS, CLKOUT/LED1, INT/PWDN, RESET	3.0	3.3	3.6	V
	XI Osclliator Input	3.0	3.3	3.6	V
	LED0	3.0	3.3	3.6	V

8.4 Thermal Information

THERMAL METRIC(1)			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	31.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.1	°C/W
Y_{JT}	Junction-to-top characterization parameter	31.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx Conformance (100BaseTx)						
	Differential Output Voltage		950		1050	mV
IEEE Tx Conformance (10BaseTe)						
	Output Differential Voltage (2)		1.54	1.75	1.96	V
Power consumption Baseline (Active mode, 50% Traffic, Packet Size : 1518, Random Content, 150 meter Cable)						
I(VDDA3V3=3V3)	MII (100BaseTx)			45	53	mA
	MII (10BaseTe)			35	46	mA
	RMII Master (100BaseTx)			45	53	mA
	RMII Master (10BaseTe)			35	46	mA
	RMII Slave (100BaseTx)			45	53	mA
	RMII Slave (10BaseTe)			35	46	mA
I(VDDIO=3V3)	MII (100BaseTx)			8	14	mA
	MII (10BaseTe)			5	12	mA
	RMII Master (100BaseTx)			9	14	mA
	RMII Master (10BaseTe)			9	12	mA
	RMII Slave (100BaseTx)			7	8.5	mA
	RMII Slave (10BaseTe)			5	6	mA
I(VDDIO=1V8)	MII (100BaseTx)			5	7	mA
	MII (10BaseTe)			3	6	mA
	RMII Master (100BaseTx)			5	7	mA
	RMII Master (10BaseTe)			5	6	mA
	RMII Slave (100BaseTx)			3	6	mA
	RMII Slave (10BaseTe)			2	3	mA
Power consumption (Active mode worst case, 100% Traffic, Packet Size : 1518, Random Content, 150 meter Cable)						
I(VDDA3V3=3V3)	MII (100BaseTx)			44	55	mA
	MII (10BaseTe)			35	48	mA
	RMII Master (100BaseTx)			44	55	mA
	RMII Master (10BaseTe)			35	48	mA
	RMII Slave (100BaseTx)			44	55	mA
	RMII Slave (10BaseTe)			35	48	mA
I(VDDIO=3V3)	MII (100BaseTx)			10	15	mA
	MII (10BaseTe)			5	12	mA
	RMII Master (100BaseTx)			11	15	mA
	RMII Master (10BaseTe)			9	12	mA
	RMII Slave (100BaseTx)			8	12	mA
	RMII Slave (10BaseTe)			5	10	mA
I(VDDIO=1V8)	MII (100BaseTx)			6	9	mA
	MII (10BaseTe)			2	6	mA

(1) Ensured by production test, characterization or design
(2) Requires register 0x030E to program to 0x4A40

Electrical Characteristics (continued)

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	RMII Master (100BaseTx)			6	9	mA
	RMII Master (10BaseTe)			5	7	mA
	RMII Slave (100BaseTx)			4	8	mA
	RMII Slave (10BaseTe)			2	6	mA
Power Consumption (Low power modes)						
	IEEE Power Down				11	mA
	Active Sleep				18	mA
	RESET				12.5	mA
I(VDDIO =3V3)	IEEE Power Down				10.5	mA
I(VDDIO =3V3)	Active Sleep				10.5	mA
I(VDDIO =3V3)	RESET				10.5	mA
I(VDDIO =1V8)	IEEE Power Down				5.5	mA
I(VDDIO =1V8)	Active Sleep				5.5	mA
I(VDDIO =1V8)	RESET				5.5	mA
Bootstrap DC Characteristics (2 Level)						
V_{IH_3v3}	High Level Bootstrap Threshold : 3V3		1.3			V
V_{IL_3v3}	Low Level Bootstrap Threshold : 3V3				0.6	V
V_{IH_1v8}	High Level Bootstrap Threshold:1V8		1.3			V
V_{IL_1v8}	Low Level Bootstrap Threshold :1V8				0.6	V
Crystal oscillator						
	Load Capacitance			15	30	pF
IO						
3V3	High Level Input Voltage	VDDIO = 3.3V ±10%	1.7			V
	Low Level Input Voltage	VDDIO = 3.3V ±10%			0.8	V
	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±10%	2.4			V
	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±10%			0.8	V
1V8	High Level Input Voltage	VDDIO = 1.8V ±10%	0.65*VDDIO			V
	Low Level Input Voltage	VDDIO = 1.8V ±10%			0.35*VDDIO	V
	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±10%	VDDIO-0.45			V
	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±10%			0.45	V
	Iih (VIN=VCC)	T_A = -40℃ to 85℃, VIN=VDDIO			15	uA
	Iih (VIN=VCC)	T_A = -40℃ to 105℃, VIN=VDDIO			25	uA
	Iil (VIN=GND)	T_A = -40℃ to 85℃, VIN=GND			15	uA
	Iil (VIN=GND)	T_A = -40℃ to 105℃, VIN=GND			25	uA
	Iozh	Tri-state Output High Current (-40 to 85C)	-15		15	uA
	Iozh	Tri-state Output High Current (-40 to 105C)	-25		25	uA
	Iozl	Tri-state Output Low Current (-40 to 85C)	-15		15	uA

Electrical Characteristics (continued)

Over operating free-air temperature range with VDDA3V3 = 3V3 (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Iozl	Tri-state Output Low Current (-40 to 105C)	-25		25	uA
	R Pull Down	Internal Pull Down Resistor	7.5	10	12.5	kΩ
	R Pull UP	Internal Pull Up Resistor	7.5	10	12.5	kΩ
C_{IN}	Input Capacitance XI			1		pF
C_{IN}	Input Capacitance INPUT PINS	Input Capacitance XI		5		pF
C_{OUT}	Output Capacitance XO	Input Capacitance INPUT PINS		1		pF
C_{OUT}	Output Capacitance OUTPUT PINS	Output Capacitance XO		5		pF
	XI input osc clock common mode VDDIO 1V8			0.9		V
	XI input osc clock common mode VDDIO 3V3			1.65		V
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK		50		Ω

8.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
Power Up Timing					
T1	Voltage Ramp Duration (0% to 100% VDDIO)	0.5		50	ms
T2	Supply Sequencing VDDA3V3 followed by VDDIO or VDDIO followed by VDDA3V3	0		200	ms
T3	Voltage Ramp Duration (0% to 100% of VDDA3V3)	0.5		50	ms
T4	POR release time / Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access			50	ms
T5	Powerup to FLP		1500		ms
	Pedestal Voltage on VDDA3V3, VDDIO before Power Ramp			0.3	V
Reset Timing					
T1	RESET PULSE Width: Miminum Reset pulse width to be able to reset (w/o debouncing caps)	25			us
T2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access			2	ms
T3	Reset to FLP		1500		ms
	Reset to 100M signaling (strapped mode)		0.5		ms
	Reset to RMII Master clock		0.2		ms
Fast Link Pulse Timing					
T1	Clock Pulse to Clock Pulse Period		125		µs
T2	Clock Plse to Data Pulse Period		62		µs
T3	Clock/Data Pulse Width		114		ns
T4	FLP Burst to FLP Burst Period		16		ms
T5	FLP Burst Width		2		ms
Link Up Timing					
	Fast Link Drop enabled using straps , 150 meter cable			10	us
	Fast Link Drop Time using Mode 1 (Signal/Energy Loss indication)			10	us
	Fast Link Drop Time using Mode 2 (Low SNR Threshold)			10	us
	Fast Link Drop Time using Mode 3 (MLT3 Error count)(2)			10	us
	Fast Link Drop Time using Mode 4 (RX Error count)			10	us
	Fast Link Drop Time using Mode 5 (Descrambler link drop)(2)			10	us
100M MII Receive Timing					
T1	RX_CLK High / Low Time	16	20	24	ns
T2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	10		30	ns
100M MII Transmit Timing					
T1	TX_CLK High / Low Time	16	20	24	ns
T2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	10			ns
T3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
10M MII Receive Timing					
T1	RX_CLK High / Low Time(3)	160	200	240	ns
T2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising(3)	100		300	ns
10M MII Transmit Timing					
T1	TX_CLK High / Low Time	190	200	210	ns
T2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	25			ns
T3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
100M RMII Master Timing					

(1) Ensured by Design, Production or Characterisation test
(2) MLT3 and Descrambler fast link drop requires additional configuration. Refer to features section
(3) While receiving first nibble of data, PHY switches source from local to recovered clock. It causes stretching of RX_CLK and RX_CLK to RX_DV delay

Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
	RMII Master Clock Period		20		ns
	RMII Master Clock Duty Cycle	35		65	%
100M RMII Timing					
T2	TX_D[1:0], TX_ER, TX_EN Setup to Reference Clock rising	4			ns
T3	TX_D[1:0], TX_ER, TX_EN Hold from Reference Clock rising	2			ns
T4	RX_D[1:0], RX_ER, CRS_DV Delay from Reference Clock rising	4		14	ns
SMI Timing					
T1	MDC to MDIO (Output) Delay Time	0		13	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	24	MHz
Output Clock Timing (50M RMII Master Clock)					
	Frequency (PPM)			50	ppm
	Jitter (Long Term 500 Cyles)			450	ps
	Rise / Fall Time			5	ns
	Duty Cycle	40		60	%
Output Clock Timing (25M Clockout)					
	Frequency (PPM)			50	ppm
	Duty Cycle	35		65	%
	Rise time			4000	ps
	Fall Time			5000	ps
	Jitter (Long Term: 500 Cycles)			300	ps
	Jitter (Short Term)			250	ps
	Frequency		25		MHz
25MHz Input Clock Tolerance					
	Frequency Tolerance	-100		100	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (RMS)			4000	ps
	Jitter Tolerance (Long Term: 100,000 Cycles)				ps
	Input phase noise at 1 kHz			-98	dBc/Hz
	Input phase noise at 10 kHz			-113	dBc/Hz
	Input phase noise at 100 kHz			-113	dBc/Hz
	Input phase noise at 1 MHz			-113	dBc/Hz
	Input phase noise at 10 MHz			-113	dBc/Hz
	Duty Cycle	40		60	%
50MHz Input Clock tolerance					
	Frequency Tolerance	-100		100	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (RMS)			4000	ps
	Jitter Tolerance Long Term Jitter derived from Phase Noise (100,000 Cycles)				ps
	Input phase noise at 1 kHz			-87	dBc/Hz
	Input phase noise at 10 kHz			-107	dBc/Hz
	Input phase noise at 100 kHz			-107	dBc/Hz
	Input phase noise at 1 MHz			-107	dBc/Hz
	Input phase noise at 10 MHz			-107	dBc/Hz

Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
	Duty Cycle	40		60	%
Latency Timing					
	MII 100M Tx (MII to MDI): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	38		40	ns
	MII 100 Rx (MDI to MII): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_DV, FAST RX_DV enabled, 100 meter Cable	166		170	ns
	MII 10M Tx (MII to MDI): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI			540	ns
	RMII Slave 100M Tx (RMII to MDI) :Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	88		96	ns
	RMII Master 100M Tx (RMII to MDI) Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI, FAST RX_DV enabled, 100 meter Cable	88		96	ns
	RMII Slave 10M Tx(RMII to MDI) : Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI			1360	ns
	RMII Master 10M Tx (RMII to MDI)Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI			1360	ns
	MII 10M Rx (MDI to MII): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_DV, FAST RX_DV enabled, 100 meter Cable			1640	ns
	RMII Slave 100M Rx (MDI to RMII) : SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV, FAST RX_DV enabled, 100 meter Cable	268		288	ns
	RMII Master 100M Rx (MDI to RMII): SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV	252		270	ns
	RMII Slave 10M (MDI to RMII) :SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV (10M)	2110		2152	ns
	RMII Master 10M (MDI to RMII) : SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV (10M)	2110		2152	ns
	MII : XI to TXCLK phase difference (across Resets, Power Cycle)		2	4	ns

8.7 Timing Diagrams

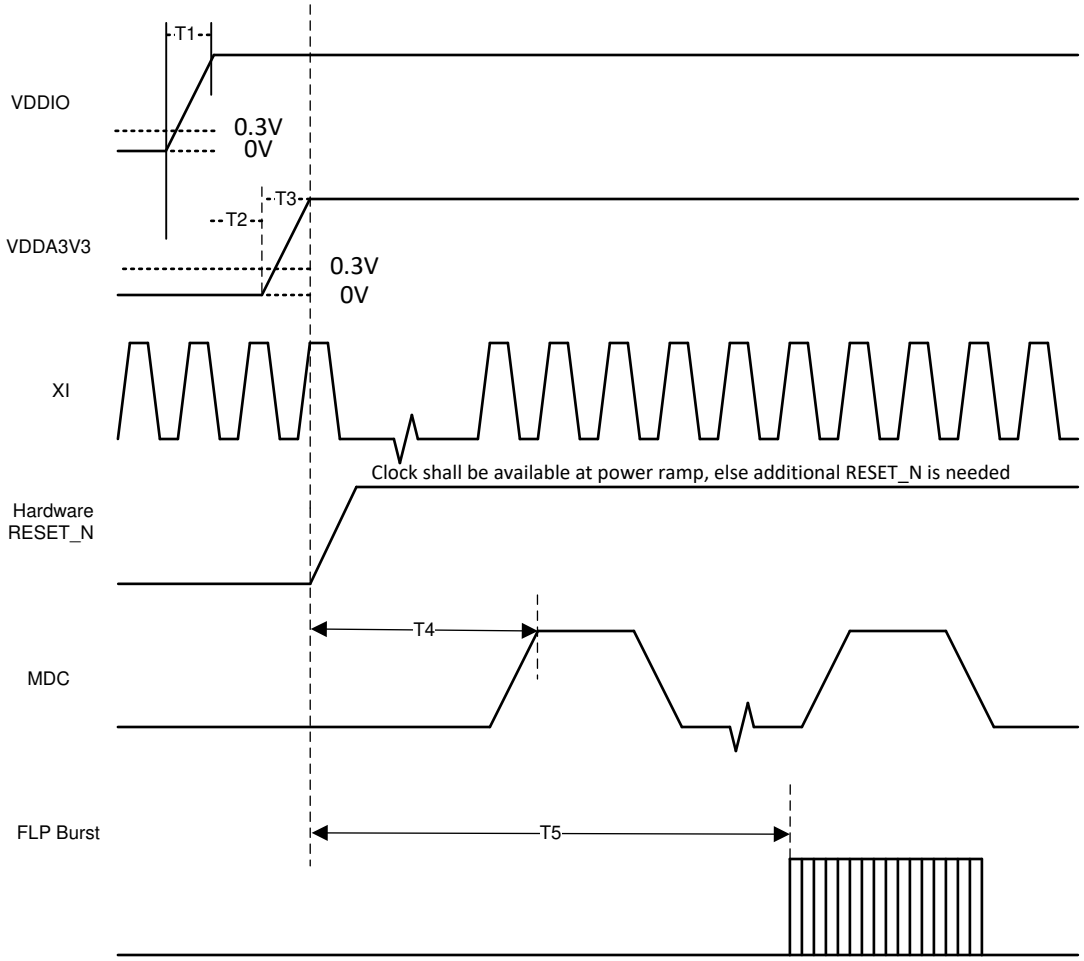


Figure 1. Power-Up Timing (Power Sequencing)

Timing Diagrams (continued)

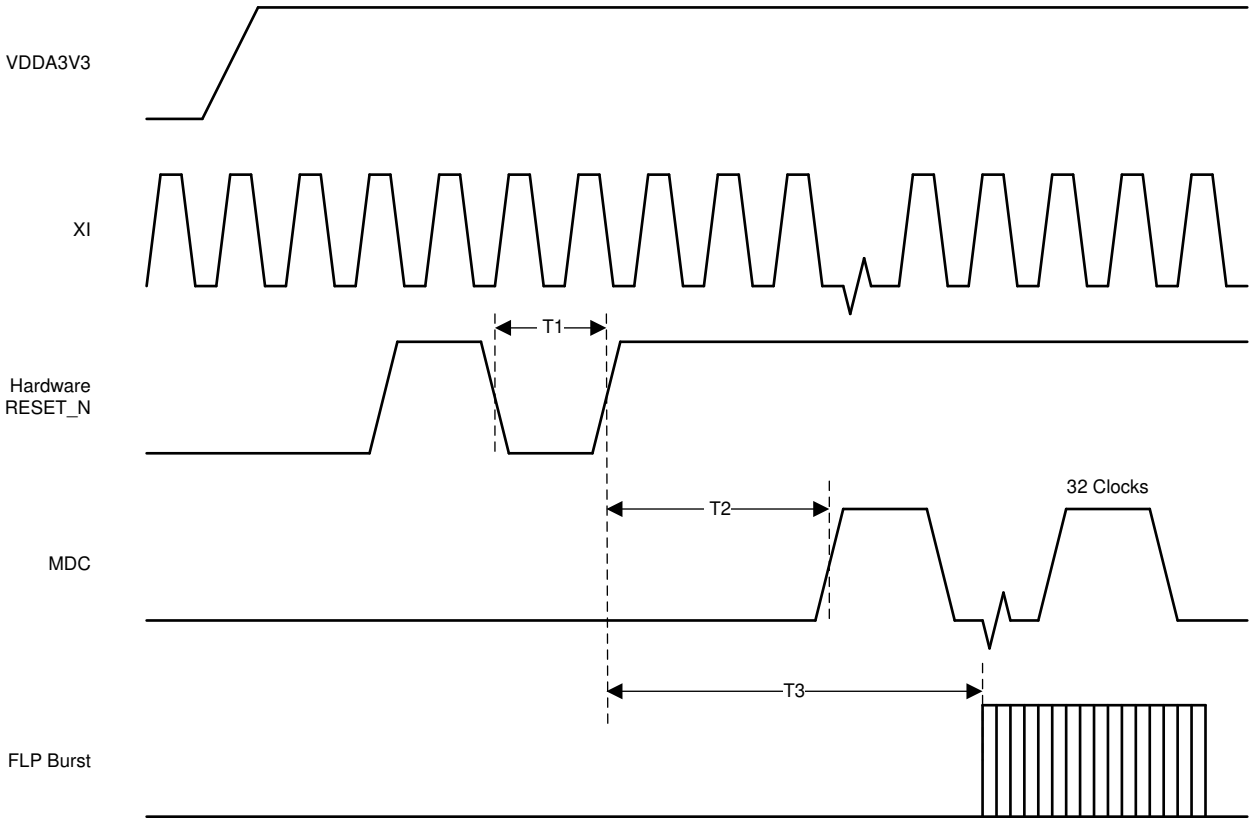


Figure 2. Reset Timing (POR)

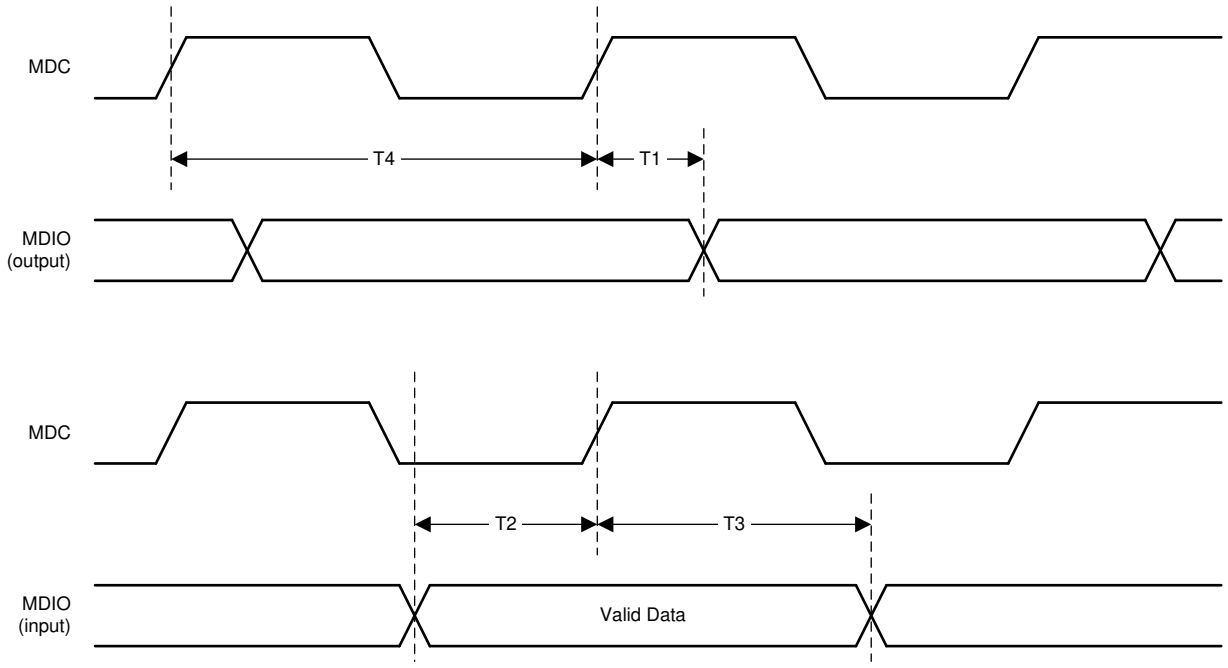


Figure 3. Serial Management Timing

Timing Diagrams (continued)

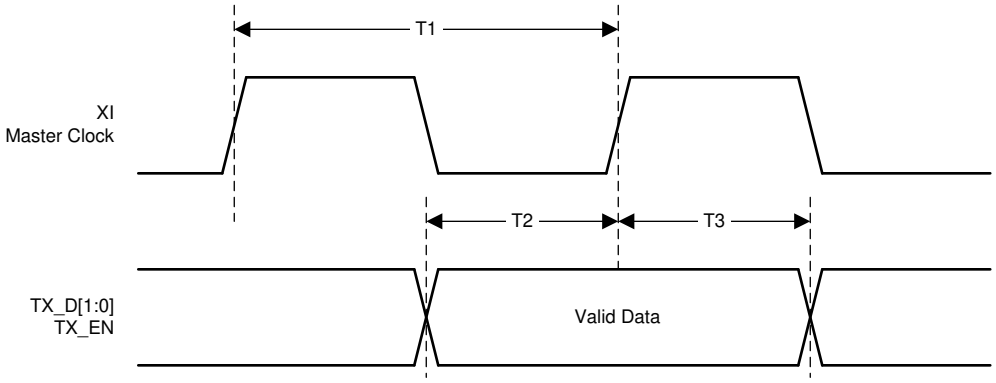


Figure 4. RMII Transmit Timing

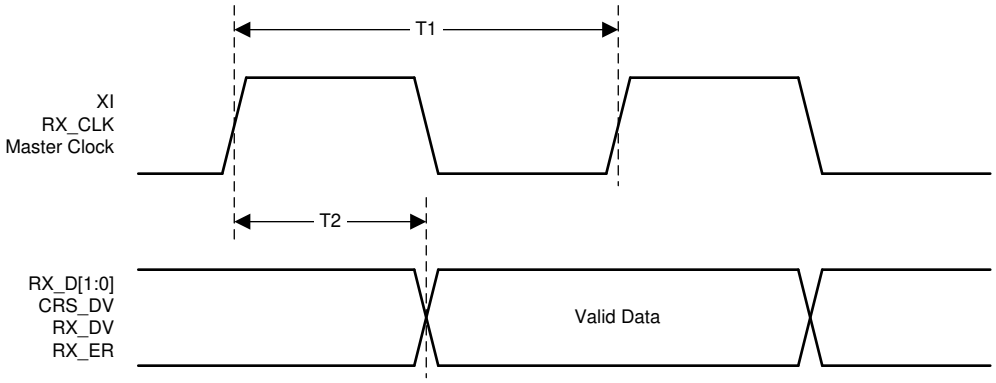


Figure 5. RMII Receive Timing

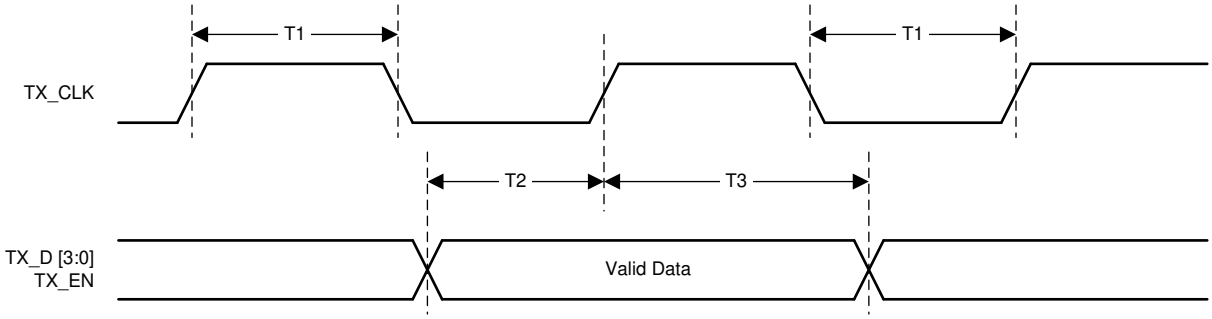


Figure 6. 100-M MII Transmit Timing

Timing Diagrams (continued)

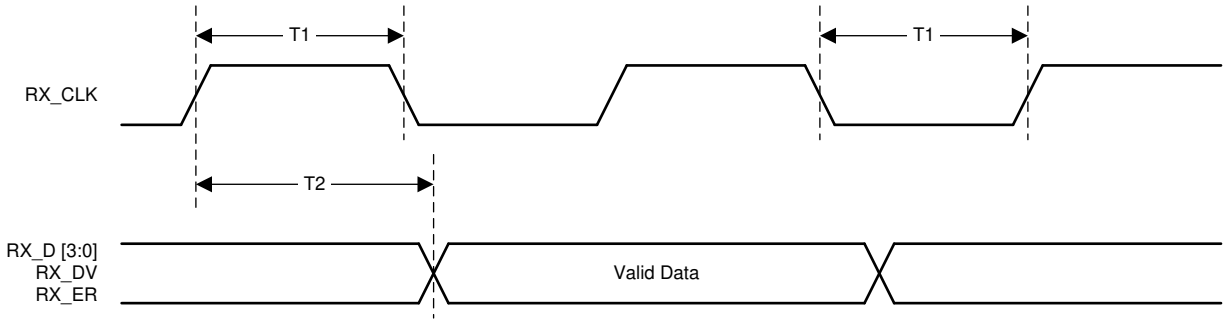


Figure 7. 100-M MII Receive Timing

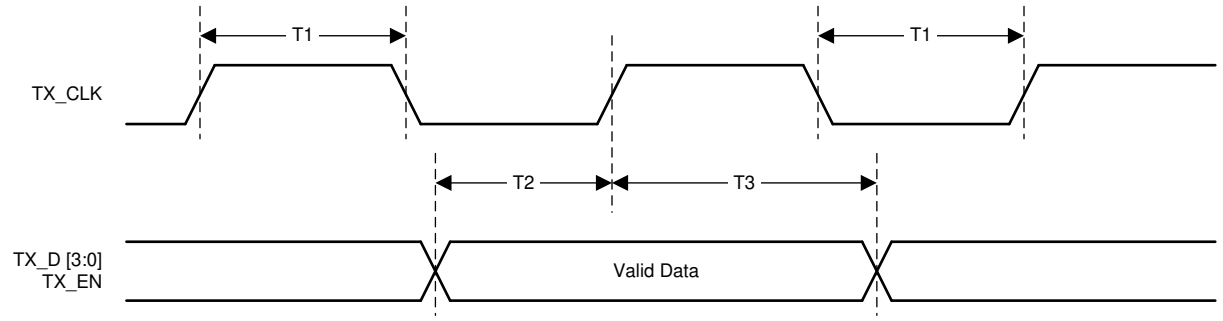


Figure 8. 10-M MII Transmit Timing

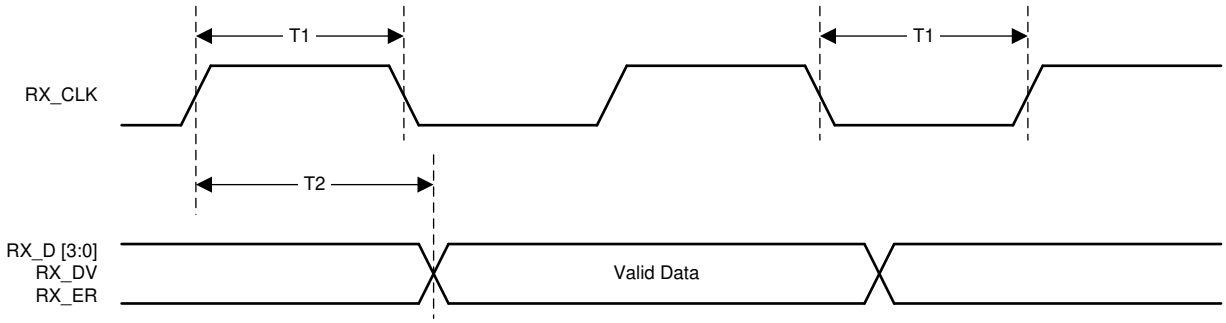


Figure 9. 10-M MII Receive Timing

Timing Diagrams (continued)

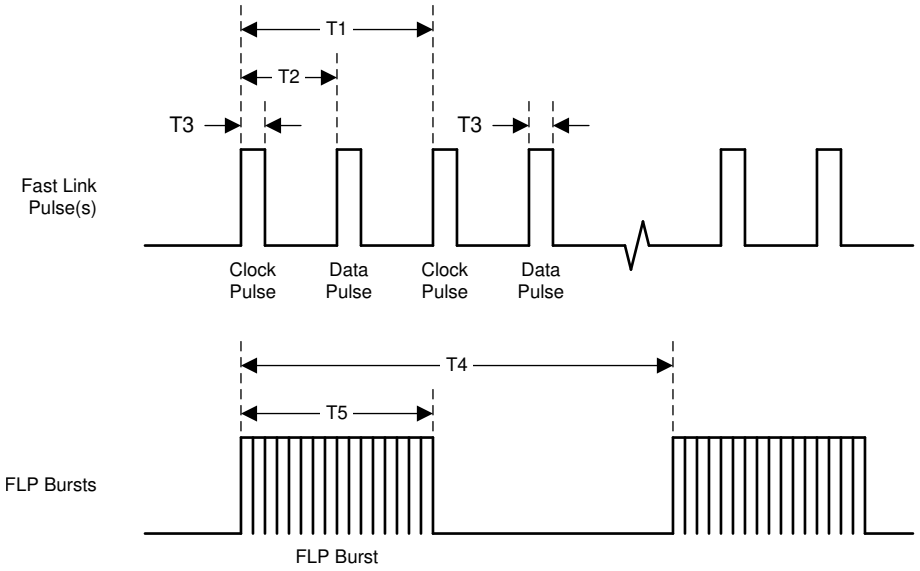


Figure 10. Fast Link Pulse Timing

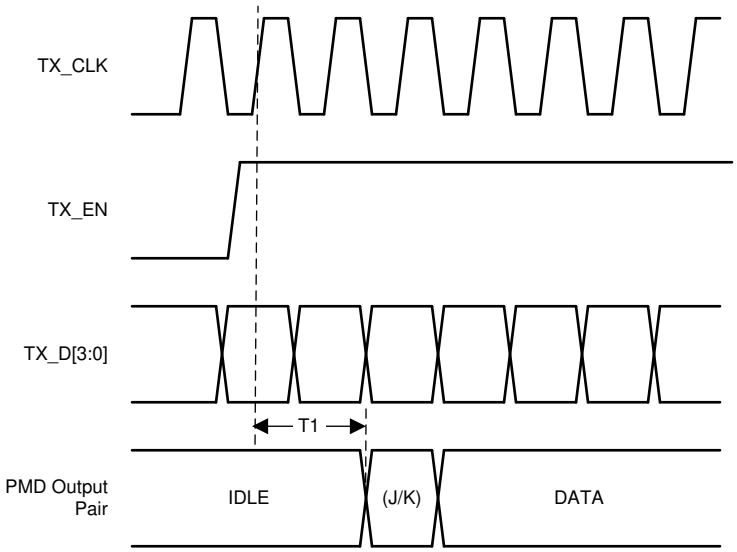


Figure 11. 100BASE-TX Transmit Latency Timing

Timing Diagrams (continued)

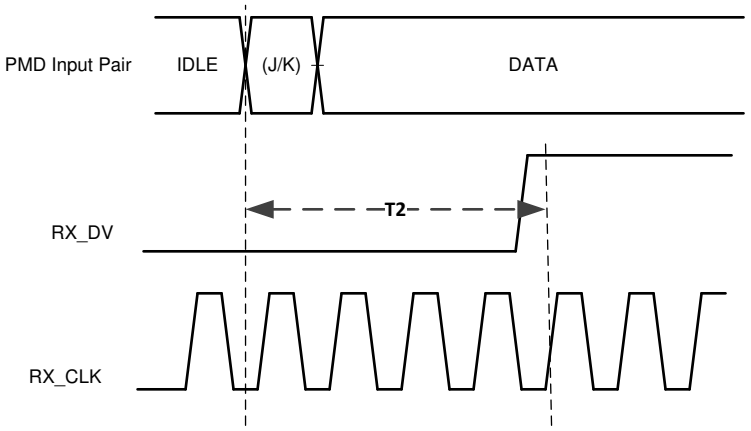


Figure 12. 100BASE-TX Receive Latency Timing

8.8 Typical Characteristics

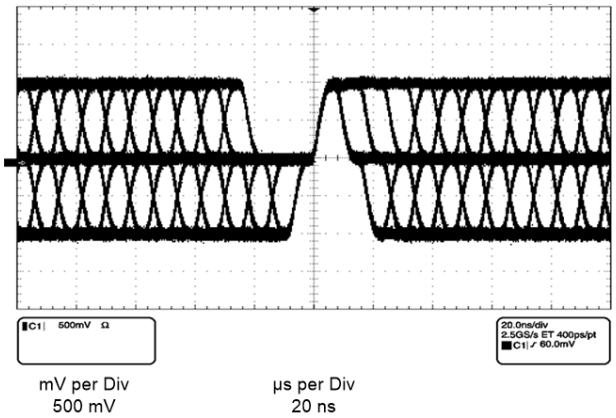


Figure 13. 100BASE-TX PMD Eye Waveform

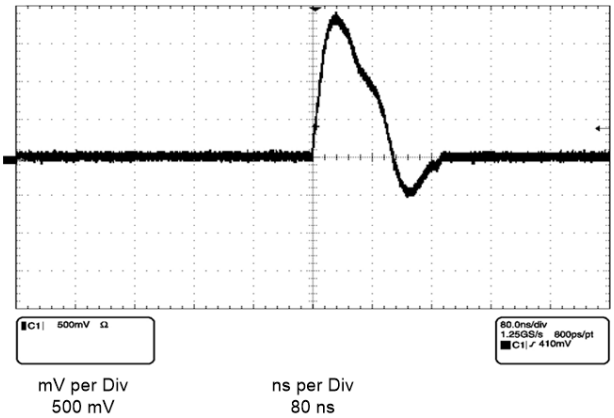


Figure 14. 10BASE-Te Link Pulse Waveform

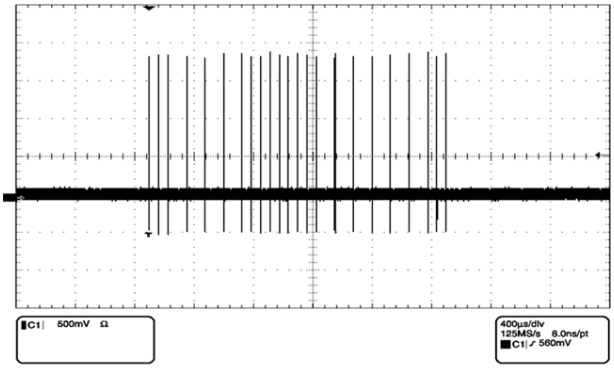


Figure 15. Auto-Negotiation Fast Link Pulses Waveform

9 Detailed Description

9.1 Overview

The DP83826 is a single-port physical layer transceiver compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The DP83826 is designed to meet stringent Industrial fieldbus applications' needs and offers very low latency, deterministic variation in latency (across reset, power cycle), fixed phase between XI and TX_CLK, low power, and configuration using hardware bootstraps to achieve fast link up. The device supports the standard MII and RMII (Master mode and Slave mode) for direct connection to the media access controller (MAC). Its dedicated CLKOUT pin can be used to clock other modules on the system. In addition, the PWRDN pin controls the DP83826 link up from power-on-reset (POR) and helps with design of asynchronous power-up of the DP83826 and host system-on-a-chip (SoC) or field-programmable-gate-array (FPGA) controller.

The device operates from a single 3.3-V power supply and has an integrated LDO to provide voltage rails needed for internal blocks. The device allows I/O voltage interfaces of 3.3 V or 1.8 V, which in turn enables the DP83826 to operate as a single-supply PHY. Automatic supply configuration within the DP83826 allows for any combination of VDDIO supply without the need for additional configuration settings.

The DP83826 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over a CAT5e twisted-pair cable length greater than 150 meters.

DP83826 offers two modes selectable during the power-up sequence using hardware bootstraps.

- BASIC mode
- ENHANCED mode

BASIC mode provides all the features required for standard Ethernet applications, using a common pinout configuration used in many of today's applications. This makes it easy to evaluate and test the product on existing platforms. The integrated MAC and MDI terminations streamline the design of boards when using the DP83826. All the required clock outputs are generated from a single PLL with a 25-MHz external crystal or oscillator input.

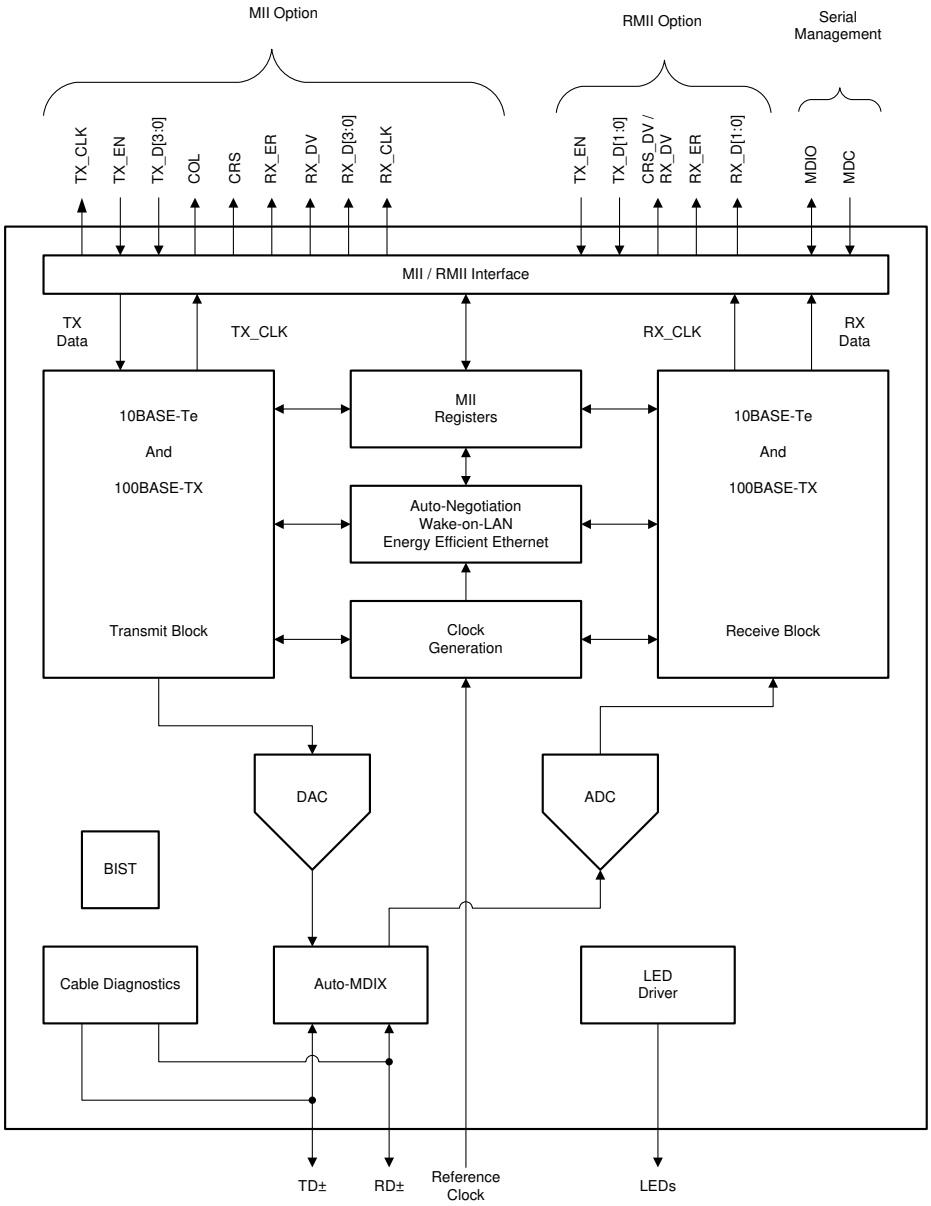
ENHANCED mode includes all the modes of operation described in BASIC Mode, however, the change in pins enable additional features. This makes it easy to use the DP83826 in ENHANCED Mode for Ethernet fieldbus applications in addition to the standard Ethernet applications. The feature includes:

- Dedicated Reference Clock Output: CLKOUT (pin 31) can be used to synchronize the whole system resulting in lower latency (reduced FIFO on MAC). This clock is enabled at POR and remains available across the reset. It also reduces the need for a dedicated clock for other PHYs and the host SoC/FPGA on the board.
- Dedicated HW Strap to use Force Mode, MDI or MDIX for fast link-up from POR and Reset.
- IEEE Power Down Pin: PWRDN (pin 21) helps asynchronous power-up of the DP83826 and host SoC/FPGA control, and can still manage the DP83826 link-up through this dedicated pin.
- PHY address hardware bootstraps on non MAC interface pins to improve Signal Integrity on MII and RMII MAC interface pins.

For pin maps of both modes, refer to section *Pin Configuration and Functions (ENHANCED Mode)*and *Pin Configuration and Functions (BASIC Mode)*.

To configure the hardware bootstraps for both modes, refer to sections *DP83826 Bootstrap Configurations (ENHANCED Mode)* and *DP83826 Strap Configuration (BASIC Mode)*.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Auto-Negotiation (Speed/Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging fast link pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83826 supports 100BASE-TX and 10BASE-Te modes of operation for auto-negotiation. Auto-negotiation ensures that the highest common speed is selected based on the advertised abilities of the link partner and the local device. Auto-negotiation can be enabled or disabled in hardware, using the bootstrap, or by register configuration, using bit[12] in the BASIC mode Control Register (BMCR, address 0x0000). For further details regarding auto-negotiation, refer to Clause 28 of the IEEE 802.3 specification.

Feature Description (continued)

9.3.2 Auto-MDIX Resolution

The DP83826 can determine if a “straight” or “crossover” cable is used to connect to the link partner. It can automatically re-assign to Td (MDI) channel and Rd (MDIX) channel to establish link with the link partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Force Mode.

Auto-MDIX can be enabled or disabled in hardware, using the hardware bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished using register configuration, using bit[14] of the PHYCR or hardware bootstraps in ENHANCED mode.

9.3.3 Wake-on-LAN Packet Detection

Wake-on-LAN (WoL) provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83826 device allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. This device supports WoL Magic Packet™ frame type. When a qualifying WoL frame is received, the device WoL logic circuit generates a user-defined event (either pulses or level change) through the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. The device includes a cycle redundancy check (CRC) gate to prevent invalid packets from triggering a wake-up event. The Wake-on-LAN feature includes:

- Identification of WoL frames in all supported speeds (100BASE-TX and 10BASE-Te)
- Wake-up interrupt generation upon reception of a WoL frame
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames
- Magic Packet technology with SecureOn password protection

9.3.3.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83826 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station’s IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF.

Feature Description (continued)

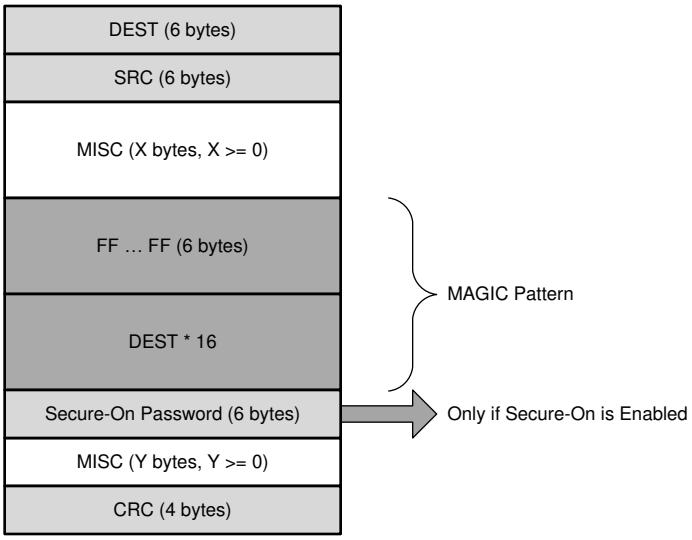


Figure 16. Magic Packet Structure

9.3.3.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a SecureOn password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

9.3.3.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Receiver Status Register (RXFS, address 0x04A1). The Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register #2 (MISR2, address 0x0013).

9.3.4 Low Power Modes

The DP83826 device supports three low power modes. This section discusses the principles behind these low power modes and configuration to enable them.

9.3.4.1 Active Sleep

When the device enters into active sleep mode, all internal circuitry shuts down in the PHY except for the SMI and energy detection circuitry on the TD± and RD± pins. In this mode, the device transmits normal link pulses (NLP) every 1.4 seconds to wake up the link partner. An automatic power-up sequence occurs when a link partner is detected.

The device enables active sleep mode by setting bits[14:12] = 0b110 in the PHY Specific Control Register (PHYSCR, address 0x0011).

9.3.4.2 IEEE Power-Down

IEEE power-down switch disables all PHY circuitry except the SMI and internal clock circuitry.

IEEE power-down switch can be activated by either register access or through the INTR/PWRDN pin when the pin is configured for power-down function.

Feature Description (continued)

To enable IEEE power-down switch through the INTR/PWRDN pin, the pin must be driven LOW to ground.

To enable IEEE power-down switch through the SMI, set bit[11] = 1 in the BASIC mode Control Register (BMCR, address 0x0000).

9.3.4.3 Deep Power Down State

A Deep Power Down state (DPD) disables all PHY circuitry except the SMI. In this mode, the device disables the PHY PLL to further reduce power consumption.

The device uses this sequence to enter DPD state.

1. Enable DPD state (0x0428.2 = 1)
2. Enable IEEE power-down state (pin or 0x0000.11 = 1)

9.3.5 RMII Repeater Mode

The DP83826 device provides the option to enable RMII back-to-back repeater mode functionality to extend cable reach. Two DP83826 devices can be connected in RMII repeater mode without need of any external configuration. It provides a hardware strap to configure the CRS_DV pin of RMII interface to RX_DV pin for back-to-back operation. Figure 17 and Figure 18 show the RMII pin connections that enables the device to operate in repeater mode.

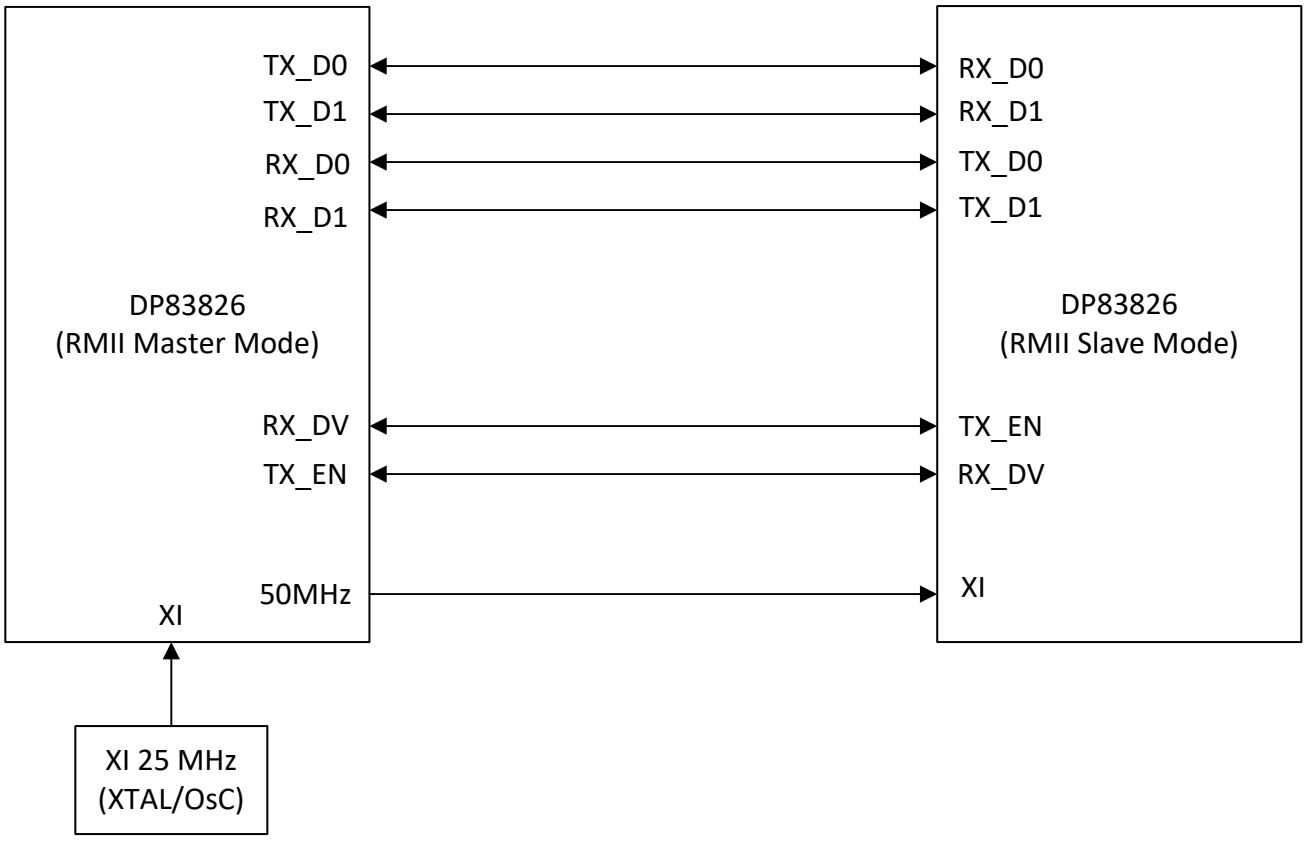


Figure 17. RMII Repeater Mode: Master-Slave

Feature Description (continued)

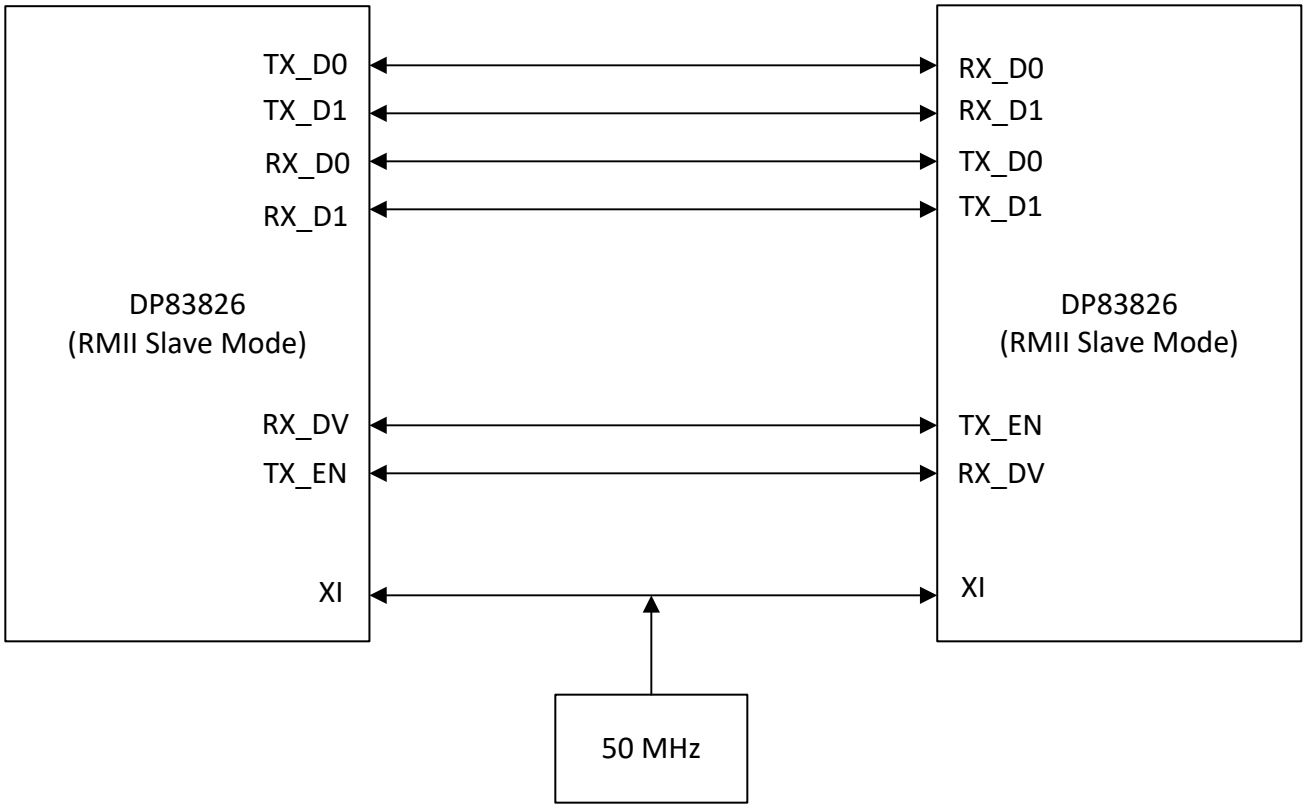


Figure 18. RMII Repeater Mode: Slave-Slave

9.3.6 Clock Output

The device has several clock output configuration options. An external crystal or CMOS-level oscillator provides the stimulus for the internal PHY reference clock. The local reference clock acts as the central source for all clocking within the device.

Clock output options supported by the device include:

- MAC IF clock
- XI clock
- Free-running clock
- Recovered clock

MAC IF clock operates at the same rate as the MAC interface selected. For RMII operation, MAC IF Clock frequency is 50 MHz.

XI clock is a pass-through option, which allows for the XI pin clock to be passed to a GPIO pin. Note that the clock is buffered prior to transmission out of the GPIOs, and output clock amplitude is at the selected VDDIO level.

The Free-running clock is an internally generated 125-MHz free-running clock generated by the PLL. The free-running clock is suitable for asynchronous data transmission applications.

The recovered clock is a 125-MHz recovered clock that is recovered from the connected link partner. The PHY recovers the clock from the data received (transmitted from the link partner).

All clock configuration options are enabled using the LED GPIO configuration registers.

CLKOUT can be disabled by configuring this pin as an input pin via register configuration. To do this set bit[0] = 1 in the PIN_CFG1 Register (Address = 0x459) and then set bit[0] = 1 in the PIN_CFG2 Register (Address = 0x45A).

Feature Description (continued)

9.3.7 Media Independent Interface (MII)

The media-independent interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2002 clause 22.

The MII signals are summarized below:

Table 4. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Line-Status Signals	CRS
	COL
Error Signals	RX_ER

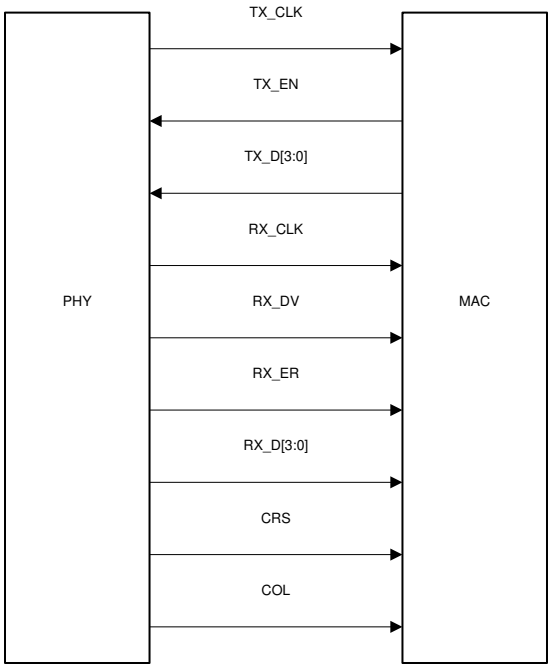


Figure 19. MII Signaling

Additionally, the MII interface includes the carrier sense signal (CRS), as well as a collision detect signal (COL). The CRS signal asserts to indicate the reception or transmission of data. The COL signal asserts as an indication of a collision which can occur during half-duplex mode when both transmit and receive operations occur simultaneously.

9.3.8 Reduced Media Independent Interface (RMII)

The DP83826 incorporates the reduced media-independent interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83826 offers two types of RMII operations: RMII Slave and RMII Master. In RMII Master operation, the DP83826 operates from either a 25-MHz CMOS-level oscillator connected to XI pin, a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referenced from DP83826 can be connected to the MAC. In RMII Slave operation, the DP83826 operates from a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII slave mode, the PHY can operate from a 50-MHz clock provided by the Host MAC

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are 2 bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized below:

Table 5. RMII Signals

FUNCTION	PINS
Receive data lines	TX_D[1:0]
Transmit data lines	RX_D[1:0]
Receive control signal	TX_EN
Transmit control signal	CRS_DV

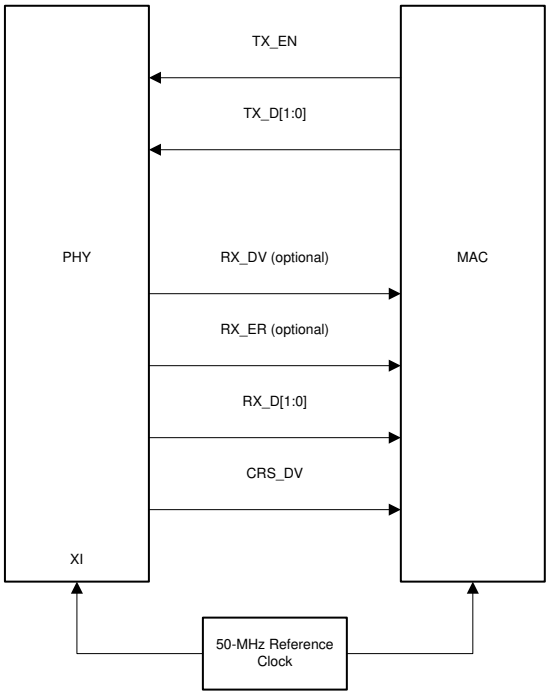


Figure 20. RMII Slave Signaling

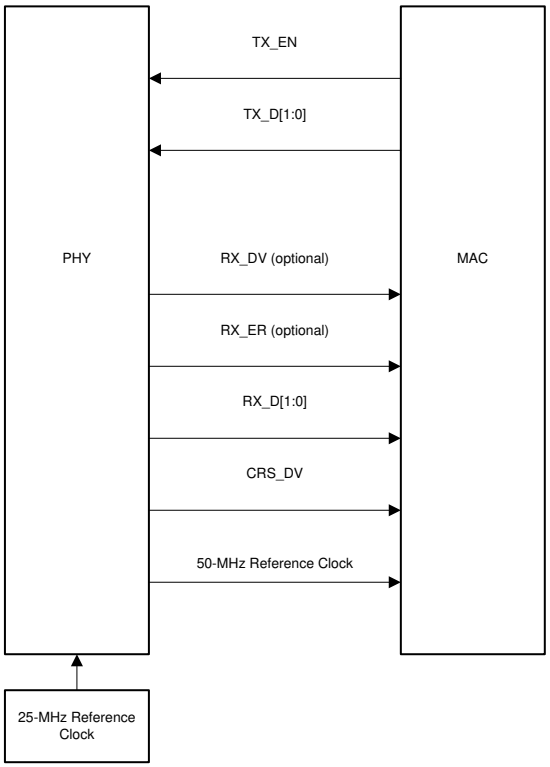


Figure 21. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the 50 MHz-clock in RMII master mode and slave mode. Data on RX_D[1:0] is provided in reference to 50-MHz clock.

In addition, CRX_DV can be configured as RX_DV signal. It allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

9.3.9 Serial Management Interface

The Serial Management Interface provides access to the DP83826 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83826.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ or 1.5 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 8 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83826 latches the Phy_Address[2:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is de-asserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83826 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83826, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 6. SMI Protocol

SMI PROTOCOL	<idle><start><op code><PHY address><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

9.3.9.1 Extended Register Space Access

The DP83826 SMI function supports read and write access to the extended register set using the Register Control Register (REGCR, address 0x000D), the Data Register (ADDAR, address 0x000E), and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah draft for Clause 22 for accessing the extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR and register ADDAR, which are accessed only using the normal MDIO transaction. The SMI function ignores indirect access to these registers.

REGCR is the MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of the ADDAR register to the appropriate MMD.

The DP83826 supports three MMD device addresses:

1. The Vendor-Specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00011 is used for Energy Efficient Ethernet MMD register accesses. Register names for registers accessible at this device address are preceded by MMD3.
3. DEVAD[4:0] = 00111 is used for Energy Efficient Ethernet MMD registers accesses. Register names for registers accessible at this device address are preceded by MMD7.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111). For register accesses to the MMD3 or MMD7 registers the corresponding device address would be used.

9.3.9.2 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

9.3.9.3 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

9.3.9.4 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

9.3.9.5 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) results in the output of the register set in step 3.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

9.3.9.6 Example Write Operation (No Post Increment)

This example demonstrates a write operation with no post increment. In this example, the MAC impedance is adjusted to 99.25 Ω using the IO MUX GPIO Control Register (IOCTRL, address 0x0461).

1. Write the value 0x001F to register 0x000D.
2. Write the value 0x0461 to register 0x000E (sets desired register to the IOCTRL).
3. Write the value 0x401F to register 0x000D.
4. Write the value 0x0400 to register 0x000E (sets MAC impedance to 99.25 Ω).

9.3.10 100BASE-TX

9.3.10.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125-Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in Table 7 below.

The transmitter section consists of the following functional blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83826 implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

Table 7. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T and R in data fields are mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

9.3.10.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 7 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

9.3.10.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB.

9.3.10.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable. There is no ability to bypass this block within the DP83826. The NRZI data is sent to the 100-Mbps Driver.

9.3.10.1.4 Binary to MLT-3 Converter

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output pair common driver is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD standard compliant transition times (3 ns < T_{RISE} (and T_{FALL}) < 5 ns).

9.3.10.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125-Mbps serial data stream to synchronous to 4-bit data provided to the MII and 2-bit wide data to the RMII.

The receive section consists of the following functional blocks:

- Input and BLW compensation
- Signal detect
- Digital adaptive equalization
- MLT-3 to binary decoder
- Clock recovery module
- NRZI to NRZ decoder
- Descrambler
- Serial-to-parallel data conversion
- Code-group alignment
- 4B/5B decoder
- Link integrity monitor
- Bad SSD detection

9.3.11 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision detection, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

NOTE

When using the DP83826 for 10BASE-Te applications, configure VOD_CFG3 (register address: 0x030E) to 0x4A40.

9.3.11.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50 ns. Finally, the signal must again exceed the original squelch level no earlier than 50 ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

DP83826 supports both IEEE Preamble Mode and Short Preamble Mode. Refer to the 10M_CFG Register (address = 0x2A).

9.3.11.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

9.3.11.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83826 output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100 ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500 ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te Mode.

9.3.11.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair causes polarity errors. Wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because it uses MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

9.3.12 Loopback Modes

There are several loopback options within the DP83826 that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83826 may be configured to any one of the Near-end Loopback modes or to the far-end (reverse) loopback mode. MII loopback is configured using the BASIC mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

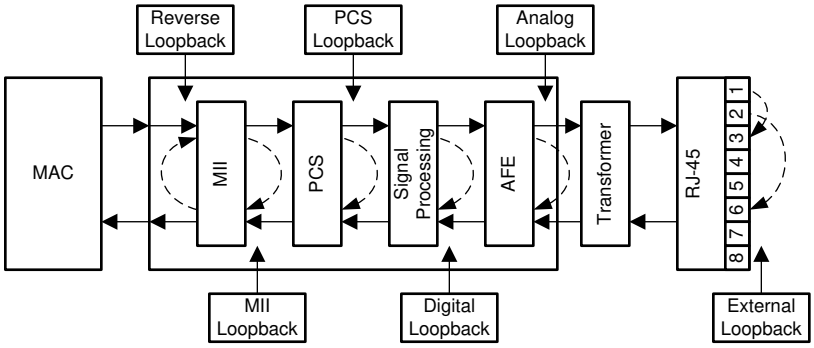


Figure 22. Loopback Test Modes

9.3.12.1 Near-end Loopback

Near-end Loopback provides the ability to loop the transmitted data back to the receiver via the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits[3:0] in the BISCR register. Auto-Negotiation should be disabled before selecting the Near-end Loopback modes. This constraint does not apply for External Loopback Mode.

9.3.12.2 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83826 to the RX pins where it can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR and bit[2] in BISCR.

9.3.12.3 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

9.3.12.4 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuitry.

Digital Loopback is requires following configuration:

- 0x0000 = 0x2100 // Disable Auto-Neg
- 0x0016 = 0x0104 // Digital Loopback
- 0x0122 = 0x2000 /
- 0x0123 = 0x2000
- 0x0130 = 0x47FF
- 0x001F = 0x4000 // Soft Reset

9.3.12.5 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end.

Analog Loopback is enabled by setting bit[3] in the BISCR.

9.3.12.6 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the Link Partner. While in reverse loopback mode, all data signals that come from the MAC are ignored.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

9.3.13 BIST Configurations

The DP83826 incorporates an internal PRBS built-in self-test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and inter-packet gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST packet length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This setting locks the current value of the BIST errors for reading. Setting bit[15] also clears the BIST Error Counter.

9.3.14 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies and connectors deployed results in the need to non-intrusively identify and report cable faults. The DP83826 offers time domain reflectometry (TDR) capabilities in its Cable Diagnostic tool kit.

9.3.14.1 Time Domain Reflectometry (TDR)

The DP83826 uses TDR to determine the quality of the cables, connectors and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts and any other discontinuities along the cable.

The DP83826 transmits a test pulse of known amplitude (1 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, connector and from the end of the cable itself. After the pulse transmission, the DP83826 measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1-m accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains “quiet” (for example, in power down mode)
- TDR could be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Regsiter #1 (CR1, address 0x0009). When a link-drops, TDR automatically executes and stores the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170). Refer to the application report *Solving Cable Faults Challenges with TI Ethernet PHYs* for details.

9.3.14.2 Fast Link-Drop Functionality

The DP83826 includes advanced link-drop capabilities that support various real-time applications. The link-drop mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83826 supports an enhanced link-drop mechanism, also called fast link-drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference. FLD can be enabled in software using register configuration. FLD can be configured using the Control Register #3 (CR3, address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When link-drop occurs, indication of a particular fault condition can be read from the Fast Link Drop Status Register (FLDS, address 0x000F).

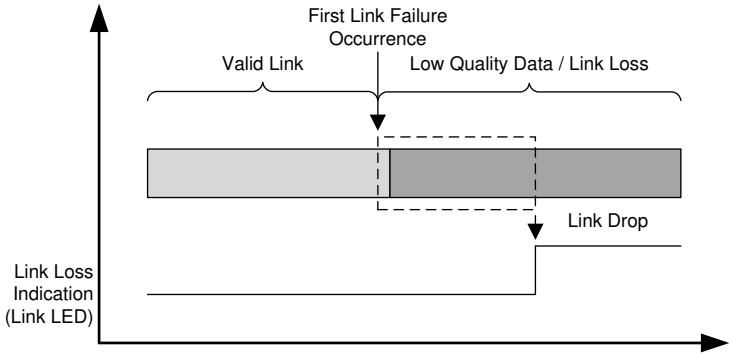


Figure 23. Fast Link-Drop

Fast link-drop criteria include:

- RX error count - when a predefined number of 32 RX_ERs occur in a 10-µs window, the link is dropped.
- MLT3 error count - when a predefined number of 20 MLT3 errors occur in a 10-µs window, the link is dropped. To use the MLT3 error based FLD, please configure register Fast Link Drop Config Register 1 (FLDCFG1, address 0x0117) to 0x0417.
- Low SNR threshold - when a predefined number of 20 threshold crossings occur in a 10-µs window, the link is dropped.
- Signal/energy loss - when the energy detector indicates energy loss, the link is dropped.
- Descrambler link loss - when the Descrambler loses lock, the link is dropped. To use the Descrambler link loss based FLD, please configure bits[5:0] of Fast Link Drop Config Register 2 (FLDCFG2, address 0x0131) to 0x08.

The fast link-drop functionality allows the use of each of these options separately or in any combination.

9.3.15 LED and GPIO Configuration

The DP83826 offers flexible LED and GPIO pins which can be set for various functions using register configuration. Refer to Figure 24, for details on LED and GPIO configuration.

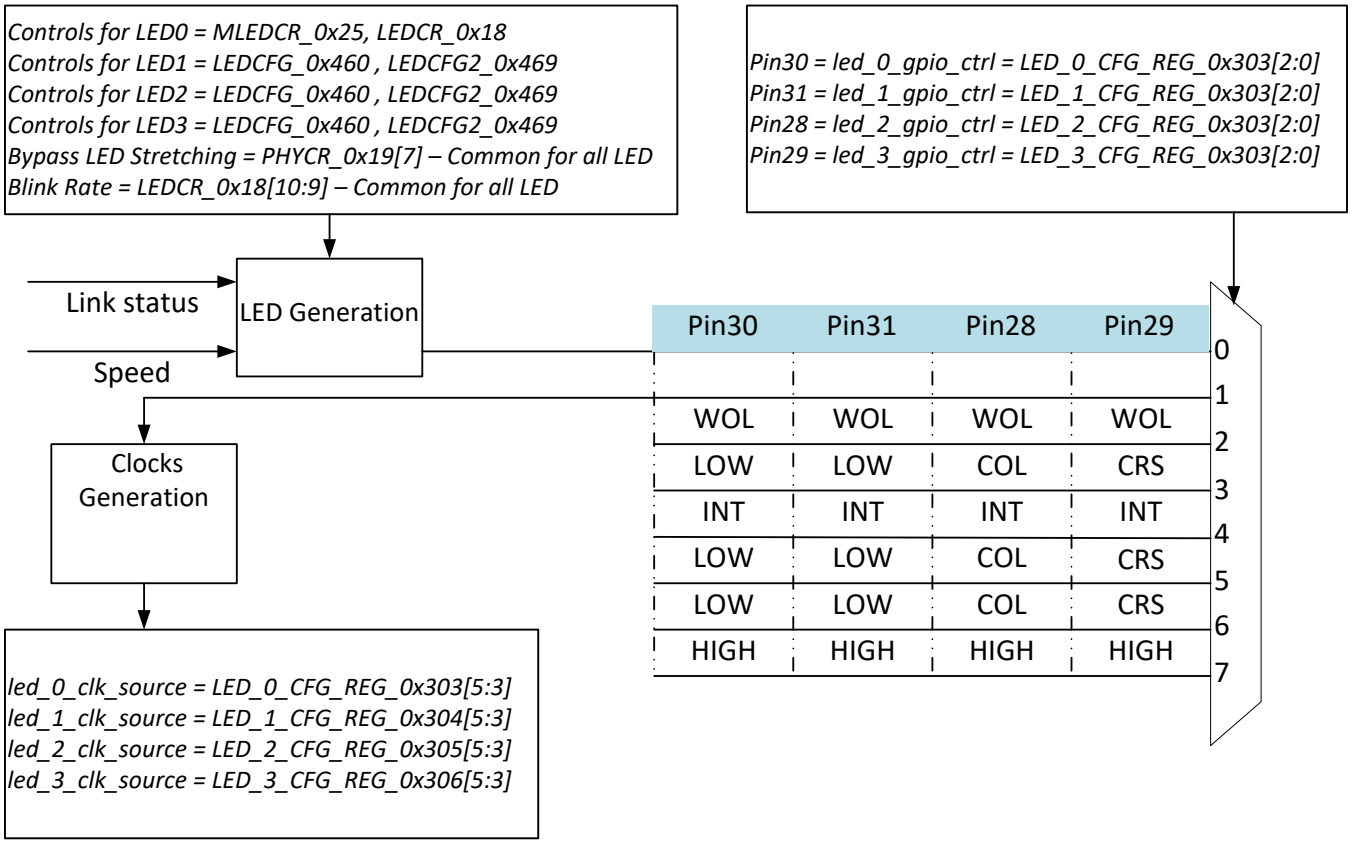


Figure 24. LED and GPIO Configuration

NOTE

A clock output is available on Pin 28 and 29 in ENHANCED mode only. These pins can be configured to output only a 25-MHz or 50-MHz clock.

9.4 Programming

The DP83826 provides hardware based configuration (via bootstraps) and the IEEE defined register set for programming and status indications. It also provides an additional register set to configure other features not supported through IEEE registers.

9.4.1 Hardware Bootstraps Configuration

DP83826 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. Configuration of the device may be done through the strap pins or through the management register interface. A pullup resistor or a pulldown resistor of suggested values may be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes. All strap pins have two levels.

Programming (continued)

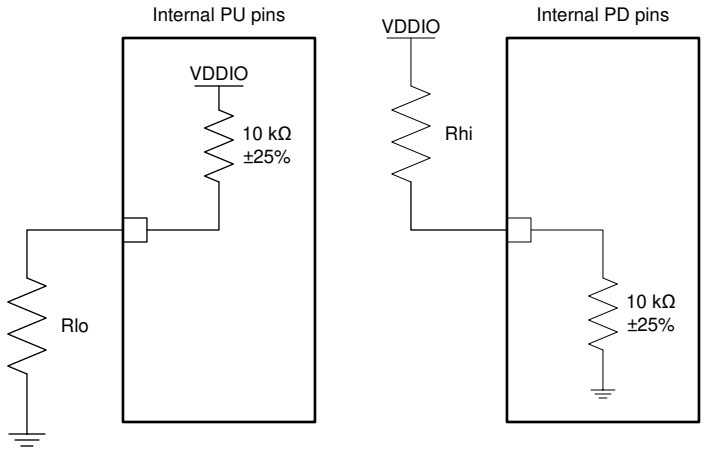


Figure 25. Strap Circuit

Table 8. 2-Level Strap Resistor Ratios(1)

Mode	SUGGESTED RESISTORS	
	R_{HI} (kΩ)	R_{LO} (kΩ)
INTERNAL 10-kΩ PULLDOWN (PD) PINS		
0-DEFAULT	OPEN	OPEN
1	2.49	OPEN
INTERNAL 10-kΩ PULLUP (PU) PINS		
0	OPEN	2.49
1-DEFAULT	OPEN	OPEN

(1) Resistor ratios are only a recommendation. Use the bootstrap threshold values contained within the Electrical Characteristics table for more precise mode selections.

9.4.1.1 DP83826 Bootstrap Configurations (ENHANCED Mode)

This section describes the hardware bootstraps available for DP83826.

9.4.1.1.1 Bootstraps for PHY Address

Table 9. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	0		PHY_ADD0
				0	0
				1	1
CRS/LED3	Strap3	29	0		PHY_ADD1
				0	0
				1	1
COL/LED2	Strap4	28	0		PHY_ADD2
				0	0
				1	1

Table 10. MAC Mode Selection Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D2	Strap8	14	0	0	MII MAC mode
				1	RMII MAC mode

Table 11. MII MAC Mode Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	0	0	fast link-drop disable
				1	fast link-drop enable

Table 12. RMII MAC Mode Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
TX_CLK	Strap5	22	0	0	RMII master mode
				1	RMII slave mode
RX_D3	Strap7	13	0	0	RMII_CRS_DV
				1	RMII_RX_DV (for RMII repeater mode)

Table 13. Auto_Neg Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D1	Strap9	15	0	0	auto MDIX enable
				1	auto MDIX disable
RX_D0	Strap0	16	0	0	auto negotiation enable
				1	auto-negotiation disable. force mode 100 M enabled
RX_DV	Strap10	18	0	0	MDIX (applicable only when auto-MDIX is disabled)
				1	MDI (applicable only when auto-MDIX is disabled)

Table 14. CLKOUT/LED1 Bootstraps

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6	20	0	0	CLKOUT 25 MHz on Pin 31
				1	LED1 on Pin 31

9.4.1.2 DP83826 Strap Configuration (BASIC Mode)

This section describes the strap configuration available for BASIC mode.

9.4.1.2.1 Bootstraps for PHY Address

Table 15. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	1		PHY_ADD0
				0	0
				1	1
RX_D2	Strap8	14	0		PHY_ADD1
				0	0
				1	1
RX_D1	Strap9	15	0		PHY_ADD2
				0	0
				1	1

Table 16. MAC Mode Selection Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Strap10	Strap3	Strap4	Function
COL	Strap4	28	0	0	0	0	MII MAC mode
				0	0	1	RMII master mode
				1	0	1	RMII slave mode
CRS	Strap3	29	0	other values are reserved			
RX_DV	Strap10	18	0				

Table 17. Auto Negotiation Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	1	0	Auto Negotiation Disable
				1	Auto Negotiation Enable

Table 18. Speed Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
TX_ER/LED 1	Strap1	31	1	0	Speed 10 M
				1	Speed 100 M

Table 19. Full/Half Duplex Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D0	Strap0	16	1	0	Half Duplex
				1	Full Duplex

Table 20. MII Isolate Bootstraps

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6	20	0	0	MII Isolate Disable
				1	MII Isolate Enable

9.5 Register Maps

Table 21 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 21 should be considered as reserved locations and the register contents should not be modified.

Table 21. Device Registers

Address	Acronym	Register Name	Section
0x0	BMCR		Go
0x1	BMSR		Go
0x2	PHYIDR1		Go
0x3	PHYIDR2		Go
0x4	ANAR		Go
0x5	ALNPAR		Go
0x6	ANER		Go
0x7	ANNPTR		Go
0x8	ANLNPTR		Go
0x9	CR1		Go
0xA	CR2		Go
0xB	CR3		Go
0xD	REGCR		Go
0xE	ADDAR		Go
0xF	FLDS		Go
0x10	PHYSTS		Go
0x11	PHYSCR		Go
0x12	MISR1		Go
0x13	MISR2		Go
0x14	FCSCR		Go
0x15	RECR		Go
0x16	BISCR		Go
0x17	RCSR		Go
0x18	LEDCR		Go
0x19	PHYCR		Go
0x1A	10BTSCR		Go
0x1B	BICSR1		Go
0x1C	BICSR2		Go
0x1E	CDCR		Go
0x1F	PHYRCR		Go
0x25	MLEDCR		Go
0x27	COMPT		Go
0x2A	10M_CFG		Go
0x117	FLD_CFG1		Go
0x131	FLD_CFG2		Go
0x170	CDSCR		Go
0x171	CDSCR2		Go
0x172	TDR_172		Go
0x173	CDSCR3		Go
0x174	TDR_174		Go
0x175	TDR_175		Go
0x176	TDR_176		Go
0x177	CDSCR4		Go

Table 21. Device Registers (continued)

Address	Acronym	Register Name	Section
0x178	TDR_178		Go
0x180	CDLRR1		Go
0x181	CDLRR2		Go
0x182	CDLRR3		Go
0x183	CDLRR4		Go
0x184	CDLRR5		Go
0x185	CDLAR1		Go
0x186	CDLAR2		Go
0x187	CDLAR3		Go
0x188	CDLAR4		Go
0x189	CDLAR5		Go
0x18A	CDLAR6		Go
0x302	IO_CFG1		Go
0x303	LED0_GPIO_CFG		Go
0x304	LED1_GPIO_CFG		Go
0x305	LED2_GPIO_CFG		Go
0x306	LED3_GPIO_CFG		Go
0x308	CLK_OUT_LED_STATUS		Go
0x30B	VOD_CFG1		Go
0x30C	VOD_CFG2		Go
0x30E	VOD_CFG3		Go
0x404	ANA_LD_PROG_SL		Go
0x40D	ANA_RX10BT_CTRL		Go
0x456	GENCFG		Go
0x459	PIN_CFG1		Go
0x45A	PIN_CFG2		Go
0x460	LEDCFG		Go
0x461	IOCTRL		Go
0x467	SOR1		Go
0x468	SOR2		Go
0x469	LEDCFG2		Go
0x4A0	RXFCFG1		Go
0x4A1	RXFS		Go
0x4A2	RXFPMD1		Go
0x4A3	RXFPMD2		Go
0x4A4	RXFPMD3		Go
0x4A5	RXFSOP1		Go
0x4A6	RXFSOP2		Go
0x4A7	RXFSOP3		Go

Complex bit access types are encoded to fit into small table cells. Table 22 shows the codes that are used for access types in this section.

Table 22. Device Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read

Table 22. Device Access Type Codes (continued)

Access Type	Code	Description
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W, STRAP	W	Write
W, W1S	W	Write
W0C	W 0C	Write 0 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

9.5.1 BMCR Register (Address = 0x0) [reset = 0x3100]

BMCR is shown in Table 23.

Return to Summary Table.

Table 23. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reset	HW1S	0x0	PHY Software Reset: Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is completed,, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared. 0x0 = Normal Operation 0x1 = Initiate software Reset / Reset in Progress
14	MII Loopback	R/W	0x0	MII Loopback: When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally. Additionally set following additional bit BISCR 0x0016[4:0] = 0b00100 for 100Base-TX and BISCR 0x0016[4:0] = 00001b for 10Base-Te 0x0 = Normal Operation 0x1 = MII Loopback enabled
13	Speed Selection	R/W,STRAP	0x1	Speed Selection: When Auto-Negotiation is disabled (bit [12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected. In BASIC Mode: It is also determined by strap when Auto-Negotiation is disabled. 0x0 = 10 Mbps 0x1 = 100 Mbps
12	Auto-Negotiation Enable	R/W,STRAP	0x1	Auto-Negotiation Enable: In BASIC Mode and ENHANCED Mode: Latched by strap 0x0 = Disable Auto-Negotiation - bits [8] and [13] determine the port speed and duplex mode 0x1 = Enable Auto-Negotiation - bits [8] and [13] of this register are ignored when this bit is set

Table 23. BMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IEEE Power Down	R/W	0x0	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N (in ENHANCED mode) pin. When the active low INT/PWDN_N is asserted, this bit is set. 0x0 = Normal Operation 0x1 = IEEE Power Down
10	Isolate	R/W,STRAP	0x0	In BASIC Mode, the value is Latched by strap 0x0 = Normal Operation 0x1 = Isolates the port from the MII with the exception of the serial management interface. It also disables50MHz clock in RMII Master Mode
9	Restart Auto-Negotiation	RH/W,W1S	0x0	Restart Auto-Negotiation: If Auto-Negotiation is disabled (bit [12] = 0), bit [9] is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0x0 = Normal Operation 0x1 = Restarts Auto-Negotiation, Re-initiates the Auto-Negotiation process
8	Duplex Mode	R/W,STRAP	0x1	Duplex Mode: When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected. In BASIC Mode, this bit is Latched by strap 0x0 = Half-Duplex 0x1 = Full-Duplex
7	Collision Test	R/W	0x0	Collision Test: When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN. 0x0 = Normal Operation 0x1 = Enable COL Signal Test
6-0	RESERVED	R	0x0	Reserved

9.5.2 BMSR Register (Address = 0x1) [reset = 0x7849]

BMSR is shown in Table 24.

Return to Summary Table.

Table 24. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0x0	100Base-T4 Capable: This protocol is not available. Always reads as 0.
14	100Base-TX Full-Duplex	R	0x1	100Base-TX Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 100Base-TX 0x1 = Device able to perform Full-Duplex 100Base-TX
13	100Base-TX Half-Duplex	R	0x1	100Base-TX Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 100Base-TX 0x1 = Device able to perform Half-Duplex 100Base-TX

Table 24. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	10Base-T Full-Duplex	R	0x1	10Base-T Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 10Base-T 0x1 = Device able to perform Full-Duplex 10Base-T
11	10Base-T Half-Duplex	R	0x1	10Base-T Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 10Base-T 0x1 = Device able to perform Half-Duplex 10Base-T
10-7	RESERVED	R	0x0	Reserved
6	SMI Preamble Suppression	R	0x1	Preamble Suppression Capable: If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. The device requires minimum of 500ns gap between two transactions, followed by one positive edge of MDC and MDIO=1, before starting the next transaction. 0x0 = Device not able to perform management transaction with preambles suppressed 0x1 = Device able to perform management transaction with preamble suppressed
5	Auto-Negotiation Complete	R	0x0	Auto-Negotiation Complete: 0x0 = Auto Negotiation process not completed (either still in process, disabled or reset) 0x1 = Auto-Negotiation process completed
4	Remote Fault	H	0x0	Remote Fault: Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset. 0x0 = No remote fault condition detected 0x1 = Remote fault condition detected
3	Auto-Negotiation Ability	R	0x1	Auto-Negotiation Ability: 0x0 = Device is not able to perform Auto-Negotiation 0x1 = Device is able to perform Auto-Negotiation
2	Link Status	RC	0x0	Link Status: Last latched value is cleared on read 0x0 = Link not established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps operation)
1	Jabber Detect	H	0x0	Jabber Detect: 0x0 = No jabber condition detected This bit only has meaning for 10Base-T operation. 0x1 = Jabber condition detected
0	Extended Capability	R	0x1	Extended Capability: 0x0 = Basic register set capabilities only 0x1 = Extended register capabilities

9.5.3 PHYIDR1 Register (Address = 0x2) [reset = 0x2000]

PHYIDR1 is shown in Table 25.

Return to Summary Table.

Table 25. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier Bits 21:6	R	0x2000	PHY Identifier Register #1

9.5.4 PHYIDR2 Register (Address = 0x3) [reset = 0xA130]

PHYIDR2 is shown in Table 26.

Return to Summary Table.

Table 26. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally Unique Identifier Bits 5:0	R	0x28	PHY Identifier Register #2
9-4	Model Number	R	0x13	Vendor Model Number: The six bits of vendor model number are mapped from bits [9] to [4] 0x11 = Basic Mode 0x13 = ENHANCED Mode
3-0	Revision Number	R	0x0	Model Revision Number: Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

9.5.5 ANAR Register (Address = 0x4) [reset = 0x1E1]

ANAR is shown in Table 27.

Return to Summary Table.

Table 27. ANAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R/W	0x0	Next Page Indication: 0x0 = Next Page Transfer not desired 0x1 = Next Page Transfer desired
14	RESERVED	R	0x0	Reserved
13	Remote Fault	R/W	0x0	Remote Fault: 0x0 = No Remote Fault detected 0x1 = Advertises that this device has detected a Remote Fault. Please note DP83826 does not support Remote Fault. This bit shall not be set by Application
12	RESERVED	R	0x0	Reserved
11	Asymmetric Pause	R/W	0x0	Asymmetric Pause Support For Full-Duplex Links: 0x0 = Do not advertise asymmetric pause ability 0x1 = Advertise asymmetric pause ability
10	Pause	R/W	0x0	Pause Support for Full-Duplex Links: 0x0 = Do not advertise pause ability 0x1 = Advertise pause ability

Table 27. ANAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	100Base-T4	R	0x0	100Base-T4 Support: 0x0 = Do not advertise 100Base-T4 ability 0x1 = Advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	R/W,STRAP	0x1	100Base-TX Full-Duplex Support: Values does not matter in force-mode BASIC Mode : Latched by strap 0x0 = Do not advertise 100Base-TX Full-Duplex ability Values does not matter in force-mode 0x1 = Advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	R/W,STRAP	0x1	100Base-TX Half-Duplex Support: Values does not matter in force-mode BASIC Mode: Latched by strap 0x0 = Do not advertise 100Base-TX Half-Duplex ability Values does not matter in force-mode 0x1 = Advertise 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	R/W,STRAP	0x1	10Base-T Full-Duplex Support: Values does not matter in force-mode BASIC Mode: Latched by strap 0x0 = Do not advertise 10Base-T Full-Duplex ability Values does not matter in force-mode 0x1 = Advertise 10Base-T Full-Duplex ability
5	10Base-T Half-Duplex	R/W,STRAP	0x1	10Base-T Half-Duplex Support: Values does not matter in force-mode BASIC Mode/ENHANCED Mode : Latched by strap 0x0 = Do not advertise 10Base-T Half-Duplex ability Values does not matter in force-mode 0x1 = Advertise 10Base-T Half-Duplex ability
4-0	Selector Field	R/W	0x1	Protocol Selection Bits: Technology selector field (IEEE802.3u <00001>)

9.5.6 ALNPAR Register (Address = 0x5) [reset = 0x0]

ALNPAR is shown in Table 28.

Return to Summary Table.

Table 28. ALNPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R	0x0	Next Page Indication: 0x0 = Link partner does not desire Next Page Transfer 0x1 = Link partner desires Next Page Transfer
14	Acknowledge	R	0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code word 0x1 = Link partner acknowledges reception of link code word
13	Remote Fault	R	0x0	Remote Fault: 0x0 = Link partner does not advertise remote fault event detection 0x1 = Link partner advertises remote fault event detection
12	RESERVED	R	0x0	Reserved

Table 28. ALNPAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	Asymmetric Pause	R	0x0	Asymmetric Pause: 0x0 = Link partner does not advertise asymmetric pause ability 0x1 = Link partner advertises asymmetric pause ability
10	Pause	R	0x0	Pause: 0x0 = Link partner does not advertise pause ability 0x1 = Link partner advertises pause ability
9	100Base-T4	R	0x0	100Base-T4 Support: 0x0 = Link partner does not advertise 100Base-T4 ability 0x1 = Link partner advertises 100Base-T4 ability
8	100Base-TX Full-Duplex	R	0x0	100Base-TX Full-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Full-Duplex ability 0x1 = Link partner advertises 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	R	0x0	100Base-TX Half-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Half-Duplex ability 0x1 = Link partner advertises 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	R	0x0	10Base-T Full-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Full-Duplex ability 0x1 = Link partner advertises 10Base-T Full-Duplex ability
5	10Base-T Half-Duplex	R	0x0	10Base-T Half-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Half-Duplex ability 0x1 = Link partner advertises 10Base-T Half-Duplex ability
4-0	Selector Field	R	0x0	Protocol Selection Bits: Technology selector field (IEEE802.3 <00001>)

9.5.7 ANER Register (Address = 0x6) [reset = 0x4]

ANER is shown in Table 29.

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Table 29. ANER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4	Parallel Detection Fault	H	0x0	Parallel Detection Fault: 0x0 = No fault detected 0x1 = A fault has been detected during the parallel detection process
3	Link Partner Next Page Able	R	0x0	Link Partner Next Page Ability: 0x0 = Link partner is not able to exchange next pages 0x1 = Link partner is able to exchange next pages
2	Local Device Next Page Able	R	0x1	Next Page Ability: 0x0 = Local device is not able to exchange next pages 0x1 = Local device is able to exchange next pages

Table 29. ANER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	Page Received	H	0x0	Link Code Word Page Received: 0x0 = A new page has not been received 0x1 = A new page has been received
0	Link Partner Auto-Negotiation Able	R	0x0	Link Partner Auto-Negotiation Ability: 0x0 = Link partner does not support Auto-Negotiation 0x1 = Link partner supports Auto-Negotiation

9.5.8 ANNPTR Register (Address = 0x7) [reset = 0x2001]

ANNPTR is shown in Table 30.

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Table 30. ANNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R/W	0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	RESERVED	R	0x0	Reserved
13	Message Page	R/W	0x1	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge 2	R/W	0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle	R	0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	CODE	R/W	0x1	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

9.5.9 ANLNPTR Register (Address = 0x8) [reset = 0x0]

ANLNPTR is shown in Table 31.

Return to Summary Table.

Table 31. ANLNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next Page	R	0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	Acknowledge	R	0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code work 0x1 = Link partner acknowledges reception of link code word
13	Message Page	R	0x0	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge 2	R	0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle	R	0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	Message/Unformatted Field	R	0x0	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

9.5.10 CR1 Register (Address = 0x9) [reset = 0x0]

CR1 is shown in Table 32.

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Table 32. CR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	TDR Auto-Run	R/W	0x0	TDR Auto-Run at Link Down 0x0 = Disable automatic execution of TDR 0x1 = Enable execution of TDR procedure after link down event
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

Table 32. CR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Robust Auto MDIX	R/W	0x0	Robust Auto-MDIX: If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. When using in Force Mode, Robust Auto-MDIX shall be enabled 0x0 = Disable Auto-MDIX 0x1 = Enable Robust Auto-MDIX
4	RESERVED	R	0x0	Reserved
3-2	RESERVED	R	0x0	Reserved
1	Fast RXDV Detection	R/W	0x0	Fast RXDV Detection: 0x0 = Disable Fast RX_DV detection. The PHY operates in normal mode. RX_DV assertion after detection of /JK/. 0x1 = Enable assertion high of RX_DV on receive packet due to detection of /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated.
0	RESERVED	R	0x0	Reserved

9.5.11 CR2 Register (Address = 0xA) [reset = 0x0]

CR2 is shown in Table 33.

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Table 33. CR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13-7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	Extended Full-Duplex Ability	R/W	0x0	Extended Full-Duplex Ability: 0x0 = Disable Extended Full-Duplex Ability. Decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification 0x1 = Enable Full-Duplex while working with link partner in force 100Base-TX. When the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RX_ER During IDLE	R/W	0x0	Detection of Receive Symbol Error During IDLE State: 0x0 = Disable detection of Receive symbol error during IDLE state 0x1 = Enable detection of Receive symbol error during IDLE state
1	Odd-Nibble Detection Disable	R/W	0x0	Detection of Transmit Error: 0x0 = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle 0x1 = Disable detection of transmit error in odd-nibble boundary

Table 33. CR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0x0	Reserved

9.5.12 CR3 Register (Address = 0xB) [reset = 0x0]

CR3 is shown in Table 34.

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Table 34. CR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	Descrambler Fast Link Down Mode	R/W	0x0	Descrambler Fast Link Drop: This option can be enabled in parallel to the other fast link down modes in bits [3:0]. 0x0 = Do not drop the link on descrambler link loss 0x1 = Drop the link on descrambler link loss
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	Polarity Swap	R/W	0x0	Polarity Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [5] high. 0x1 = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0h = Normal polarity
5	MDI/MDIX Swap	R/W	0x0	MDI/MDIX Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [6] high. 0x0 = MDI pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = Swap MDI pairs (Receive on TD pair, Transmit on RD pair)
4	RESERVED	R	0x0	Reserved
3-0	Fast Link Down Mode	R/W,STRAP	0x0	Fast Link Down Modes: Bit 3 Drop the link based on RX Error count of the MII interface. When a predefined number of 32 RX Error occurences in a 10us interval is reached, the link will be dropped. Bit 2 Drop the link based on MLT3 Error count (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in10us interval is reached, the link will be dropped. Bit 1 Drop the link based on Low SNR Threshold. When a predefined number of 20 Threshold crossing occurences in a 10us interval is reached, the link will be dropped. Bit 0 Drop the link based on Signal/Energy Loss indication. When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10us C : Bit 0 default is 0 NC+ MII: Bit 0 is taken from STRAP in ENHANCED mode NC + RMII: Bit 0 default is 0 The Fast Link Down function is an OR of all 5 options (bits [10] and [3:0]), the designer can enable any combination of these conditions.

9.5.13 REGCR Register (Address = 0xD) [reset = 0x0]

REGCR is shown in Table 35.

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Table 35. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended Register Command	R/W	0x0	Extended Register Command: 0x0 = Address 0x1 = Data, no post increment 0x2 = Data, post increment on read and write 0x3 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved
4-0	DEVAD	R/W	0x0	Device Address: Bits [4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83826 uses the vendor specific DEVAD [4:0] = '11111' for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

9.5.14 ADDAR Register (Address = 0xE) [reset = 0x0]

ADDAR is shown in Table 36.

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Table 36. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0x0	If REGCR register bits [15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

9.5.15 FLDS Register (Address = 0xF) [reset = 0x0]

FLDS is shown in Table 37.

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Table 37. FLDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Reserved
8-4	Fast Link Down Status	RC	0x0	Fast Link Down Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled) 0x1 = Signal/Energy Lost 0x2 = SNR Level 0x4 = MLT3 Errors 0x8 = RX Errors 0x10 = Descrambler Loss Sync
3-0	RESERVED	R	0x0	Reserved

9.5.16 PHYSTS Register (Address = 0x10) [reset = 0x6]

PHYSTS is shown in Table 38.

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Table 38. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	MDI/MDIX Mode	R	0x0	MDI/MDIX Mode Status: 0x0 = MDI Pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair)
13	Receive Error Latch	RC	0x0	Receive Error Latch: This bit will be cleared upon a read of the RECR register 0x0 = No receive error event has occurred 0x1 = Receive error event has occurred since last read of RXERCNT register (0x0015)
12	Polarity Status	RC	0x0	Polarity Status: This bit is a duplication of bit [4] in the 10BTSCR register (0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
11	False Carrier Sense Latch	RC	0x0	False Carrier Sense Latch: This bit will be cleared upon a read of the FCSR register. 0x0 = No False Carrier event has occurred 0x1 = False Carrier even has occurred since last read of FCSCR register (0x0014)
10	Signal Detect	RC	0x0	Signal Detect: Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler Lock	RC	0x0	Descrambler Lock: Active high 100Base-TX Descrambler Lock indication from PMD
8	Page Received	RC	0x0	Link Code Word Page Received: This bit is a duplicate of Page Received (bit [1]) in the ANER register and it is cleared on read of the ANER register (0x0006). 0x0 = Link Code Word Page has not been received 0x1 = A new Link Code Word Page has been received
7	MII Interrupt	RC	0x0	MII Interrupt Pending: Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR will clear this interrupt bit indication. 0x0 = No interrupt pending 0x1 = Indicates that an internal interrupt is pending
6	Remote Fault	RC	0x0	Remote Fault: Cleared on read of BMSR register (0x0001) or by reset. 0x1 = Remote Fault condition detected. Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation 0h = No Remote Fault condition detected

Table 38. PHYSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Jabber Detect	RC	0x0	Jabber Detection: This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No Jabber 0x1 = Jabber condition detected
4	Auto-Negotiation Status	R	0x0	Auto-Negotiation Status: 0x0 = Auto-Negotiation not complete 0x1 = Auto-Negotiation complete
3	MII Loopback Status	R	0x0	MII Loopback Status: 0x0 = Normal operation 0x1 = Loopback enabled
2	Duplex Status		0x1	Duplex Status: BASIC Mode: Latched by Strap when Auto-Negotiation is disabled ENHANCED Mode : 1 when Auto-Negotiation is disabled 0x0 = Half-Duplex mode 0x1 = Full-Duplex mode
1	Speed Status		0x1	Speed Status: BASIC Mode : Latched by Strap when Auto-Negotiation is disabled ENHANCED Mode : 1 when Auto-Negotiation is disabled 0x0 = 100 Mbps mode 0x1 = 10 Mbps mode
0	Link Status	R	0x0	Link Status: This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No link established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps)

9.5.17 PHYSCR Register (Address = 0x11) [reset = 0x108]

PHYSCR is shown in Table 39.

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Table 39. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable PLL	R/W	0x0	Disable PLL: Note: clock circuitry can be disabled only in IEEE power down mode. 0x0 = Normal operation 0x1 = Disable internal clocks circuitry
14	Power Save Mode Enable	R/W	0x0	Power Save Mode Enable: 0x0 = Normal operation 0x1 = Enable power save modes

Table 39. PHYSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	Power Save Modes	R/W	0x0	Power Save Mode: 0x0 = Normal operation mode. PHY is fully functional 0x1 = Reserved 0x2 = Active Sleep, Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
11	Scrambler Bypass	R/W	0x0	Scrambler Bypass: 0x0 = Scrambler bypass disabled 0x1 = Scrambler bypass enabled
10	RESERVED	R	0x0	Reserved
9-8	Loopback FIFO Depth	R/W	0x1	Far-End Loopback FIFO Depth: This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles. 0x0 = 4 nibbles FIFO 0x1 = 5 nibbles FIFO 0x2 = 6 nibbles FIFO 0x3 = 8 nibbles FIFO
7-5	RESERVED	R	0x0	Reserved
4	COL Full-Duplex Enable	R/W	0x0	Collision in Full-Duplex Mode: 0x0 = Disable Collision in Full-Duplex mode. Collision will be active in Half-Duplex only. 0x1 = Enable generating Collision signaling in Full-Duplex mode
3	Interrupt Polarity	R/W	0x1	Interrupt Polarity: 0x0 = Steady state (normal operation) is 0 logic and during interrupt is 1 logic 0x1 = Steady state (normal operation) is 1 logic and during interrupt is 0 logic
2	Test Interrupt	R/W	0x0	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 0x0 = Do not generate interrupt 0x1 = Generate an interrupt
1	Interrupt Enable	R/W	0x0	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register (0x0012). 0x0 = Disable event based interrupts 0x1 = Enable event based interrupts
0	Interrupt Output Enable	R/W	0x0	Interrupt Output Enable: Enable active low interrupt events via the INTR/PWERDN pin by configuring the INTR/PWRDN pin as an output(for ENHANCED mode) 0x0 = INTR/PWRDN is a Power Down pin 0x1 = INTR/PWRDN is an interrupt output

9.5.18 MISR1 Register (Address = 0x12) [reset = 0x0]

MISR1 is shown in Table 40.

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Table 40. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link Quality Interrupt	RC	0x0	Change of Link Quality Status Interrupt: 0x0 = Link quality is Good 0x1 = Change of link quality when link is ON
14	Energy Detect Interrupt	RC	0x0	Change of Energy Detection Status Interrupt: 0x0 = No change of energy detected 0x1 = Change of energy detected
13	Link Status Changed Interrupt	RC	0x0	Change of Link Status Interrupt: 0x0 = No change of link status 0x1 = Change of link status interrupt is pending
12	Speed Changed Interrupt	RC	0x0	Change of Speed Status Interrupt: 0x0 = No change of speed status 0x1 = Change of speed status interrupt is pending
11	Duplex Mode Changed Interrupt	RC	0x0	Change of Duplex Status Interrupt: 0x0 = No change of duplex status 0x1 = Change of duplex status interrupt is pending
10	Auto-Negotiation Completed Interrupt	RC	0x0	Auto-Negotiation Complete Interrupt: 0x0 = No Auto-Negotiation complete event is pending 0x1 = Auto-Negotiation complete interrupt is pending
9	False Carrier Counter Half-Full Interrupt	RC	0x0	False Carrier Counter Half-Full Interrupt: 0x0 = False Carrier half-full event is not pending 0x1 = False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending
8	Receive Error Counter Half-Full Interrupt	RC	0x0	Receiver Error Counter Half-Full Interrupt: 0x0 = Receive Error half-full event is not pending 0x1 = Receive Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending
7	Link Quality Interrupt Enable	R/W	0x0	Enable interrupt on change of link quality
6	Energy Detect Interrupt Enable	R/W	0x0	Enable interrupt on change of energy detection
5	Link Status Changed Enable	R/W	0x0	Enable interrupt on change of link status
4	Speed Changed Interrupt Enable	R/W	0x0	Enable Interrupt on change of speed status
3	Duplex Mode Changed Interrupt Enable	R/W	0x0	Enable Interrupt on change of duplex status
2	Auto-Negotiation Completed Enable	R/W	0x0	Enable Interrupt on Auto-negotiation complete event
1	False Carrier HF Enable	R/W	0x0	Enable Interrupt on False Carrier Counter Register half-full event
0	Receive Error HF Enable	R/W	0x0	Enable Interrupt on Receive Error Counter Register half-full event

9.5.19 MISR2 Register (Address = 0x13) [reset = 0x0]

MISR2 is shown in Table 41.

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Table 41. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	Auto-Negotiation Error Interrupt	RC	0x0	Auto-Negotiation Error Interrupt: 0x0 = No Auto-Negotiation error even pending 0x1 = Auto-Negotiation error interrupt is pending
13	Page Received Interrupt	RC	0x0	Page Receiver Interrupt: 0x0 = Page has not been received 0x1 = Page has been received
12	Loopback FIFO OF/UF Event Interrupt	RC	0x0	Loopback FIFO Overflow/Underflow Event Interrupt: 0x0 = No FIFO Overflow/Underflow event pending 0x1 = FIFO Overflow/Underflow event interrupt pending
11	MDI Crossover Change Interrupt	RC	0x0	MDI/MDIX Crossover Status Change Interrupt: 0x0 = MDI crossover status has not changed 0x1 = MDI crossover status changed interrupt is pending
10	Sleep Mode Interrupt	RC	0x0	Sleep Mode Event Interrupt: 0x0 = No Sleep mode event pending 0x1 = Sleep mode event interrupt is pending
9	Inverted Polarity Interrupt / WoL Packet Received Interrupt	RC	0x0	Inverted Polarity Interrupt / WoL Packet Received Interrupt: 0x0 = No Inverted polarity event pending / No WoL oacket received 0x1 = Inverted Polarity interrupt pending / WoL packet was recieved
8	Jabber Detect Interrupt	RC	0x0	Jabber Detect Event Interrupt: 0x0 = No Jabber detect event pending 0x1 = Jabber detect even interrupt pending
7	RESERVED	R	0x0	Reserved
6	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Enable Interrupt on Auto-Negotiation error event
5	Page Received Interrupt Enable	R/W	0x0	Enable Interrupt on page receive event
4	Loopback FIFO OF/UF Enable	R/W	0x0	Enable Interrupt on loopback FIFO Overflow/Underflow event
3	MDI Crossover Change Enable	R/W	0x0	Enable Interrupt on change of MDI/X status
2	Sleep Mode Event Enable	R/W	0x0	Enable Interrupt on sleep mode event
1	Polarity Changed / WoL Packet Enable	R/W	0x0	Enable Interrupt on change of polarity status
0	Jabber Detect Enable	R/W	0x0	Enable Interrupt on Jabber detection event

9.5.20 FCSCR Register (Address = 0x14) [reset = 0x0]

FCSCR is shown in Table 42.

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Table 42. FCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	False Carrier Event Counter		0x0	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

9.5.21 RECR Register (Address = 0x15) [reset = 0x0]

RECR is shown in Table 43.

Return to Summary Table.

Table 43. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive Error Counter		0x0	RX_ER Counter: When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

9.5.22 BISCR Register (Address = 0x16) [reset = 0x100]

BISCR is shown in Table 44.

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Table 44. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	BIST Error Counter Mode	R/W	0x0	BIST Error Counter Mode: 0x0 = Single mode, when BIST Error Counter reaches its max value, PRBS checker stops counting. 0x1 = Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again.
13	PRBS Checker Config	R/W	0x0	PRBS Checker Config:bit[13:12] 0x0 = PRBS Generator and Checker both are disabled 0x1 = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 0x2 = PRBS Generation is disabled. PRBS Checker is Enabled 0x3 = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C

Table 44. BISCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	Packet Generation Enable	R/W	0x0	Packet Generation Enable:bit[13:12] 0x0 = PRBS Generator and Checker both are disabled 0x1 = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 0x2 = PRBS Generation is disabled. PRBS Checker is Enabled 0x3 = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C
11	PRBS Checker Lock/Sync	R	0x0	PRBS Checker Lock/Sync Indication: 0x0 = PRBS checker is not locked 0x1 = PRBS checker is locked and synced on received bit stream
10	PRBS Checker Sync Loss	H	0x0	PRBS Checker Sync Loss Indication: 0x0 = PRBS checker has not lost sync 0x1 = PRBS checker has lost sync
9	Packet Generator Status	R	0x0	Packet Generation Status Indication: 0x0 = Packet Generator is off 0x1 = Packet Generator is active and generating packets
8	Power Mode	R	0x1	Sleep Mode Indication: 0x0 = Indicates that the PHY is in active sleep mode 0x1 = Indicates that the PHY is in normal power mode
7	RESERVED	R	0x0	Reserved
6	Transmit in MII Loopback	R/W	0x0	Transmit Data in MII Loopback Mode (valid only at 100 Mbps) 0x0 = Data is not transmitted to the line in MII loopback 0x1 = Enable transmission of data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit may be set only in MII Loopback mode - setting bit [14] in in BMCR register (0x0000)
5	RESERVED	R	0x0	Reserved
4-0	Loopback Mode	R/W	0x0	Loopback Mode Select: The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83826 digital and analog data paths 0x1 = PCS Input Loopback (Use for 10Base-Te only) 0x2 = PCS Output Loopback 0x4 = Digital Loopback (Use for 100Base-TX Only) Additional Register writes are required. 0x8 = Analog Loopback (requires 100Ω termination) 0x10 = Reverse Loopback

9.5.23 RCSR Register (Address = 0x17) [reset = 0x1]

RCSR is shown in Table 45.

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Table 45. RCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved

Table 45. RCSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RMII TX Clock Shift	R/W	0x0	RMII TX Clock Shift: Applicable only in RMII Slave Mode 0x0 = Transmit path internal clock shift is disabled 0x1 = Transmit path internal clock shift is enabled
7	RMII Clock Select	R/W,STRAP	0x0	RMII Reference Clock Select: BASIC Mode: Latched by strap ENHANCED Modie: Latched by strap 0x0 = 25MHz clock reference, crystal or CMOS-level oscillator 0x1 = 50MHz clock reference, CMOS-level oscillator
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RMII Revision Select	R/W	0x0	RMII Revision Select: 0x0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS 0x1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet
3	RMII Overflow Status		0x0	RX FIFO Overflow Status: 0x0 = Overflow detected 0x1 = Normal
2	RMII Underflow Status		0x0	RX FIFO Underflow Status: 0x0 = Underflow detected 0x1 = Normal
1-0	Receive Elasticity Buffer Size	R/W	0x1	Receive Elasticity Buffer Size: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at +/-50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for +/-100ppm), divide the packet lengths by 2). 0x0 = 14 bit tolerance (up to 16800 byte packets) 0x1 = 2 bit tolerance (up to 2400 byte packets) 0x2 = 6 bit tolerance (up to 7200 byte packets) 0x3 = 10 bit tolerance (up to 12000 byte packets)

9.5.24 LEDCR Register (Address = 0x18) [reset = 0x480]

LEDCR is shown in Table 46.

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Table 46. LEDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved

Table 46. LEDCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	Blink Rate	R/W	0x2	LED Blinking Rate (ON/OFF duration): 0x0 = 20Hz (50 ms) 0x1 = 10Hz (100 ms) 0x2 = 5Hz (200 ms) 0x3 = 2Hz (500 ms)
8	RESERVED	R	0x0	Reserved
7	LED Link Polarity	R/W,STRAP	0x1	LED Link Polarity Setting: Link LED polarity defined by direction of strapping on this pin. This register allows for override of this strap value. 0x0 = Active Low polarity setting 0x1 = Active High polarity setting
6-5	RESERVED	R	0x0	Reserved
4	Drive Link LED	R/W	0x0	Drive Link LED Select: 0x0 = Normal operation 0x1 = Drive value of ON/OFF bit [1] onto LED0 output pin
3-2	RESERVED	R	0x0	Reserved
1	Link LED ON/OFF Setting	R/W	0x0	Value to force on Link LED output 0x0 = LOW 0x1 = HIGH
0	RESERVED	R	0x0	Reserved

9.5.25 PHYCR Register (Address = 0x19) [reset = 0x8000]

PHYCR is shown in Table 47.

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Table 47. PHYCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Auto MDI/X Enable	R/W,STRAP	0x1	Auto-MDIX Enable: BASIC Mode: Default to A-MDIX enabled. ENHANCED Mode : Latched by strap A-MDIX 0x0 = Disable Auto-Negotiation Auto-MDIX capability 0x1 = Enable Auto-Negotiation Auto-MDIX capability
14	Force MDI/X	R/W,STRAP	0x0	Force MDIX: ENHANCED Mode: When A-MDIX strap is disabled, latched by FORCE MDI/MDIX strap 0x0 = Normal operation (Receive on RD pair, Transmit on TD pair) 0x1 = Force MDI pairs to cross (Receive on TD pair, Transmit on RD pair)
13	Pause RX Status	R	0x0	Pause Receive Negotiation Status: Indicates that pause receive should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause TX Status	R	0x0	Pause Transmit Negotiated Status: Indicates that pause should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.

Table 47. PHYCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MII Link Status	R	0x0	MII Link Status: 0x0 = No active 100Base-TX Full-Duplex link, established using Auto-Negotiation 0x1 = 100Base-TX Full-Duplex link is active and it was established using Auto-Negotiation
10-8	RESERVED	R	0x0	Reserved
7	Bypass LED Stretching	R/W	0x0	Bypass LED Stretching: Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value. 0x0 = Normal LED operation 0x1 = Bypass LED stretching
6	RESERVED	R	0x0	Reserved
5	LED Configuration	R/W	0x0	
4-0	PHY Address		0x0	PHY Address: BASIC Mode: Latched by Strap ENHANCED Mode: Latched by Strap

9.5.26 10BTSCR Register (Address = 0x1A) [reset = 0x0]

10BTSCR is shown in Table 48.

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Table 48. 10BTSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	Receiver Threshold Enable	R/W	0x0	Lower Receiver Threshold Enable: 0x0 = Normal 10Base-T operation 0x1 = Enable 10Base-T lower receiver threshold to allow operation with longer cables
12-9	Squelch	R/W	0x0	Squelch Configuration: Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0x0 = 200mV 0x1 = 250mV 0x2 = 300mV 0x3 = 350mV 0x4 = 400mV 0x5 = 450mV 0x6 = 500mV 0x7 = 550mV 0x8 = 600mV
8	RESERVED	R	0x0	Reserved
7	NLP Disable	R/W	0x0	NLP Transmission Control: 0x0 = Enable transmission of NLPs 0x1 = Disable transmission of NLPs
6-5	RESERVED	R	0x0	Reserved

Table 48. 10BTSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	Polarity Status	R	0x0	Polarity Status: This bit is a duplication of bit [12] in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
3-1	RESERVED	R	0x0	Reserved
0	Jabber Disable	R/W	0x0	Jabber Disable: Note: This function is only applicable in 10Base-Te operation. 0x0 = Jabber function enabled 0x1 = Jabber function disabled

9.5.27 BICSR1 Register (Address = 0x1B) [reset = 0x7D]

BICSR1 is shown in Table 49.

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Table 49. BICSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	BIST Error Count	R	0x0	BIST Error Count: Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit [15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) Note: Writing '1' to bit [15] will lock the counter's value for successive read operation and clear the BIST Error Counter.
7-0	BIST IPG Length	R/W	0x7D	BIST IPG Length: Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes*4 = 500 bytes). Binary values shall be multiplied by 4 to get the actual IPG length

9.5.28 BICSR2 Register (Address = 0x1C) [reset = 0x5EE]

BICSR2 is shown in Table 50.

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Table 50. BICSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-0	BIST Packet Length	R/W	0x5EE	BIST Packet Length: Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x05EE, which is equal to 1518 bytes.

9.5.29 CDCR Register (Address = 0x1E) [reset = 0x0]

CDCR is shown in Table 51.

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Table 51. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Cable Diagnostic Start	R/W	0x0	Cable Diagnostic Process Start: Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered. 0x0 = Cable Diagnostic is disabled 0x1 = Start cable measurement
14	cfg_rescal_en	R/W	0x0	Resistor calibration Start
13-2	RESERVED	R	0x0	Reserved
1	Cable Diagnostic Status	R	0x0	Cable Diagnostic Process Done: 0x0 = Cable Diagnostic had not completed 0x1 = Indication that cable measurement process is complete
0	Cable Diagnostic Test Fail	R	0x0	Cable Diagnostic Process Fail: 0x0 = Cable Diagnostic has not failed 0x1 = Indication that cable measurement process failed

9.5.30 PHYRCR Register (Address = 0x1F) [reset = 0x0]

PHYRCR is shown in Table 52.

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Table 52. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software Hard Reset	HW1S	0x0	Software Hard Reset: 0x0 = Normal Operation 0x1 = Reset PHY. This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital reset	HW1S	0x0	Software Restart: 0x0 = Normal Operation 0x1 = Restart PHY. This bit is self cleared and resets all PHY circuitry except the registers.
13	RESERVED	R	0x0	Reserved
12-0	RESERVED	R	0x0	Reserved

9.5.31 MLEDCR Register (Address = 0x25) [reset = 0x41]

MLEDCR is shown in Table 53.

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Table 53. MLEDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved

Table 53. MLEDCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MLED Polarity Swap	R/W	0x0	MLED Polarity Swap: The polarity of MLED depends on the routing configuration and the strap on COL pin. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high.
8-7	RESERVED	R	0x0	Reserved
6-3	LED0 Configuration	R/W	0x8	MLED Configurations: Selects the source for LED0 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = Reserved 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved
2-1	RESERVED	R	0x0	Reserved
0	cfg_mled_en	R/W	0x1	MLED Route to LED0: 0x0 = Reserved 0x1 = Value routed as per MLEDCR[6:3]

9.5.32 COMPT Register (Address = 0x27) [reset = 0x0]

COMPT is shown in Table 54.

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Table 54. COMPT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0x0	Reserved

Table 54. COMPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	Compliance Test Configuration	R/W	0x0	Compliance Test Configuration Select: Bit [4] in Register 0x0027 = 1, Enables 10Base-T Test Patterns Bit [4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits [3:0] select the 10Base-T test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' ... 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register Note 1: To reconfigure the 100Base-TX Test Mode, bit [4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. Note 2: When performing 100Base-TX or 10Base-T tests modes, the speed must be force using the Basic Mode Control Register (BMCR), address 0x0000.

9.5.33 10M_CFG Register (Address = 0x2A) [reset = 0x4000]

10M_CFG is shown in Table 55.

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Table 55. 10M_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	10M Preamble Mode	R/W	0x1	It supports two preamble modes when operating at 10Mbps a) IEEE Preamble mode b) Short Preamble mode. - When set to IEEE mode, preambles need to meet the IEEE defined preamble of 7 bytes. - When set to Short preamble mode, preambles can be as low as 4 bytes 0x0 = IEEE Preamble Mode 0x1 = Short Preamble Mode
13-0	RESERVED	R	0x0	Reserved

9.5.34 FLD_CFG1 Register (Address = 0x117) [reset = 0x0]

FLD_CFG1 is shown in Table 56.

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Table 56. FLD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Config MLT3 Error Cnt Len	R/W	0x0	MLT3 Error count window. Sets the window in terns if number of clocks (8ns). The counter counts in steady state. 0x0 = Reserved 0x1 = 2 cycle 0x3F = 64 cycle
9-4	Config MLT3 Error Number Cnt	R/W	0x0	Numbers of MLT3 errors to be counted for link down 0x0 = Reserved 0x1 = 1 Error 0x3F = 63 Errors
3-0	RESERVED	R	0x0	Reserved

9.5.35 FLD_CFG2 Register (Address = 0x131) [reset = 0x0]

FLD_CFG2 is shown in Table 57.

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Table 57. FLD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-0	Config Scrambler Threshold	R/W	0x0	Configures the window to declare link down based on descrambler errors. 0x0 = Reserved 0x1 = 1 Error 0x3F = 63 Errors

9.5.36 CDSCR Register (Address = 0x170) [reset = 0x410]

CDSCR is shown in Table 58.

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Table 58. CDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	Cable Diagnostic Cross Disable	R/W	0x0	Cross TDR Diagnostic Mode: 0x0 = TDR looks for reflections on channel other than the transmit channel configured by 0x170[13] 0x1 = TDR looks for reflections on same channel as transmit channel configured by 0x170[13]
13	cfg_tdr_chan_sel	R/W	0x0	TDR TX channel select: 0x0 = Select channel A as transmit channel. 0x1 = Select channel B as transmit channel.
12	cfg_tdr_dc_rem_no_init	R/W	0x0	To make sure DC removal module is not reset before TDR and dc removal is effective on TDR reflection

Table 58. CDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESERVED	R	0x0	Reserved
10-8	Cable Diagnostic Average Cycles	R/W	0x4	Number of TDR Cycles to Average: 0x0 = 1 TDR cycle 0x1 = 2 TDR cycles 0x2 = 4 TDR cycles 0x3 = 8 TDR cycles 0x4 = 16 TDR cycles 0x5 = 32 TDR cycles 0x6 = 64 TDR cycles 0x7 = Reserved
7	RESERVED	R	0x0	Reserved
6-4	cfg_tdr_seg_num	R/W	0x1	Selects cable segment on which TDR is to be performed - 000b = Reserved 001b = 0m to 10m 010b = 10m to 20m 011b = 20m to 40m 100b = 40m to 80m 101b = 80m and beyond 110b = Reserved 111b = Reserved
3-0	RESERVED	R	0x0	Reserved

9.5.37 CDSCR2 Register (Address = 0x171) [reset = 0x0]

CDSCR2 is shown in Table 59.

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Table 59. CDSCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.38 TDR_172 Register (Address = 0x172) [reset = 0x0]

TDR_172 is shown in Table 60.

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Table 60. TDR_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.39 CDSCR3 Register (Address = 0x173) [reset = 0xD04]

CDSCR3 is shown in Table 61.

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Table 61. CDSCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_tdr_seg_duration	R/W	0xD	Duration of the segment selected for TDR, calculated by - (Length_in_meters*2*5.2)/8 For Segment #1, 8'hD For Segment #2, 8'hD For Segment #3, 8'h1A For Segment #4, 8'h34 For Segment #5, 8'h8F
7-0	cfg_tdr_initial_skip	R/W	0x4	No of samples to be avoided before start of segment configured - For Segment #1, 8'h7 For Segment #2, 8'h14 For Segment #3, 8'h21 For Segment #4, 8'h3B For Segment #5, 8'h6F

9.5.40 TDR_174 Register (Address = 0x174) [reset = 0x0]

TDR_174 is shown in Table 62.

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Table 62. TDR_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.41 TDR_175 Register (Address = 0x175) [reset = 0x1004]

TDR_175 is shown in Table 63.

Return to Summary Table.

Table 63. TDR_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-11	cfg_tdr_sdw_avg_loc	R/W	0x2	TDR shadow average location - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h2
10-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3-0	cfg_tdr_fwd_shadow	R/W	0x4	Length of forward shadow for the segment configured (to avoid shadow of a fault peak be seen as another fault peak) - For Segment #1, 4'h4 For Segment #2, 4'h4 For Segment #3, 4'h5 For Segment #4, 4'h8 For Segment #5, 4'hB

9.5.42 TDR_176 Register (Address = 0x176) [reset = 0x5]

TDR_176 is shown in Table 64.

Return to Summary Table.

Table 64. TDR_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4-0	cfg_tdr_p_loc_thresh_seg	R/W	0x5	

9.5.43 CDSCR4 Register (Address = 0x177) [reset = 0x1E00]

CDSCR4 is shown in Table 65.

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Table 65. CDSCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12-8	Short Cables Threshold	R/W	0x1E	TH to compensate for strong reflections in short cables
7-0	RESERVED	R	0x0	Reserved

9.5.44 TDR_178 Register (Address = 0x178) [reset = 0x2]

TDR_178 is shown in Table 66.

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Table 66. TDR_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0x0	Reserved
2-0	cfg_tdr_tx_pulse_width_seg	R/W	0x2	TDR TX Pulse width for Segment - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h6

9.5.45 CDLRR1 Register (Address = 0x180) [reset = 0x0]

CDLRR1 is shown in Table 67.

Return to Summary Table.

Table 67. CDLRR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	TD Peak Location 1	R	0x0	Location of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

9.5.46 CDLRR2 Register (Address = 0x181) [reset = 0x0]

CDLRR2 is shown in Table 68.

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Table 68. CDLRR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.47 CDLRR3 Register (Address = 0x182) [reset = 0x0]

CDLRR3 is shown in Table 69.

Return to Summary Table.

Table 69. CDLRR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.48 CDLRR4 Register (Address = 0x183) [reset = 0x0]

CDLRR4 is shown in Table 70.

Return to Summary Table.

Table 70. CDLRR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.49 CDLRR5 Register (Address = 0x184) [reset = 0x0]

CDLRR5 is shown in Table 71.

Return to Summary Table.

Table 71. CDLRR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.50 CDLAR1 Register (Address = 0x185) [reset = 0x0]

CDLAR1 is shown in Table 72.

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Table 72. CDLAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0x0	Reserved
6-0	TD Peak Amplitude 1	R	0x0	Amplitude of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

9.5.51 CDLAR2 Register (Address = 0x186) [reset = 0x0]

CDLAR2 is shown in Table 73.

Return to Summary Table.

Table 73. CDLAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.52 CDLAR3 Register (Address = 0x187) [reset = 0x0]

CDLAR3 is shown in Table 74.

Return to Summary Table.

Table 74. CDLAR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.53 CDLAR4 Register (Address = 0x188) [reset = 0x0]

CDLAR4 is shown in Table 75.

Return to Summary Table.

Table 75. CDLAR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.54 CDLAR5 Register (Address = 0x189) [reset = 0x0]

CDLAR5 is shown in Table 76.

Return to Summary Table.

Table 76. CDLAR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.55 CDLAR6 Register (Address = 0x18A) [reset = 0x0]

CDLAR6 is shown in Table 77.

Return to Summary Table.

Table 77. CDLAR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	TD Peak Polarity 1	R	0x0	Polarity of the First peak discovered by the TDR mechanism on Transmit Channel (TD).
10-6	RESERVED	R	0x0	Reserved
5	Cross Detect on TD	R	0x0	Cross Reflections were detected on TD. Indicate on Short between TD and TD
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

9.5.56 IO_CFG1 Register (Address = 0x302) [reset = 0x0]

IO_CFG1 is shown in Table 78.

Return to Summary Table.

Table 78. IO_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MaC Impedance Control	R/W	0x0	MAC Impedance Control: MAC interface impedance control sets the series termination for the digital pins. 0x0 = Slow Mode 0x1 = Fast Mode
13	RESERVED	R	0x0	Reserved
12-9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	cfg_clkout25m_off	R/W	0x0	For ENHANCED Mode only : Configure Clockout or LED1 0x0 = CLKOUT25 available 0x1 = LED1_GPIO is available
5-0	RESERVED	R	0x0	Reserved

9.5.57 LED0_GPIO_CFG Register (Address = 0x303) [reset = 0x8]

LED0_GPIO_CFG is shown in Table 79.

Return to Summary Table.

Table 79. LED0_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-3	cfg_led0_clk_sel	R/W	0x1	Selects one of the internal clock, for output on LED0. This is enabled when cfg_led0_gpio_ctrl[2:0] = 001b. The possible configurations are: 0x0 = Reserved 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved 0x4 = Reserved 0x5 = PLL Clock out 0x6 = Recovered Clock 0x7 = Reserved
2-0	cfg_led0_gpio_ctrl	R	0x0	GPIO Configuration for LED0: 0x0 = LED0 0x1 = Clock output selected by register field cfg_led0_clk_sel 0x2 = WoL 0x3 = 0 0x4 = Interrupt 0x5 = 0 0x6 = 0 0x7 = 1

9.5.58 LED1_GPIO_CFG Register (Address = 0x304) [reset = 0xD]

LED1_GPIO_CFG is shown in Table 80.

Return to Summary Table.

Table 80. LED1_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-3	cfg_led1_clk_sel	R/W	0x1	Selects one of the internal clock, for output on LED1. This is enabled when cfg_led0_gpio_ctrl[2:0] = 001b. The possible configurations are: 0x0 = Reserved 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved 0x4 = Reserved 0x5 = PLL Clock out 0x6 = Recovered Clock 0x7 = Reserved

Table 80. LED1_GPIO_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	cfg_led1_gpio_ctrl	R	0x5	GPIO Configuration for LED1: 0x0 = LED1 (in ENHANCED Mode, selectable by Strap) 0x1 = Clock output selected by register field cfg_led1_clk_sel 0x2 = WoL 0x3 = Reserved 0x4 = Interrupt 0x5 = TX_ER (default in BASIC mode) 0x6 = CLKOUT25M (default in ENHANCED Mode, selectable by Strap) 0x7 = Reserved

9.5.59 LED2_GPIO_CFG Register (Address = 0x305) [reset = 0x0]

LED2_GPIO_CFG is shown in Table 81.

Return to Summary Table.

Table 81. LED2_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-3	RESERVED	R	0x0	Reserved
2-0	cfg_led2_gpio_ctrl	R/W	0x0	GPIO Configuration for LED2: 0x0 = LED2 0x1 = Reserved 0x2 = WoL 0x3 = COL 0x4 = Interrupt 0x5 = COL 0x6 = COL 0x7 = High

9.5.60 LED3_GPIO_CFG Register (Address = 0x306) [reset = 0x0]

LED3_GPIO_CFG is shown in Table 82.

Return to Summary Table.

Table 82. LED3_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-3	RESERVED	R	0x0	Reserved

Table 82. LED3_GPIO_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	cfg_led3_gpio_ctrl	R	0x0	GPIO Configuration for LED3: 0x0 = LED3 0x1 = Reserved 0x2 = WoL 0x3 = CRS 0x4 = Interrupt 0x5 = CRS 0x6 = CRS 0x7 = High

9.5.61 CLK_OUT_LED_STATUS Register (Address = 0x308) [reset = 0x0]

CLK_OUT_LED_STATUS is shown in Table 83.

Return to Summary Table.

Table 83. CLK_OUT_LED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0x0	Reserved
0	cfg_clkout_25m_off_status	R	0x0	This bit is applicable in ENHANCED mode only 0x0 = CLKOUT25 available 0x1 = LED1_GPIO is available

9.5.62 VOD_CFG1 Register (Address = 0x30B) [reset = 0xC00]

VOD_CFG1 is shown in Table 84.

Return to Summary Table.

Table 84. VOD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-12	RESERVED	R	0x0	Reserved

Table 84. VOD_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	cfg_dac_minus_one_val_mdi	R/W	0x30	LD data for mlt3 encoded data of minus one in MDI mode. 0x28 = 150% 0x29 = 143.75% 0x2A = 137.50% 0x2B = 131.25% 0x2C = 125% 0x2D = 118.75% 0x2E = 112.50% 0x2F = 106.25% 0x30 = 100% 0x31 = 93.75% 0x32 = 87.50% 0x33 = 81.25% 0x34 = 75% 0x35 = 68.75% 0x36 = 62.50% 0x37 = 56.25% 0x38 = 50%
5-0	cfg_dac_zero_val	R/W	0x0	LD data for mlt3 encoded data of zero

9.5.63 VOD_CFG2 Register (Address = 0x30C) [reset = 0x410]

VOD_CFG2 is shown in Table 85.

Return to Summary Table.

Table 85. VOD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_dac_minus_one_val_mdix_3_to_0	R/W	0x0	LD data for mlt3 encoded data of minus one in MDX mode. 6 bit data is split into two fields - {cfg_dac_minus_one_val_mdix_5_to_4, cfg_dac_minus_one_val_mdix_3_to_0} 0x28 = 150% 0x29 = 143.75% 0x2A = 137.50% 0x2B = 131.25% 0x2C = 125% 0x2D = 118.75% 0x2E = 112.50% 0x2F = 106.25% 0x30 = 100% 0x31 = 93.75% 0x32 = 87.50% 0x33 = 81.25% 0x34 = 75% 0x35 = 68.75% 0x36 = 62.50% 0x37 = 56.25% 0x38 = 50%

Table 85. VOD_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	cfg_dac_plus_one_val_mdix	R/W	0x10	LD data for mlt3 encoded data of plus one in MDIX mode 0x08 = 50% 0x09 = 56.25% 0x0A = 62.50% 0x0B = 68.75% 0x0C = 75% 0x0D = 81.25% 0x0E = 87.50% 0x0F = 93.75% 0x10 = 100% 0x11 = 106.25% 0x12 = 112.50% 0x13 = 118.75% 0x14 = 125% 0x15 = 131.25% 0x16 = 137.50% 0x17 = 143.75% 0x18 = 150%
5-0	cfg_dac_plus_one_val_mdi	R/W	0x10	LD data for mlt3 encoded data of plus one in MDI mode 0x08 = 50% 0x09 = 56.25% 0x0A = 62.50% 0x0B = 68.75% 0x0C = 75% 0x0D = 81.25% 0x0E = 87.50% 0x0F = 93.75% 0x10 = 100% 0x11 = 106.25% 0x12 = 112.50% 0x13 = 118.75% 0x14 = 125% 0x15 = 131.25% 0x16 = 137.50% 0x17 = 143.75% 0x18 = 150%

9.5.64 VOD_CFG3 Register (Address = 0x30E) [reset = 0x0]

VOD_CFG3 is shown in Table 86.

Return to Summary Table.

Table 86. VOD_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	ld_term_mdi_10M_reg	R/W	0x0	10M mode, MDI Termination Value Register 0x0 = 122 0x1 = 119 0x2 = 116 0x3 = 113 0x4 = 110 0x5 = 107 0x6 = 105 0x7 = 102 0x8 = 100 0x9 = 98 0x0A = 96 0x0B = 94 0x0C = 92 0x0D = 90 0x0E = 88 0x0F = 86
11	ld_term_mdi_10M_en	R/W	0x0	10M mode, MDI Termination Value Register Enable 0x0 = Disable 0x1 = Enable
10-7	ld_term_mdix_10M_reg	R/W	0x0	10M mode, MDIX Termination Value Register 0x0 = 122 0x01 = 119 0x2 = 116 0x3 = 113 0x4 = 110 0x5 = 107 0x6 = 105 0x7 = 102 0x8 = 100 0x9 = 98 0x0A = 96 0x0B = 94 0x0C = 92 0x0D = 90 0x0E = 88 0x0F = 86
6	ld_term_mdix_10M_en	R/W	0x0	10M mode, MDIX Termination Value Register Enable 0x0 = Disable 0x1 = Enable
5-2	RESERVED	R	0x0	Reserved

Table 86. VOD_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RESERVED	R	0x0	Reserved

9.5.65 ANA_LD_PROG_SL Register (Address = 0x404) [reset = 0x0]

ANA_LD_PROG_SL is shown in Table 87.

Return to Summary Table.

Table 87. ANA_LD_PROG_SL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

9.5.66 ANA_RX10BT_CTRL Register (Address = 0x40D) [reset = 0x0]

ANA_RX10BT_CTRL is shown in Table 88.

Return to Summary Table.

Table 88. ANA_RX10BT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4-0	rx10bt_comp_sl	R/W	0x0	10B-T current Gain, common for both POS and NEG, Starting from 200mV to 575mV, step size of 25mV

9.5.67 GENCFG Register (Address = 0x456) [reset = 0x8]

GENCFG is shown in Table 89.

Return to Summary Table.

Table 89. GENCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	RESERVED	R/W	0x0	Link Fail Indication by assertingt RX_ERR HIGH for 32 clock cycles 0x0 = Default operation 0x1 = Extend RX_ERR for 32 cycles
12-4	RESERVED	R	0x0	Reserved
3	Min IPG Enable	R/W	0x1	Min IPG Enable: 0x0 = Minimal IPG set to 200 ns 0x1 = Enable Minimum Interpacket Gap (IPG is set to 120ns instead of 200ns)
2-0	RESERVED	R	0x0	Reserved

9.5.68 PIN_CFG1 Register (Address = 0x459) [reset = 0x0]

PIN_CFG1 is shown in Table 90.

Return to Summary Table.

Table 90. PIN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0x0	Reserved

Table 90. PIN_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLKOUT io_oe_n_force_ctrl	R/W	0x0	Enable CLKOUT pin direction configuration 0x0 = Default operation 0x1 = Force pin I/O mode

9.5.69 PIN_CFG2 Register (Address = 0x45A) [reset = 0x0]

PIN_CFG2 is shown in Table 91.

Return to Summary Table.

Table 91. PIN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0x0	Reserved
0	CLKOUT io_force_dir	R/W	0x0	Force CLKOUT pin direction 0x0 = Output 0x1 = Input

9.5.70 LEDCFG Register (Address = 0x460) [reset = 0x650]

LEDCFG is shown in Table 92.

Return to Summary Table.

Table 92. LEDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-8	LED3 Control	R/W	0x6	LED3 Control:Selects the source for LED3. This control is available in ENHANCED mode only. 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = LPI Mode (Energy Efficient Ethernet) 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved

Table 92. LEDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	LED2 Control	R/W	0x5	LED2 Control: Selects the source for LED2. This control is available in ENHANCED mode only. 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = LPI Mode (Energy Efficient Ethernet) 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved
3-0	LED1 Control	R/W	0x0	LED1 Control: Selects the source for LED1. 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = LPI Mode (Energy Efficient Ethernet) 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved

9.5.71 IOCTRL Register (Address = 0x461) [reset = 0x0]

IOCTRL is shown in Table 93.

Return to Summary Table.

Table 93. IOCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved

Table 93. IOCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10-7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R	0x0	Reserved
4-0	RESERVED	R	0x0	Reserved

9.5.72 SOR1 Register (Address = 0x467) [reset = 0x0]

SOR1 is shown in Table 94.

Return to Summary Table.

Table 94. SOR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	Strap10		0x0	Strap on pin#18
9	Strap9		0x0	Strap on pin#15
8	Strap8		0x0	Strap on pin#14
7	Strap7		0x0	Strap on pin#13
6	Strap6		0x0	Strap on pin#20
5	Strap5		0x0	Strap on pin#22
4	Strap4		0x0	Strap on pin#28
3	Strap3		0x0	Strap on pin#29
2	Strap2		0x0	Strap on pin#30
1	Strap1		0x0	Strap on pin#31
0	Strap0		0x0	Strap on pin#16

9.5.73 SOR2 Register (Address = 0x468) [reset = 0x87]

SOR2 is shown in Table 95.

Return to Summary Table.

Table 95. SOR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	XMII_ISOLATE_EN		0x0	Applicable in BASIC Mode. Controls the MII Isolation bit field in register BMCR[10] 0x0 = No Isolation 0x1 = MAC pins Isolated
13	RESERVED	R	0x0	Reserved

Table 95. SOR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CRS_DV_vs_RX_DV		0x0	RMII mode RX_DV pin as CRS_DV or RX_DV 0x0 = RMI CRS_DV 0x1 = RMII RX_DV
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	CFG_FLD_EN		0x0	Configures Fast Link Down Feature. This affects register CR3[3:0]. 0x0 = CR3[10,3:0] is set to 5b00000 0x1 = CR3[10,3:0] is set to 5b11010
7	CFG_AMDIX		0x1	AMDIX Enable. This captures the inversion of AMDIX_DIS strap 0x0 = AMDIX Disable 0x1 = AMDIX Enable
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	CFG_RMII_MODE		0x0	MII/RMII mode Selection 0x0 = MII 0x1 = RMII
3	CFG_XI_50_SLAVE		0x0	RMII Master / Slave mode Selection 0x0 = RMII Master Mode 0x1 = RMII Slave Mode
2	CFG_AN_1		0x1	This is to derive ANAR register bit [8:5]
1	CFG_AN_0		0x1	This is to derive ANAR register bit [8:5]
0	CFG_AN_EN		0x1	ANEG Enable. This captures the inversion of ANEG_DIS

9.5.74 LEDCFG2 Register (Address = 0x469) [reset = 0x40]

LEDCFG2 is shown in Table 96.

Return to Summary Table.

Table 96. LEDCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	LED2_polarity	R/W,STRAP	0x1	led 2 polarity 0x0 = active low, 0x1 = active high
5	LED2_drv_val	R/W	0x0	led 2 drive value
4	LED2_drv_en	R/W	0x0	led 2 drive enable 0x0 = Normal operation 0x1 = drive LED polarity,

Table 96. LEDCFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0x0	Reserved
2	LED1_polarity	R/W,STRAP	0x0	led 1 polarity 0x0 = active low, 0x1 = active high
1	LED1_drv_val	R/W	0x0	led1 drive value
0	LED1_drv_en	R/W	0x0	led 1 drive enable 0x0 = Normal operation 0x1 = drive LED polarity,

9.5.75 RXFCFG1 Register (Address = 0x4A0) [reset = 0x1081]

RXFCFG1 is shown in Table 97.

Return to Summary Table.

Table 97. RXFCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	CRC Gate	R/W	0x1	CRC Gate: If Magic Packet has Bad CRC there will be no indication (status, interrupt, GPIO) when enabled. 0x0 = Bad CRC does not gate Magic Packet or Pattern Indications 0x1 = Bad CRC gates Magic Packet and Pattern Indications
11	WoL Level Change Indication Clear	W0C	0x0	WoL Level Change Indication Clear: If WoL Indication is set for Level change mode, this bit clears the level upon a write. 0x0 = Clear
10-9	WoL Pulse Indication Select	R/W	0x0	WoL Pulse Indication Select: Only valid when WoL Indication is set for Pulse mode. 0x0 = 8 clock cycles (of 125MHz clock) 0x1 = 16 clock cycles 0x2 = 32 clock cycles 0x3 = 64 clock cycles
8	WoL Indication Select	R/W	0x0	WoL Indication Select: 0x0 = Pulse mode 0x1 = Level change mode
7	WoL Enable	R/W	0x1	WoL Enable: 0x0 = normal operation 0x1 = Enable Wake-on-LAN (WoL)
6	Bit Mask Flag	R/W	0x0	Bit Mask Flag
5	Secure-ON Enable	R/W	0x0	Enable Secure-ON password for Magic Packets
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved

Table 97. RXFCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WoL Magic Packet Enable	R/W,STRAP	0x1	Enable Interrupt upon reception of Magic Packet

9.5.76 RXFS Register (Address = 0x4A1) [reset = 0x1000]

RXFS is shown in Table 98.

Return to Summary Table.

Table 98. RXFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	WoL Interrupt Source	R/W	0x1	WoL Interrupt Source: Source of Interrupt for bit [1] of register 0x0013. When enabling WoL, this bit is automatically set to WoL Interrupt. 0x0 = Data Polarity Interrupt 0x1 = WoL Interrupt
11-8	RESERVED	R	0x0	Reserved
7	SFD Error	H	0x0	SFD Error: 0x0 = No SFD error 0x1 = Packet with SFD error (without the SFD byte indicated in bit [13] register 0x04A0)
6	Bad CRC	H	0x0	Bad CRC: 0x0 = No bad CRC received 0x1 = Bad CRC was received
5	Secure-On Hack Flag	H	0x0	Secure-ON Hack Flag: 0x0 = Valid Secure-ON Password 0x1 = Invalid Password detected in Magic Packet
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	WoL Magic Packet Status	H	0x0	WoL Magic Packet Status:

9.5.77 RXFPMD1 Register (Address = 0x4A2) [reset = 0x0]

RXFPMD1 is shown in Table 99.

Return to Summary Table.

Table 99. RXFPMD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 4	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 5 (MSB)	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

9.5.78 RXFPMD2 Register (Address = 0x4A3) [reset = 0x0]

RXFPMD2 is shown in Table 100.

Return to Summary Table.

Table 100. RXFPMD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 2	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 3	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

9.5.79 RXFPMD3 Register (Address = 0x4A4) [reset = 0x0]

RXFPMD3 is shown in Table 101.

Return to Summary Table.

Table 101. RXFPMD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Destination Address Byte 0	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC Destination Address Byte 1	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

9.5.80 RXFSOP1 Register (Address = 0x4A5) [reset = 0x0]

RXFSOP1 is shown in Table 102.

Return to Summary Table.

Table 102. RXFSOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 1	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 0	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets

9.5.81 RXFSOP2 Register (Address = 0x4A6) [reset = 0x0]

RXFSOP2 is shown in Table 103.

Return to Summary Table.

Table 103. RXFSOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 3	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 2	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets

9.5.82 RXFSOP3 Register (Address = 0x4A7) [reset = 0x0]

RXFSOP3 is shown in Table 104.

Return to Summary Table.

Table 104. RXFSOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Secure-ON Password Byte 5	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets
7-0	Secure-ON Password Byte 4	R/W	0x0	Secure-ON Password Select: Secure-ON password for Magic Packets

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DP83826 is a single-port 10/100-Mbps Ethernet PHY. It supports connections to an Ethernet MAC through MII and RMII. Connections to the Ethernet media are made via the IEEE 802.3 defined media-dependent interface.

When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

10.2 Typical Applications

Following figure shows a typical application for the DP83826.

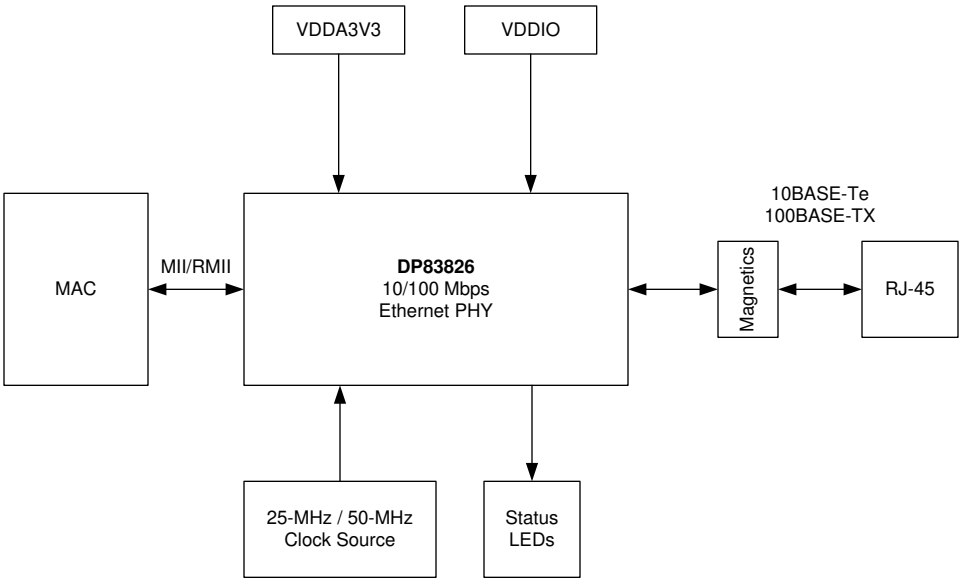

Figure 26. Typical DP83826 Application

Typical Applications (continued)

10.2.1 Twisted-Pair Interface (TPI) Network Circuit

Figure 27 shows the recommended twisted-pair interface network circuit for 10 Mbps or 100 Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

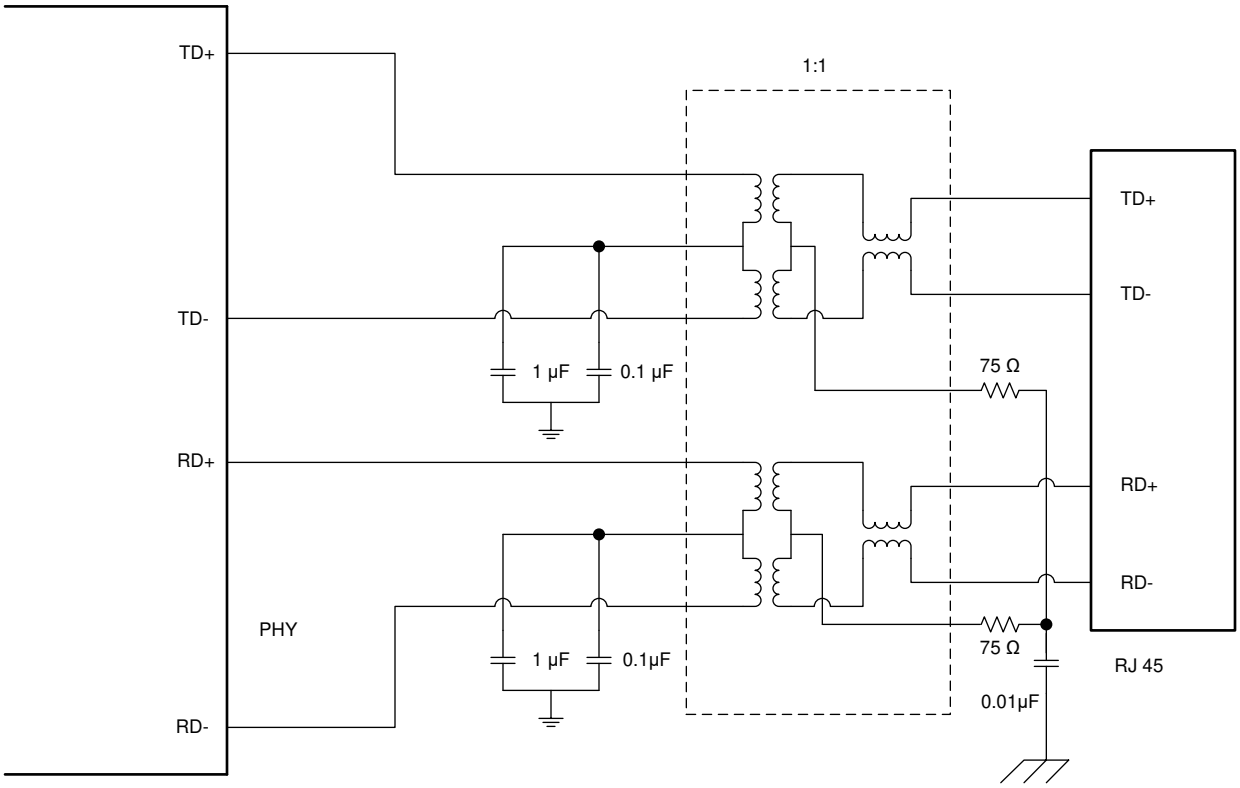

Figure 27. TPI Network Circuit

10.2.2 Design Requirements

The design requirements for the DP83826 in TPI operation (100BASE-TX or 10BASE-Te) are:

- VDDA3V3 supply = 3.3 V
- VDDIO supply = 3.3 V or 1.8 V
- Reference clock input = 25 MHz or 50 MHz (RMII slave)

10.2.2.1 Clock Requirements

The DP83826 supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

10.2.2.1.1 Oscillator

If an external clock source is used, tie XI to the clock source, and leave XO floating. The amplitude of the oscillator clock must be a nominal voltage of VDDIO.

10.2.2.1.2 Crystal

The use of a 25-MHz, parallel resonant, 20-pF load crystal is recommended if operating with a crystal. See Figure 28 for a typical connection diagram for a crystal resonator circuit. The load capacitor values vary with the crystal vendors; check with the vendor for the recommended loads. Refer to the application report *Selection and specification of crystals for Texas Instruments ethernet physical layer transceivers* for more details.

Typical Applications (continued)

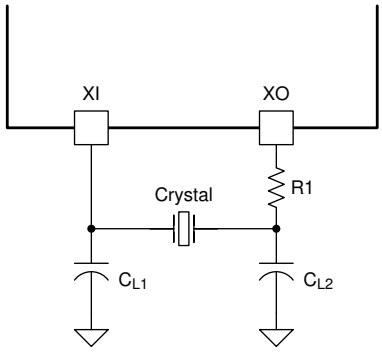

Figure 28. Crystal Oscillator Circuit

Table 105. 25-MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Including operational temperature, aging and other factors	–100		100	ppm
Load capacitance			15	40	pF
ESR				50	Ω

10.2.3 Detailed Design Procedure

10.2.3.1 MII Layout Guidelines

1. MII signals are single-ended signals
2. Traces should be routed with 50-Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches (~5 cm) is recommended and less than six inches (~15 cm) maximum

10.2.3.2 RMII Layout Guidelines

- RMII signals are single-ended signals
- Traces should be routed with 50-Ω impedance to ground
- Keep trace lengths as short as possible, less than two inches (~5 cm) is recommended and less than six inches (~15 cm) maximum

10.2.3.3 MDI Layout Guidelines

- MDI signals are differential.
- Route traces with 50-Ω impedance to ground and 100-Ω differential controlled impedance.
- Route MDI traces to the transformer on the same layer.
- Use a metal shielded RJ-45 connector and electrically connect the shield to chassis ground.
- Avoid supplies and ground beneath the magnetics.
- Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

10.2.4 Application Curves

Figure 29 depicts the DP83826 output pin drive characteristics for I/O supply voltages of 1.8 V and 3.3 V.

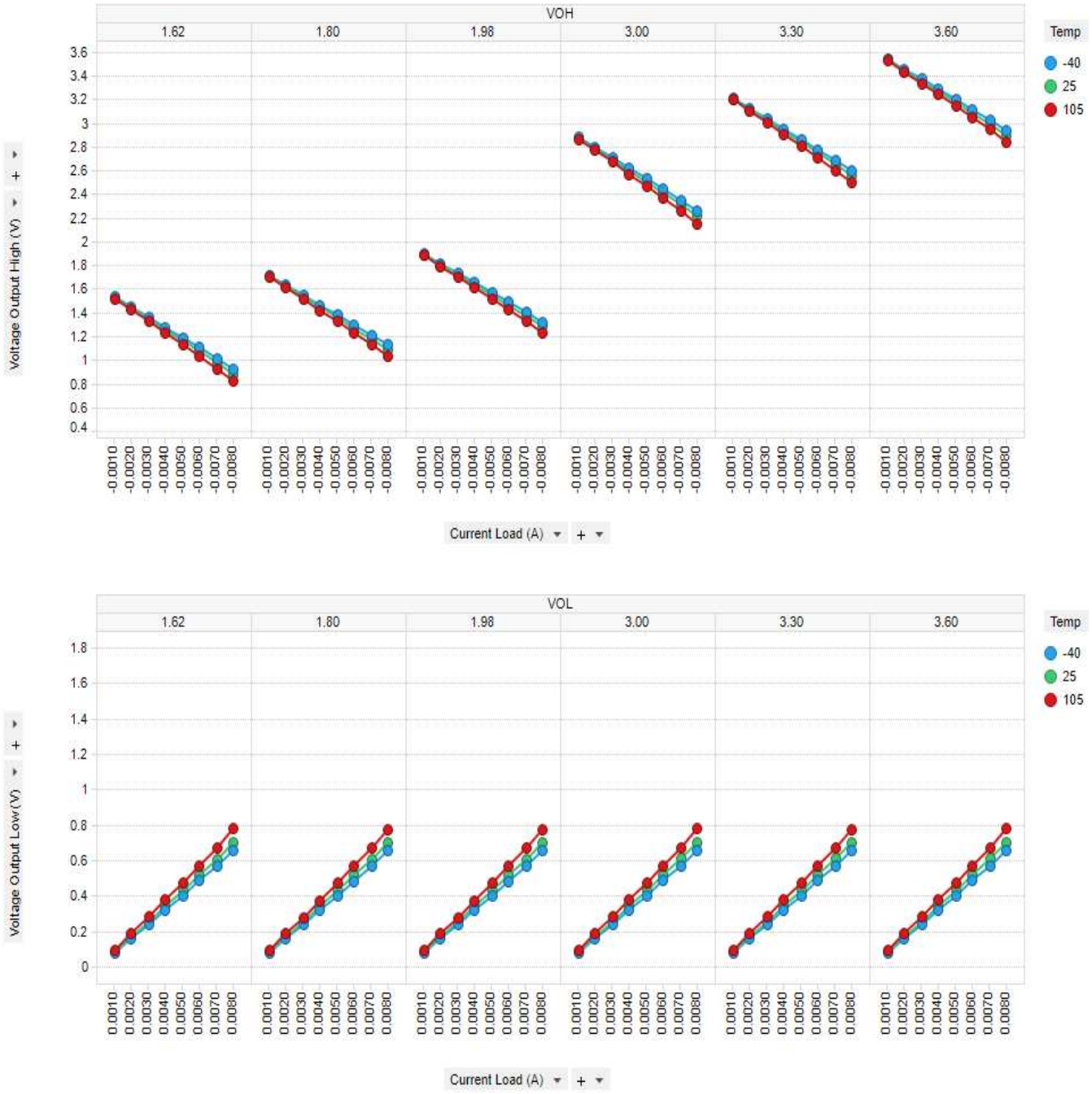

Figure 29. DP83826 Output Pin Drive Characteristics

11 Power Supply Recommendations

The DP83826 is capable of operating with a 3.3-V or 1.8-V I/O supply voltage along with an analog supply of 3.3 V. If a 3.3-V I/O supply voltage is desired, the DP83826 can also operate on a single 3.3-V power rail. An internal LDO generates all the power rails required for the device to operate. The single voltage supply simplifies the design requirements, decreases the BOM cost and the overall solution size, making the DP83826 a viable solution in a wide range of applications. The recommended power supply de-coupling network is shown below:

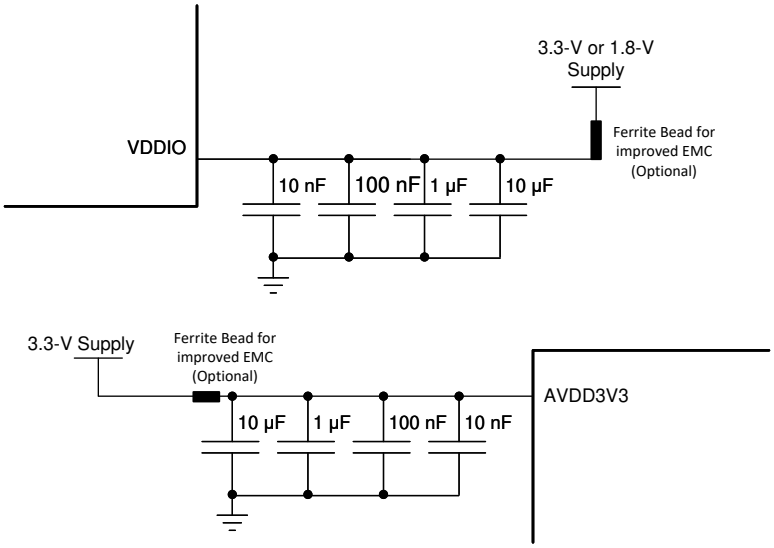

Figure 30. Power Supply Decoupling Recommendation

12 Layout

12.1 Layout Guidelines

Please see DP83826EVM.

12.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Keep all traces as short as possible. Unless mentioned otherwise, all signal traces must be 50-Ω single-ended impedance. Differential traces must be 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities causes reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

Layout Guidelines (continued)

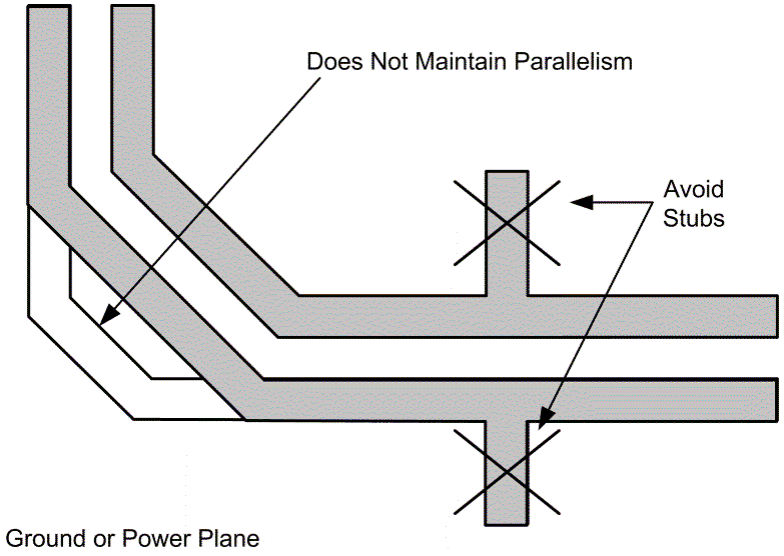

Figure 31. Differential Signal Traces

Within the differential pairs, trace lengths must be run parallel to each other and be matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All MII and RMII transmit signal traces should be length matched to each other and all MII and RMII receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

12.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Avoid breaks in return path between the signal traces at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

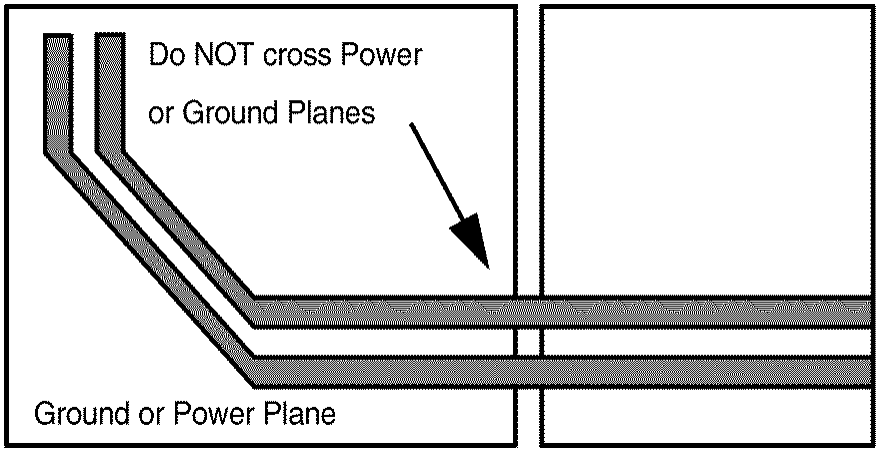

Figure 32. Differential Signal Pair and Plane Crossing

Layout Guidelines (continued)

12.1.3 Transformer Layout

There must be no metal layer running beneath the transformer. Transformers can inject noise into metal beneath them, which can affect the performance of the system. See Figure 27.

12.1.3.1 Transformer Recommendations

The following magnetics have been tested using the DP83826.

Table 106. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse electronics	HX1198FNL
	HX1188NL
	HX1188FNL

Table 107. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn ratio	±2%	1:1	-
Insertion loss	1 - 100 MHz	–1	dB
Return loss	1 - 30 MHz	–16	dB
	30 - 60 MHz	–12	dB
	60 - 80 MHz	–10	dB
Differential to common rejection ratio	1 - 50 MHz	–30	dB
	50 - 150 MHz	–20	dB
Crosstalk	30 MHz	–35	dB
	60 MHz	–30	dB
Isolation	HPOT	1500	Vrms

12.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

12.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB should be used when possible.

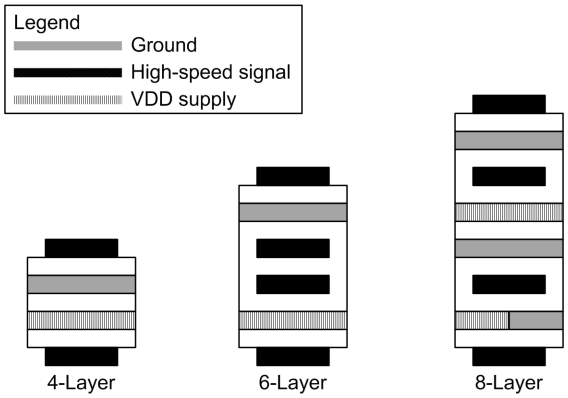

Figure 33. Recommended Layer Stack-Up

12.2 Layout Example

See the DP83826EVM for more information regarding layout.

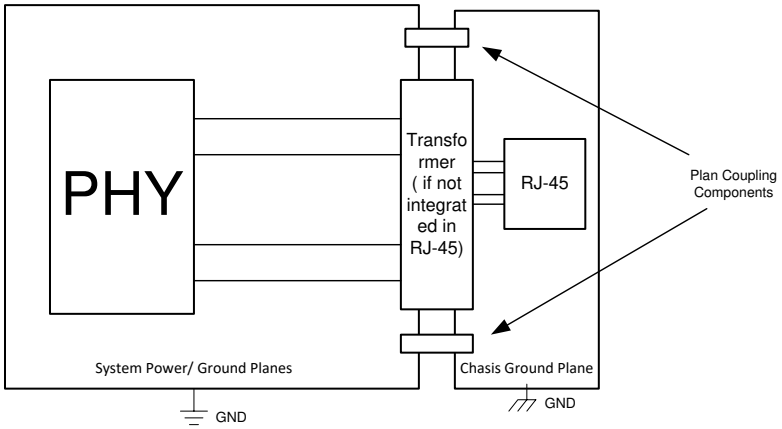

Figure 34. Layout Example

13 Device and Documentation Support

13.1 Related Documentation

For related documentation see the following:

Solving Cable Faults Challenges with TI Ethernet PHYs

Selection and specification of crystals for Texas Instruments ethernet physical layer transceivers

Chinese and English Definitions of Acronyms Related to Ethernet Products

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

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Magic Packet is a trademark of Advanced Micro Devices, Inc..

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83826ERHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	826E	Samples
DP83826ERHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	826E	Samples
DP83826IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	826I	Samples
DP83826IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	826I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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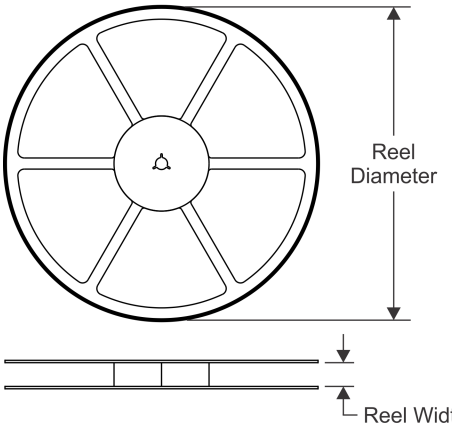
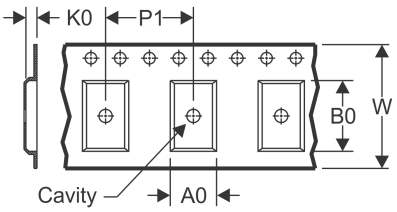
TAPE AND REEL INFORMATION

REEL DIMENSIONS

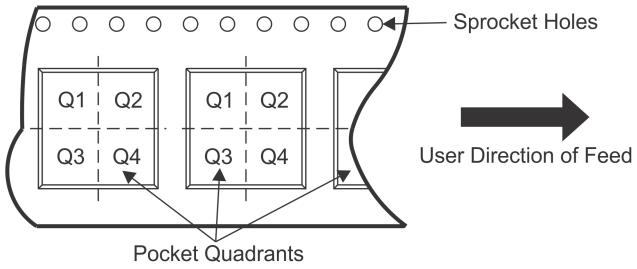


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

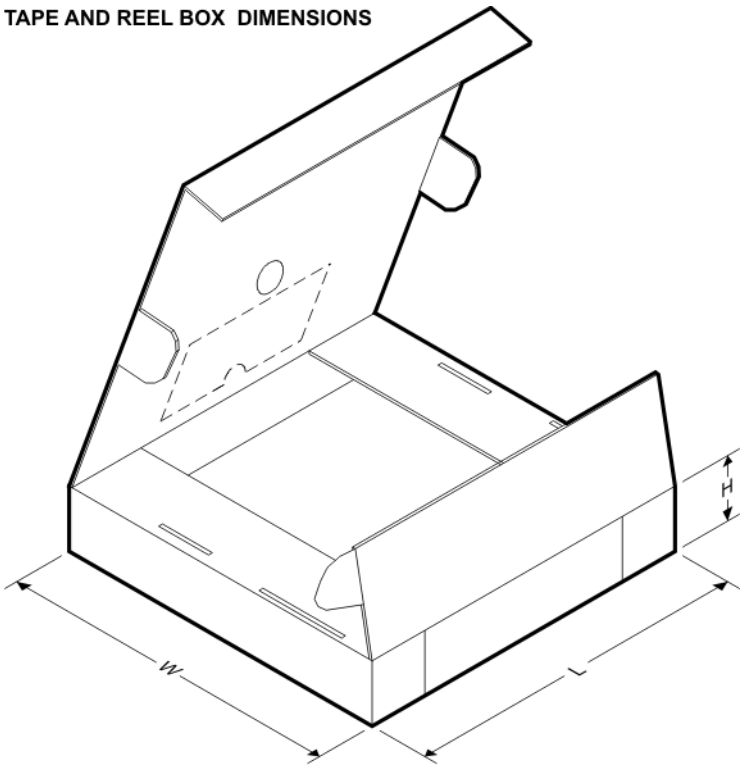
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83826ERHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826ERHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DP83826IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83826ERHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83826ERHBT	VQFN	RHB	32	250	210.0	185.0	35.0
DP83826IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83826IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

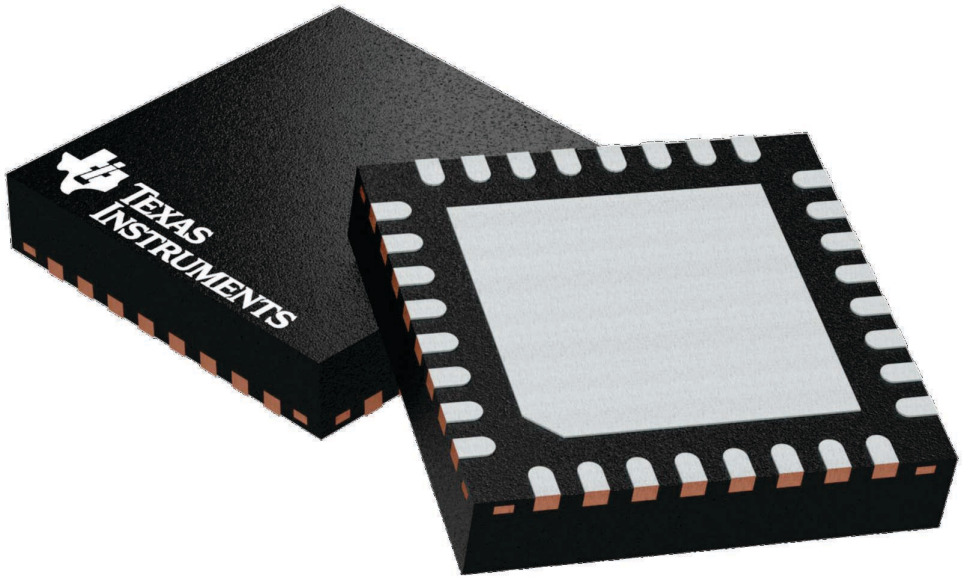
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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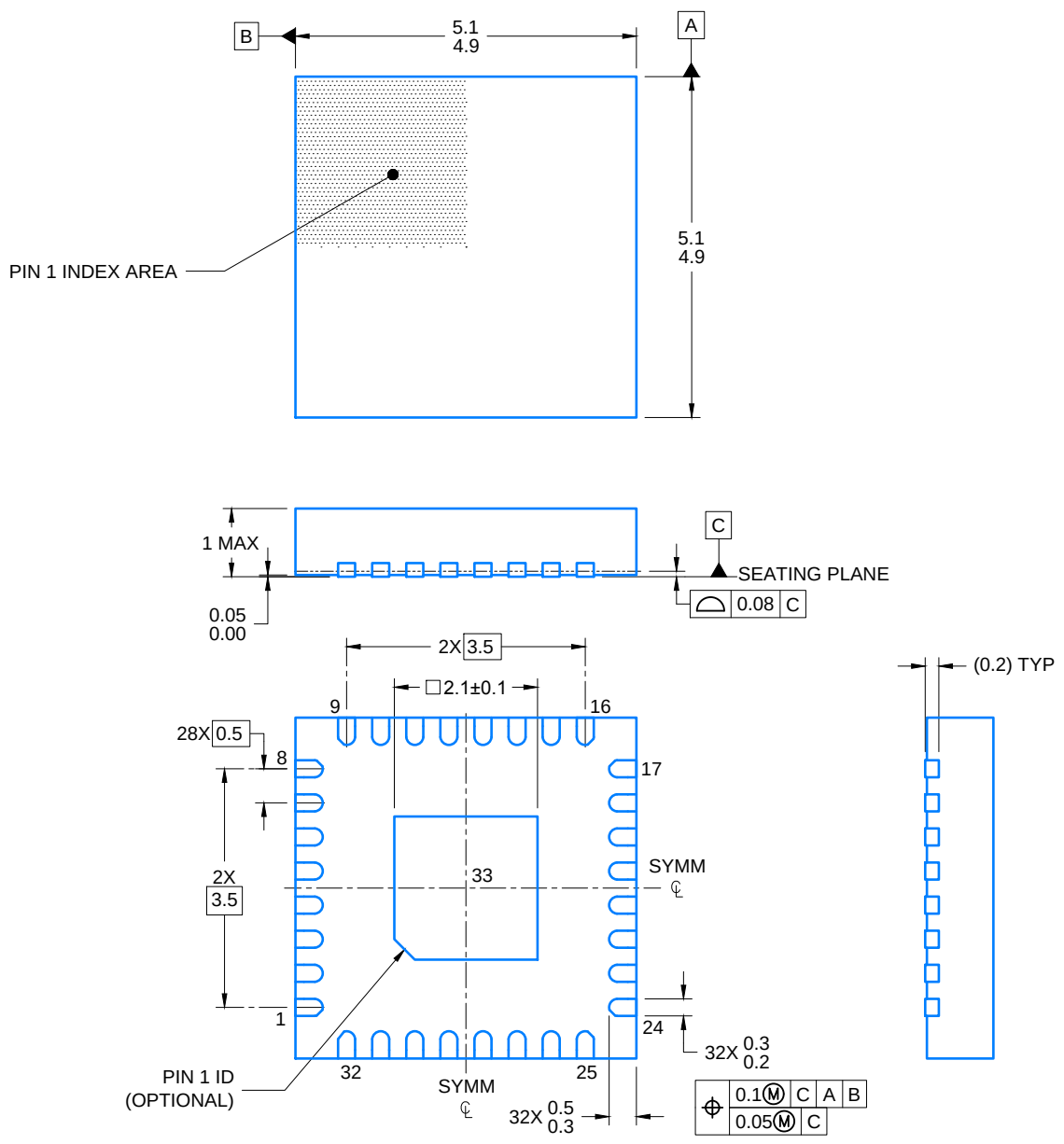
PACKAGE OUTLINE

RHB0032M

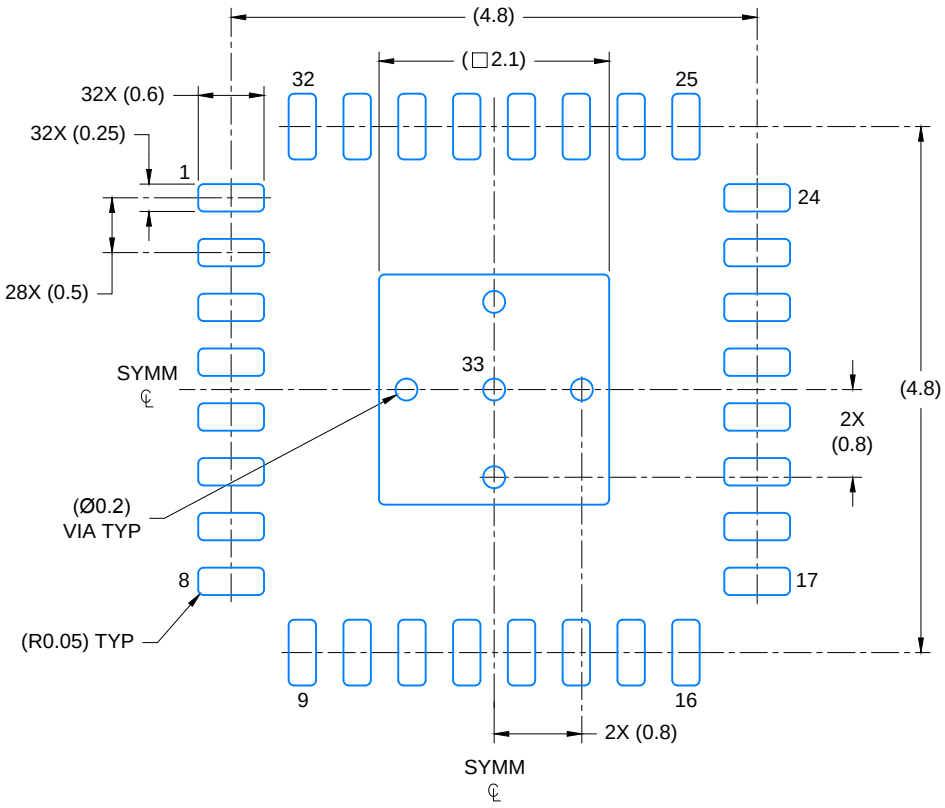
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

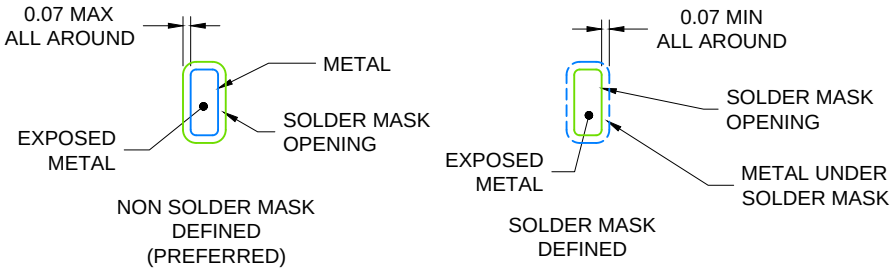


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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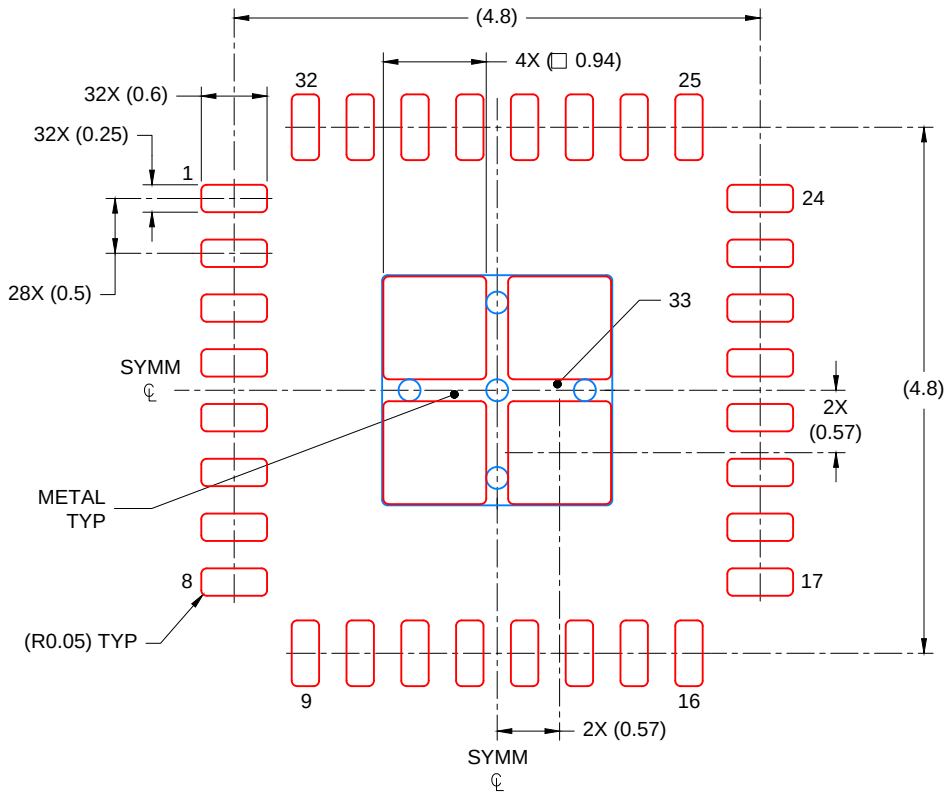
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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