DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver

1 Features

- IEEE 802.3 Compliant: 100BASE-FX, 100BASE-TX and 10BASE-T
- Low Deterministic Transmit and Receive Latency
- ±8000-V IEC 61000-4-2 ESD Protection
- Start of Frame Detect for IEEE 1588 Time Stamp
- Fast Link-Down Timing
- Auto-Crossover in Force Modes
- Operating Temperature: -40°C to 125°C
- **Key Specifications:**
  - MII / RMII / RGMII MAC Interfaces
  - Single Supply Options:
    - 1.8-V AVD < 120 mW
    - 3.3-V AVD < 220 mW
  - I/O Voltages: 3.3-V, 2.5-V and 1.8-V
  - Power Savings Features
    - Energy Efficient Ethernet (EEE) IEEE 802.3az
    - WoL (Wake-on-LAN) Support with Magic Packet Detection
    - Programmable Energy Savings Modes
  - Cable Diagnostics
  - BIST (Built-in Self-Test)
  - MDC / MDIO Interface

2 Applications

- Industrial Networks and Factory Automation
- Motor and Motion Control
- IP Network Cameras
- Building Automation

3 Description

The DP83822 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted pair cables or connect to an external fiber optic transceiver. Additionally, the DP83822 provides flexibility to connect to a MAC through a standard MII, RMII or RGMII interface.

The DP83822 offers integrated cable diagnostic tools, built-in self-test and loopback capabilities for ease of use. It supports multiple industrial buses with its low deterministic transmit and receive latency as well as fast link-down timing.

The DP83822 offers and innovative and robust approach for reducing power consumption through EEE, WoL and other programmable energy savings modes.

The DP83822 is a feature rich and pin-to-pin upgradeable option for the TLK105L and TLK106L 10/100 Mbps Ethernet PHYs.

The DP83822 comes in a QFN 32-pin 5.00-mm × 5.00-mm package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83822	WQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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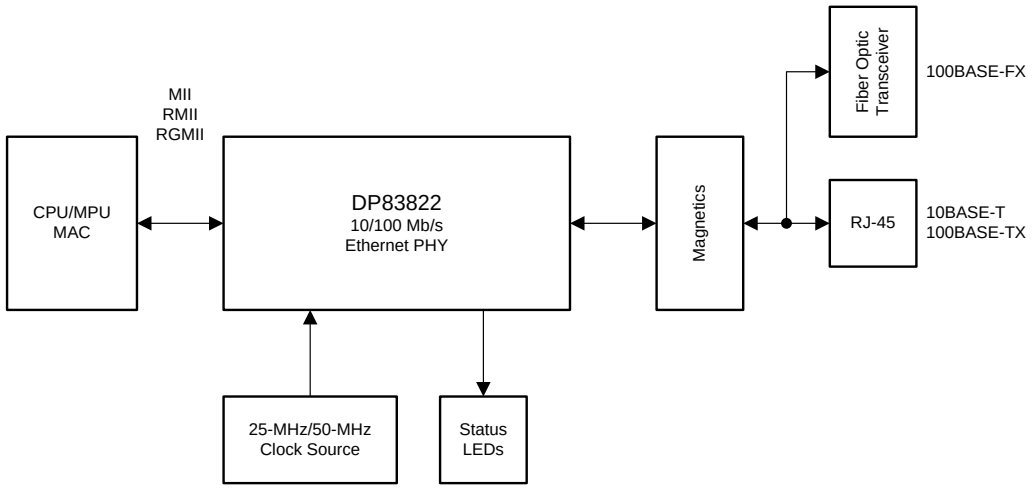
Simplified Schematic



4 Device Comparison Table

PART NUMBER	100BASE-FX SUPPORT	OPERATING TEMPERATURE
DP83822HF	Yes	-40°C to 125°C
DP83822H	No	-40°C to 125°C
DP83822IF	Yes	-40°C to 85°C
DP83822I	No	-40°C to 85°C

5 Detailed Description

5.1 Register Maps

In the register definitions under the “TYPE” heading, the following definitions apply:

COR Clear on Read

Strap Default value loads from strapping pin after reset

LH Latched high and held until read

LL Latched low and held until read

RO Read Only Access

RO/COR Read Only, Clear on Read

RO/P Read Only, Permanently set to a default value

RW Read Write access

RW/SC Read Write access, Self Clearing bit

SC Register sets on event occurrence and Self-Clears when event ends

Table 1. 0x0000 Basic Mode Control Register (BMCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reset	RW, SC	0	**PHY Software Reset:** 1 = Initiate software Reset / Reset in Progress 0 = Normal Operation Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared.
14	MII Loopback	RW	0	**MII Loopback:** 1 = MII Loopback enabled 0 = Normal Operation When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally.
13	Speed Selection	RW, Strap	1	**Speed Select:** 1 = 100 Mbps 0 = 10 Mbps When Auto-Negotiation is disabled (bit[12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected.
12	Auto-Negotiation Enable	RW, Strap	1	**Auto-Negotiation Enable:** 1 = Enable Auto-Negotiation 0 = Disable Auto-Negotiation If Auto-Negotiation is disabled, bit[8] and bit[13] of this register determine the port speed and duplex mode.
11	IEEE Power Down	RW	0	**Power Down:** 1 = IEEE Power Down 0 = Normal Operation The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set.
10	Isolate	RW	0	**Isolate:** 1 = Isolates the port from the MII with the exception of the SMI 0 = Normal Operation

Register Maps (continued)

Table 1. 0x0000 Basic Mode Control Register (BMCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
9	Restart Auto-Negotiation	RW, SC	0	**Restart Auto-Negotiation:** 1 = Restarts Auto-Negotiation 0 = Normal Operation If Auto-Negotiation is disabled (bit[12] = 0), bit[9] is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit.
8	Duplex Mode	RW, Strap	1	**Duplex Mode:** 1 = Full-Duplex 0 = Half-Duplex When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected.
7	Collision Test	RW	0	**Collision Test:** 1 = Enable COL Signal Test 0 = Normal Operation When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN.
6:0	Reserved	RO	0	Reserved

Table 2. 0x0001 Basic Mode Status Register (BMCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	100Base-T4	RO	0	**100Base-T4 Capable:** This protocol is not available. Always reads as 0.
14	100Base-TX Full-Duplex	RO	1	**100Base-TX Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 100Base-TX 0 = Device not able to perform Full-Duplex 100Base-TX
13	100Base-TX Half-Duplex	RO	1	**100Base-TX Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 100Base-TX 0 = Device not able to perform Half-Duplex 100Base-TX
12	10Base-T Full-Duplex	RO	1	**10Base-T Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 10Base-T 0 = Device not able to perform Full-Duplex 10Base-T
11	10Base-T Half-Duplex	RO	1	**10Base-T Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 10Base-T 0 = Device not able to perform Half-Duplex 10Base-T
10:7	Reserved	RO	0	Reserved
6	SMI Preamble Suppression	RO	1	**Preamble Suppression Capable:** 1 = Device able to perform SMI transaction with preamble suppressed 0 = Device not able to perform SMI transaction with preamble suppressed If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	RO	0	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process completed 0 = Auto Negotiation process not completed (either still in process, disabled or reset)
4	Remote Fault	RO, LH	0	**Remote Fault:** 1 = Remote fault condition detected 0 = No remote fault condition detected Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset.
3	Auto-Negotiation Ability	RO	1	**Auto-Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation 0 = Device is not able to perform Auto-Negotiation

Table 2. 0x0001 Basic Mode Status Register (BMCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
2	Link Status	RO, LL	0	**Link Status:** 1 = Valid link established (for either 10 Mbps or 100 Mbps operation) 0 = Link not established
1	Jabber Detect	RO, LH	0	**Jabber Detect:** 1 = Jabber condition detected 0 = No jabber condition detected This bit only has meaning for 10Base-T operation.
0	Extended Capability	RO	1	**Extended Capability:** 1 = Extended register capabilities 0 = Basic register set capabilities only

Table 3. 0x0002 PHY Identifier Register #1 (PHYIDR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Organizationally Unique Identifier Bits 21:6	RO	0010 0000 0000 0000	

Table 4. 0x0003 PHY Identifier Register #2 (PHYIDR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Organizationally Unique Identifier Bits 5:0	RO	1010 00	
9:4	Model Number	RO	10 0100	**Vendor Model Number:** The six bits of vendor model number are mapped from bits [9] to [4]
3:0	Revision Number	RO	0000	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

Table 5. 0x0004 Auto-Negotiation Advertisement Register (ANAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RW	0	**Next Page Indication:** 1 = Next Page Transfer desired 0 = Next Page Transfer not desired
14	Reserved	RO	0	Reserved
13	Remote Fault	RW	0	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault 0 = No Remote Fault detected
12	Reserved	RO	0	Reserved
11	Asymmetric Pause	RW	0	**Asymmetric Pause Support For Full-Duplex Links:** 1 = Advertise asymmetric pause ability 0 = Do not advertise asymmetric pause ability
10	Pause	RW	0	**Pause Support for Full-Duplex Links:** 1 = Advertise pause ability 0 = Do not advertise pause ability
9	100Base-T4	RO	0	**100Base-T4 Support:** 1 = Advertise 100Base-T4 ability 0 = Do not advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	RW, Strap	1	**100Base-TX Full-Duplex Support:** 1 = Advertise 100Base-TX Full-Duplex ability 0 = Do not advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	RW, Strap	1	**100Base-TX Half-Duplex Support:** 1 = Advertise 100Base-TX Half-Duplex ability 0 = Do not advertise 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	RW, Strap	1	**10Base-T Full-Duplex Support:** 1 = Advertise 10Base-T Full-Duplex ability 0 = Do not advertise 10Base-T Full-Duplex ability

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Table 5. 0x0004 Auto-Negotiation Advertisement Register (ANAR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
5	10Base-T Half-Duplex	RW, Strap	1	**10Base-T Half-Duplex Support:** 1 = Advertise 10Base-T Half-Duplex ability 0 = Do not advertise 10Base-T Half-Duplex ability
4:0	Selector Field	RW	0 0001	**Protocol Selection Bits:** Technology selector field (IEEE802.3u <00001>)

Table 6. 0x0005 Auto-Negotiation Link Partner Ability Register (ALNPAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RO	0	**Next Page Indication:** 1 = Link partner desires Next Page Transfer 0 = Link partner does not desire Next Page Transfer
14	Acknowledge	RO	0	**Acknowledge:** 1 = Link partner acknowledges reception of link code word 0 = Link partner does not acknowledge reception of link code word
13	Remote Fault	RO	0	**Remote Fault:** 1 = Link partner advertises remote fault event detection 0 = Link partner does not advertise remote fault event detection
12	Reserved	RO	0	Reserved
11	Asymmetric Pause	RO	0	**Asymmetric Pause:** 1 = Link partner advertises asymmetric pause ability 0 = Link partner does not advertise asymmetric pause ability
10	Pause	RO	0	**Pause:** 1 = Link partner advertises pause ability 0 = Link partner does not advertise pause ability
9	100Base-T4	RO	0	**100Base-T4 Support:** 1 = Link partner advertises 100Base-T4 ability 0 = Link partner does not advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	RO	0	**100Base-TX Full-Duplex Support:** 1 = Link partner advertises 100Base-TX Full-Duplex ability 0 = Link partner does not advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	RO	0	**100Base-TX Half-Duplex Support:** 1 = Link partner advertises 100Base-TX Half-Duplex ability 0 = Link partner does not advertise 100Base-TX Half-Duplex ability
6	10Base-T Full-Duplex	RO	0	**10Base-T Full-Duplex Support:** 1 = Link partner advertises 10Base-T Full-Duplex ability 0 = Link partner does not advertise 10Base-T Full-Duplex ability
5	10Base-T Half-Duplex	RO	0	**10Base-T Half-Duplex Support:** 1 = Link partner advertises 10Base-T Half-Duplex ability 0 = Link partner does not advertise 10Base-T Half-Duplex ability
4:0	Selector Field	RO	0 0000	**Protocol Selection Bits:** Technology selector field (IEEE802.3 <00001>)

Table 7. 0x0006 Auto-Negotiation Expansion Register (ANER)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RO	0	Reserved
4	Parallel Detection Fault	RO, LH	0	**Parallel Detection Fault:** 1 = A fault has been detected during the parallel detection process 0 = No fault detected
3	Link Partner Next Page Able	RO	0	**Link Partner Next Page Ability:** 1 = Link partner is able to exchange next pages 0 = Link partner is not able to exchange next pages
2	Local Device Next Page Able	RO	1	**Next Page Ability:** 1 = Local device is able to exchange next pages 0 = Local device is not able to exchange next pages
1	Page Received	RO, LH	0	**Link Code Word Page Received:** 1 = A new page has been received 0 = A new page has not been received

Table 7. 0x0006 Auto-Negotiation Expansion Register (ANER) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
0	Link Partner Auto-Negotiation Able	RO	0	**Link Partner Auto-Negotiation Ability:** 1 = Link partner supports Auto-Negotiation 0 = Link partner does not support Auto-Negotiation

Table 8. 0x0007 Auto-Negotiation Next Page Register (ANNPTR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RW	0	**Next Page Indication:** 1 = Advertise desire to send additional next pages 0 = Do not advertise desire to send additional next pages
14	Reserved	RO	0	Reserved
13	Message Page	RW	1	**Message Page:** 1 = Current page is a message page 0 = Current page is an unformatted page
12	Acknowledge 2	RW	0	**Acknowledge2:** 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	RO	0	**Toggle:** 1 = Toggle bit in previously transmitted Link Code Word was 0 0 = Toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	RW	000 0000 0001	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

Table 9. 0x0008 Auto-Negotiation Link Partner Ability Next Page Register (ANLNPTR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RO	0	**Next Page Indication:** 1 = Advertise desire to send additional next pages 0 = Do not advertise desire to send additional next pages
14	Acknowledge	RO	0	**Acknowledge:** 1 = Link partner acknowledges reception of link code word 0 = Link partner does not acknowledge reception of link code work
13	Message Page	RO	0	**Message Page:** 1 = Current page is a message page 0 = Current page is an unformatted page
12	Acknowledge 2	RO	0	**Acknowledge2:** 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	RO	0	**Toggle:** 1 = Toggle bit in previously transmitted Link Code Word was 0 0 = Toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.

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Table 9. 0x0008 Auto-Negotiation Link Partner Ability Next Page Register (ANLNPTR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
10:0	Message/ Unformatted Field	RO	0 0000 0001	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

Table 10. 0x0009 Control Register #1 (CR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Reserved	RO	0	Reserved
9	RMII Enhanced Mode	RW	0	**RMII Enhanced Mode:** 1 = Enable RMII Enhanced Mode 0 = RMII operated in normal mode In normal RMII mode, if the line is not idle, CRS_DV goes high. As soon as the False Carrier is detected, RX_ER is asserted and RXD is set to "2" (0010). This situation remains for the duration of the receive event. While in enhanced mode, CRS_DV is disqualified and de-asserted when the False Carrier is detected. This status also remains for the duration of the receive event. In addition, in normal mode, the start of the packet is intact. Each symbol error is indicatied by setting RX_ER high. The data on RXD is replaced with "1" starting with the first symbol error. While in enhanced mode, the CRS_DV is de-asserted with the first symbol error.
8	TDR Auto-Run	RW	0	**TDR Auto-Run at Link Down:** 1 = Enable execution of TDR procedure after link down event 0 = Disable automatic execution of TDR
7	Link Loss Recovery	RW	0	**Link Loss Recovery:** 1 = Enable Link Loss Recovery mechanism 0 = Normal Link Loss operation This mode allows recovery from short interference and continue to hold the link up for a period of additional mSec until the short interference is gone and the signal is OK. Under Normal Link Loss operation, Link status will go down approximately 250µs from signal loss.
6	Fast Auto MDIX	RW	0	**Fast Auto-MDIX:** 1 = Enable Fast Auto-MDIX 0 = Normal Auto-MDIX If both link partners are configured to work in Force 100Base-TX mode (Auto-Negotiation disabled), this mode enables Automatic MDI/MDIX resolution in a shortened time.
5	Robust Auto MDIX	RW	0	**Robust Auto-MDIX:** 1 = Enable Robust Auto-MDIX 0 = Disable Auto-MDIX If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. When the DP83822 is strapped for 100 Mbps operation with Auto-MDIX capabilities, Robust Auto-MDIX will be automatically set to aid in MDI/MDIX resolution and deadlock prevention.
4	Fast Auto-Negotiation Enable	RW	0	**Fast Auto-Negotiation Enable:** 1 = Enable Fast Auto-Negotiation 0 = Disable Fast Auto-Negotiation The PHY Auto-Negotiaties using timer setting according to Fast Auto-Negotiation Select bits (bits[3:2] in this register).

Table 10. 0x0009 Control Register #1 (CR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3:2	Fast Auto-Negotiation Select	RW	0	**Fast Auto-Negotiation Select Bits:** Adjusting these bits reduces the time it takes to Auto-Negotiate between two PHYs. In Fast Auto-Negotiation, both PHYs should be set to the same configuration. These 2 bits define the duration for each state of the Auto-Negotiation process according to the table above. The new duration time must be enabled by setting "Fast Auto Negotiation Enable" (bit [4] of this register). Note: Using this mode in cases where both link partners are not configured to the same Fast-Autonegotiation configuration might produce scenarios with unexpected behavior.

Fast Auto-Negotiation Select	Break Link Timer	Link Fail Inhibit Timer	Auto-Negotitation Wait Timer
<00>	80	50	35
<01>	120	75	50
<10>	240	150	100
<11>	NA	NA	NA

BIT	NAME	TYPE	DEFAULT	FUNCTION
1	Fast RX_DV Detection	RW	0	**Fast RX_DV Detection:** 1 = Enable Fast RX_DV detection 0 = Diable Fast RX_DV detection When Fast RX_DV is enabled, RX_DV will assert high on receive packet due to detection of the /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated. In normal mode, RX_DV will only be asserted after detection of /JK/.
0	Reserved	RO	0	**Reserved**

Table 11. 0x000A Control Register #2 (CR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	100Base-TX Force Far-End Link drop	RW	0	**100Base-TX Force Far-End Link Drop:** Writing a 1 asserts the 100Base-TX Force Far-End link drop mode. In this mode (only valid for 100 Mbps), the PHY disables the TX upon link drop to allow the far-end peer to drop its link as well, thus allowing both link partners to be aware of the system link failure. This mode exceeds the standard definition of force 100 Mbps.
14	100Base-FX Enable	RW, Strap	0	**100Base-FX Enable:** 1 = 100Base-FX mode enabled 0 = 100Base-FX mode disabled
13:7	Reserved	RW	00 0001 0	**Reserved**
6	Fast Link-Up in Parallel Detect	RW	0	**Fast Link-Up in Parallel Detect Mode:** 1 = Enable Fast Link-Up time during Paralled Detection 0 = Normal Parallel Detection Link establishment In Fast Auto MDIX and in Robust Auto-MDIX modes (bit[6] and bit[5] in register CR1), this bit is automatically set.
5	Extended Full-Duplex Ability	RW	0	**Extended Full-Duplex Ability:** 1 = Enable Extended Full-Duplex Ability 0 = Diable Extended Full-Duplex Ability In Extended Full-Duplex ability, when the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex. When disabled, the decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification.
4	Enhanced LED Link	RW	0	**Enhanced LED Link:** 1 = LED ON only when link is 100Base-TX Full-Duplex mode 0 = LED ON when link is established In Enhanced LED Link mode, TX/RX BLINK on activity is disabled for this LED pin. LED will only indicate LINK for established 100Base-TX Full-Duplex links.

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Table 11. 0x000A Control Register #2 (CR2) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3	Isolate MII in 100Base-TX Half-Duplex or 10Base-T	RW	0	**Isolate MII:** 1 = Isolate MII Enabled 0 = Normal MII output operation In Isolate MII, MII outputs are isolated when Half-Duplex link established for 100Base-TX or when Half-Duplex or Full-Duplex link established for 10Base-T.
2	RX_ER During IDLE	RW	1	**Detection of Receive Symbol Error During IDLE State:** 1 = Enable detection of Receive symbol error during IDLE state 0 = Disable detection of Receive symbol error during IDLE state
1	Odd-Nibble Detection Disable	RW	0	**Detection of Transmit Error:** 1 = Disable detection of transmit error in odd-nibble boundary 0 = Enable detection of transmit error in odd-nibble boundary Detection of odd-nibble will extend TX_EN by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle
0	RMII Receive Clock	RW	0	**RMII Receive Clock:** 1 = RMII Data (RXD[1:0]) is sampled and referenced to RX_CLK 0 = RMII Data (RXD[1:0]) is sampled and referenced to XI

Table 12. 0x000B Control Register #3 (CR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RW	0001 0	**Reserved**
10	Descrambler Fast Link Down Mode	RW	0	**Descrambler Fast Link Drop:** 1 = Drop the link on descrambler link loss 0 = Do not drop the link on descrambler link loss This option can be enabled in parallel to the other fast link down modes in bits[3:0].
9:7	Reserved	RW	0	**Reserved**
6	Polarity Swap	RW	0	**Polarity Swap:** 1 = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0 = Normal polarity **Port Mirror Function:** To enable port mirroring, set this bit and bit [5] high.
5	MDI/MDIX Swap	RW	0	**MDI/MDIX Swap:** 1 = Swap MDI pairs (Receive on TD pair, Transmit on RD pair) 0 = MDI pairs normal (Receive on RD pair, Transmit on TD pair) **Port Mirror Function:** To enable port mirroring, set this bit and bit[6] high.
4	Reserved	RW	0	**Reserved**
3:0	Fast Link Down Mode	RW	0000	**Fast Link Down Modes:** **Bit 3** Drop the link based on **RX Error count** of the MII interface. When a predefined number of 32 RX Error occurences in a 10µs interval is reached, the link will be dropped. **Bit 2** Drop the link based on **MLT3 Error count** (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in a 10µs interval is reached, the link will be dropped. **Bit 1** Drop the link based on **Low SNR Threshold**. When a predefined number of 20 Threshold crossing occurences in a 10µs interval is reached, the link will be dropped. **Bit 0** Drop the link based on **Signal/Energy Loss** indication. When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10µs. The Fast Link Down function is an OR of all 5 options (bit[10] and bits[3:0]), the designer can enable any combination of these conditions.

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Table 13. 0x000D Register Control Register (REGCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Extended Register Command	RW	0	**Extended Register Command:** 00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	Reserved	RO	0	**Reserved**
4:0	DEVAD	RW	0	**Device Address:** Bits[4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83822 uses the vendor specific DEVAD [4:0] = "11111" for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

Table 14. 0x000E Data Register (ADDAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Address/Data	RW	0	If REGCR register bits[15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

Table 15. 0x000F Fast Link Down Status Register (FLDS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:9	Reserved	RO	0	**Reserved**
8:4	Fast Link Down Status	RO, LH	0	**Fast Link Down Status:** 1 0000 = Descrambler Loss Sync 0 1000 = RX Errors 0 0100 = MLT3 Errors 0 0010 = SNR Level 0 0001 = Signal/Energy Lost Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled)
3:0	Reserved	RO	0	**Reserved**

Table 16. 0x0010 PHY Status Register (PHYSTS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	MDI/MDIX Mode	RO	0	**MDI/MDIX Mode Status:** 1 = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair) 0 = MDI Pairs normal (Receive on RD pair, Transmit on TD pair)
13	Receive Error Latch	RO, LH	0	**Receive Error Latch:** 1 = Receive error event has occurred 0 = No receive error event has occurred Receive error event has occured since last read of RECR register (address 0x0015). This bit will be cleared upon a read of the RECR register.
12	Polarity Status	RO, LH	0	**Polarity Status**: 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit[4] in the 10BTSCR register (address 0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register.

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Table 16. 0x0010 PHY Status Register (PHYSTS) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
11	False Carrier Sense Latch	RO, LH	0	**False Carrier Sense Latch:** 1 = False Carrier event has occurred 0 = No False Carrier event has occurred False Carrier event has occurred since last read of FCSCR register (address 0x0014). This bit will be cleared upon a read of the FCSR register.
10	Signal Detect	RO, LL	0	**Signal Detect:** Active high 100Base-TX unconditional Signal Detect indication from PMD **Note:** During EEE_LPI the value of this register bit should be ignored
9	Descrambler Lock	RO, LL	0	**Descrambler Lock:** Active high 100Base-TX Descrambler Lock indication from PMD **Note:** During EEE_LPI the value of this register bit should be ignored
8	Page Received	RO	0	**Link Code Word Page Received:** 1 = A new Link Code Word Page has been received 0 = Link Code Word Page has not been received This bit is a duplicate of Page Received (bit[1]) in the ANER register and it is cleared on read of the ANER register (address 0x0006).
7	MII Interrupt	RO, LH	0	**MII Interrupt Pending:** 1 = Indicates that an internal interrupt is pending 0 = No interrupt pending Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR will clear this interrupt bit indication.
6	Remote Fault	RO	0	**Remote Fault:** 1 = Remote Fault condition detected 0 = No Remote Fault condition detected Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation. Cleared on read of BMSR register (address 0x0001) or by reset.
5	Jabber Detect	RO	0	**Jabber Detection:** 1 = Jabber condition detected 0 = No Jabber This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register.
4	Auto-Negotiation Status	RO	0	**Auto-Negotiation Status:** 1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete
3	MII Loopback Status	RO	0	**MII Loopback Status:** 1 = Loopback enabled 0 = Normal operation
2	Duplex Status	RO	0	**Duplex Status:** 1 = Full-Duplex mode 0 = Half-Duplex mode
1	Speed Status	RO	0	**Speed Status:** 1 = 10 Mbps mode 0 = 100 Mbps mode
0	Link Status	RO	0	**Link Status:** 1 = Valid link established (for either 10 Mbps or 100 Mbps) 0 = No link established This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register.

Table 17. 0x0011 PHY Specific Control Register (PHYSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Disable PLL	RW	0	**Disable PLL:** 1 = Disable internal clocks circuitry 0 = Normal operation **Note:** clock circuitry can be disabled only in IEEE power down mode.
14	Power Save Mode Enable	RW	0	**Power Save Mode Enable:** 1 = Enable power save modes 0 = Normal operation
13:12	Power Save Modes	RW	00	**Power Saving Modes Selection Field:** Power Save Mode Enable (bit[14]) must be set to '1' for power save modes to be enabled.

Power Mode	Name	Description
<00>	Normal	Normal operation mode. PHY is fully functional.
<01>	Reserved	Reserved
<10>	Active Sleep	Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
<11>	Passive Sleep	Low Power Passive Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. Automatic power-up is done when link partner is detected.

11	Scrambler Bypass	RW	0	**Scrambler Bypass:** 1 = Scrambler bypass enabled 0 = Scrambler bypass disabled
10	Reserved	RW	0	**Reserved**
9:8	Loopback FIFO Depth	RW	01	**Far-End Loopback FIFO Depth:** 00 = 4 nibbles FIFO 01 = 5 nibbles FIFO 10 = 6 nibbles FIFO 11 = 8 nibbles FIFO This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles.
7:5	Reserved	RO	0	**Reserved**
4	COL Full-Duplex Enable	RW	0	**Collision in Full-Duplex Mode:** 1 = Enable Collision generation signaling in Full-Duplex mode 0 = Disable Collision in Full-Duplex mode **Note:** When in Half-Duplex mode, Collision will always be active.
3	Interrupt Polarity	RW	1	**Interrupt Polarity:** 1 = Normal operation is 1 logic and during interrupt is 0 logic 0 = Normal operation is 0 logic and during interrupt is 1 logic
2	Test Interrupt	RW	0	**Test Interrupt:** 1 = Generate an interrupt 0 = Do not generate interrupt Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set.
1	Interrupt Enable	RW	0	**Interrupt Enable:** 1 = Enable event based interrupts 0 = Disable event based interrupts Enable interrupt dependent on the event enables in the MISR register (address 0x0012).

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Table 17. 0x0011 PHY Specific Control Register (PHYSCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
0	Interrupt Output Enable	RW	0	**Interrupt Output Enable:** 1 = INT/PWDN_N is an interrupt output 0 = INT/PWDN_N is a Power Down pin Enable active low interrupt events via the INT/PWDN_N pin by configuring the INT/PWDN_N pin as an output.

Table 18. 0x0012 MII Interrupt Status Register #1 (MISR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Link Quality Interrupt	RO, LH	0	**Change of Link Quality Status Interrupt:** 1 = Change of link quality when link is ON 0 = Link quality is Good
14	Energy Detect Interrupt	RO, LH	0	**Change of Energy Detection Status Interrupt:** 1 = Change of energy detected 0 = No change of energy detected
13	Link Status Changed Interrupt	RO, LH	0	**Change of Link Status Interrupt:** 1 = Change of link status interrupt is pending 0 = No change of link status
12	Speed Changed Interrupt	RO, LH	0	**Change of Speed Status Interrupt:** 1 = Change of speed status interrupt is pending 0 = No change of speed status
11	Duplex Mode Changed Interrupt	RO, LH	0	**Change of Duplex Status Interrupt:** 1 = Change of duplex status interrupt is pending 0 = No change of duplex status
10	Auto-Negotiation Completed Interrupt	RO, LH	0	**Auto-Negotiation Complete Interrupt:** 1 = Auto-Negotiation complete interrupt is pending 0 = No Auto-Negotiation complete event is pending
9	False Carrier Counter Half-Full Interrupt	RO, LH	0	**False Carrier Counter Half-Full Interrupt:** 1 = False Carrier HF interrupt is pending 0 = False Carrier HF event is not pending False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending.
8	Receive Error Counter Half-Full Interrupt	RO, LH	0	**Receiver Error Counter Half-Full Interrupt:** 1 = Receive Error HF interrupt is pending 0 = Receive Error HF event is not pending Receiver Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending.
7	Link Quality Interrupt Enable	RW	0	**Enable** interrupt on change of link quality
6	Energy Detect Interrupt Enable	RW	0	**Enable** interrupt on change of energy detection
5	Link Status Changed Enable	RW	0	**Enable** interrupt on change of link status
4	Speed Changed Interrupt Enable	RW	0	**Enable** Interrupt on change of speed status
3	Duplex Mode Changed Interrupt Enable	RW	0	**Enable** Interrupt on change of duplex status
2	Auto-Negotiation Completed Enable	RW	0	**Enable** Interrupt on Auto-negotiation complete event
1	False Carrier HF Enable	RW	0	**Enable** Interrupt on False Carrier Counter Register half-full event
0	Receive Error HF Enable	RW	0	**Enable** Interrupt on Receive Error Counter Register half-full event

Table 19. 0x0013 MII Interrupt Status Register #2 (MISR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	EEE Error Interrupt	RO, LH	0	**Energy Efficient Ethernet Error Interrupt:** 1 = EEE error has occurred 0 = EEE error has not occurred
14	Auto-Negotiation Error Interrupt	RO, LH	0	**Auto-Negotiation Error Interrupt:** 1 = Auto-Negotiation error interrupt is pending 0 = No Auto-Negotiation error even pending

Table 19. 0x0013 MII Interrupt Status Register #2 (MISR2) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
13	Page Received Interrupt	RO, LH	0	**Page Receiver Interrupt:** 1 = Page has been received 0 = Page has not been received
12	Loopback FIFO OF/UF Event Interrupt	RO, LH	0	**Loopback FIFO Overflow/Underflow Event Interrupt:** 1 = FIFO Overflow/Underflow event interrupt pending 0 = No FIFO Overflow/Underflow event pending
11	MDI Crossover Change Interrupt	RO, LH	0	**MDI/MDIX Crossover Status Change Interrupt:** 1 = MDI crossover status changed interrupt is pending 0 = MDI crossover status has not changed
10	Sleep Mode Interrupt	RO, LH	0	**Sleep Mode Event Interrupt:** 1 = Sleep mode event interrupt is pending 0 = No Sleep mode event pending
9	Polarity Changed Interrupt / WoL Packet Received Interrupt	RO, LH	0	**Polarity Change Interrupt / WoL Packet Received Interrupt:** 1 = Data polarity interrupt pending / WoL packet was recieved 0 = No Data polarity pending / No WoL packet received
8	Jabber Detect Interrupt	RO, LH	0	**Jabber Detect Event Interrupt:** 1 = Jabber detect even interrupt pending 0 = No Jabber detect event pending
7	EEE Error Interrupt Enable	RW	0	**Enable** interrupt on EEE Error
6	Auto-Negotiation Error Interrupt Enable	RW	0	**Enable** Interrupt on Auto-Negotiation error event
5	Page Received Interrupt Enable	RW	0	**Enable** Interrupt on page receive event
4	Loopback FIFO OF/UF Enable	RW	0	**Enable** Interrupt on loopback FIFO Overflow/Underflow event
3	MDI Crossover Change Enable	RW	0	**Enable** Interrupt on change of MDI/X status
2	Sleep Mode Event Enable	RW	0	**Enable** Interrupt on sleep mode event
1	Polarity Changed / WoL Packet Enable	RW	0	**Enable** Interrupt on change of polarity status
0	Jabber Detect Enable	RW	0	**Enable** Interrupt on Jabber detection event

Table 20. 0x0014 False Carrier Sense Counter Register (FCSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Reserved	RO	0	**Reserved**
7:0	False Carrier Event Counter	RO, COR	0	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

Table 21. 0x0015 Receive Error Count Register (RECR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Receive Error Counter	RO, COR	0	**RX_ER Counter:** When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

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Table 22. 0x0016 BIST Control Register (BISCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	BIST Error Counter Mode	RW	0	**BIST Error Counter Mode:** 1 = Continuous mode 0 = Single mode Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again. When in Single mode, if the BIST Error Counter reaches its max value, PRBS checker will stop counting.
13	PRBS Checker	RW	0	**PRBS Checker:** 1 = PRBS Checker Enabled 0 = PRBS Checker Disabled When PRBS checker is enabled, DP83822 will check PRBS data received.
12	Packet Generation Enable	RW	0	**Packet Generation Enable:** 1 = Enable packet generator with PRBS data 0 = Disable packet generator
11	PRBS Checker Lock/Sync	RO	0	**PRBS Checker Lock/Sync Indication:** 1 = PRBS checker is locked and synced on received bit stream 0 = PRBS checker is not locked
10	PRBS Checker Sync Loss	RO, LH	0	**PRBS Checker Sync Loss Indication:** 1 = PRBS checker has lost sync 0 = PRBS checker has not lost sync
9	Packet Generator Status	RO	0	**Packet Generation Status Indication:** 1 = Packet Generator is active and generating packets 0 = Packet Generator is off
8	Power Mode	RO	1	**Sleep Mode Indication:** 1 = Indicates that the PHY is in normal power mode 0 = Indicates that the PHY is in one of the sleep modes
7	Reserved	RO	0	**Reserved**
6	Transmit in MII Loopback	RW	0	**Transmit Data in MII Loopback Mode (valid only at 100 Mbps):** 1 = Enable transmission 0 = Disable transmission When enabled, data received from the MAC on the TX pins will be routed to the MDI in parallel to the MII loopback (to RX pins). This bit may be set only in MII Loopback mode - setting bit[14] in in BMCR register (address 0x0000). When disabled, data from the MAC is not transmitted to the MDI.
5	Reserved	RO	0	**Reserved**
4:0	Loopback Mode	RW	0	**Loopback Mode Select:** The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83822 digital and analog data paths **Near-end Loopback** 00001 = PCS Input Loopback 00010 = PCS Output Loopback 00100 = Digital Loopback 01000 = Analog Loopback (requires 100-Ω termination) **Far-end Loopback** 10000 = Reverse Loopback

Table 23. 0x0017 RMII and Status Register (RCSR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RO	0	**Reserved**
12	RGMII RX Clock Shift	RW	0	**RGMII RX Clock Shift:** 1 = Receive path internal clock shift is enabled 0 = Receive path internal clock shift is disabled When enabled, receive path internal clock (RX_CLK) is delayed by 3.5ns relative to recieve data. When disabled, data and clock are in align mode.

Table 23. 0x0017 RMII and Status Register (RCSR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
11	RGMII TX Clock Shift	RW	0	**RGMII TX Clock Shift:** 1 = Transmit path internal clock shift is disabled 0 = Transmit path internal clock shift is enabled When enabled, transmit path internal clock (TX_CLK) is delayed by 3.5ns relative to transmit data.
10	RGMII TX Synced	RW	0	**RGMII TX Clock Sync:** 1 = PHY and MAC share same clock reference 0 = PHY operates from same or independent clock source as MAC This mode, when enabled, reduces latency since both MAC and PHY are synchronized to the same clock source. This mode can also be used when enabling the PHY Clock Output by connecting the MAC to the PHY Output Clock.
9	RGMII Mode	RW, Strap	0	**RGMII Mode Enable:** 1 = Enable RGMII mode of operation 0 = Mode determined by bit[5]
8	RMII TX Clock Shift	RW	0	**RMII TX Clock Shift:** 1 = Transmit path internal clock shift is enabled 0 = Transmit path internal clock shift is disabled
7	RMII Clock Select	RW, Strap	0	**RMII Reference Clock Select:** Strap XI_50 determines the clock reference requirement. 1 = 50-MHz clock reference, CMOS-level oscillator 0 = 25-MHz clock reference, crystal or CMOS-level oscillator
6	RMII Recovered Clock Async FIFO Bypass	RW	1	**RMII Recovered Clock Async FIFO Bypass:** 1 = Bypass Asynchronous FIFO 0 = Normal operation When in RMII Recovered Clock mode, the asynchronous FIFO can be bypassed to reduce the receive path latency within the DP83822.
5	RMII Mode	RW	0	**RMII Mode Enable:** 1 = Enable RMII mode of operation 0 = Enable MII mode of operation
4	RMII Revision Select	RW	0	**RMII Revision Select:** 1 = RMII revision 1.0 0 = RMII revision 1.2 RMII revision 1.0, CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet. RMII revision 1.2, CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS.
3	RMII Overflow Status	RO, COR	0	**RX FIFO Overflow Status:** 1 = Normal 0 = Overflow detected
2	RMII Underflow Status	RO, COR	0	**RX FIFO Underflow Status:** 1 = Normal 0 = Underflow detected
1:0	Receive Elasticity Buffer Size	RW	01	**Receive Elasticity Buffer Size:** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50-MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for ±100ppm), divide the packet lengths by 2). 00 = 14 bit tolerance (up to 16800 byte packets) 01 = 2 bit tolerance (up to 2400 byte packets) 10 = 6 bit tolerance (up to 7200 byte packets) 11 = 10 bit tolerance (up to 12000 byte packets)

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Table 24. 0x0018 LED Control Register (LEDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10:9	Blink Rate	RW	10	**LED_0 Blinking Rate (ON/OFF duration):** 00 = 20Hz (50 ms) 01 = 10Hz (100 ms) 10 = 5Hz (200 ms) 11 = 2Hz (500 ms)
8	Reserved	RW	0	**Reserved**
7	LED_0 Polarity	RW, Strap	0	**LED_0 Link Polarity Setting:** 1 = Active High polarity setting 0 = Active Low polarity setting LED_0 polarity defined by strapping value of this pin. This register allows for override of this strap value.
6:5	Reserved	RW	0	**Reserved**
4	Drive LED_0	RW	0	**Drive Link LED_0 Select:** 1 = Drive value of ON/OFF bit[1] onto LED_0 output pin 0 = Normal operation
3:2	Reserved	RW	0	**Reserved**
1	LED_0 ON/OFF Setting	RW	0	Value to force LED_0 output
0	Reserved	RW	0	**Reserved**

Table 25. 0x0019 PHY Control Register (PHYCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Auto MDI/X Enable	RW, Strap	0	**Auto-MDIX Enable:** 1 = Enable Auto-Negotiation Auto-MDIX capability 0 = Disable Auto-Negotiation Auto-MDIX capability
14	Force MDI/X	RW	0	**Force MDIX:** 1 = Force MDI pairs to cross (MDIX) 0 = Normal operation (MDI) When Force MDI/X is enabled, receive data is on the TD pair and transmit data is on the RD pair. When disabled, receive data is on the RD pair and transmit data is on the TD pair.
13	Pause RX Status	RO	0	**Pause Receive Negotiation Status:** Indicates that pause receive should be enabled in the MAC. Based on bits[11:10] in ANAR register and bits[11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, "Pause Resolution", only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause TX Status	RO	0	**Pause Transmit Negotiated Status:** Indicates that pause should be enabled in the MAC. Based on bits[11:10] in ANAR register and bits[11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, "Pause Resolution", only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
11	MII Link Status	RO	0	**MII Link Status:** 1 = 100Base-TX Full-Duplex link is active 0 = No active 100Base-TX Full-Duplex link
10:8	Reserved	RO	0	**Reserved**
7	Bypass LED Stretching	RW	0	**Bypass LED Stretching:** 1 = Bypass LED stretching 0 = Normal LED operation Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value.
6	Reserved	RW	0	**Reserved**

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Table 25. 0x0019 PHY Control Register (PHYCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION		
				Configuration	LED_CFG	LED_0
5	LED Configuration	RW, Strap	1	1	1	ON for LINK OFF for no LINK
				2	0	ON for LINK BLINK for TX/RX Activity
4:0	PHY Address	RO, Strap	0000 1	**PHY Address:** Strapping configuration for PHY Address		

Table 26. 0x001A 10Base-T Status/Control Register (10BTSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Reserved	RO	0	**Reserved**
13	Receiver Threshold Enable	RW	0	**Lower Receiver Threshold Enable:** 1 = Enable 10Base-T lower receiver threshold 0 = Normal 10Base-T operation When enabled, receiver threshold is lowered to allow for operation with longer cables.
12:9	Squelch	RW	0000	**Squelch Configuration:** Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0000 = 200mV 0001 = 250mV 0010 = 300mV 0011 = 350mV 0100 = 400mV 0101 = 450mV 0110 = 500mV 0111 = 550mV 1000 = 600mV
8	Reserved	RW	0	**Reserved**
7	NLP Disable	RW	0	**NLP Transmission Control:** 1 = Disable transmission of NLPs 0 = Enable transmission of NLPs
6:5	Reserved	RO	0	**Reserved**
4	Polarity Status	RO	0	**Polarity Status:** 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit[12] in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register.
3:1	Reserved	RO	0	**Reserved**
0	Jabber Disable	RW	0	**Jabber Disable:** 1 = Jabber function disabled 0 = Jabber function enabled **Note:** This function is only applicable in 10Base-T operation.

Table 27. 0x001B BIST Control and Status Register #1 (BICSR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	BIST Error Count	RO	0x0	**BIST Error Count:** Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit[15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) **Note:** Writing '1' to bit[15] will lock the counter's value for successive read operation and clear the BIST Error Counter.

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Table 27. 0x001B BIST Control and Status Register #1 (BICSR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	BIST IPG Length	RW	0111 1101	**BIST IPG Length:** Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes).

Table 28. 0x001C BIST Control and Status Register #2 (BICSR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10:0	BIST Packet Length	RW	101 1101 1100	**BIST Packet Length:** Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5DC, which is equal to 1500 bytes.

Table 29. 0x001E Cable Diagnostic Control Register (CDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Cable Diagnostic Start	RW	0	**Cable Diagnostic Process Start:** 1 = Start cable measurement 0 = Cable Diagnostic is disabled Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered.
14:2	Reserved	RO	0	**Reserved**
1	Cable Diagnostic Status	RO	0	**Cable Diagnostic Process Done:** 1 = Indication that cable measurement process is complete 0 = Cable Diagnostic had not completed
0	Cable Diagnostic Test Fail	RO	0	**Cable Diagnostic Process Fail:** 1 = Indication that cable measurement process failed 0 = Cable Diagnostic has not failed

Table 30. 0x001F PHY Reset Control Register (PHYRCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Software Reset	RW, SC	0	**Software Reset:** 1 = Reset PHY 0 = Normal Operation This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital Restart	RW, SC	0	**Digital Restart:** 1 = Restart PHY 0 = Normal Operation This bit is self cleared and resets all PHY digital circuitry except the registers.
13:0	Reserved	RW	0	**Reserved**

Table 31. 0x0025 Multi-LED Control Register Multi LED Control Register (MLEDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Reserved	RW	0	**Reserved**
9	MLED Polarity Swap	RW	Strap	**MLED Polarity Swap:** The polarity of MLED depends on the routing configuration and the strap on COL pin. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high.
8:7	Reserved	RW	0	**Reserved**

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Table 31. 0x0025 Multi-LED Control Register Multi LED Control Register (MLEDCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
6:3	MLED Configuration (COL Pin)	RW	000 0	**MLED Configurations:** 000 0 = LINK OK 000 1 = RX/TX Activity 001 0 = TX Activity 001 1 = RX Activity 010 0 = Collision 010 1 = Speed, High for 100Base-TX 011 0 = Speed, High for 10Base-T 011 1 = Full-Duplex 100 0 = LINK OK / BLINK on TX/RX Activity 100 1 = Active Stretch Signal 101 0 = MII LINK (100BT+FD) 101 1 = LPI Mode (EEE) 110 0 = TX/RX MII Error 110 1 = Link Lost 111 0 = Blink for PRBS error 111 1 = Reserved Link Lost, LED remains ON until BMCR register (address 0x0001) is read. Blink for PRBS Errors, LED remains ON for single error and remains until BICSR1 register (address 0x001B) is cleared.
2	Reserved	RW	0	**Reserved**
1:0	MLED Route to LED_0	RW	00	**MLED Route to LED_0:** 00 = MLED routed to COL 01 = Reserved 10 = Reserved 11 = MLED routed to LED_0

Table 32. 0x0027 Compliance Test Register (COMPT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RW	0	**Reserved**
4	10Base-T Test Patterns Enable	RW	0	**10Base-T Test Pattern Enable:** 1 = Enable 10Base-T Test Patterns 0 = Disable 10Base-T Test Patterns

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Table 32. 0x0027 Compliance Test Register (COMPT) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3:0	Compliance Test Configuration	RW	0 0000	**Compliance Test Configuration Select:** Bit[4] in Register 0x0027 = 1, Enables 10Base-T Test Patterns. Bit[4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits[3:0] select the **10Base-T** test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 **100Base-TX** Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' ... 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register **Note 1:** To reconfigure the 100Base-TX Test Mode, bit[4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. **Note 2:** When performing 100Base-TX or 10Base-T tests modes, the speed must be forced using the Basic Mode Control Register (BMCR), address 0x0000.

Table 33. 0x003E IEEE 1588 PTP Pin Select Register (PTPPSEL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:7	Reserved	RO	0	**Reserved**
6:4	IEEE 1588 TX Pin Select	RW	000	**IEEE 1588 TX Pin Select:** Assigns transmit SFD pulse indication to pin selected by value 001 = Reserved 010 = Reserved 011 = LED_0 Pin 100 = CRS Pin 101 = COL Pin 110 = INT/PWDN_N Pin 111 = No pulse output
3	Reserved	RO	0	**Reserved**
2:0	IEEE 1588 RX Pin Select	RW	000	**IEEE 1588 RX Pin Select:** Assigns receive SFD pulse indication to pin selected by value 001 = Reserved 010 = Reserved 011 = LED_0 Pin 100 = CRS Pin 101 = COL Pin 110 = INT/PWDN_N Pin 111 = No pulse output

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Table 34. 0x003F IEEE 1588 PTP Configuration Register IEEE 1588 Precision Timing Configuration Register (PTPCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	PTP Transmit Timing	RW	101	**PTP Transmit Timing:** Set IEEE 1588 indication for TX path (8ns step)
12:10	PTP Receive Timing	RW	101	**PTP Receive Timing:** Set IEEE 1588 indication for RX path (8ns step)
9:8	TX Error Input Pin	RW	00	**Configure TX Error Input Pin:** 00 = No TX Error 01 = Reserved 10 = Use INT/PWDN_N pin as TX error 11 = Use COL pin as TX error
7:0	Reserved	RW	1111 1111	**Reserved**

Table 35. 0x0042 TX_CLK Phase Shift Register (TXCPSR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RO	0	**Reserved**
4	Phase Shift Enable	RW, SC	0	**TX Clock Phase Shift Enable:** 1 = Perform Phase Shift to TX_CLK 0 = No change in TX_CLK phase When enabled, TX_CLK phase shift is according to the value written to TX Clock Phase Shift Value (bits[4:0]).
3:0	Phase Shift Value	RW	0000	**TX Clock Phase Shift Value:** The value of this register represents the current phase shift between Reference clock at XI and MII tramsmit clock at TX_CLK. Any different value that will be written to these bits will shift TX_CLK by 4 times the difference (in ns). Example: If the value of the register is 0x0002, writing 0x0009 to this register will shift TX_CLK by 28ns. (4 times 7ns)

Table 36. 0x0155 ALCD Control and Results 1 Register (ALCDRR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	ALCD Start Test	SC	0	**Active Link Cable Diagnostic Start:** 1 = Start ALCD test 0 = Do not start ALCD test
14:13	Reserved	RO	00	**Reserved**
12	ALCD Test Status	RO	1	**Active Link Cable Diagnostic Status:** 1 = ALCD is not complete 0 = ALCD is complete
11:4	ALCD Sum Out	RO	1111 0100	
3:0	Reserved	RW	0001	**Reserved**

Table 37. 0x0170 Cable Diagnostic Specific Control Register (CDSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	Cable Diagnostic Cross Disable	RW	0	**Cross TDR Diagnostic Mode:** 1 = Disable TDR Cross Mode 0 = Enable TDR Cross Mode When enabled, the TDR mechanism is looking for reflection on the other pair to check for shorts between pairs.
13	Cable Diagnostic TD Bypass	RW	0	**TD Diagnostic Bypass:** 1 = Bypass TD pair diagnostic 0 = TDR is executed on TD pair When enabled, TDR on TD pair will not be executed.
12	Cable Diagnostic RD Bypass	RW	0	**RD Diganostic Bypass:** 1= Bypass RD pair diagnostic 0 = TDR is executed on RD pair When enabled, TDR on RD pair will not be executed.

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Table 37. 0x0170 Cable Diagnostic Specific Control Register (CDSCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
11	Reserved	RW	1	**Reserved**
10:8	Cable Diagnostic Average Cycles	RW	110	**Number of TDR Cycles to Average:** 000 = 1 TDR cycle 001 = 2 TDR cycles 010 = 4 TDR cycles 011 = 8 TDR cycles 100 = 16 TDR cycles 101 = 32 TDR cycles 110 = 64 TDR cycles 111 = Reserved
7:0	Reserved	RW	0101 0010	**Reserved**

Table 38. 0x0171 Cable Diagnostic Specific Control Register 2 (CDSCR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	1100 1000 0101	**Reserved**
3:0	TDR Pulse Control	RW	1100	Configure expected self reflection in TDR

Table 39. 0x0173 Cable Diagnostic Specific Control Register 3 (CDSCR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Cable Length Configuration	RW	1111 1111	Configure duration of listening to detect long cable reflections
7:0	Reserved	RW	0001 1110	**Reserved**

Table 40. 0x0177 Cable Diagnostic Specific Control Register 4 (CDSCR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RW	000	**Reserved**
12:8	Short Cables Threshold	RW	1 1000	Threshold to compensate for strong reflections in short cables
7:0	Reserved	RW	1001 1011	**Reserved**

Table 41. 0x0180 Cable Diagnostic Location Result Register #1 (CDLRR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	TD Peak Location 2	RO	0000 0000	Location of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.
7:0	TD Peak Location 1	RO	0000 0000	Location of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 42. 0x0181 Cable Diagnostic Location Result Register #2 (CDLRR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	TD Peak Location 4	RO	0000 0000	Location of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.
7:0	TD Peak Location 3	RO	0000 0000	Location of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 43. 0x0182 Cable Diagnostic Location Result Register #3 (CDLRR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 1	RO	0000 0000	Location of the **First** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.

Table 43. 0x0182 Cable Diagnostic Location Result Register #3 (CDLRR3) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	TD Peak Loaction 5	RO	0000 0000	Location of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 44. 0x0183 Cable Diagnostic Location Result Register #4 (CDLRR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 3	RO	0000 0000	Location of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.
7:0	RD Peak Location 2	RO	0000 0000	Location of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.

Table 45. 0x0184 Cable Diagnostic Location Result Register #5 (CDLRR5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 5	RO	0000 0000	Location of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.
7:0	RD Peak Location 4	RO	0000 0000	Location of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.

Table 46. 0x0185 Cable Diagnostic Amplitude Result Register #1 (CDLAR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	TD Peak Amplitude 2	RO	000 0000	Amplitude of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 1	RO	000 0000	Amplitude of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

Table 47. 0x0186 Cable Diagnostic Amplitude Result Register #2 (CDLAR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	TD Peak Amplitude 4	RO	000 0000	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 3	RO	000 0000	Amplitude of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

Table 48. 0x0187 Cable Diagnostic Amplitude Result Register #3 (CDLAR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 1	RO	000 0000	Amplitude of the **First** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 5	RO	000 0000	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

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Table 49. 0x0188 Cable Diagnostic Amplitude Result Register #4 (CDLAR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 3	RO	000 0000	Amplitude of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	RD Peak Amplitude 2	RO	000 0000	Amplitude of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.

Table 50. 0x0189 Cable Diagnostic Amplitude Result Register #5 (CDLAR5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 5	RO	000 0000	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	RD Peak Amplitude 4	RO	000 0000	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.

Table 51. 0x018A Cable Diagnostic General Result Register (CDLAR5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	TD Peak Polarity 5	RO	0	Polarity of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD).
14	TD Peak Polarity 4	RO	0	Polarity of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD).
13	TD Peak Polarity 3	RO	0	Polarity of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD).
12	TD Peak Polarity 2	RO	0	Polarity of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD).
11	TD Peak Polarity 1	RO	0	Polarity of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD).
10	RD Peak Polarity 5	RO	0	Polarity of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD).
9	RD Peak Polarity 4	RO	0	Polarity of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD).
8	RD Peak Polarity 3	RO	0	Polarity of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD).
7	RD Peak Polarity 2	RO	0	Polarity of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD).
6	RD Peak Polarity 1	RO	0	Polarity of the **First** peak discovered by the TDR mechanism on Receive Channel (RD).
5	Cross Detect on TD	RO	0	Cross Reflections were detected on TD. Indicate on Short between TD and TD
4	Cross Detect on RD	RO	0	Cross Reflections were detected on RD. Indicate on Short between TD and RD
3	Above 5 TD Peaks	RO	0	More than 5 reflections were detected on TD
2	Above 5 RD Peaks	RO	0	More than 5 reflections were detected on RD
1:0	Reserved	RO	0	**Reserved**

Table 52. 0x0215 ALCD Control and Results 2 Register (ALCDRR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RO	0	**Reserved**
3:0	PGA Control	RO	0011	Control word to analog PGA

Table 53. 0x021D ALCD Control and Results 3 Register (ALCDRR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11:0	FAGC Accumulator	RW	0110 0000 0000	FAGC Accumulator

Table 54. 0x0403 Line Driver Control Register (LDCTRL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RW	1001	**Reserved**
11:8	100Base-FX Line Driver Swing Select	RW	1111	**100Base-FX Line Driver Swing Select (peak-to-peak):** 0000 = 0.533-V 0001 = 0.567-V 0010 = 0.600-V 0011 = 0.633-V 0100 = 0.667-V 0101 = 0.700-V 0110 = 0.733-V 0111 = 0.767-V 1000 = 0.800-V 1001 = 0.833-V 1010 = 0.867-V 1011 = 0.900-V 1100 = 0.933-V 1101 = 0.976-V 1110 = 1.000-V 1111 = 1.033-V (Default Setting)
7:4	100Base-TX Line Driver Swing Select	RW	1100	**100Base-TX Line Driver Swing Select (peak-to-peak):** 0000 = 1.600-V 0001 = 1.633-V 0010 = 1.667-V 0011 = 1.700-V 0100 = 1.733-V 0101 = 1.767-V 0110 = 1.800-V 0111 = 1.833-V 1000 = 1.867-V 1001 = 1.900-V 1010 = 1.933-V 1011 = 1.967-V 1100 = 2.000-V (Default Setting) 1101 = 2.033-V 1110 = 2.067-V 1111 = 2.100-V
3:0	10Base-T Line Driver Swing Select	RW	1111	**10Base-T Line Driver Swing Select:** 0000 = 3.200-V 0001 = 3.233-V 0010 = 3.267-V 0011 = 3.300-V 0100 = 3.333-V 0101 = 3.367-V 0110 =3.400-V 0111 = 3.433-V 1000 = 3.467-V 1001 = 3.500-V 1010 = 3.533-V 1011 = 3.567-V 1100 = 3.600-V 1101 = 3.633-V 1110 = 3.667-V 1111 = 3.700-V (Default Setting)

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Table 55. 0x0428 Deep Power Down Control Register (DPDWN)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:6	Reserved	RO	0	**Reserved**
5	MSB 100Base-TX Idle Pattern	RW	0	**MSB 100Base-TX Idle Pattern:** 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' . .. 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register
4	100Base-TX Idle Pattern Test Mode	RW	0	**100Base-TX Idle Pattern Test Mode:** 1 = 100Base-TX Idle Pattern Enable 0 = Normal operation When enabled, 100Base-TX Idle Pattern is determined by bit[5] in register 0x0428 and bits[3:0] in register 0x0027.
3	Deep Power Down Speed	RW	0	**Deep Power Down Speed Selection:** 1 = 50ms duration to exit Deep Power Down 0 = 100ms duration to exit Deep Power Down
2	Deep Power Down Enable	RW	0	**Deep Power Down Enable:** 1 = Deep Power Down activated 0 = Normal operation **Note:** If set, the DP83822 enters into deep power down mode. Deep power down mode requires that IEEE Power Down be enabled first by either register access (set bit[11] = '1' in register 0x0000) or using INT/PWDN pin.
1:0	Reserved	RW	0	**Reserved**

Table 56. 0x0456 General Configuration Register (GENCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	0	**Reserved**
3	Min IPG Enable	RW	1	**Min IPG Enable:** 1 = Enable Minimum Inter-Packet Gap (IPG is set to 120ns) 0 = IPG set to 0.20µs
2:0	Reserved	RW	0	**Reserved**

Table 57. 0x0460 LEDs Configuration Register #1 (LEDCFG1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11:8	LED_1 Control	RW	0101	**LED_1 Control:** Selects the source for LED_1. Please reference bits[3:0] for list of sources.
7:4	LED_3 Control (RX_D3)	RW	0101	**LED_3 Control:** Selects the source for RX_D3. Please reference bits[3:0] for list of sources.

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Table 57. 0x0460 LEDs Configuration Register #1 (LEDCFG1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3:0	LED_0 Control	RW	0001	**LED_0 Control:** Selects the source for LED_0. 000 0 = LINK OK 000 1 = RX/TX Activity 001 0 = TX Activity 001 1 = RX Activity 010 0 = Collision 010 1 = Speed, High for 100Base-TX 011 0 = Speed, High for 10Base-T 011 1 = Full-Duplex 100 0 = LINK OK / BLINK on TX/RX Activity 100 1 = Active Stretch Signal 101 0 = MII LINK (100BT+FD) 101 1 = LPI Mode (EEE) 110 0 = TX/RX MII Error 110 1 = Link Lost 111 0 = Blink for PRBS error 111 1 = Reserved Link Lost, LED remains ON until BMCR register (address 0x0001) is read. Blink for PRBS Errors, LED remains ON for single error and remains until BICSR1 register (address 0x001B) is cleared.

Table 58. 0x0461 IO MUX GPIO Control Register (IOCTRL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RW	0000 0100 000	**Reserved**
4:1	MAC Impedance Control	RW	1 000	**MAC Impedance Control:** MAC interface impedance control sets the series termination for the digital pins. 0 000 = 99.25 Ω 0 001 = 91.13 Ω 0 010 = 84.24 Ω 0 011 = 78.31 Ω 0 100 = 73.17 Ω 0 101 = 68.65 Ω 0 110 = 64.66 Ω 0 111 = 61.11 Ω 1 000 = 58.07 Ω (Default Setting) 1 001 = 55.18 Ω 1 010 = 52.57 Ω 1 011 = 50.20 Ω 1 100 = 48.03 Ω 1 101 = 46.04 Ω 1 110 = 44.20 Ω 1 111 = 42.51 Ω
0	Reserved	RW	0	**Reserved**

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Table 59. 0x0462 IO MUX GPIO Control Register #1 (IOCTRL1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:12	RX_D3 / GPIO_3 Clock Source	RW	000	**Clock Source:** If RX_D3 is configured as a clock source from bits[10:8] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
11	Reserved	RO	0	**Reserved**
10:8	RX_D3 / GPIO_3 Control	RW	000	**RX_D3 GPIO Configuration:** 000 = Normal operation 001 = LED_3 (Default: Speed, High for 100Base-TX) 010 = WoL 011 = Clock reference according to bits[14:12] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'
7	Reserved	RO	0	**Reserved**
6:4	LED_1 / GPIO_1 Clock Source	RW	000	**Clock Source:** If LED_1 is configured as a clock source from bits[2:0] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
3	Reserved	RO	0	**Reserved**
2:0	LED_1 / GPIO_1 Control	RW	000	**LED_1 GPIO Configuration:** 000 = Tri-state 001 = LED_1 (Default: Speed, High for 100Base-TX) 010 = WoL 011 = Clock reference according to bits[6:4] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'

Table 60. 0x0463 IO MUX GPIO Control Register #2 (IOCTRL2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:7	Reserved	RO	0	**Reserved**
6:4	COL / GPIO_2 Clock Source	RW	000	**Clock Source:** If COL is configured as a clock source from bits[2:0] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
3	Reserved	RO	0	**Reserved**
2:0	COL / GPIO_2 Control	RW	000	**COL GPIO Configuration:** 000 = Normal operation 001 = MLED (Register 0x0025) 010 = WoL 011 = Clock reference according to bits[6:4] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'

Table 61. 0x0465 General Configuration Register (GENCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:1	Reserved	RW	1111 1111 0000 000	**Reserved**
0	100Base-FX Signal Detect Polarity	RW	0	**100Base-FX Signal Detect Polarity:** 1 = Signal Detect is Active HIGH 0 = Signal Detect is Active LOW When set to Active HIGH, Link drop will occur if SD pin senses a LOW state (SD = '0'). When set to Active LOW, Link drop will occur if SD pin senses a HIGH state (SD = '1'). **Note:** To enable 100Base-FX Signal Detection on LED_1 (pin #24), strap SD_DISABLE = '0'

Table 62. 0x0467 Strap Latch-In Register #1 (SOR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	RX_D1 Strap Mode	RO, Strap	00	**RX_D1 Strap Mode:** 00 = Mode 1 01 = Mode 2 10 = Mode 3 11 = Mode 4 Please refer to the strap section in the datasheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the datasheet.
13:12	RX_D0 Strap Mode	RO, Strap	00	**RX_D0 Strap Mode:** Use same reference as defined by bits[15:14] in this register.
11:10	COL Strap Mode	RO, Strap	11	**COL Strap Mode:** Use same reference as defined by bits[15:14] in this register.

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Table 62. 0x0467 Strap Latch-In Register #1 (SOR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
9:8	RX_ER Strap Mode	RO, Strap	11	**RX_ER Strap Mode:** Use same reference as defined by bits[15:14] in this register.
7:6	CRS Strap Mode	RO, Strap	11	**CRS Strap Mode:** Use same reference as defined by bits[15:14] in this register.
5:4	RX_DV Strap Mode	RO, Strap	00	**RX_DV Strap Mode:** Use same reference as defined by bits[15:14] in this register.
3:2	Reserved	RO	00	**Reserved**
1:0	LED_0 Strap Mode	RO, Strap	11	**LED_0 Strap Mode:** 00 = Mode 1 01 = Reserved 10 = Reserved 11 = Mode 4 Please refer to the strap section in the datasheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the datasheet.

Table 63. 0x0468 Strap Latch-In Register #2 (SOR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RO	0	**Reserved**
3:2	RX_D3 Strap Mode	RO, Strap	00	**RX_D3 Strap Mode:** Use same reference as defined by bits[15:14] in register 0x0467.
1:0	RX_D2 Strap Mode	RO, Strap	00	**RX_D2 Strap Mode:** Use same reference as defined by bits[15:14] in register 0x0467.

Table 64. 0x0469 LEDs Configuration Register #2 (LEDCFG2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10	LED_1 Polarity	RW	0	**LED_1 Polarity:** 1 = Active High 0 = Active Low
9	LED_1 Force Override Value	RW	0	**LED_1 Force Override Value:** 1 = LED_1 forced High 0 = LED_1 forced Low
8	LED_1 Force Override Enable	RW	0	**LED_1 Force Override Enable:** 1 = Enable Force Override 0 = Disable Force Override When enabled, bit[9] in this register determines state of LED_1.
7	Reserved	RO	0	**Reserved**
6	LED_3 Polarity	RW	1	**LED_3 Polarity:** 1 = Active High 0 = Active Low
5	LED_3 Force Override Value	RW	0	**LED_3 Force Override Value:** 1 = RX_D3 forced High 0 = RX_D3 forced Low
4	LED_3 Force Override Enable	RW	0	**LED_3 Force Override Enable:** 1 = Enable Force Override 0 = Disable Force Override When enabled, bit[5] in this register determines state of RX_D3.
3	Reserved	RO	0	**Reserved**
2	LED_0 Polarity	RW	0	**LED_0 Polarity:** 1 = Active High 0 = Active Low

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Table 64. 0x0469 LEDs Configuration Register #2 (LEDCFG2) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
1	LED_0 Force Override Value	RW	0	**LED_0 Force Override Value:** 1 = LED_0 forced High 0 = LED_0 forced Low
0	LED_0 Force Override Enable	RW	0	**LED_0 Force Override Enable:** 1 = Enable Force Override 0 = Disable Force Override When enabled, bit[1] in this register determines state of LED_0.

Table 65. 0x04A0 Receive Configuration Register (RXFCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Bit Nibble Swap	RW	00	**Bit Nibble Swap:** 00 = Normal order, no swap (RXD[3:0]) 01 = Swap bits order (RXD[0:3]) 10 = Swap nibbles order (RXD[3:0] , RXD[7:4]) 11 = Swap bits order in each nibble (RXD[4:7] , RXD[0:3])
13	SFD Byte	RW	0	**SFD Byte Search:** 1 = SFD is 0x5D (i.e. Receive module searches for 0x5D) 0 = SFD is 0xD5 (i.e. Receive module searches for 0xD5)
12	CRC Gate	RW	1	**CRC Gate:** 1 = Bad CRC gates Magic Packet and Pattern Indications 0 = Bad CRC does not gate Magic Packet or Pattern Indications If Magic Packet has Bad CRC there will be no indication (status, interrupt, GPIO) when enabled.
11	WoL Level Change Indication Clear	W, SC	0	**WoL Level Change Indication Clear:** If WoL Indication is set for Level change mode, this bit clears the level upon a write.
10:9	WoL Pulse Indication Select	RW	00	**WoL Pulse Indication Select:** Only valid when WoL Indication is set for Pulse mode. 00 = 8 clock cycles (of 125-MHz clock) 01 = 16 clock cycles 10 = 32 clock cycles 11 = 64 clock cycles
8	WoL Indication Select	RW	0	**WoL Indication Select:** 1 = Level change mode 0 = Pulse mode
7	WoL Enable	RW	0	**WoL Enable:** 1 = Enable Wake-on-LAN (WoL) 0 = Normal operation
6	Bit Mask Flag	RW	0	**Bit Mask Flag**
5	Secure-ON Enable	RW	0	**Enable** Secure-ON password for Magic Packets
4:2	Reserved	RW	0	**Reserved**
1	WoL Pattern Enable	RW	0	**Enable** Interrupt upon reception of packet with configured pattern
0	WoL Magic Packet Enable	RW	0	**Enable** Interrupt upon reception of Magic Packet

Table 66. 0x04A1 Receive Status Register (RXFS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RO	0	**Reserved**
12	WoL Interrupt Source	RW	0	**WoL Interrupt Source:** Source of Interrupt for bit[1] of register 0x0013. 1 = WoL Interrupt 0 = Data Polarity Interrupt When enabling WoL, this bit is automatically set to WoL Interrupt.
11:8	Reserved	RO	0	**Reserved**
7	SFD Error	RO, LH, SC	0	**SFD Error:** 1 = Packet with SFD error 0 = No SFD error

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Table 66. 0x04A1 Receive Status Register (RXFS) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
6	Bad CRC	RO, LH, SC	0	**Bad CRC:** 1 = Bad CRC was received 0 = No bad CRC received
5	Secure-On Hack Flag	RO, LH, SC	0	**Secure-ON Hack Flag:** 1 = Invalid Password detected in Magic Packet 0 = Valid Secure-ON Password
4:2	Reserved	RO, LH, SC	0	**Reserved**
1	WoL Pattern Status	RO, LH, SC	0	**WoL Pattern Status:** 1 = Valid packet with configured pattern received 0 = No valid packet with configured pattern received
0	WoL Magic Packet Status	RO, LH, SC	0	**WoL Magic Packet Status:** 1 = Valid Magic Packet received 0 = No valid Magic Packet received

Table 67. 0x04A2 Receive Perfect Match Data Register #1 (RXFPMD1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 4	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 5	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 68. 0x04A3 Receive Perfect Match Data Register #2 (RXFPMD2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 2	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 3	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 69. 0x04A4 Receive Perfect Match Data Register #3 (RXFPMD3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 0	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 1	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 70. 0x04A5 Receive Secure-ON Password Register #1 (RXFSOP1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 1	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 0	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 71. 0x04A6 Receive Secure-ON Password Register #2 (RXFSOP2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 3	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 2	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 72. 0x04A7 Receive Secure-ON Password Register #3 (RXFSOP3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 5	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

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Table 72. 0x04A7 Receive Secure-ON Password Register #3 (RXFSOP3) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	Secure-ON Password Byte 4	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 73. 0x04A8 Receive Pattern Register #1 (RXFPAT1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 1	RW	0	**Pattern Configuration:** Configures byte 1 of the pattern
7:0	Pattern Byte 0	RW	0	**Pattern Configuration:** Configures byte 0 of the pattern

Table 74. 0x04A9 Receive Pattern Register #2 (RXFPAT2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 3	RW	0	**Pattern Configuration:** Configures byte 3 of the pattern
7:0	Pattern Byte 2	RW	0	**Pattern Configuration:** Configures byte 2 of the pattern

Table 75. 0x04AA Receive Pattern Register #3 (RXFPAT3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 5	RW	0	**Pattern Configuration:** Configures byte 5 of the pattern
7:0	Pattern Byte 4	RW	0	**Pattern Configuration:** Configures byte 4 of the pattern

Table 76. 0x04AB Receive Pattern Register #4 (RXFPAT4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 7	RW	0	**Pattern Configuration:** Configures byte 7 of the pattern
7:0	Pattern Byte 6	RW	0	**Pattern Configuration:** Configures byte 6 of the pattern

Table 77. 0x04AC Receive Pattern Register #5 (RXFPAT5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 9	RW	0	**Pattern Configuration:** Configures byte 9 of the pattern
7:0	Pattern Byte 8	RW	0	**Pattern Configuration:** Configures byte 8 of the pattern

Table 78. 0x04AD Receive Pattern Register #6 (RXFPAT6)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 11	RW	0	**Pattern Configuration:** Configures byte 11 of the pattern
7:0	Pattern Byte 10	RW	0	**Pattern Configuration:** Configures byte 10 of the pattern

Table 79. 0x04AE Receive Pattern Register #7 (RXFPAT7)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 13	RW	0	**Pattern Configuration:** Configures byte 13 of the pattern
7:0	Pattern Byte 12	RW	0	**Pattern Configuration:** Configures byte 12 of the pattern

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Table 80. 0x04AF Receive Pattern Register #8 (RXFPAT8)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 15	RW	0	**Pattern Configuration:** Configures byte 15 of the pattern
7:0	Pattern Byte 14	RW	0	**Pattern Configuration:** Configures byte 14 of the pattern

Table 81. 0x04B0 Receive Pattern Register #9 (RXFPAT9)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 17	RW	0	**Pattern Configuration:** Configures byte 17 of the pattern
7:0	Pattern Byte 16	RW	0	**Pattern Configuration:** Configures byte 16 of the pattern

Table 82. 0x04B1 Receive Pattern Register #10 (RXFPAT10)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 19	RW	0	**Pattern Configuration:** Configures byte 19 of the pattern
7:0	Pattern Byte 18	RW	0	**Pattern Configuration:** Configures byte 18 of the pattern

Table 83. 0x04B2 Receive Pattern Register #11 (RXFPAT11)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 21	RW	0	**Pattern Configuration:** Configures byte 21 of the pattern
7:0	Pattern Byte 20	RW	0	**Pattern Configuration:** Configures byte 20 of the pattern

Table 84. 0x04B3 Receive Pattern Register #12 (RXFPAT12)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 23	RW	0	**Pattern Configuration:** Configures byte 23 of the pattern
7:0	Pattern Byte 22	RW	0	**Pattern Configuration:** Configures byte 22 of the pattern

Table 85. 0x04B4 Receive Pattern Register #13 (RXFPAT13)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 25	RW	0	**Pattern Configuration:** Configures byte 25 of the pattern
7:0	Pattern Byte 24	RW	0	**Pattern Configuration:** Configures byte 24 of the pattern

Table 86. 0x04B5 Receive Pattern Register #14 (RXFPAT14)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 27	RW	0	**Pattern Configuration:** Configures byte 27 of the pattern
7:0	Pattern Byte 26	RW	0	**Pattern Configuration:** Configures byte 26 of the pattern

Table 87. 0x04B6 Receive Pattern Register #15 (RXFPAT15)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 29	RW	0	**Pattern Configuration:** Configures byte 29 of the pattern

Table 87. 0x04B6 Receive Pattern Register #15 (RXFPAT15) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	Pattern Byte 28	RW	0	**Pattern Configuration:** Configures byte 28 of the pattern

Table 88. 0x04B7 Receive Pattern Register #16 (RXFPAT16)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 31	RW	0	**Pattern Configuration:** Configures byte 31 of the pattern
7:0	Pattern Byte 30	RW	0	**Pattern Configuration:** Configures byte 30 of the pattern

Table 89. 0x04B8 Receive Pattern Register #17 (RXFPAT17)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 33	RW	0	**Pattern Configuration:** Configures byte 33 of the pattern
7:0	Pattern Byte 32	RW	0	**Pattern Configuration:** Configures byte 32 of the pattern

Table 90. 0x04B9 Receive Pattern Register #18 (RXFPAT18)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 35	RW	0	**Pattern Configuration:** Configures byte 35 of the pattern
7:0	Pattern Byte 34	RW	0	**Pattern Configuration:** Configures byte 34 of the pattern

Table 91. 0x04BA Receive Pattern Register #19 (RXFPAT19)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 37	RW	0	**Pattern Configuration:** Configures byte 37 of the pattern
7:0	Pattern Byte 36	RW	0	**Pattern Configuration:** Configures byte 36 of the pattern

Table 92. 0x04BB Receive Pattern Register #20 (RXFPAT20)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 39	RW	0	**Pattern Configuration:** Configures byte 39 of the pattern
7:0	Pattern Byte 38	RW	0	**Pattern Configuration:** Configures byte 38 of the pattern

Table 93. 0x04BC Receive Pattern Register #21 (RXFPAT21)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 41	RW	0	**Pattern Configuration:** Configures byte 41 of the pattern
7:0	Pattern Byte 40	RW	0	**Pattern Configuration:** Configures byte 40 of the pattern

Table 94. 0x04BD Receive Pattern Register #22 (RXFPAT22)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 43	RW	0	**Pattern Configuration:** Configures byte 43 of the pattern
7:0	Pattern Byte 42	RW	0	**Pattern Configuration:** Configures byte 42 of the pattern

Table 95. 0x04BE Receive Pattern Register #23 (RXFPAT23)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 45	RW	0	**Pattern Configuration:** Configures byte 45 of the pattern
7:0	Pattern Byte 44	RW	0	**Pattern Configuration:** Configures byte 44 of the pattern

Table 96. 0x04BF Receive Pattern Register #24 (RXFPAT24)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 47	RW	0	**Pattern Configuration:** Configures byte 47 of the pattern
7:0	Pattern Byte 46	RW	0	**Pattern Configuration:** Configures byte 46 of the pattern

Table 97. 0x04C0 Receive Pattern Register #25 (RXFPAT25)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 49	RW	0	**Pattern Configuration:** Configures byte 49 of the pattern
7:0	Pattern Byte 48	RW	0	**Pattern Configuration:** Configures byte 48 of the pattern

Table 98. 0x04C1 Receive Pattern Register #26 (RXFPAT26)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 51	RW	0	**Pattern Configuration:** Configures byte 51 of the pattern
7:0	Pattern Byte 50	RW	0	**Pattern Configuration:** Configures byte 50 of the pattern

Table 99. 0x04C2 Receive Pattern Register #27 (RXFPAT27)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 53	RW	0	**Pattern Configuration:** Configures byte 53 of the pattern
7:0	Pattern Byte 52	RW	0	**Pattern Configuration:** Configures byte 52 of the pattern

Table 100. 0x04C3 Receive Pattern Register #28 (RXFPAT28)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 55	RW	0	**Pattern Configuration:** Configures byte 55 of the pattern
7:0	Pattern Byte 54	RW	0	**Pattern Configuration:** Configures byte 54 of the pattern

Table 101. 0x04C4 Receive Pattern Register #29 (RXFPAT29)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 57	RW	0	**Pattern Configuration:** Configures byte 57 of the pattern
7:0	Pattern Byte 56	RW	0	**Pattern Configuration:** Configures byte 56 of the pattern

Table 102. 0x04C5 Receive Pattern Register #30 (RXFPAT30)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 59	RW	0	**Pattern Configuration:** Configures byte 59 of the pattern

Table 102. 0x04C5 Receive Pattern Register #30 (RXFPAT30) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	Pattern Byte 58	RW	0	**Pattern Configuration:** Configures byte 58 of the pattern

Table 103. 0x04C6 Receive Pattern Register #31 (RXFPAT31)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 61	RW	0	**Pattern Configuration:** Configures byte 61 of the pattern
7:0	Pattern Byte 60	RW	0	**Pattern Configuration:** Configures byte 60 of the pattern

Table 104. 0x04C7 Receive Pattern Register #32 (RXFPAT32)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 63	RW	0	**Pattern Configuration:** Configures byte 63 of the pattern
7:0	Pattern Byte 62	RW	0	**Pattern Configuration:** Configures byte 62 of the pattern

Table 105. 0x04C8 Receive Pattern Byte Mask Register #1 (RXFPBM1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 0 to 15	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 0 to 15. For each byte '1' means it is masked.

Table 106. 0x04C9 Receive Pattern Byte Mask Register #2 (RXFPBM2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 16 to 31	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 16 to 31. For each byte '1' means it is masked.

Table 107. 0x04CA Receive Pattern Byte Mask Register #3 (RXFPBM3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 32 to 47	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 32 to 47. For each byte '1' means it is masked.

Table 108. 0x04CB Receive Pattern Byte Mask Register #4 (RXFPBM4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 48 to 63	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 48 to 63. For each byte '1' means it is masked.

Table 109. 0x04CC Receive Pattern Control Register (RXFPATC)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:6	Reserved	RO	0	**Reserved**
5:0	Pattern Start Point	RW	0	**Pattern Start Point:** Number of bytes after SFD where comparison begins on RX packets to the configured pattern. 00000 = Start compare on 1st byte after SFD 00001 = Start compare on 2nd byte after SFD ... 01100 = Start compare on 13th byte (Default) Default setting is 0xC, which means the pattern comparision will begin after source and destination addresses since they are each 6 bytes.

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Table 110. 0x04D0 Energy Efficient Ethernet Configuration Register #2 (EEECFG2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	TX_ER for LPI Request	RW	0	**TX_ER for LPI Request:** 1 = TX_ER used for LPI Request 0 = TX_ER not used for LPI Request
13:7	Reserved	RO	00 0011 0	**Reserved**
6:5	TX_ER Pin Select	RW	00	**TX_ER Pin Select:** 00 = No Pin Selected 01 = INT/PWDN 10 = COL/GPIO 11 = No Pin Selected
4:0	Reserved	RO	0 0010	**Reserved**

Table 111. 0x04D1 Energy Efficient Ethernet Configuration Register #2 (EEECFG3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	0000 0001 1000	**Reserved**
3	EEE Capabilities Bypass	RW	1	**EEE Advertise Bypass:** 1 = Bit [0] determines EEE Auto-Negotiation Abilities 0 = MMD3 and MMD7 determine EEE Auto-Negotiation Abilities Allows for EEE Advertisment during Auto-Negotiation to be determined by bit[0] in register 0x04D1 rather than the Next Page Registers (Register 0x003C and Register 0x003D in MMD7).
2	EEE Next Page Disable	RW	0	**EEE Next Page Disable:** 1 = Reception of EEE Next Pages is disabled 0 = Reception of EEE Next Pages is enabled
1	EEE RX Path Shutdown	RW	1	**EEE RX Path Shutdown:** 1= Enable shutdown of Analog RX path at LPI_Quiet 0 = Analog RX path is active during LPI_Quiet
0	EEE Capabilities Enable	RW, Strap	0	**EEE Capabilities Enable:** 1 = PHY supports EEE capabilities 0 = PHY does not support EEE When enabled, Auto-Negotiation will negotiate to EEE as defined by register 0x003C and register 0x003D in MMD7. When disabled, register 0x0014 in MMD3, register 0x003C and register 0x003D in MMD7 are ignored.

Table 112. 0x3000 MMD3 PCS Control Register #1 (MMD3_PCS_CTRL_1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	PCS Reset	RW, SC	0	**PCS Reset:** 1 = Soft Reset of MMD3, MMD7 and PCS registers 0 = Normal operation Reset clears MMD3, MMD7 and PCS registers. Reset does not clear Vendor Specific Registers (DEVAD = 31).
14:11	Reserved	RO	0	**Reserved**
10	RX Clock Stoppable	RW	0	**RX Clock Stoppable:** 1 = Receive Clock stoppable during LPI 0 = Receive Clock not stoppable
9:0	Reserved	RO	0	**Reserved**

Table 113. 0x3001 MMD3 PCS Status Register #1 (MMD3_PCS_STATUS_1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11	TX LPI Received	RO	0	**TX LPI Received:** 1 = TX PCS has received LPI 0 = LPI not received

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Table 113. 0x3001 MMD3 PCS Status Register #1 (MMD3_PCS_STATUS_1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
10	RX LPI Received	RO	0	**RX LPI Received:** 1 = RX PCS has received LPI 0 = LPI not received
9	TX LPI Indication	RO	0	**TX LPI Indication:** 1 = TX PCS is currently receiving LPI 0 = TX PCS is not currently receiving LPI
8	RX LPI Indication	RO	0	**RX LPI Indication:** 1 = RX PCS is currently receiving LPI 0 = RX PCS is not currenly receiving LPI
7	Reserved	RO	0	**Reserved**
6	TX Clock Stoppable	RO	0	**TX Clock Stoppable:** 1 = MAC may stop clock during LPI 0 = TX Clock is not stoppable
5:0	Reserved	RO	0	**Reserved**

Table 114. 0x3014 MMD3 Energy Efficient Ethernet Capability Register (MMD3_EEE_CAPABILITY)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:3	Reserved	RO	0	**Reserved**
2	EEE 1Gbps Enable	RO	0	**EEE 1Gbps Enable:** 1 = EEE is supported for 1000Base-T 0 = EEE is not supported for 1000Base-T
1	EEE 100Mbps Enable	RO	0	**EEE 100Mbps Enable:** 1 = EEE is supported for 100Base-TX 0 = EEE is not supported for 100Base-TX
0	Reserved	RO	0	**Reserved**

Table 115. 0x3016 MMD3 Wake Error Counter Register (MMD3_WAKE_ERR_CNT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	EEE Wake Error Counter	RO, LH	0	**EEE Wake Error Counter:** This register counts the wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is cleared after a read and holds at all ones in the case of overflow. PCS Reset also clears this register.

Table 116. 0x703C MMD7 Energy Efficient Ethernet Advertisement Register (MMD7_EEE_ADVERTISEMENT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:2	Reserved	RO	0	**Reserved**
1	Advertise 100Base-TX EEE	RW	1	**Advertise 100Base-TX EEE:** 1 = Energy Efficient Ethernet is advertised for 100Base-TX 0 = Energy Efficient Ethernet is not advertised
0	Reserved	RO	0	**Reserved**

Table 117. 0x703D MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:2	Reserved	RO	0	**Reserved**
1	Link Partner EEE Capability	RO	0	**Link Partner EEE Capability:** 1 = Link Partner is advertising EEE capability for 100Base-TX 0 = Link Partner is not advertising EEE capability for 100Base-TX
0	Reserved	RO	0	**Reserved**

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6 Device and Documentation Support

6.1 Device Support

6.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 118. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DP83822HF	Click here	Click here	Click here	Click here	Click here
DP83822IF	Click here	Click here	Click here	Click here	Click here
DP83822H	Click here	Click here	Click here	Click here	Click here
DP83822I	Click here	Click here	Click here	Click here	Click here

6.1.2 Development Support

For additional information or questions, see the Texas Instruments E2E community at http://www.ti.e2e.com.

6.2 Trademarks

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83822HFRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125	822HF	
DP83822HFRHBT	PREVIEW	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 125	822HF	
DP83822HRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125	822H	
DP83822HRHBT	PREVIEW	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 125	822H	
DP83822IFRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 85	822IF	
DP83822IFRHBT	PREVIEW	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 85	822IF	
DP83822IRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 85	822I	
DP83822IRHBT	PREVIEW	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 85	822I	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

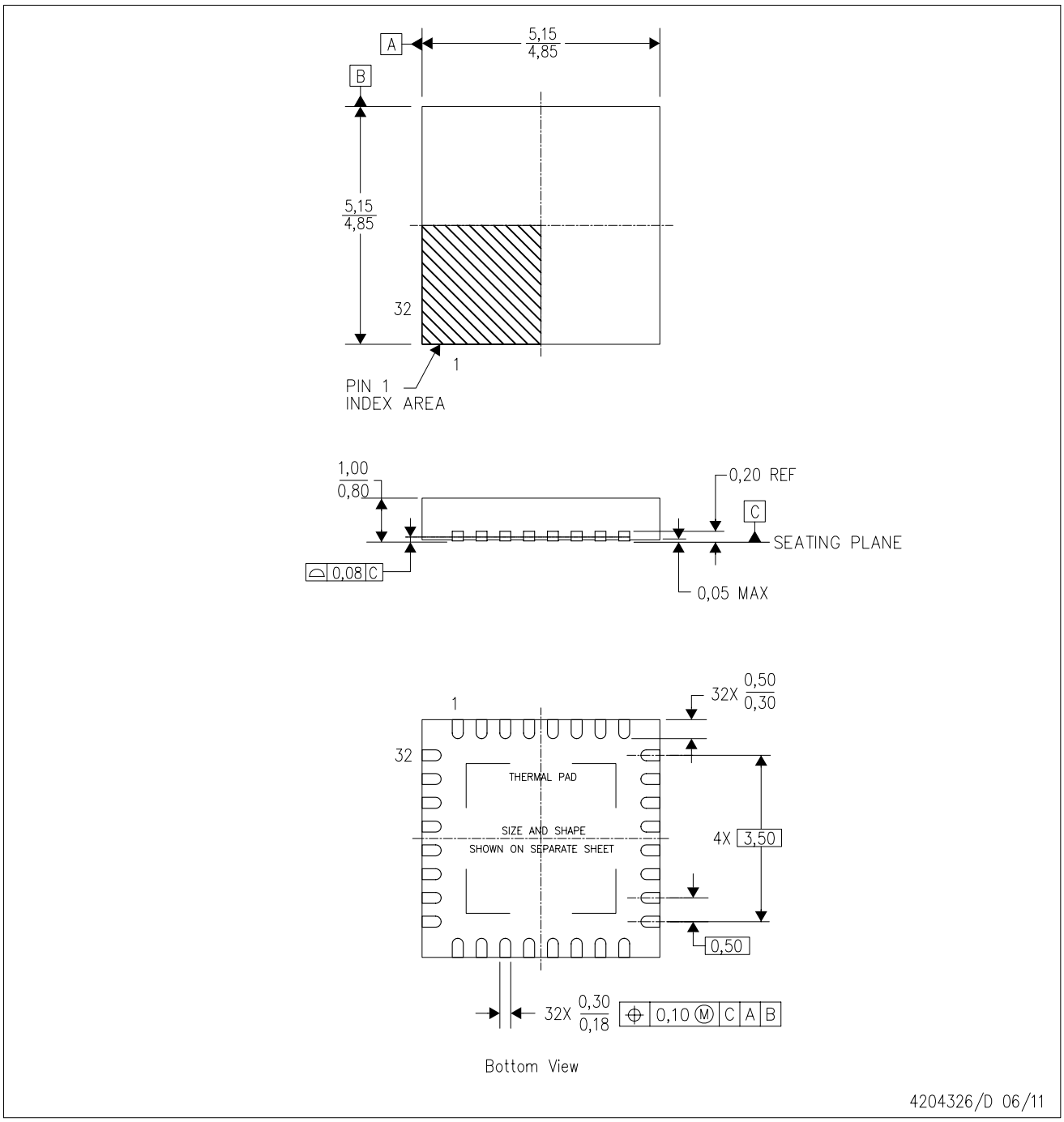
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

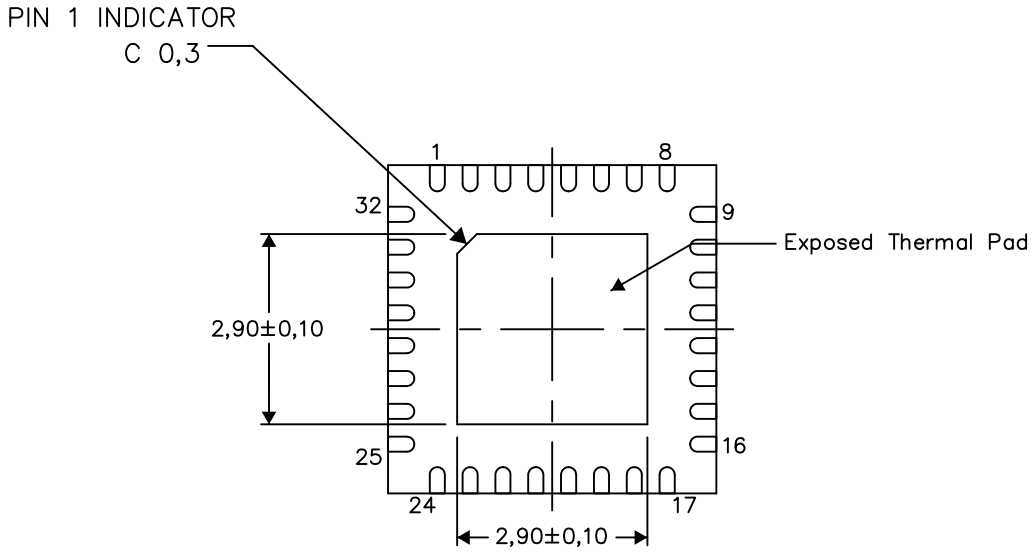
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356–10/AC 05/15

NOTE: A. All linear dimensions are in millimeters

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