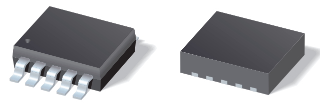


DUAL 16-/14-/12-BIT, ULTRALOW-GLITCH, LOW-POWER, BUFFERED, VOLTAGE-OUTPUT DAC WITH 2.5-V, 4-PPM/°C INTERNAL REFERENCE IN SMALL 3-MM × 3-MM QFN

Check for Samples: DAC8562, DAC8563, DAC8162, DAC8163, DAC7562, DAC7563

FEATURES

- **Relative Accuracy:**
  - **DAC856x (16-Bit): 4 LSB INL**
  - **DAC816x (14-Bit): 1 LSB INL**
  - **DAC756x (12-Bit): 0.3 LSB INL**
- **Glitch Energy: 0.1 nV-s**
- **Bidirectional Reference: Input or 2.5-V Output**
  - **Output Disabled by Default**
  - **±5-mV Initial Accuracy (Max)**
  - **4-ppm/°C Temperature Drift (Typ)**
  - **10-ppm/°C Temperature Drift (Max)**
  - **20-mA Sink/Source Capability**
- **Power-On Reset to Zero Scale or Mid-Scale**
- **Low-Power: 4 mW (Typ, 5-V AV_{DD}, Including Internal Reference Current)**
- **Wide Power-Supply Range: 2.7 V to 5.5 V**
- **50-MHz SPI With Schmitt-Triggered Inputs**
- **$\overline{LDAC}$ and $\overline{CLR}$ Functions**
- **Output Buffer With Rail-to-Rail Operation**
- **Packages: QFN-10 (3x3 mm), MSOP-10**
- **Temperature Range: –40°C to 125°C**

APPLICATIONS

- **Portable Instrumentation**
- **Bipolar Outputs (reference design)**
- **PLC Analog Output Module (reference design)**
- **Closed-Loop Servo Control**
- **Voltage Controlled Oscillator Tuning**
- **Data Acquisition Systems**
- **Programmable Gain and Offset Adjustment**

DESCRIPTION

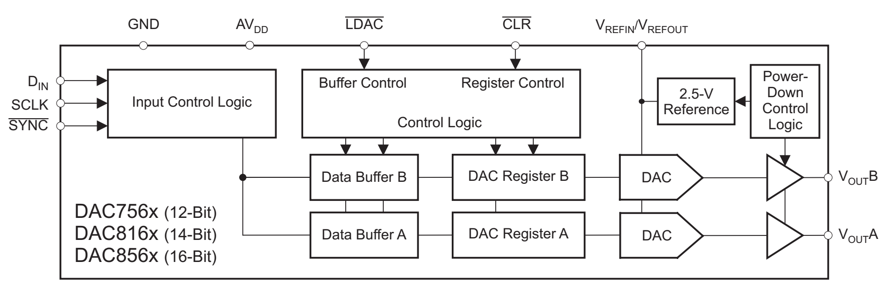
The DAC856x, DAC816x, and DAC756x are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 4-ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN}/V_{REFOUT} pin.

These devices are monotonic, providing excellent linearity and minimizing undesired code-to-code transient voltages (glitch). They use a versatile three-wire serial interface that operates at clock rates up to 50 MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces. The DACxx62 devices incorporate a power-on-reset circuit that ensures the DAC output powers up at zero scale until a valid code is written to the device, whereas the DACxx63s similarly power up at mid-scale. These devices contain a power-down feature that reduces current consumption to typically 10 nA at 5 V. The low power consumption, internal reference, and small footprint make these devices ideal for portable, battery-operated equipment.

The DACxx62 devices are drop-in and function-compatible with each other, as are the DACxx63s. The entire family is available in MSOP-10 and QFN-10 packages.

Table 1. RELATED DEVICES

	16-BIT	14-BIT	12-BIT
Reset to zero	DAC8562	DAC8162	DAC7562
Reset to mid-scale	DAC8563	DAC8163	DAC7563



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Microwire is a trademark of National Semiconductor.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	RESET TO	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPER-ATURE RANGE	PACKAGE MARKING
DAC8562	±12	±1	10	Zero	QFN-10	DSC	–40°C to 125°C	8562
					MSOP-10	DGS		
DAC8563				Mid-scale	QFN-10	DSC		8563
					MSOP-10	DGS		
DAC8162	±3	±0.5	10	Zero	QFN-10	DSC	–40°C to 125°C	8162
					MSOP-10	DGS		
DAC8163				Mid-scale	QFN-10	DSC		8163
					MSOP-10	DGS		
DAC7562	±0.75	±0.25	10	Zero	QFN-10	DSC	–40°C to 125°C	7562
					MSOP-10	DGS		
DAC7563				Mid-scale	QFN-10	DSC		7563
					MSOP-10	DGS		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	VALUE	UNIT
AV_{DD} to GND	–0.3 to 6	V
$\overline{CLR}$, D_{IN}, $\overline{LDAC}$, SCLK and $\overline{SYNC}$ input voltage to GND	–0.3 to AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to AV_{DD} + 0.3	V
V_{REFIN}/V_{REFOUT} to GND	–0.3 to AV_{DD} + 0.3	V
Operating temperature range	–40 to 125	°C
Junction temperature, maximum ($T_{J\ max}$)	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		DAC856x, DAC816x, DAC756x		UNIT
		DSC	DGS	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	62.8	173.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	44.3	48.5	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)	26.5	79.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)	0.4	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)	25.5	68.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	46.2	N/A	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC856x	Resolution		16			Bits
	Relative accuracy	Using line passing through codes 512 and 65,024		±4	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.2	±1	LSB
DAC816x	Resolution		14			Bits
	Relative accuracy	Using line passing through codes 128 and 16,256		±1	±3	LSB
	Differential nonlinearity	14-bit monotonic		±0.1	±0.5	LSB
DAC756x	Resolution		12			Bits
	Relative accuracy	Using line passing through codes 32 and 4,064		±0.3	±0.75	LSB
	Differential nonlinearity	12-bit monotonic		±0.05	±0.25	LSB
Offset error		Extrapolated from two-point line(1), unloaded		±1	±4	mV
Offset error drift				±2		μV/°C
Full-scale error		DAC register loaded with all 1s		±0.03	±0.2	% FSR
Zero-code error		DAC register loaded with all 0s		1	4	mV
Zero-code error drift				±2		μV/°C
Gain error		Extrapolated from two-point line(1), unloaded		±0.01	±0.15	% FSR
Gain temperature coefficient				±1		ppm FSR/°C
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time(3)		DACs unloaded		7		μs
		R_L = 1 MΩ		10		
Slew rate		Measured between 20% - 80% of a full-scale transition		0.75		V/μs
Capacitive load stability		R_L = ∞		1		nF
		R_L = 2 kΩ		3		
Code-change glitch impulse		1-LSB change around major carry		0.1		nV-s
Digital feedthrough		SCLK toggling, $\overline{SYNC}$ high		0.1		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 470 pF, AV_{DD} = 5.5 V		40		mV
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel, External reference		5		μV
		Full-scale swing on adjacent channel, Internal reference		15		
DC output impedance		At mid-scale input		5		Ω
Short-circuit current		DAC outputs at full-scale, DAC outputs shorted to GND		40		mA
Power-up time, including settling time		Coming out of power-down mode		50		μs
AC PERFORMANCE(2)						
DAC output noise density		T_A = 25°C, at mid-scale input, f_{OUT} = 1 kHz		90		nV/√Hz
DAC output noise		T_A = 25°C, at mid-scale input, 0.1 Hz to 10 Hz		2.6		$μV_{PP}$
LOGIC INPUTS(2)						
Input pin Leakage current			–1	±0.1	1	μA
Logic input LOW voltage $V_{IN}L$			0		0.8	V
Logic input HIGH voltage $V_{IN}H$			0.7 × AV_{DD}		AV_{DD}	V
Pin capacitance					3	pF

(1) 16-bit: codes 512 and 65,024; 14-bit: codes 128 and 16,256; 12-bit: codes 32 and 4,064
(2) Specified by design or characterization
(3) Transition time between 1/4 scale and 3/4 scale including settling to within ±0.024% FSR

ELECTRICAL CHARACTERISTICS (continued)

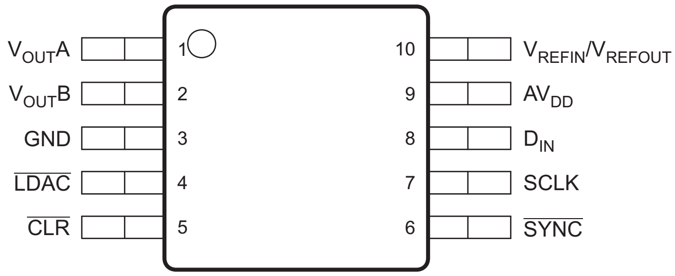
At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
External reference current		External V_{REF} = 2.5 V (when internal reference is disabled), all channels active using gain = 1		15		µA
V_{REFIN} reference input range			0		AV_{DD}	V
Reference input impedance		Internal reference disabled, gain = 1		170		kΩ
		Internal reference disabled, gain = 2		85		
REFERENCE OUTPUT						
Output voltage		T_A = 25°C	2.495	2.5	2.505	V
Initial accuracy		T_A = 25°C	–5	±0.1	5	mV
Output voltage temperature drift(4)				4	10	ppm/°C
Output voltage noise		f = 0.1 Hz to 10 Hz		12		$µV_{PP}$
Output voltage noise density (high-frequency noise)		T_A = 25°C, f = 1 kHz, C_L = 0 µF		250		nV/√Hz
		T_A = 25°C, f = 1 MHz, C_L = 0 µF		30		
		T_A = 25°C, f = 1 MHz, C_L = 4.7 µF		10		
Load regulation, sourcing(5)		T_A = 25°C		20		µV/mA
Load regulation, sinking(5)		T_A = 25°C		185		µV/mA
Output current load capability(6)				±20		mA
Line regulation		T_A = 25°C		50		µV/V
Long-term stability/drift (aging)(5)		T_A = 25°C, time = 0 to 1900 hours		100		ppm
Thermal hysteresis(5)		First cycle		200		ppm
		Additional cycles		50		
POWER REQUIREMENTS(7)						
Power supply voltage			2.7		5.5	V
I_{DD}	AV_{DD} = 3.6 V to 5.5 V	Normal mode, internal reference off		0.25	0.5	mA
		Normal mode, internal reference on		0.8	1.3	
		Power-down modes(8)		0.01	1	µA
		Power-down modes(9)		0.01	3	
	AV_{DD} = 2.7 V to 3.6 V	Normal mode, internal reference off		0.2	0.4	mA
		Normal mode, internal reference on		0.73	1.3	
		Power-down modes(8)		0.008	1	µA
		Power-down modes(9)		0.008	3	
Power dissipation	AV_{DD} = 3.6 V to 5.5 V	Normal mode, internal reference off		0.9	2.75	mW
		Normal mode, internal reference on		2.9	7.15	
		Power-down modes(8)		0.04	5.5	µW
		Power-down modes(9)		0.04	16.5	
	AV_{DD} = 2.7 V to 3.6 V	Normal mode, internal reference off		0.54	1.44	mW
		Normal mode, internal reference on		1.97	4.68	
		Power-down modes(8)		0.02	3.6	µW
		Power-down modes(9)		0.02	10.8	
TEMPERATURE RANGE						
Specified performance			–40		125	°C

(4) Internal reference output voltage temperature drift is characterized from –40°C to 125°C.
(5) Explained in more detail in the *Application Information* section of this data sheet.
(6) Specified by design or characterization
(7) Input code = mid-scale, no load, $V_{IN}H$ = AV_{DD}, and $V_{IN}L$ = GND
(8) Temperature range –40°C to 105°C
(9) Temperature range –40°C to 125°C

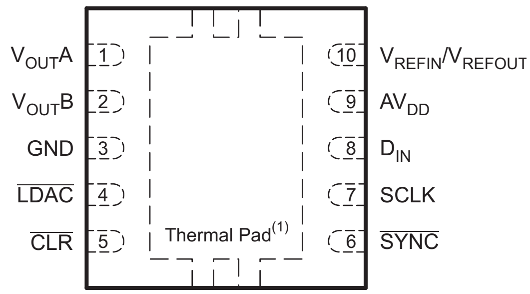
PIN CONFIGURATIONS

DGS
(Top View)



MSOP Package

DSC
(Top View)



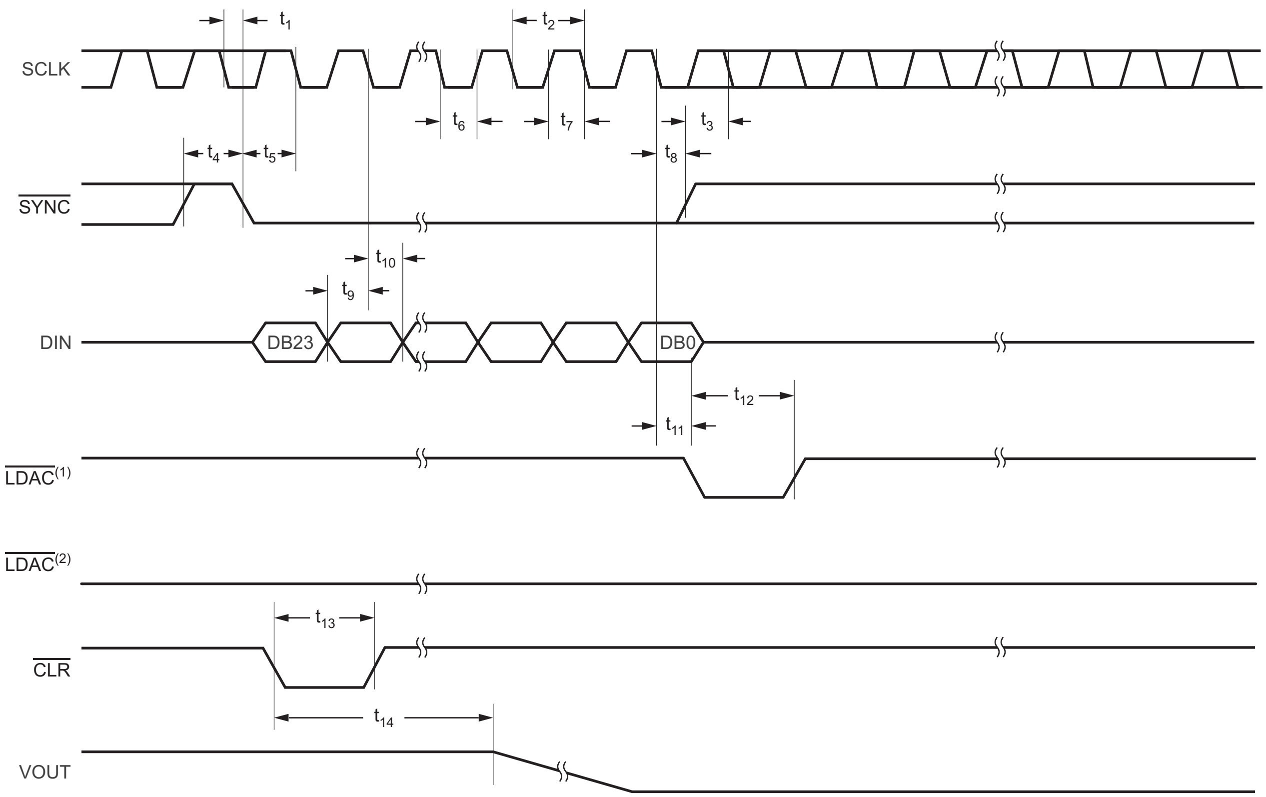
QFN Package

(1) It is recommended to connect the thermal pad to the ground plane for better thermal dissipation.

Table 2. PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
AV_{DD}	9	Power-supply input, 2.7 V to 5.5 V
$\overline{\text{CLR}}$	5	Asynchronous clear input. The $\overline{\text{CLR}}$ input is falling-edge sensitive. When $\overline{\text{CLR}}$ is activated, zero scale (DACxx62) or mid-scale (DACxx63) is loaded to all input and DAC registers. This sets the DAC output voltages accordingly. The part exits clear code mode on the 24^{th} falling edge of the next write to the part. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted.
D_{IN}	8	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-trigger logic input
GND	3	Ground reference point for all circuitry on the device
$\overline{\text{LDAC}}$	4	In *synchronous* mode, data are updated with the falling edge of the 24^{th} SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such *synchronous* updates, the $\overline{\text{LDAC}}$ pin is not required, and it must be connected to GND permanently or asserted and held low before sending commands to the device. In *asynchronous* mode, the $\overline{\text{LDAC}}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel commands can be written in order to set different channel buffers to desired values and then make a falling edge on $\overline{\text{LDAC}}$ pin to simultaneously update the DAC output registers.
SCLK	7	Serial clock input. Data can be transferred at rates up to 50 MHz. Schmitt-trigger logic input
$\overline{\text{SYNC}}$	6	Level-triggered control input (active-low). This input is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24^{th} clock falling edge. If $\overline{\text{SYNC}}$ is taken high before the 23^{rd} clock edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC756x/DAC816x/DAC856x. Schmitt-trigger logic input
$V_{OUT}A$	1	Analog output voltage from DAC-A
$V_{OUT}B$	2	Analog output voltage from DAC-B
V_{REFIN} / V_{REFOUT}	10	Bidirectional voltage reference pin. If internal reference is used, 2.5-V output.

TIMING DIAGRAM



(1) Asynchronous LDAC update mode. For more information, see the *LDAC Functionality* section.

(2) Synchronous LDAC update mode; LDAC remains low. For more information, see the *LDAC Functionality* section.

Figure 1. Serial Write Operation

TIMING REQUIREMENTS(1)(2)

At AV_{DD} = 2.7 V to 5.5 V and over –40°C to 125°C (unless otherwise noted).

PARAMETER		DAC756x/DAC816x/DAC856x MIN	TYP	MAX	UNIT
t_1	SCLK falling edge to SYNC falling edge (for successful write operation)	10			ns
t_2 (3)	SCLK cycle time	20			ns
t_3	SYNC rising edge to 23rd SCLK falling edge (for successful SYNC interrupt)	13			ns
t_4	Minimum SYNC HIGH time	80			ns
t_5	SYNC to SCLK falling edge setup time	13			ns
t_6	SCLK LOW time	8			ns
t_7	SCLK HIGH time	8			ns
t_8	SCLK falling edge to SYNC rising edge	10			ns
t_9	Data setup time	6			ns
t_{10}	Data hold time	5			ns
t_{11}	SCLK falling edge to LDAC falling edge for asynchronous LDAC update mode	5			ns
t_{12}	LDAC pulse duration, LOW time	10			ns
t_{13}	CLR pulse duration, LOW time	80			ns
t_{14}	CLR falling edge to start of VOUT transition		100		ns

(1) All input signals are specified with $t_R = t_F$ = 3 ns (10% to 90% of AV_{DD}) and timed from a voltage level of ($V_{IN}L + V_{IN}H$)/2.
(2) See the *Serial Write Operation* timing diagram (Figure 1).
(3) Maximum SCLK frequency is 50 MHz at AV_{DD} = 2.7 V to 5.5 V.

TABLES OF GRAPHS

Table 3. Typical Characteristics: Internal Reference Performance

MEASUREMENT	POWER-SUPPLY VOLTAGE	FIGURE NUMBER
Internal Reference Voltage vs Temperature	5.5 V	Figure 2
Internal Reference Voltage Temperature Drift Histogram		Figure 3
Internal Reference Voltage vs Load Current		Figure 4
Internal Reference Voltage vs Time		Figure 5
Internal Reference Noise Density vs Frequency		Figure 6
Internal Reference Voltage vs Supply Voltage	2.7 V – 5.5 V	Figure 7

Table 4. Typical Characteristics: DAC Static Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
FULL-SCALE, GAIN, OFFSET AND ZERO-CODE ERRORS			
Full-Scale Error vs Temperature		5.5 V	Figure 16
Gain Error vs Temperature			Figure 17
Offset Error vs Temperature			Figure 18
Zero-Code Error vs Temperature			Figure 19
Full-Scale Error vs Temperature		2.7 V	Figure 63
Gain Error vs Temperature			Figure 64
Offset Error vs Temperature			Figure 65
Zero-Code Error vs Temperature			Figure 66
LOAD REGULATION			
DAC Output Voltage vs Load Current		5.5 V	Figure 30
		2.7 V	Figure 74
DIFFERENTIAL NONLINEARITY ERROR			
Differential Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 9
	T = 25°C		Figure 11
	T = 125°C		Figure 13
Differential Linearity Error vs Temperature			Figure 15
Differential Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 56
	T = 25°C		Figure 58
	T = 125°C		Figure 60
Differential Linearity Error vs Temperature			Figure 62
INTEGRAL NONLINEARITY ERROR (RELATIVE ACCURACY)			
Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 8
	T = 25°C		Figure 10
	T = 125°C		Figure 12
Linearity Error vs Temperature			Figure 14
Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 55
	T = 25°C		Figure 57
	T = 125°C		Figure 59
Linearity Error vs Temperature			Figure 61

Table 4. Typical Characteristics: DAC Static Performance (continued)

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
POWER-DOWN CURRENT			
Power-Down Current vs Temperature		5.5 V	Figure 28
Power-Down Current vs Power-Supply Voltage		2.7 V – 5.5 V	Figure 29
Power-Down Current vs Temperature		2.7 V	Figure 73
POWER-SUPPLY CURRENT			
Power-Supply Current vs Temperature	External V_{REF}	5.5 V	Figure 20
	Internal V_{REF}		Figure 21
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 22
	Internal V_{REF}		Figure 23
Power-Supply Current Histogram	External V_{REF}		Figure 24
	Internal V_{REF}		Figure 25
Power-Supply Current vs Power-Supply Voltage	External V_{REF}	2.7 V – 5.5 V	Figure 26
	Internal V_{REF}		Figure 27
Power-Supply Current vs Temperature	External V_{REF}	3.6 V	Figure 49
	Internal V_{REF}		Figure 50
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 51
	Internal V_{REF}		Figure 52
Power-Supply Current Histogram	External V_{REF}		Figure 53
	Internal V_{REF}		Figure 54
Power-Supply Current vs Temperature	External V_{REF}	2.7 V	Figure 67
	Internal V_{REF}		Figure 68
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 69
	Internal V_{REF}		Figure 70
Power-Supply Current Histogram	External V_{REF}		Figure 71
	Internal V_{REF}		Figure 72

Table 5. Typical Characteristics: DAC Dynamic Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
CHANNEL-TO-CHANNEL CROSSTALK			
Channel-to-Channel Crosstalk	5-V Rising Edge	5.5 V	Figure 43
	5-V Falling Edge		Figure 44
CLOCK FEEDTHROUGH			
Clock Feedthrough	500 kHz, Midscale	5.5 V	Figure 48
		2.7 V	Figure 87
GLITCH ENERGY			
Glitch Energy, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	5.5 V	Figure 37
	Falling Edge, Code 8000h to 7FFFh		Figure 38
Glitch Energy, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 39
	Falling Edge, Code 8000h to 7FFCh		Figure 40
Glitch Energy, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 41
	Falling Edge, Code 8000h to 7FF0h		Figure 42
Glitch Energy, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	2.7 V	Figure 79
	Falling Edge, Code 8000h to 7FFFh		Figure 80
Glitch Energy, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 81
	Falling Edge, Code 8000h to 7FFCh		Figure 82
Glitch Energy, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 83
	Falling Edge, Code 8000h to 7FF0h		Figure 84
NOISE			
DAC Output Noise Density vs Frequency	External V_{REF}	5.5 V	Figure 45
	Internal V_{REF}		Figure 46
DAC Output Noise 0.1 Hz to 10 Hz	External V_{REF}		Figure 47
POWER-ON GLITCH			
Power-on Glitch	Reset to Zero Scale	5.5 V	Figure 35
	Reset to Midscale		Figure 36
	Reset to Zero Scale	2.7 V	Figure 85
	Reset to Midscale		Figure 86
SETTLING TIME			
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	5.5 V	Figure 31
	Falling Edge, Code FFFFh to 0h		Figure 32
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 33
	Falling Edge, Code C000h to 4000h		Figure 34
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	2.7 V	Figure 75
	Falling Edge, Code FFFFh to 0h		Figure 76
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 77
	Falling Edge, Code C000h to 4000h		Figure 78

TYPICAL CHARACTERISTICS: Internal Reference

At T_A = 25°C, AV_{DD} = 5.5 V, gain = 2 and V_{REFOUT}, unloaded unless otherwise noted.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

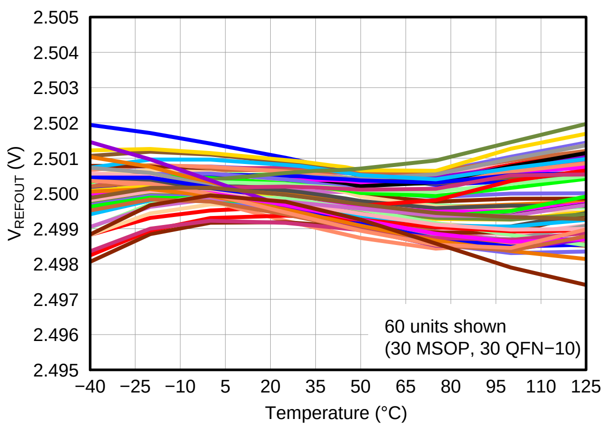


Figure 2.

INTERNAL REFERENCE VOLTAGE TEMPERATURE DRIFT HISTOGRAM

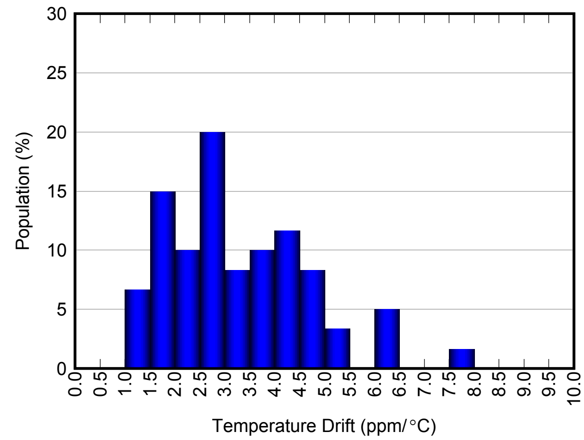


Figure 3.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT

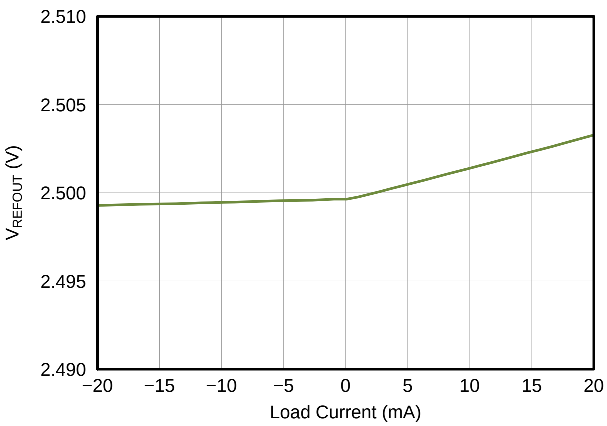


Figure 4.

INTERNAL REFERENCE VOLTAGE vs TIME

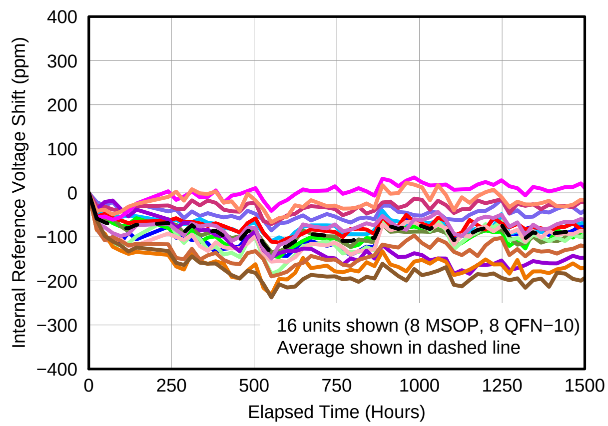


Figure 5.

INTERNAL REFERENCE NOISE DENSITY vs FREQUENCY

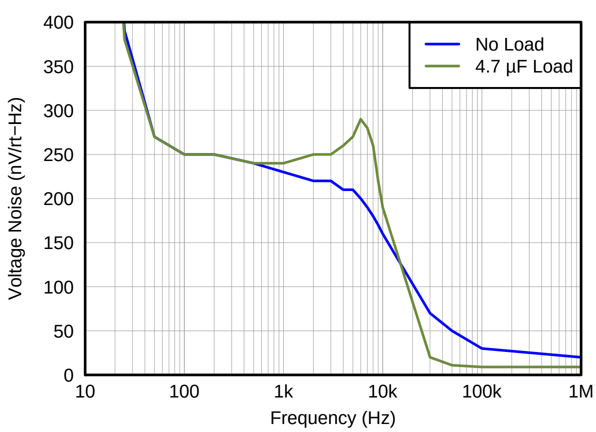


Figure 6.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE

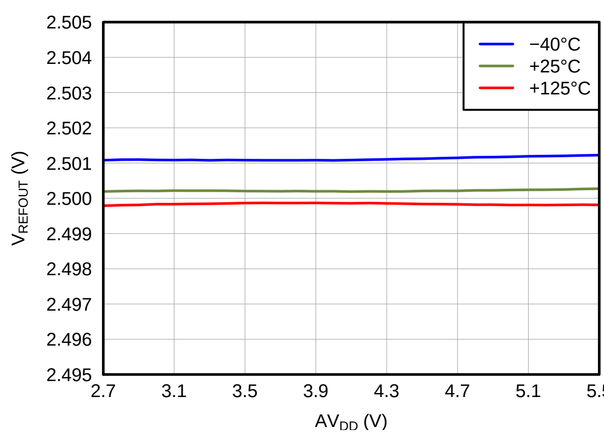


Figure 7.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

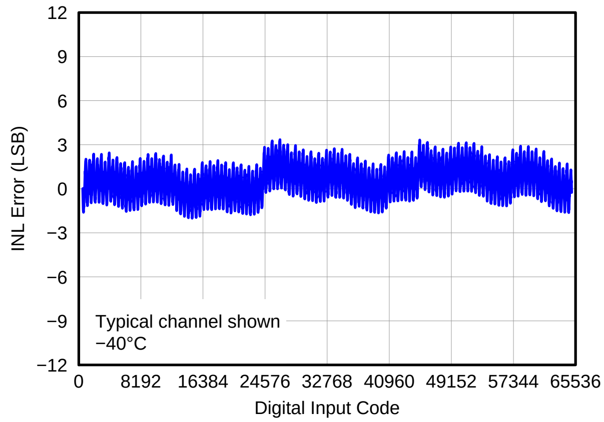


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

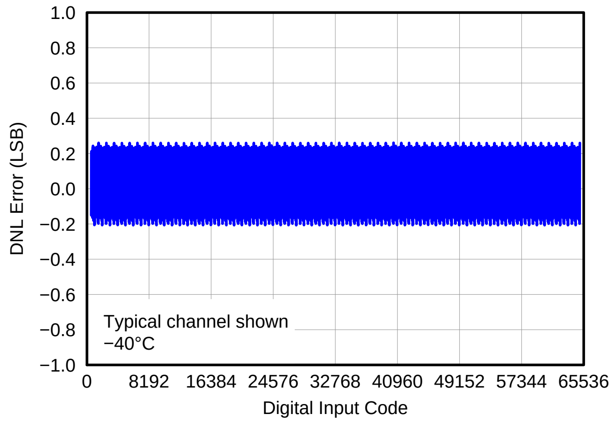


Figure 9.

LINEARITY ERROR vs DIGITAL INPUT CODE (25°C)

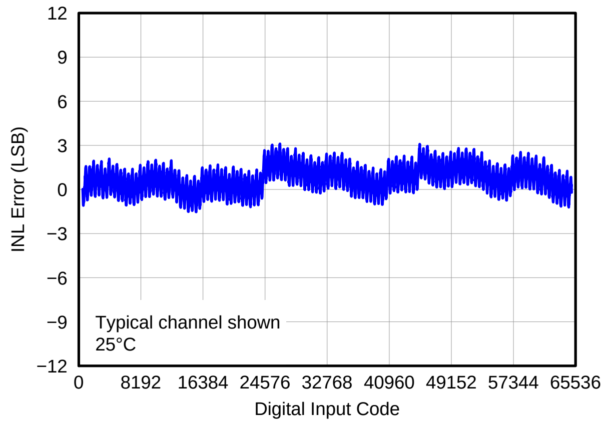


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (25°C)

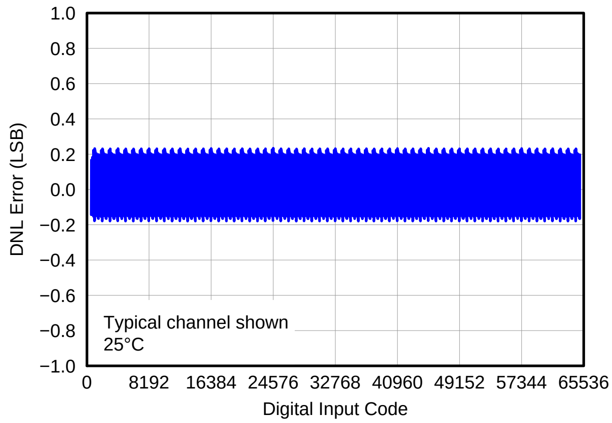


Figure 11.

LINEARITY ERROR vs DIGITAL INPUT CODE (125°C)

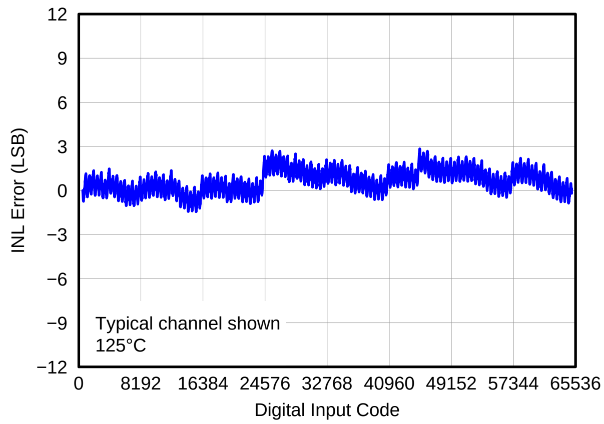


Figure 12.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (125°C)

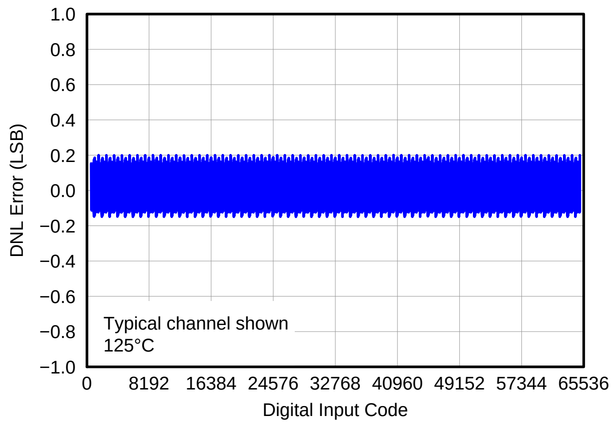


Figure 13.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

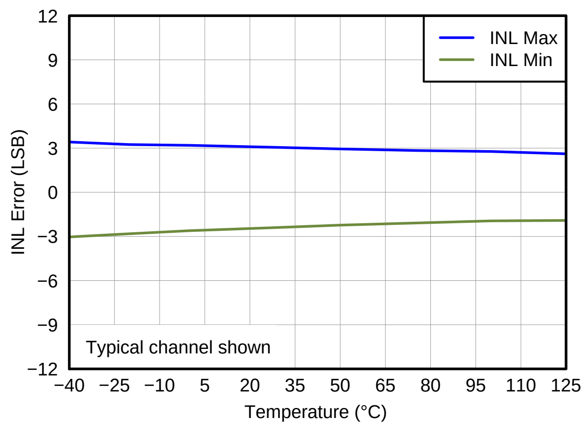


Figure 14.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

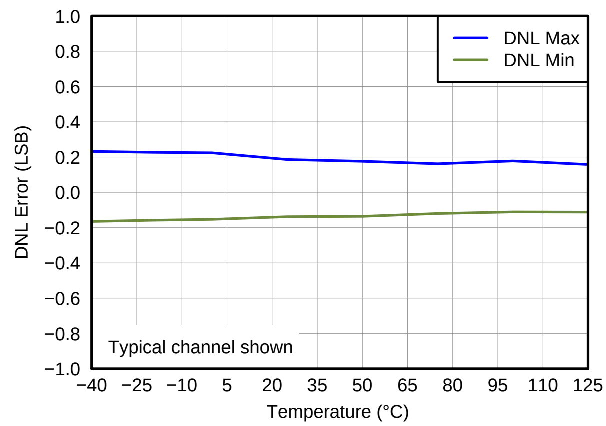


Figure 15.

FULL-SCALE ERROR vs TEMPERATURE

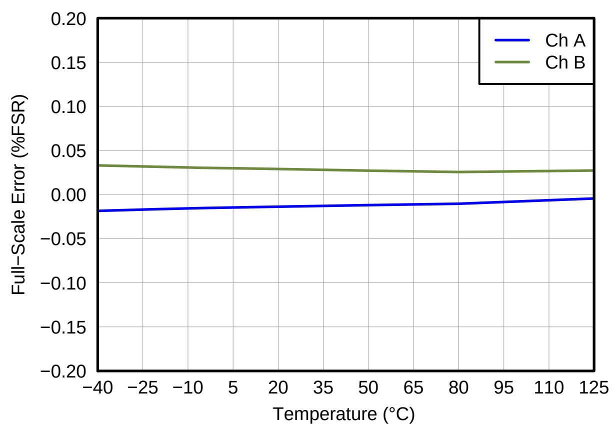


Figure 16.

GAIN ERROR vs TEMPERATURE

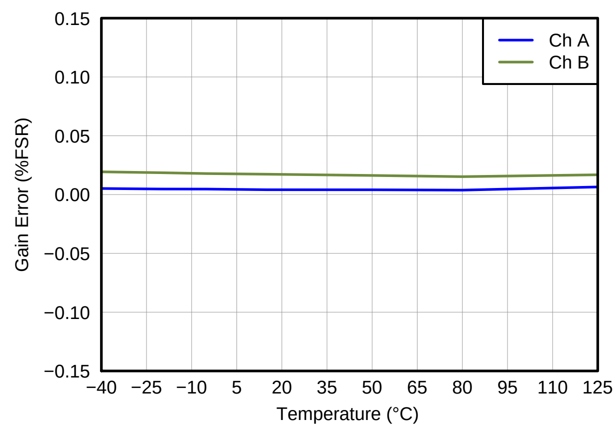


Figure 17.

OFFSET ERROR vs TEMPERATURE

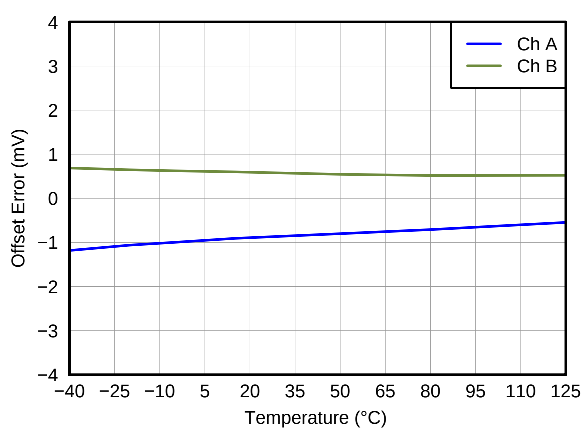


Figure 18.

ZERO-CODE ERROR vs TEMPERATURE

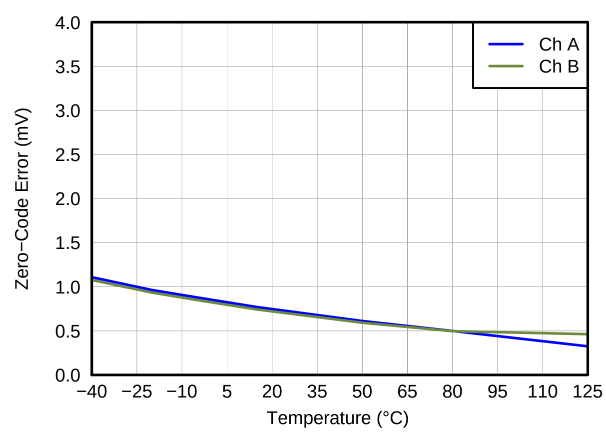


Figure 19.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-SUPPLY CURRENT vs TEMPERATURE

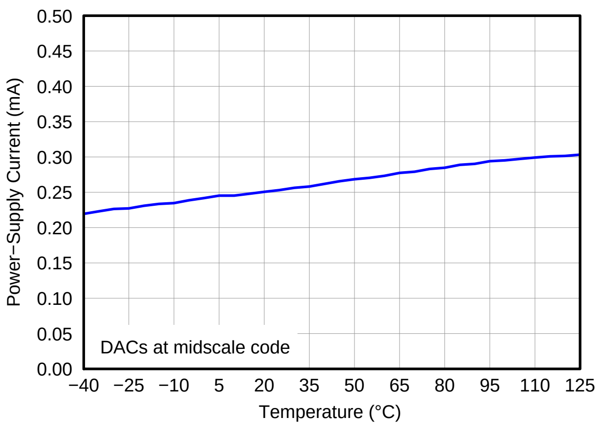


Figure 20.

POWER-SUPPLY CURRENT vs TEMPERATURE

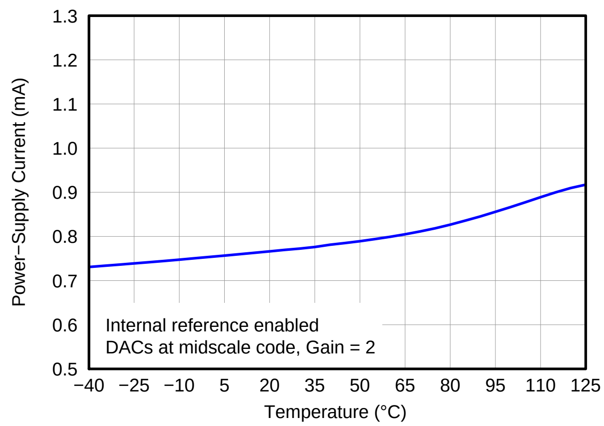


Figure 21.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

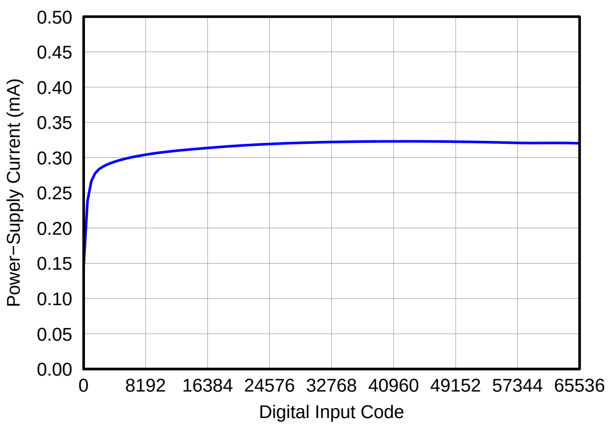


Figure 22.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

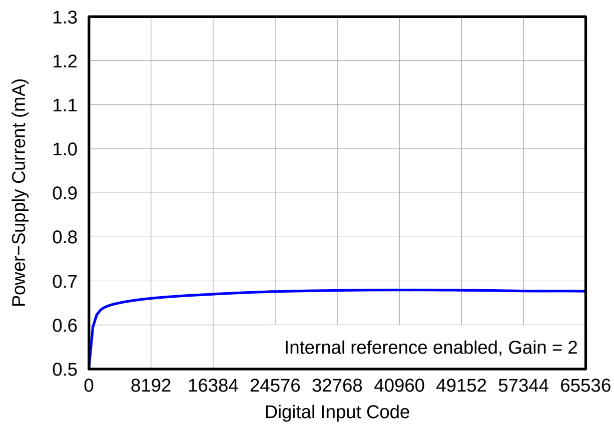


Figure 23.

POWER-SUPPLY CURRENT HISTOGRAM

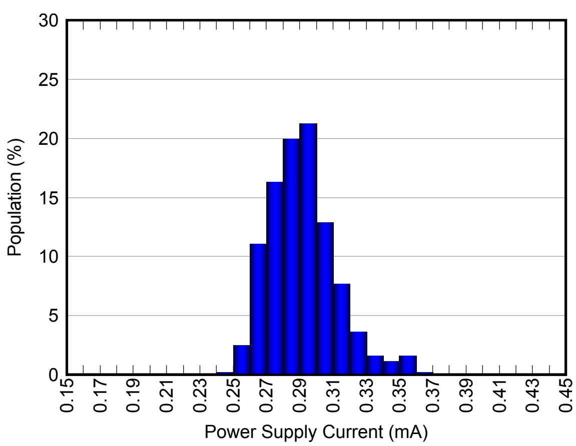


Figure 24.

POWER-SUPPLY CURRENT HISTOGRAM

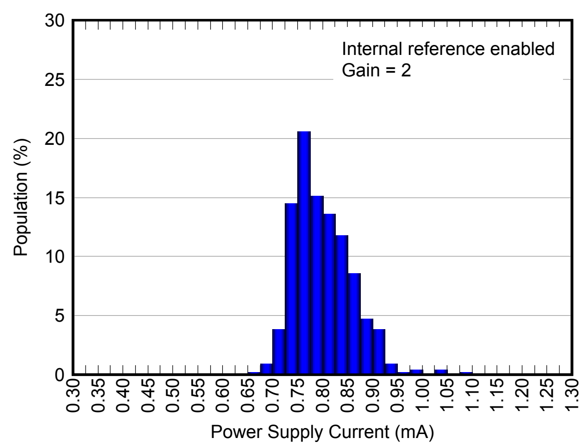


Figure 25.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

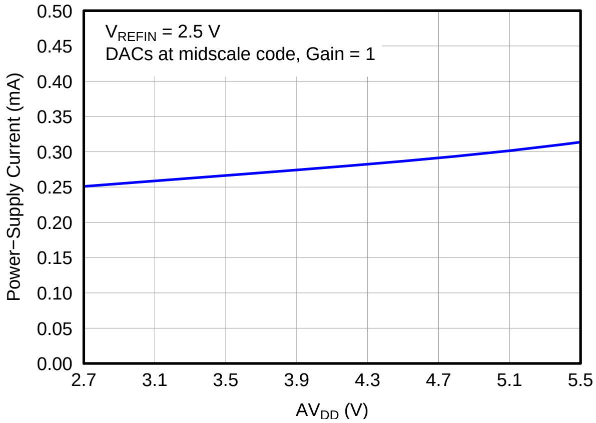


Figure 26.

POWER-SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

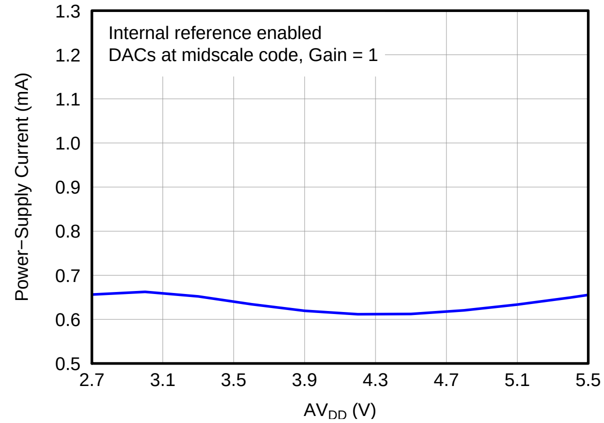


Figure 27.

POWER-DOWN CURRENT vs TEMPERATURE

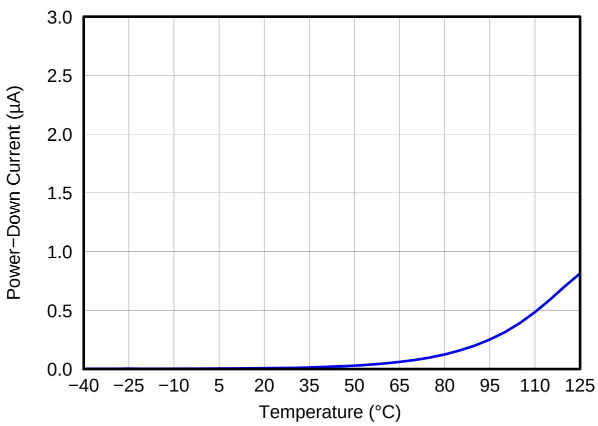


Figure 28.

POWER-DOWN CURRENT vs POWER-SUPPLY VOLTAGE

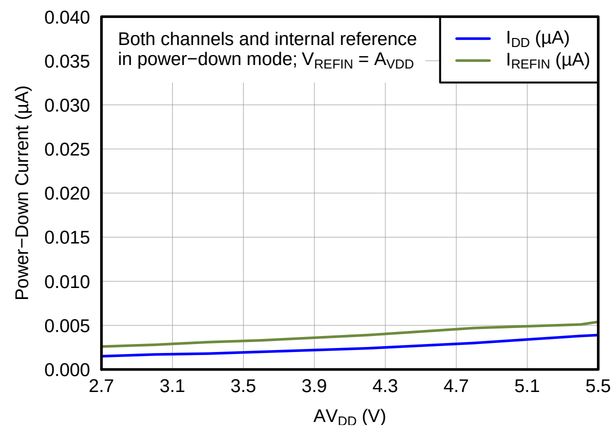


Figure 29.

DAC OUTPUT VOLTAGE vs LOAD CURRENT

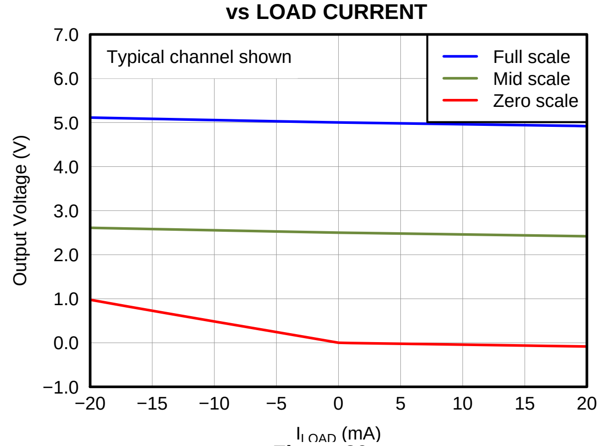


Figure 30.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

FULL-SCALE SETTLING TIME: RISING EDGE

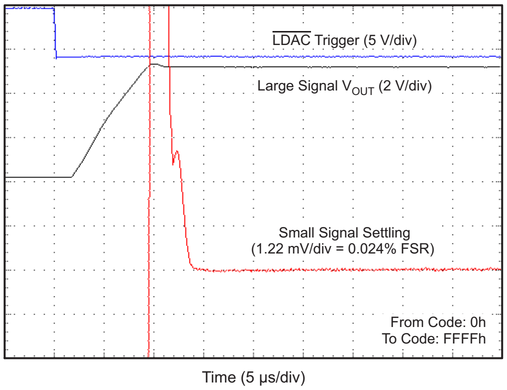


Figure 31.

FULL-SCALE SETTLING TIME: FALLING EDGE

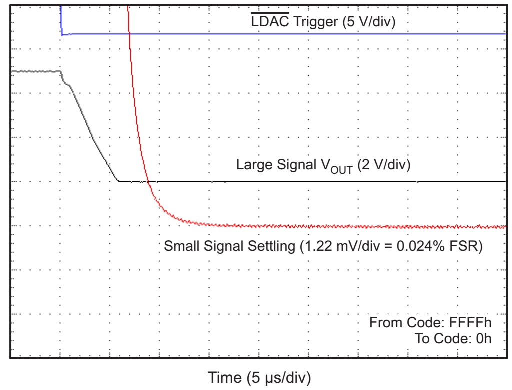


Figure 32.

HALF-SCALE SETTLING TIME: RISING EDGE

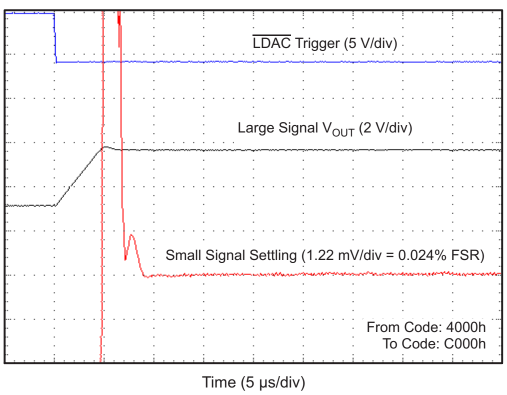


Figure 33.

HALF-SCALE SETTLING TIME: FALLING EDGE

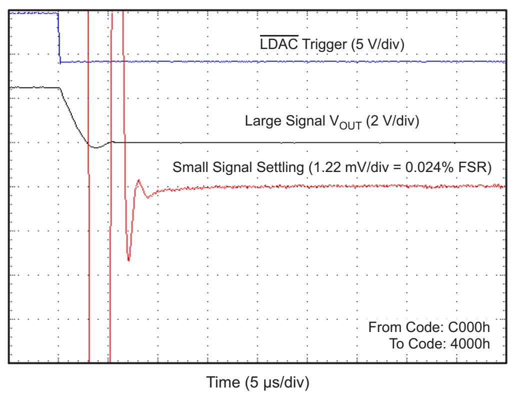


Figure 34.

POWER-ON GLITCH RESET TO ZERO SCALE

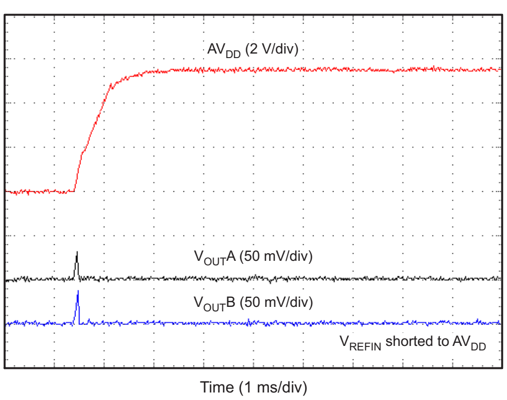


Figure 35.

POWER-ON GLITCH RESET TO MIDSCALE

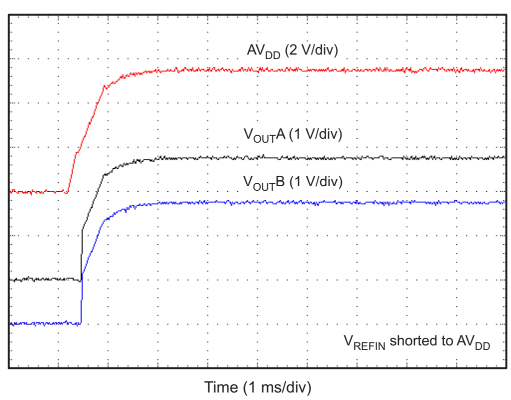


Figure 36.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

GLITCH ENERGY RISING EDGE, 1-LSB STEP

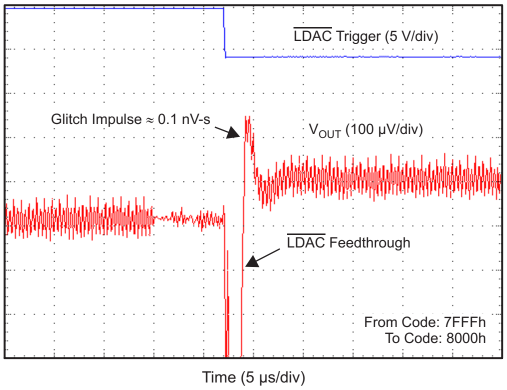


Figure 37.

GLITCH ENERGY FALLING EDGE, 1-LSB STEP

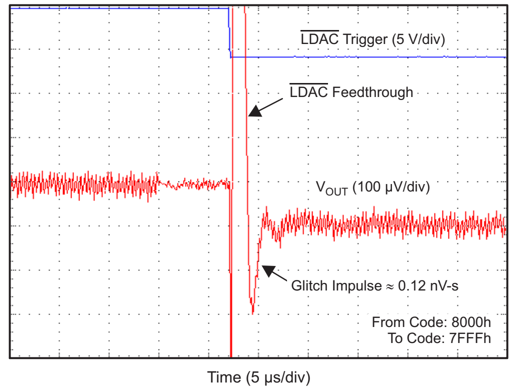


Figure 38.

GLITCH ENERGY RISING EDGE, 4-LSB STEP

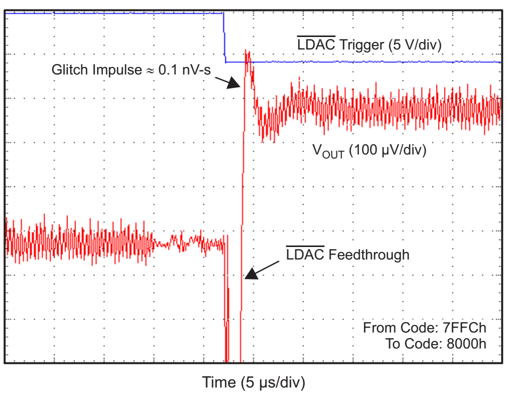


Figure 39.

GLITCH ENERGY FALLING EDGE, 4-LSB STEP

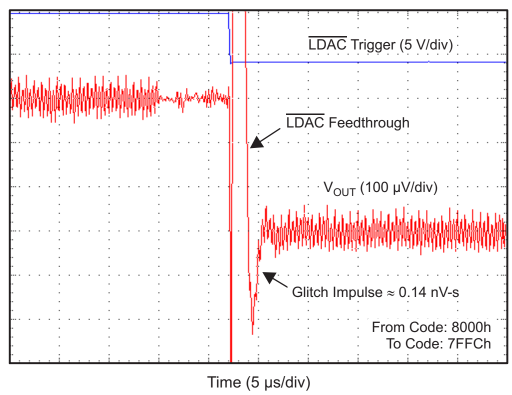


Figure 40.

GLITCH ENERGY RISING EDGE, 16-LSB STEP

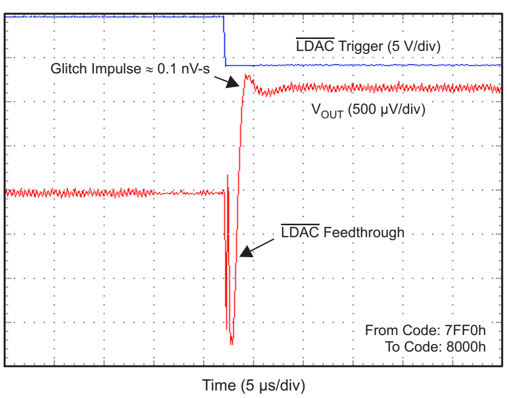


Figure 41.

GLITCH ENERGY FALLING EDGE, 16-LSB STEP

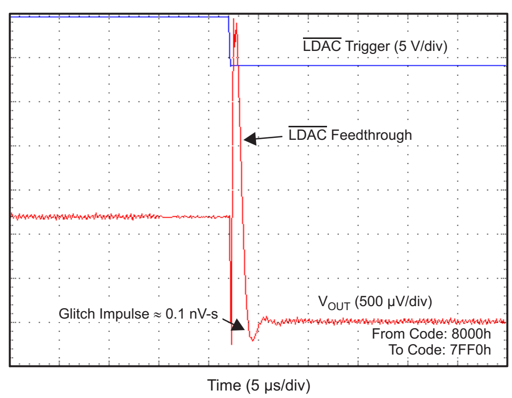


Figure 42.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

CHANNEL-TO-CHANNEL CROSSTALK 5-V RISING EDGE

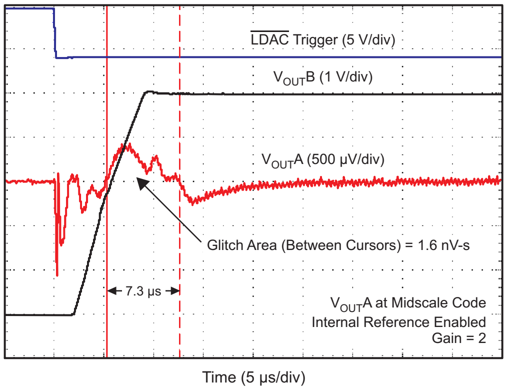


Figure 43.

CHANNEL-TO-CHANNEL CROSSTALK 5-V FALLING EDGE

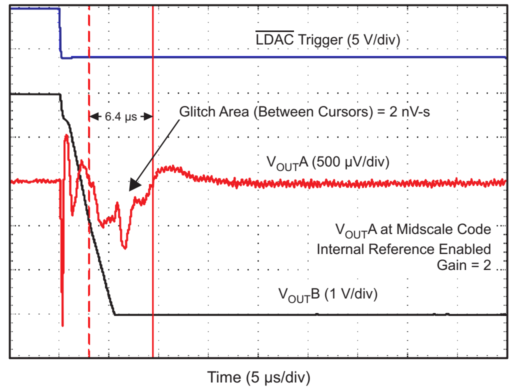


Figure 44.

DAC OUTPUT NOISE DENSITY vs FREQUENCY

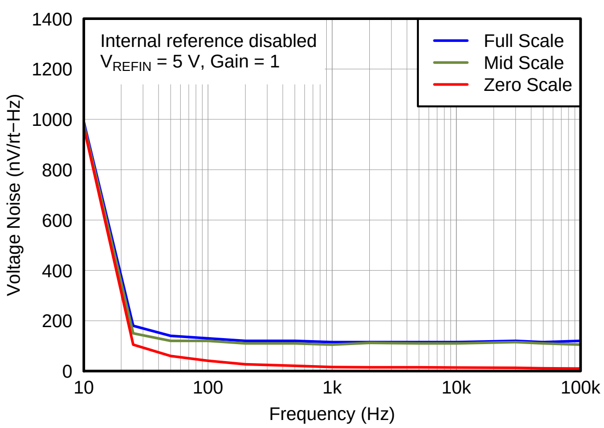


Figure 45.

DAC OUTPUT NOISE DENSITY vs FREQUENCY

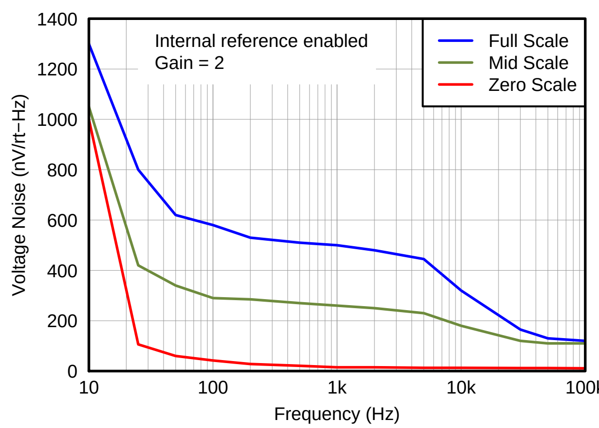


Figure 46.

DAC OUTPUT NOISE 0.1 Hz TO 10 Hz

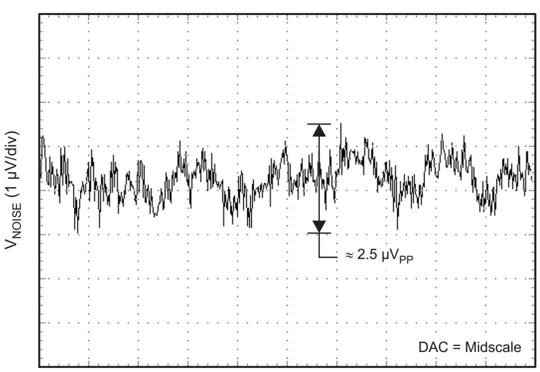


Figure 47.

CLOCK FEEDTHROUGH 500 kHz, MIDSCALE

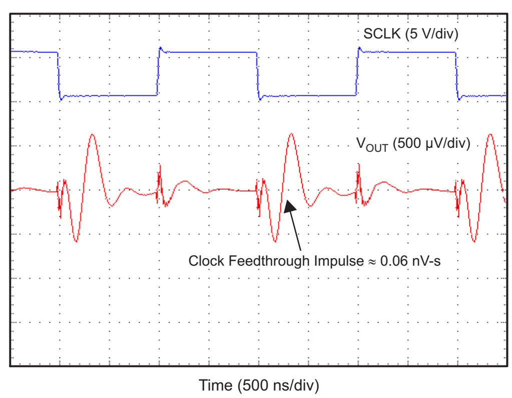


Figure 48.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 3.6 V

At T_A = 25°C, 3.3-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-SUPPLY CURRENT vs TEMPERATURE

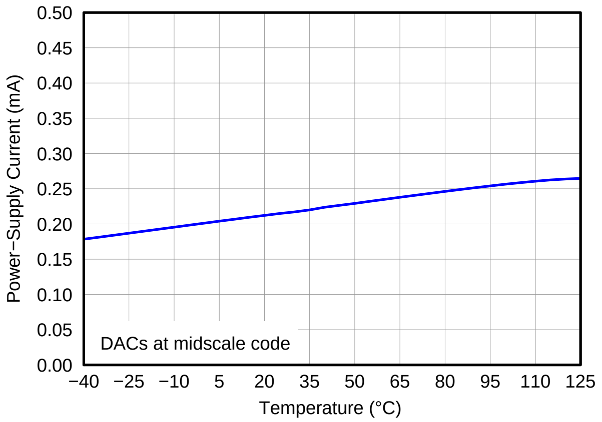


Figure 49.

POWER-SUPPLY CURRENT vs TEMPERATURE

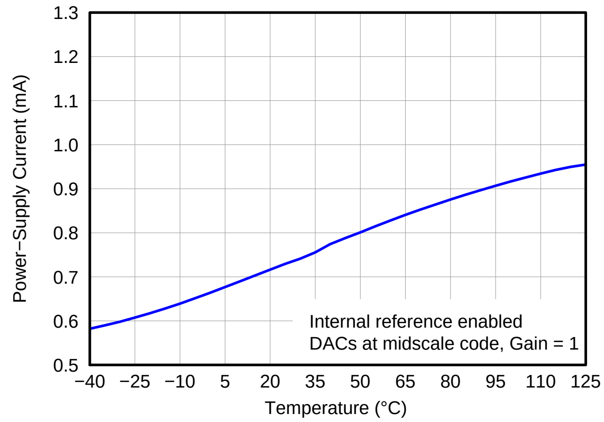


Figure 50.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

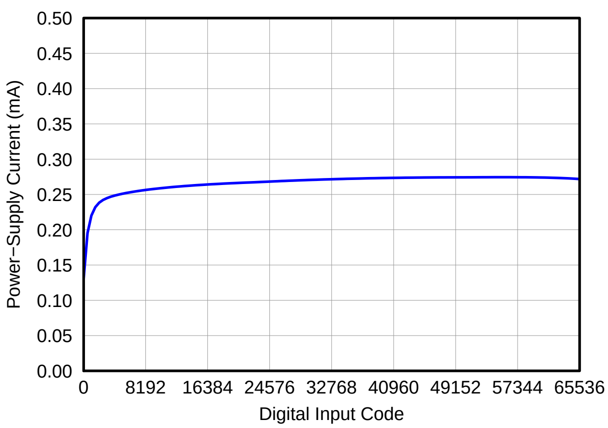


Figure 51.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

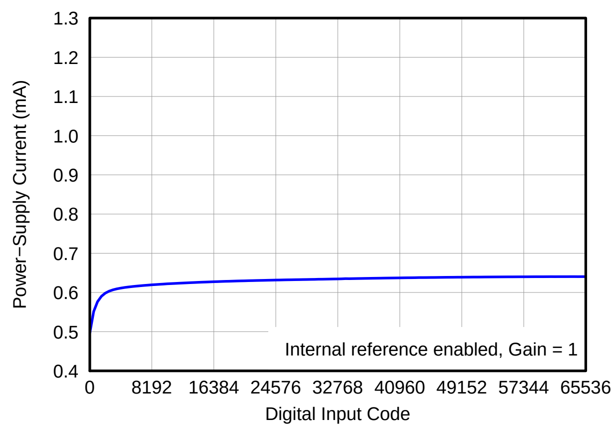


Figure 52.

POWER-SUPPLY CURRENT HISTOGRAM

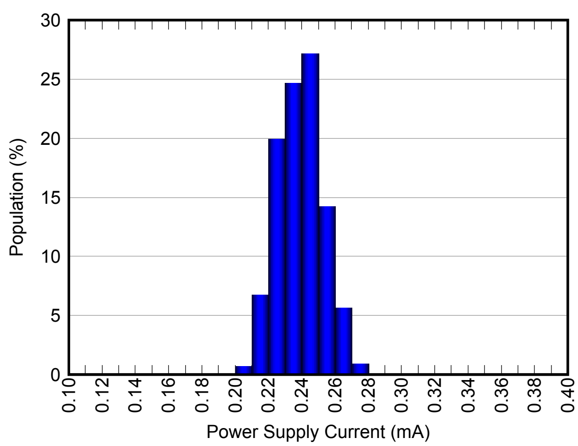


Figure 53.

POWER-SUPPLY CURRENT HISTOGRAM

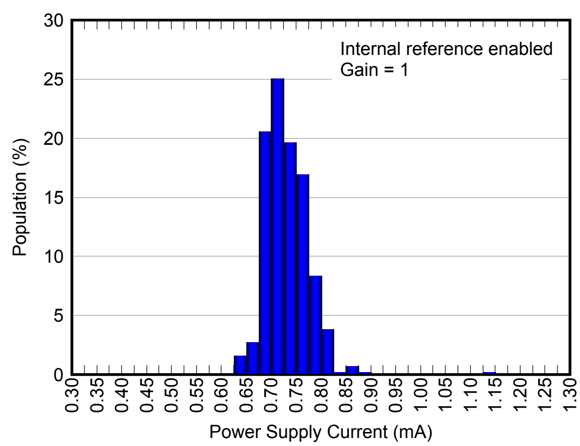


Figure 54.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

LINEARITY ERROR
vs DIGITAL INPUT CODE (–40°C)

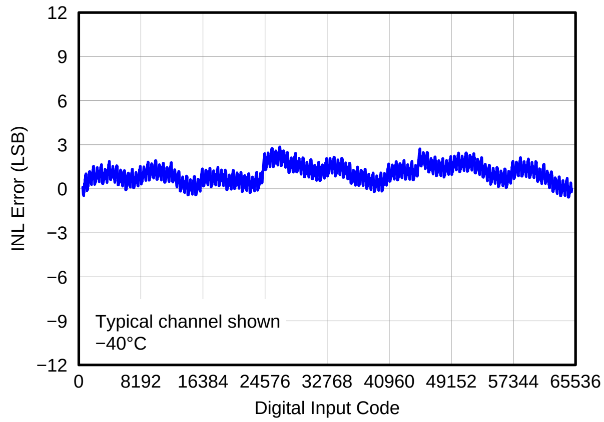


Figure 55.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE (–40°C)

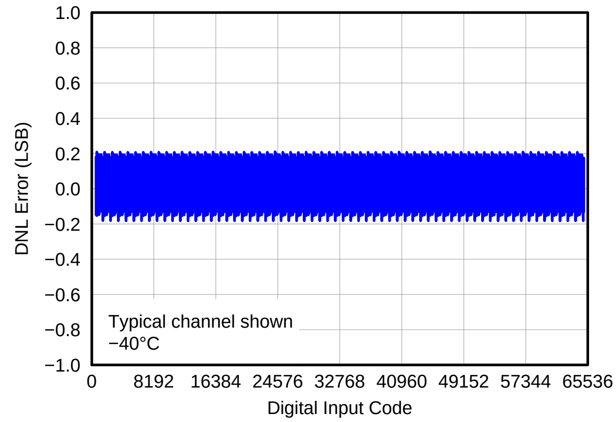


Figure 56.

LINEARITY ERROR
vs DIGITAL INPUT CODE (25°C)

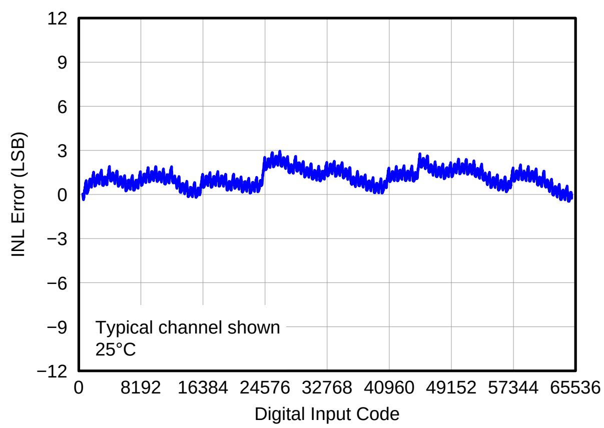


Figure 57.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE (25°C)

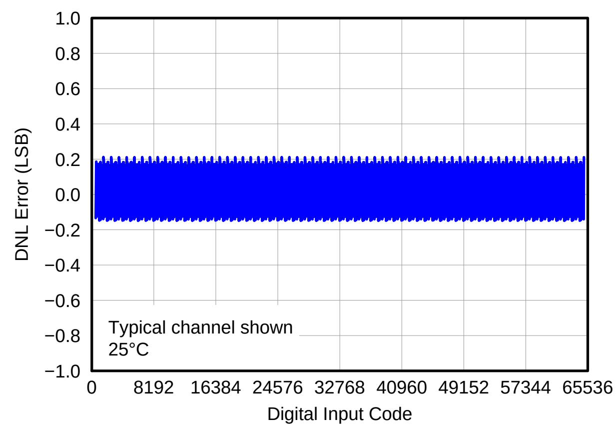


Figure 58.

LINEARITY ERROR
vs DIGITAL INPUT CODE (125°C)

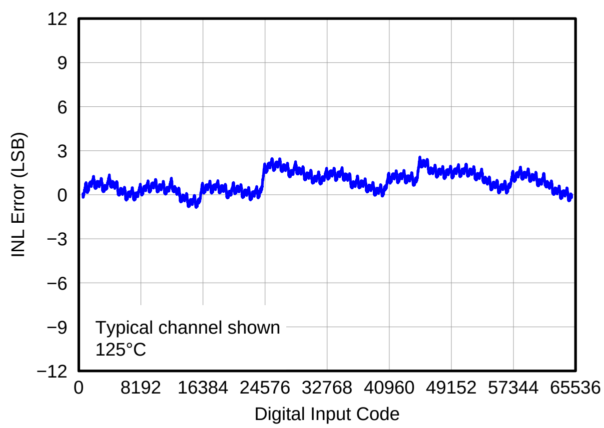


Figure 59.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE (125°C)

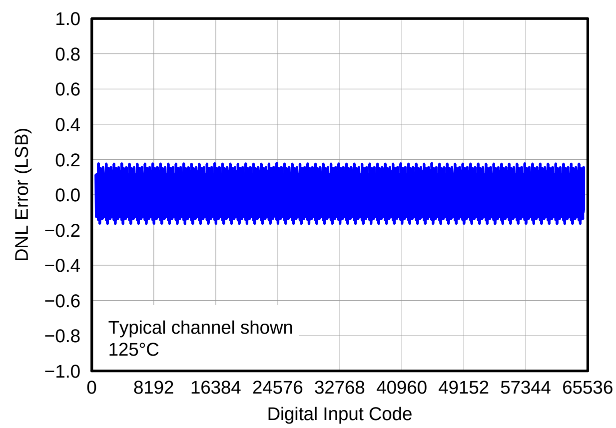


Figure 60.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

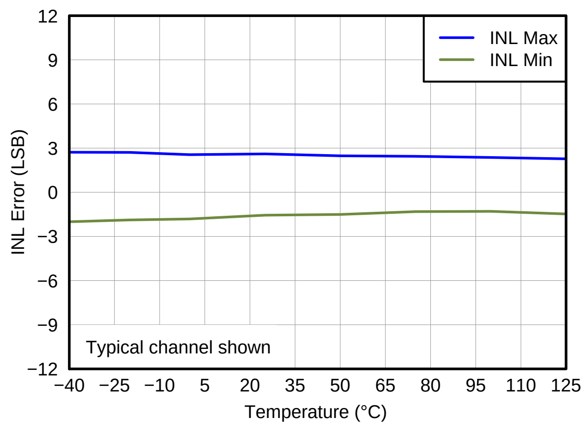


Figure 61.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

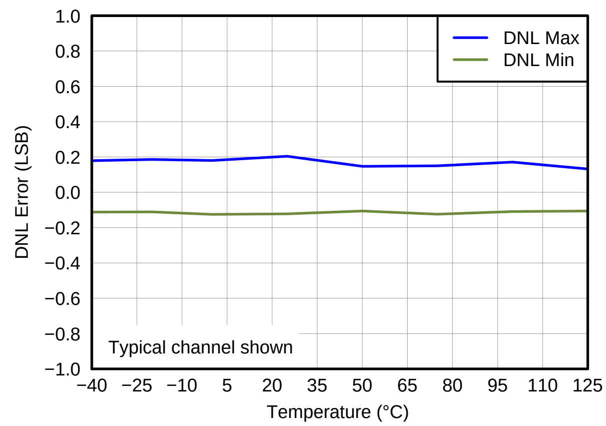


Figure 62.

FULL-SCALE ERROR vs TEMPERATURE

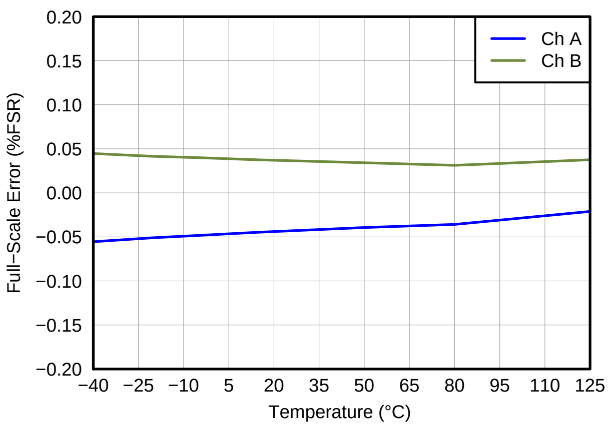


Figure 63.

GAIN ERROR vs TEMPERATURE

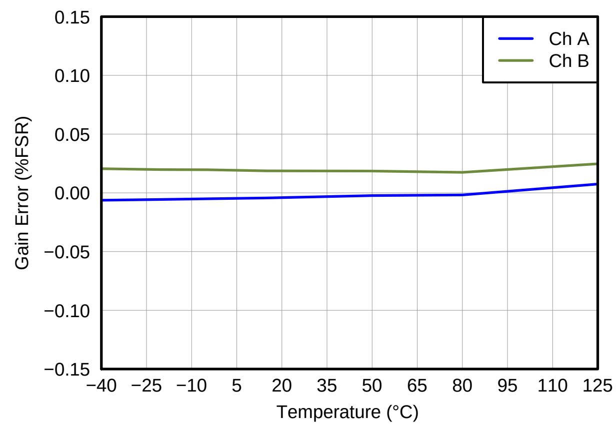


Figure 64.

OFFSET ERROR vs TEMPERATURE

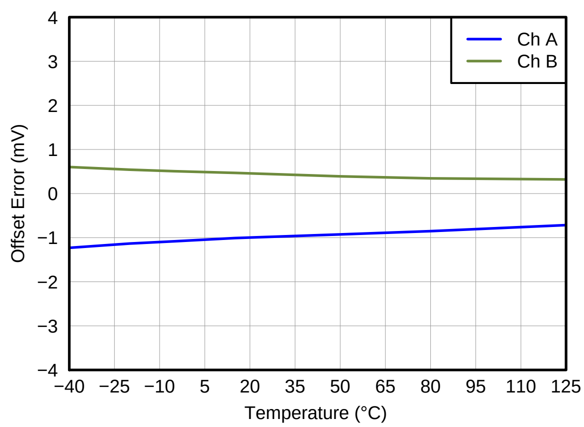


Figure 65.

ZERO-CODE ERROR vs TEMPERATURE

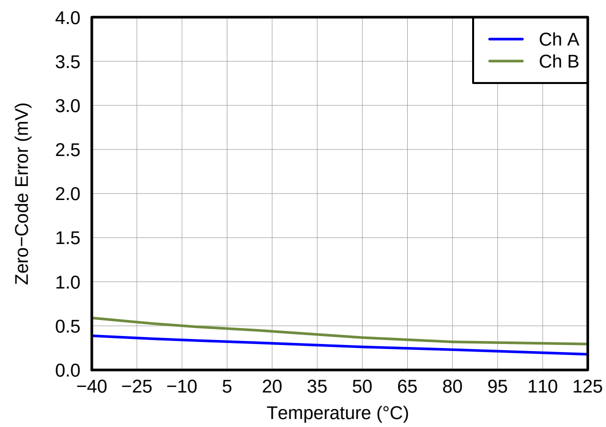


Figure 66.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-SUPPLY CURRENT vs TEMPERATURE

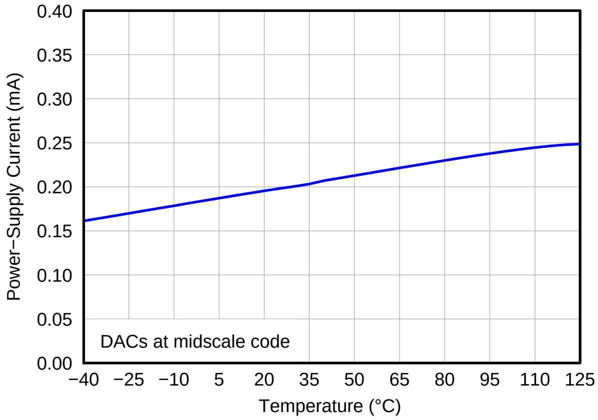


Figure 67.

POWER-SUPPLY CURRENT vs TEMPERATURE

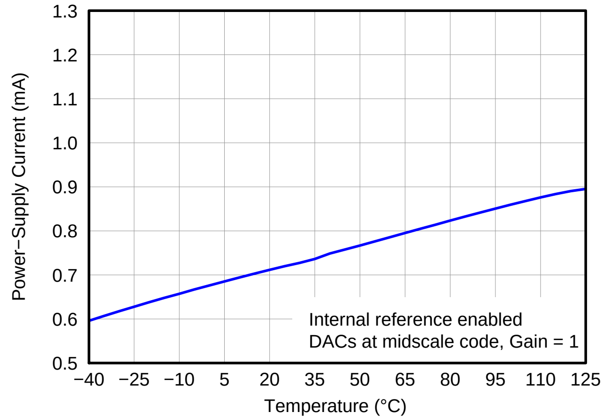


Figure 68.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

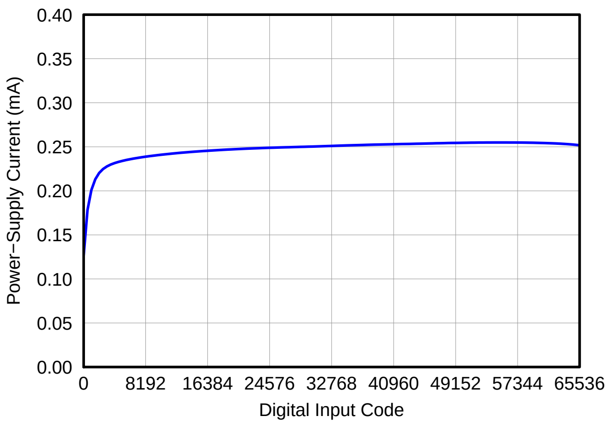


Figure 69.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

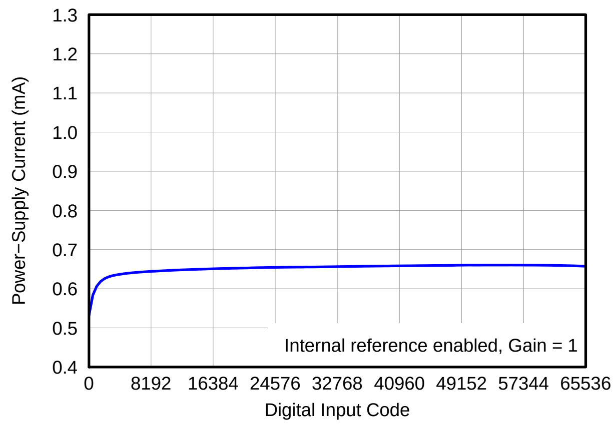


Figure 70.

POWER-SUPPLY CURRENT HISTOGRAM

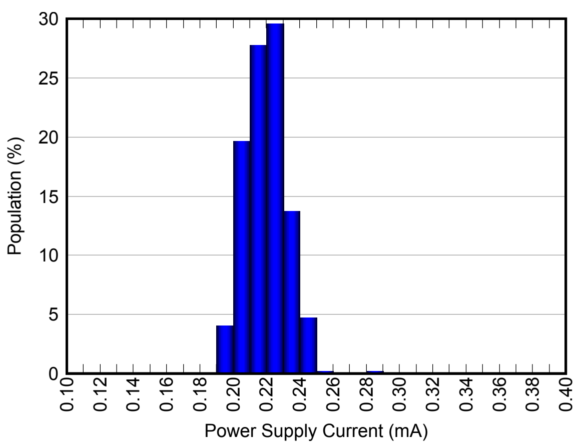


Figure 71.

POWER-SUPPLY CURRENT HISTOGRAM

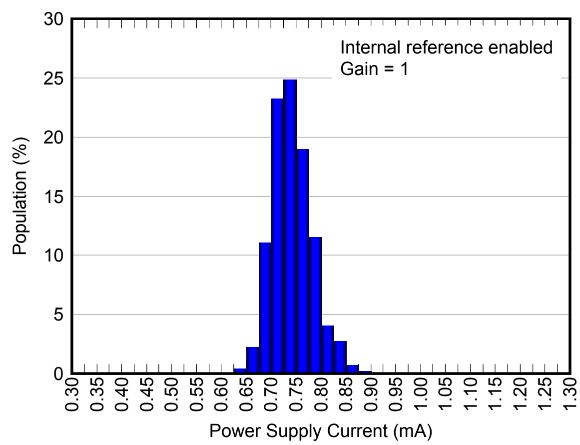


Figure 72.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-DOWN CURRENT vs TEMPERATURE

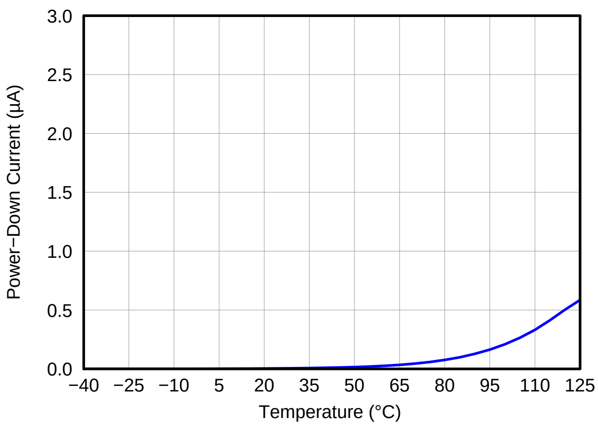


Figure 73.

DAC OUTPUT VOLTAGE vs LOAD CURRENT

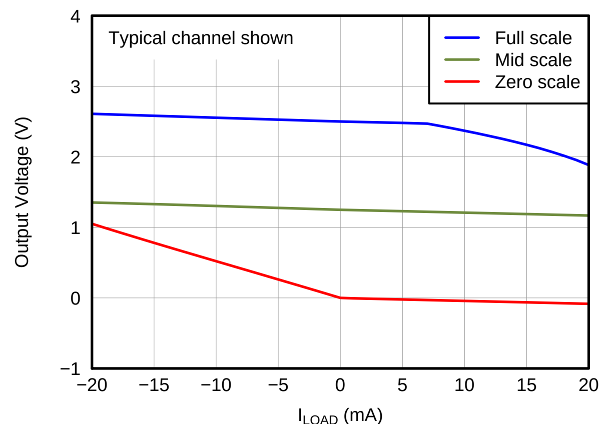


Figure 74.

FULL-SCALE SETTLING TIME: RISING EDGE

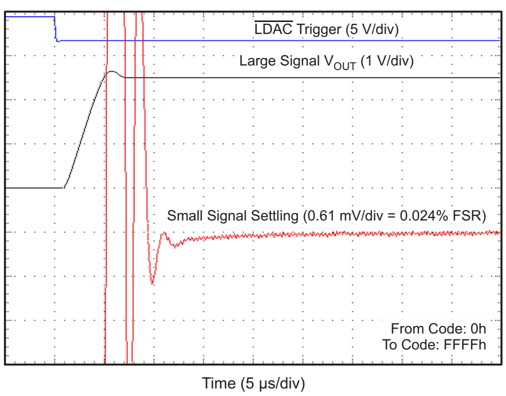


Figure 75.

FULL-SCALE SETTLING TIME: FALLING EDGE

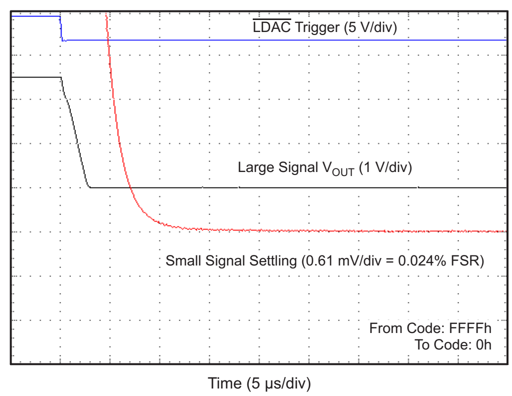


Figure 76.

HALF-SCALE SETTLING TIME: RISING EDGE

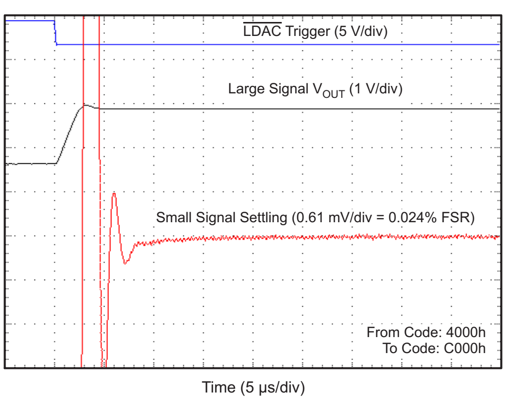


Figure 77.

HALF-SCALE SETTLING TIME: FALLING EDGE

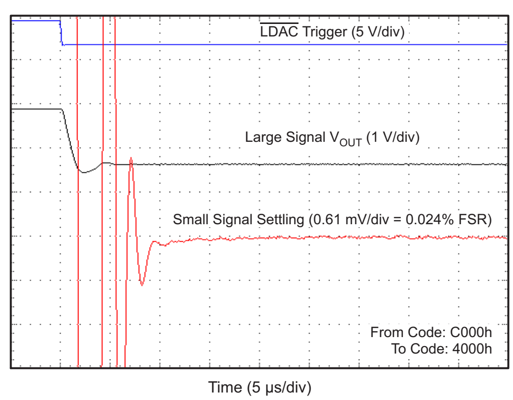


Figure 78.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

GLITCH ENERGY RISING EDGE, 1-LSB STEP

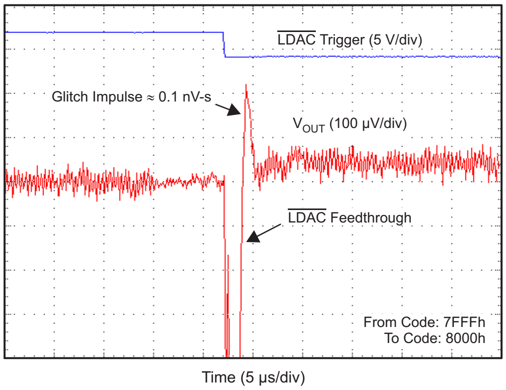


Figure 79.

GLITCH ENERGY FALLING EDGE, 1-LSB STEP

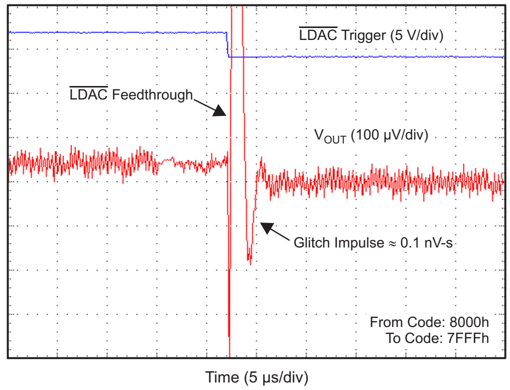


Figure 80.

GLITCH ENERGY RISING EDGE, 4-LSB STEP

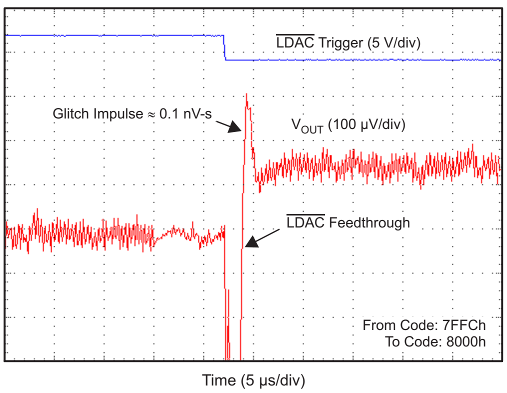


Figure 81.

GLITCH ENERGY FALLING EDGE, 4-LSB STEP

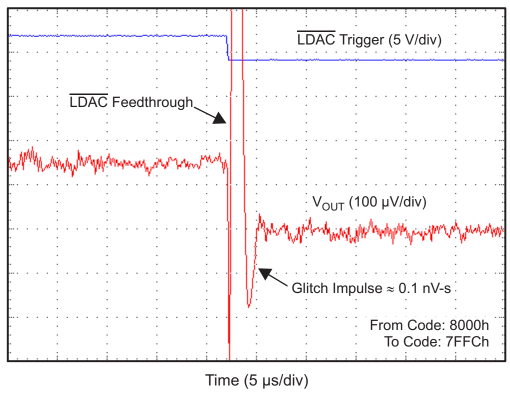


Figure 82.

GLITCH ENERGY RISING EDGE, 16-LSB STEP

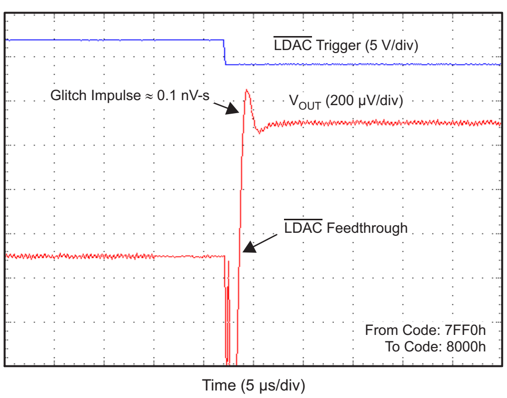


Figure 83.

GLITCH ENERGY FALLING EDGE, 16-LSB STEP

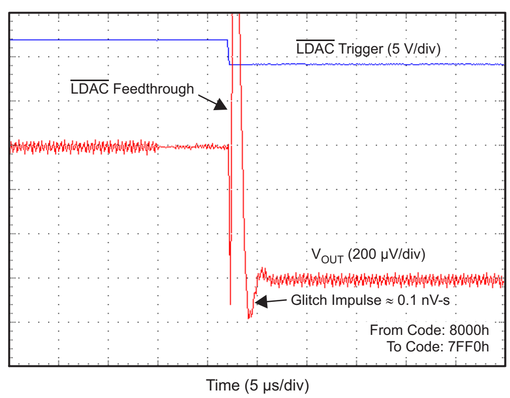


Figure 84.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

POWER-ON GLITCH
RESET TO ZERO SCALE

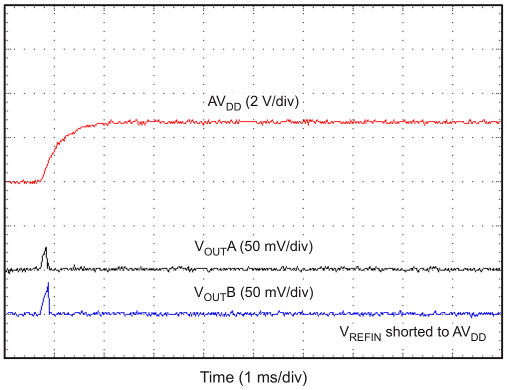


Figure 85.

POWER-ON GLITCH
RESET TO MIDSCALE

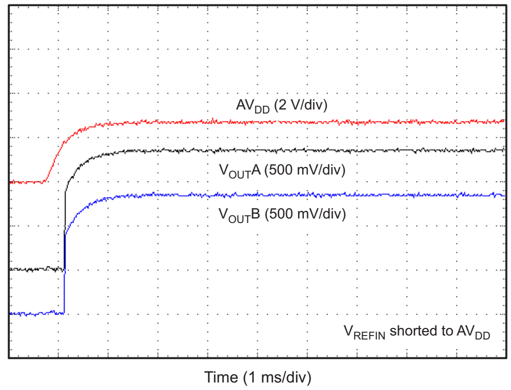


Figure 86.

CLOCK FEEDTHROUGH
500 kHz, MIDSCALE

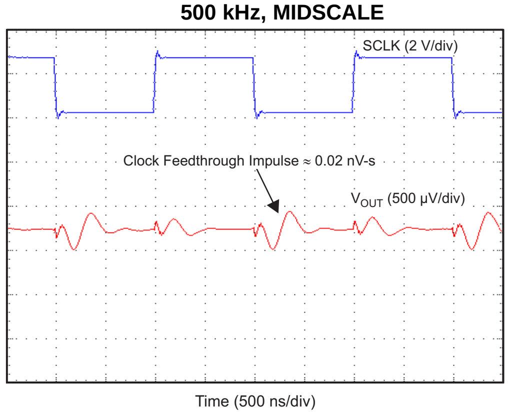


Figure 87.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC756x, DAC816x, and DAC856x architecture consists of two string DACs, each followed by an output buffer amplifier. The devices include an internal 2.5-V reference with 4-ppm/°C temperature drift performance. Figure 88 shows a principal block diagram of the DAC architecture.

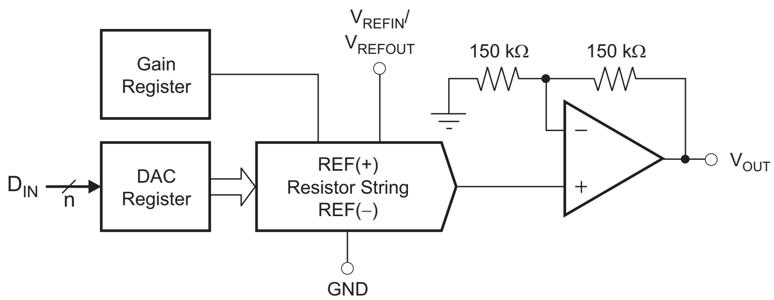


Figure 88. DAC Architecture

The input coding to the DAC756x, DAC816x, and DAC856x is straight binary, so the ideal output voltage is given by Equation 1:

$$V_{OUT} = \left(\frac{D_{IN}}{2^n}\right) \times V_{REF} \times Gain \tag{1}$$

where:

n = resolution in bits; either 12 (DAC756x), 14 (DAC816x) or 16 (DAC856x)

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. D_{IN} ranges from 0 to 2^n – 1.

V_{REF} = DAC reference voltage; either V_{REFOUT} from the internal 2.5-V reference or V_{REFIN} from an external reference.

Gain = 1 by default when internal reference is disabled (using external reference), and gain = 2 by default when using internal reference. Gain can also be manually set to either 1 or 2 using the gain register. See the *GAIN REGISTERS* section for more information.

Resistor String

The resistor string section is shown in Figure 89. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. The resistor string architecture guarantees monotonicity. The $R_{DIVIDER}$ switch is controlled by the gain registers (see the *GAIN REGISTERS* section). Because the output amplifier has a gain of two, $R_{DIVIDER}$ is not shorted when the DAC-n gain is set to one (default if internal reference is disabled), and is shorted when the DAC-n gain is set to two (default if internal reference is enabled).

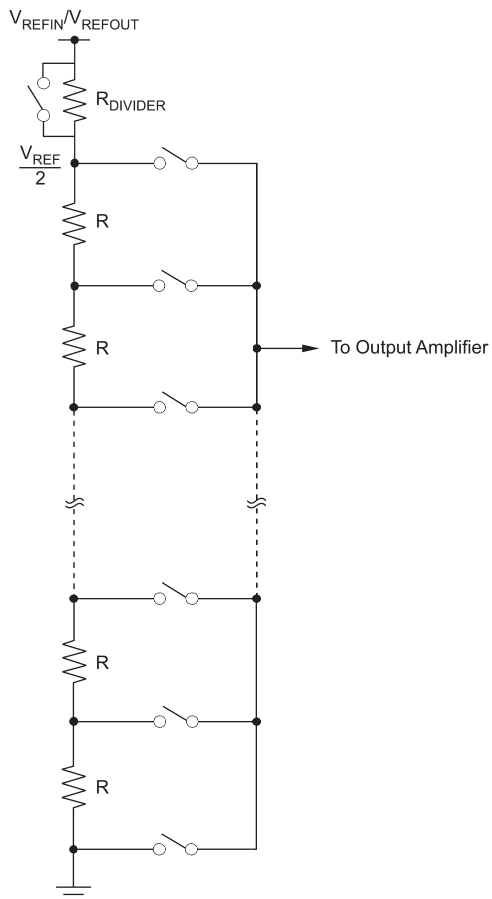


Figure 89. Resistor String

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0 V to AV_{DD}. It is capable of driving a load of 2 kΩ in parallel with 3 nF to GND. The typical slew rate is 0.75 V/μs, with a typical full-scale settling time of 14 μs as shown in Figure 31, Figure 32, Figure 75 and Figure 76.

INTERNAL REFERENCE

The DAC756x, DAC816x, and DAC856x include a 2.5-V internal reference that is disabled by default. The internal reference is externally available at the V_{REFIN}/V_{REFOUT} pin. The internal reference output voltage is 2.5 V and can sink and source up to 20 mA.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC756x, DAC816x, and DAC856x is a bipolar transistor based precision bandgap voltage reference. Figure 90 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages (V_{BE1} – V_{BE2}) has a positive temperature coefficient and is forced across resistor R_1. This voltage is amplified and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100 mA.

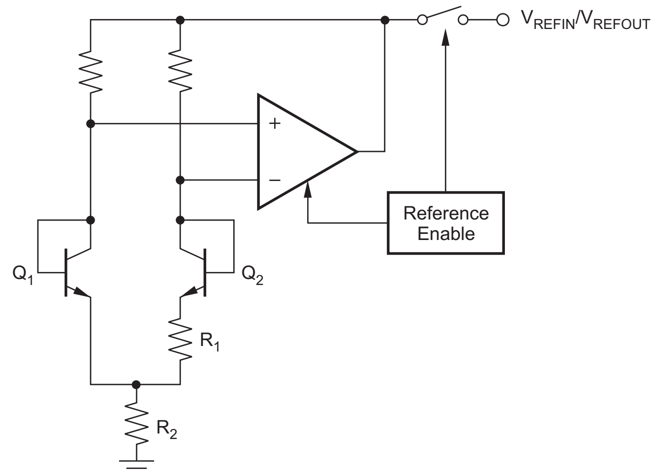


Figure 90. Bandgap Reference Simplified Schematic

POWER-ON RESET

Power-On Reset to Zero-scale

The DAC7562, DAC8162, and DAC8562 contain a power-on-reset circuit that controls the output voltage during power up. All device registers are reset as shown in Table 6. At power up all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before power is applied to the device. The internal reference is disabled by default and remains that way until a valid reference-change command is executed.

Power-On Reset to Mid-scale

The DAC7563, DAC8163, and DAC8563 contain a power-on reset circuit that controls the output voltage during power up. At power up, all DAC registers are reset to mid-scale code and the output voltages of all DAC channels are set to V_{REFIN}/2 volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before power is applied to the device. The internal reference is powered off/down by default and remains that way until a valid reference-change command is executed. If using an external reference, it is acceptable to power on the V_{REFIN} either at the same time as or after AV_{DD} is applied.

Table 6. DACxx62 and DACxx63 Power-On Reset Values

REGISTER	DEFAULT SETTING	
DAC and Input registers	DACxx62	Zero-scale
	DACxx63	Mid-scale
LDAC registers	$\overline{\text{LDAC}}$ pin enabled for both channels	
Power-down registers	DACs powered up	
Internal reference register	Internal reference disabled	
Gain registers	Gain = 1 for both channels	

$\overline{\text{CLR}}$ FUNCTIONALITY

The edge-triggered $\overline{\text{CLR}}$ pin can be used to set the input and DAC registers immediately according to Table 7. When the $\overline{\text{CLR}}$ pin receives a falling edge signal the clear mode is activated and changes the DAC output voltages accordingly. The part exits clear mode on the 24^{th} falling edge of the next write to the part. If the $\overline{\text{CLR}}$ pin receives a falling edge signal during a write sequence in normal operation, the clear mode is activated and changes the input and DAC registers immediately according to Table 7.

Table 7. Clear Mode Reset Values

DEVICE	DAC Output Entering Clear Mode
DAC8562, DAC8162, DAC7562	Zero-scale
DAC8563, DAC8163, DAC7563	Mid-scale

SERIAL INTERFACE

The DAC756x, DAC816x, and DAC856x have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and D_{IN}; see the Pin Descriptions) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram (Figure 1) for an example of a typical write sequence.

The DAC756x, DAC816x, or DAC856x input shift register is 24-bits wide, consisting of two *don't care* bits (DB23 to DB22), three command bits (DB21 to DB19), three address bits (DB18 to DB16), and 16 data bits (DB15 to DB0). The 16 data bits comprise the 16-, 14-, or 12-bit input code. All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register. It is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register, and any further clocking of data is ignored. When the DAC registers are being written to, the DAC756x, DAC816x, and DAC856x receive all 24 bits of data, ignore DB23 and DB22, and decode the next three bits (DB21 to DB19) in order to determine the DAC operating/control mode (see Table 8 through Table 10). Bits DB18 to DB16 are used to address DAC channels. The next 16/14/12 bits of data that follow are decoded by the DAC to determine the equivalent analog output. For more details on these and other commands (such as write to LDAC register, power down DACs, etc.), see their respective sections.

The data format is straight binary, with all 0s corresponding to 0-V output and all 1s corresponding to full-scale output. For all documentation purposes, the data format and representation used here is a true 16-bit pattern (that is, FFFFh data word for full scale) that the DAC756x, DAC816x, and DAC856x require.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the DAC756x, DAC816x, and DAC856x compatible with high-speed DSPs. On the 24^{th} falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data.

After receiving the 24^{th} falling clock edge, the DAC756x, DAC816x, and DAC856x decode the three command bits and three address bits and 16/14/12 data bits to perform the required function, without waiting for a $\overline{\text{SYNC}}$ rising edge. After the 24^{th} falling edge of SCLK is received, the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, the minimum delay time from the 24^{th} falling SCLK edge to the next falling $\overline{\text{SYNC}}$ edge must be met in order to begin the next cycle properly; see the Serial Write Operation timing diagram (Figure 1).

A rising edge of $\overline{\text{SYNC}}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. A new write sequence starts at the next falling edge of $\overline{\text{SYNC}}$. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible.

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24^{th} falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 23^{rd} falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 91).

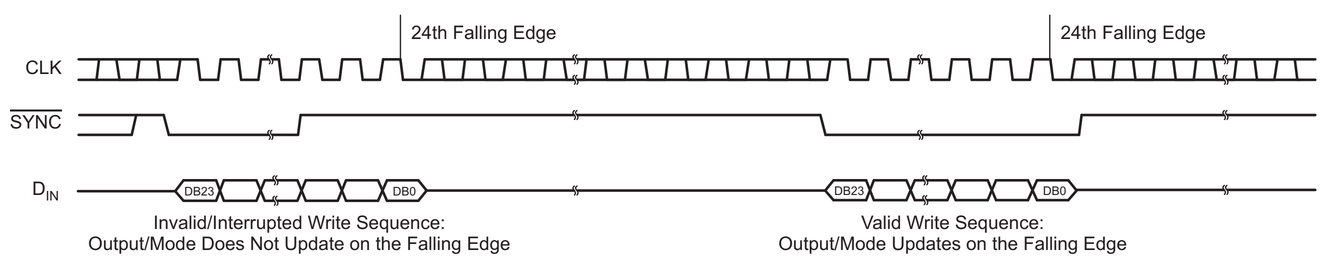


Figure 91. $\overline{\text{SYNC}}$ Interrupt Facility

Input Shift Register

The input shift register (SR) of the DAC856x, DAC816x, and DAC756x is 24 bits wide (as shown in Table 8, Table 9, and Table 10, respectively), and consists of two *don't care* bits (DB23 to DB22), three command bits (DB21 to DB19), three address bits (DB18 to DB16), and 16 data bits (DB15 to DB0). The 16 data bits comprise the 16-, 14-, or 12-bit input code.

Table 8. DAC856x Data Input Register Format

		Command			Address			Data															
X[(1)]	X	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DB23																							DB0

(1) X' denotes *don't care* bits.

Table 9. DAC816x Data Input Register Format

		Command			Address			Data															
X	X	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
DB23																							DB0

Table 10. DAC756x Data Input Register Format

		Command			Address			Data															
X	X	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
DB23																							DB0

The DAC856x, DAC816x, and DAC756x support a number of different load commands. The load commands are summarized in Table 11 and Table 12, and fully exhausted in Table 13.

Table 11. Commands for the DAC856x, DAC816x, and DAC756x

C2 (DB21)	C1 (DB20)	C0 (DB19)	Command
0	0	0	Write to input register n (Table 12)
0	0	1	Software LDAC, update DAC register n (Table 12)
0	1	0	Write to input register n (Table 12) and update all DAC registers
0	1	1	Write to input register n and update DAC register n (Table 12)
1	0	0	Set DAC power up/down mode
1	0	1	Software reset
1	1	0	Set LDAC registers
1	1	1	Enable/disable internal reference

Table 12. Address Select for the DAC856x, DAC816x, and DAC756x

A2 (DB18)	A1 (DB17)	A0 (DB16)	Channel (n)
0	0	0	DAC-A
0	0	1	DAC-B
0	1	0	Gain (only use with command 000)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	DAC-A and DAC-B

Table 13. Command Matrix for the DAC856x, DAC816x, and DAC756x

DB23-DB22	Command			Address			Data						DESCRIPTION
	C2	C1	C0	A2	A1	A0	DB15-DB6	DB5	DB4	DB3-DB2	DB1	DB0	
X[(1)]	0	0	0	0	0	0	16/14/12 bit DAC data						Write to DAC-A input register
				0	0	1	16/14/12 bit DAC data						Write to DAC-B input register
				1	1	1	16/14/12 bit DAC data						Write to DAC-A and DAC-B input registers
X	0	1	0	0	0	0	16/14/12 bit DAC data						Write to DAC-A input register and update all DACs
				0	0	1	16/14/12 bit DAC data						Write to DAC-B input register and update all DACs
				1	1	1	16/14/12 bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	1	1	0	0	0	16/14/12 bit DAC data						Write to DAC-A input register and update DAC-A
				0	0	1	16/14/12 bit DAC data						Write to DAC-B input register and update DAC-B
				1	1	1	16/14/12 bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	0	1	0	0	0	X						Update DAC-A
				0	0	1	X						Update DAC-B
				1	1	1	X						Update all DACs
X	0	0	0	0	1	0	X				0	0	Gain: DAC-B gain = 2, DAC-A gain = 2 (default with internal V_{REF})
											0	1	Gain: DAC-B gain = 2, DAC-A gain = 1
											1	0	Gain: DAC-B gain = 1, DAC-A gain = 2
											1	1	Gain: DAC-B gain = 1, DAC-A gain = 1 (power-on default)
X	1	0	0	X			X	0	0	X	0	1	Power up DAC-A
											1	0	Power up DAC-B
											1	1	Power up DAC-A and DAC-B
X	1	0	0	X			X	0	1	X	0	1	Power down DAC-A; 1 kΩ to GND
											1	0	Power down DAC-B; 1 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 1 kΩ to GND
X	1	0	0	X			X	1	0	X	0	1	Power down DAC-A; 100 kΩ to GND
											1	0	Power down DAC-B; 100 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 100 kΩ to GND
X	1	0	0	X			X	1	1	X	0	1	Power down DAC-A; Hi-Z
											1	0	Power down DAC-B; Hi-Z
											1	1	Power down DAC-A and DAC-B; Hi-Z
X	1	0	1	X			X				X	0	Reset DAC-A and DAC-B input register and update all DACs
											X	1	Reset all registers and update all DACs (Power-on-reset update)
X	1	1	0	X			X				0	0	$\overline{\text{LDAC}}$ pin active for DAC-B and DAC-A
											0	1	$\overline{\text{LDAC}}$ pin active for DAC-B; inactive for DAC-A
											1	0	$\overline{\text{LDAC}}$ pin inactive for DAC-B; active for DAC-A
											1	1	$\overline{\text{LDAC}}$ pin inactive for DAC-B and DAC-A
X	1	1	1	X			X				X	0	Disable internal reference and reset DACs to gain = 1
											X	1	Enable Internal Reference & reset DACs to gain = 2

(1) *X*' denotes *don*'*t care* bits.

GAIN REGISTERS

The gain register controls the GAIN setting in the DAC transfer function:

$$V_{OUT} = \left(\frac{D_{IN}}{2^n}\right) \times V_{REF} \times \text{Gain} \quad (2)$$

The DAC756x, DAC816x, and DAC856x have a gain register for each channel. The gain for each channel, in Equation 2, is either 1 or 2. This gain is automatically set to 2 when using the internal reference, and is automatically set to 1 when the internal reference is disabled (default). However, each channel can have either gain by setting the registers appropriately. The gain registers are accessible by using command bits = 000 and address bits = 010, and using DB1 for DAC-B and DB0 for DAC-A. See Table 13 or Table 14 and Table 15 for the full command structure. The gain registers are automatically reset to provide either gain of 1 or 2 when the internal reference is powered off or on, respectively. After the reference is powered off or on, the gain register is again accessible to change the gain.

Table 14. Gain Register Command Structure

		Command			Address			Data															
X	X	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DAC-B	DAC-A
DB23																							DB0

Table 15. DAC-n Selection for Gain Register Command

DB1/DB0	Value	Gain
DB0	0	DAC-A uses gain = 2 (default with internal reference)
	1	DAC-A uses gain = 1 (default with external reference)
DB1	0	DAC-B uses gain = 2 (default with internal reference)
	1	DAC-B uses gain = 1 (default with external reference)

POWER-DOWN MODES

The DAC756x, DAC816x, and DAC856x have two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. The internal reference is forced to a powered down state while both DAC channels are powered down, and is only enabled if any DAC channel is also in normal mode of operation. For more information on the internal reference control, see the *INTERNAL REFERENCE ENABLE REGISTER* section.

DAC Power-Down Commands

The DAC756x, DAC816x, and DAC856x DACs use four modes of operation. These modes are accessed by setting command bits C2, C1, and C0, and power-down register bits DB5 and DB4. The command bits must be set to 100. Once the command bits are set correctly, the four different power down modes are software programmable by setting bits DB5 and DB4 in the shift register. Table 13 or Table 16 through Table 18 shows how to control the operating mode with data bits PD1 (DB5), PD0 (DB4), DB1, and DB0.

Table 16. DAC Power Mode Register Command Structure

		Command			Address			Data															
X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	PD1	PD0	X	X	DAC-B	DAC-A

DB23 DB0

Table 17. DAC-n Operating Modes

PD1 (DB5)	PD0 (DB4)	DAC OPERATING MODES
0	0	Power up selected DACs (normal mode, default)
0	1	Power down selected DACs 1 kΩ to GND
1	0	Power down selected DACs 100 kΩ to GND
1	1	Power down selected DACs Hi-Z to GND

Table 18. DAC-n Selection for Operating Modes

DB1/DB0	Operating Mode
0	DAC-n does not change operating mode
1	DAC-n operating mode set to value on PD1 and PD0

It is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered up, it powers up to this new value.

The advantage of the available power-down modes is that the output impedance of the device is known while it is in power-down mode. As described in Table 17, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or open-circuited (Hi-Z). The DAC powerdown circuitry is shown in Figure 92.

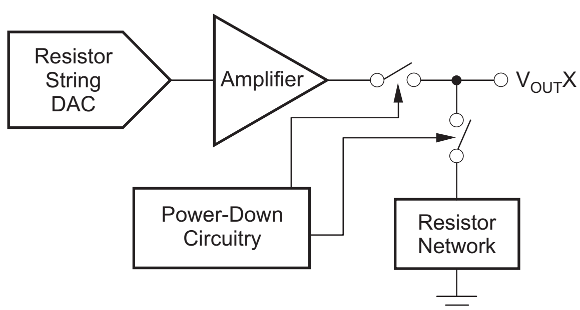


Figure 92. Output Stage

SOFTWARE RESET FUNCTION

The DAC756x, DAC816x, and DAC856x contain a software reset feature. The software reset function uses command 101. The software reset command contains two reset modes which are software-programmable by setting bit DB0 in the shift register. Table 13 and/or Table 19 and Table 20 show the available software reset commands.

Table 19. Software Reset Command Structure

		Command			Address			Data															
X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RST

DB23 DB0

Table 20. Software Reset

RST (DB0)	Registers Reset to Default Values
0	DAC registers Input registers
1	DAC registers Input registers LDAC registers Power-down registers Internal reference register Gain registers

$\overline{\text{LDAC}}$ FUNCTIONALITY

The DAC756x, DAC816x, and DAC856x offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC756x, DAC816x, and DAC856x data updates can be performed either in *synchronous* or in *asynchronous* mode.

In *asynchronous* mode, the $\overline{\text{LDAC}}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel writes can be done in order to set different channel buffers to desired values and then make a falling edge on $\overline{\text{LDAC}}$ pin to simultaneously update the DAC output registers. Data buffers of all channels must be loaded with desired data before an $\overline{\text{LDAC}}$ falling edge. After a high-to-low $\overline{\text{LDAC}}$ transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ pin is triggered. $\overline{\text{LDAC}}$ must be returned high before the next serial command is initiated.

In *synchronous* mode, data are updated with the falling edge of the 24^{th} SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such *synchronous* updates, the $\overline{\text{LDAC}}$ pin is not required, and it must be connected to GND permanently or asserted and held low before sending commands to the device.

Alternatively, all DAC outputs can be updated simultaneously using the built-in software function of LDAC. The LDAC register offers additional flexibility and control by allowing the selection of which DAC channel(s) should be updated simultaneously when the LDAC pin is being brought low. The LDAC register is loaded with a 2-bit word (DB1 and DB0) using command bits C2, C1, and C0 (see Table 13 or Table 21). The default value for each bit, and therefore for each DAC channel, is zero. If the LDAC register bit is set to 1, it overrides the LDAC pin (the LDAC pin is internally tied low for that particular DAC channel) and this DAC channel updates synchronously after the falling edge of the 24th SCLK cycle. However, if the LDAC register bit is set to 0, the DAC channel is controlled by the LDAC pin.

The combination of software and hardware simultaneous update functions is particularly useful in applications when updating a DAC channel, while keeping the other channel unaffected; see Table 13 or Table 21 and Table 22 for more information.

Table 21. LDAC Register Command Structure

		Command			Address			Data															
X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DAC-B	DAC-A
DB23																							DB0

Table 22. DAC-n Selection for LDAC Register Command

DB1/DB0	Value	LDAC Pin Functionality
DB0	0	DAC-A uses LDAC pin
	1	DAC-A operates in synchronous mode
DB1	0	DAC-B uses LDAC pin
	1	DAC-B operates in synchronous mode

INTERNAL REFERENCE ENABLE REGISTER

The internal reference in the DAC756x, DAC816x, and DAC856x is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered up and powered down using a serial command that requires a 24-bit write sequence, as shown in Table 23 and Table 24. The internal reference is forced to a powered down state while both DAC channels are powered down, and is only enabled if any DAC channel is in normal mode of operation in addition to using the command in Table 23. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the V_{REFIN}/V_{REFOUT} pin (Hi-Z output).

Enabling Internal Reference

To enable the internal reference, write the 24-bit serial command shown in Table 23. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. However, the internal reference is forced to a disabled state while both DAC channels are powered down, and remains disabled until either DAC channel is returned to the normal mode of operation. See DAC Power-Down Commands for more information on DAC channel modes of operation.

Table 23. Write Sequence for Enabling Internal Reference

		Command			Address			Data															
X	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
DB23																							DB0

Disabling Internal Reference

To disable the internal reference, write the 24-bit serial command shown in Table 24. When performing a power cycle to reset the device, the internal reference is disabled (default mode).

Table 24. Write Sequence for Disabling Internal Reference

		Command			Address			Data															
X	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
DB23																							DB0

APPLICATION INFORMATION

INTERNAL REFERENCE

The internal reference of the DAC756x, DAC816x, and DAC856x does not require an external load capacitor for stability because it is stable without any capacitive load. However, for improved noise performance, an external load capacitor of 150 nF or larger connected to the V_{REFIN}/V_{REFOUT} output is recommended. Figure 93 shows the typical connections required for operation of the DAC756x, DAC816x, and DAC856x internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

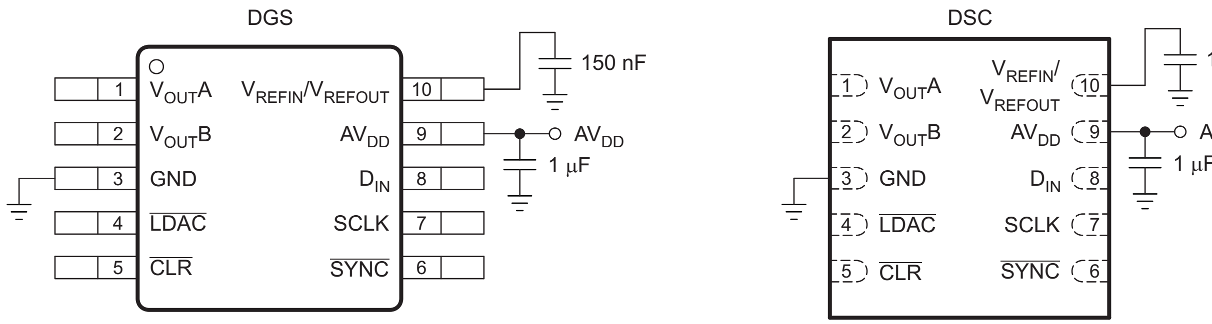


Figure 93. Typical Connections for Operating the DAC756x/DAC816x/DAC856x Internal Reference

Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5 mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, DC PSRR) is also exceptional. Within the specified supply voltage range of 2.7 V to 5.5 V, the variation at V_{REFIN}/V_{REFOUT} is typically 50 µV/V; see Figure 7.

Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the box method described by Equation 3:

$$\text{Drift Error} = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \ (\text{ppm}/{}^\circ\text{C}) \qquad (3)$$

where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.
V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.
V_{REF} = 2.5 V, target value for reference output voltage.
T_{RANGE} = the characterized range from –40°C to 125°C (165°C range)

The internal reference features an exceptional typical drift coefficient of 4 ppm/°C from –40°C to 125°C. Characterizing a large number of units, a maximum drift coefficient of 10 ppm/°C is observed. Temperature drift results are summarized in Figure 3.

Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise and noise spectral density performance are listed in the *Electrical Characteristics*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the AC performance. The output noise spectrum at the V_{REFIN}/V_{REFOUT} pin, both unloaded and with an external 4.7-µF load capacitor, is shown in Figure 6. Internal reference noise impacts the DAC output noise when the internal reference is used.

Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 94. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are shown in Figure 4. Force and sense lines should be used for applications that require improved load regulation.

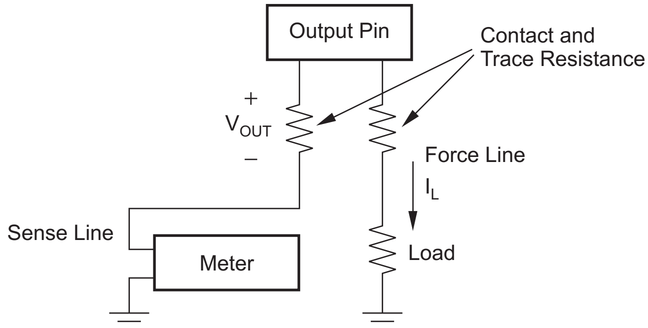


Figure 94. Accurate Load Regulation of the DAC756x/DAC816x/DAC856x Internal Reference

Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses. The typical drift value for the internal reference is listed in the *Electrical Charateristics* and measurement results are shown in Figure 5. This parameter is characterized by powering up multiple devices and measuring them at regular intervals.

Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at 25°C, cycling the device through the operating temperature range, and returning to 25°C. Hysteresis is expressed by Equation 4:

$$V_{HYST} = \left[\frac{V_{REF\_PRE} - V_{REF\_POST}}{V_{REF\_NOM}} \right] \times 10^6 (\text{ppm}/°\text{C}) \quad (4)$$

Where:

- V_{HYST} = thermal hysteresis.
- V_{REF_PRE} = output voltage measured at 25°C pre-temperature cycling.
- V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to 125°C, and returns to 25°C.
- V_{REF_NOM} = 2.5 V, target value for reference output voltage.

DAC NOISE PERFORMANCE

Output noise spectral density at the V_{OUT}-n pin versus frequency is depicted in Figure 45 and Figure 46 for full-scale, mid-scale, and zero-scale input codes. The typical noise density for mid-scale code is 90 nV/√Hz at 1 kHz. High-frequency noise can be improved by filtering the reference noise. Integrated output noise between 0.1 Hz and 10 Hz is close to 2.5 μV_{PP} (mid-scale), as shown in Figure 47.

UP TO ±15-V BIPOLAR OUTPUT USING THE DAC8562

The DAC8562 is designed to be operate from a single power supply providing a maximum output range of AV_{DD} volts. However, the DAC can be placed in the configuration shown in Figure 95 in order to be designed into bipolar systems. Depending on the ratio of the resistor values, the output of the circuit can range anywhere from ±5 V to ±15 V. The design example below shows that the DAC is configured to have its internal reference enabled and the DAC8562 internal gain set to two, however, an external 2.5-V reference could also be used (with DAC8562 internal gain set to two).

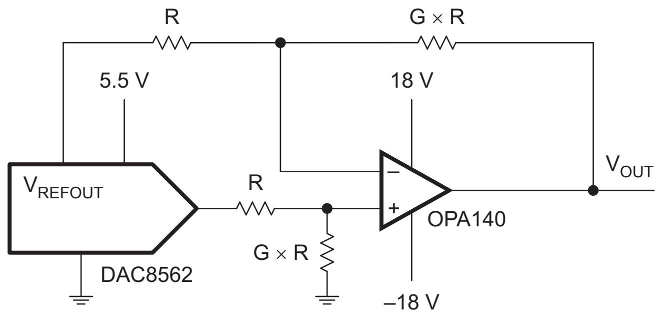


Figure 95. Bipolar Output Range Circuit Using DAC8562

The transfer function shown in Equation 5 can be used to calculate the output voltage as a function of the DAC code, reference voltage and resistor ratio:

$$V_{OUT} = G \times V_{REFOUT}\left(2 \times \frac{D_{IN}}{65{,}536} - 1\right) \quad (5)$$

where:

- D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register, ranging from 0 to 65,535 for DAC8562 (16 bit).
- V_{REFOUT} = reference output voltage with the internal reference enabled from the DAC V_{REFIN}/V_{REFOUT} pin
- G = ratio of the resistors

An example configuration to generate a ±10-V output range is shown below in Equation 6 with G = 4 and V_{REFOUT} = 2.5 V:

$$V_{OUT} = 20 \times \frac{D_{IN}}{65{,}536} - 10\text{ V} \quad (6)$$

In this example, the range is set to ±10 V by using a resistor ratio of four, V_{REFOUT} of 2.5 V, and DAC8562 internal gain of two. The resistor sizes must be selected keeping in mind the current sink/source capability of the DAC8562 internal reference. Using larger resistor values, for example R = 10 kΩ or larger is recommended. The op amp is selectable depending on the requirements of the system.

The DAC8562EVM and DAC7562EVM boards have the option to evaluate the bipolar output application by installing the components on the pre-placed footprints. For more information see either the DAC8562EVM or DAC7562EVM product folder.

PLC ANALOG OUTPUT MODULE USING THE DAC8562

The DAC8562 can be mated with one of TI's 0- to 20-mA voltage-to-current transmitters to create a low-cost, programmable current source for use in PLC applications. One specific example includes combining the DAC8562 with the XTR111 to create a voltage-to-current solution. The DAC output voltage generates a current, I_{SET}, which is determined by the value of the external resistor, R_{SET}. This current is internally amplified by 10 and output at the IS node. A p-channel MOSFET Q1 can be added in an application where a wide compliance voltage is required, for example, when using a high impedance load. The optional PNP transistor, Q2, along with the R4 resistor provides external current limiting in a case where the external FET is forced to low impedance. Additionally, resistors R2 and R3 can be used to scale the 3-V internal regulator to a desired voltage to power the DAC. Figure 96 shows a working 0- to 20-mA solution using one DAC8562 channel and a ±10-V voltage output using the other DAC8562 channel. For more information on the ±10-V voltage output circuit see the UP TO ±15-V BIPOLAR OUTPUT USING THE DAC8562 application.

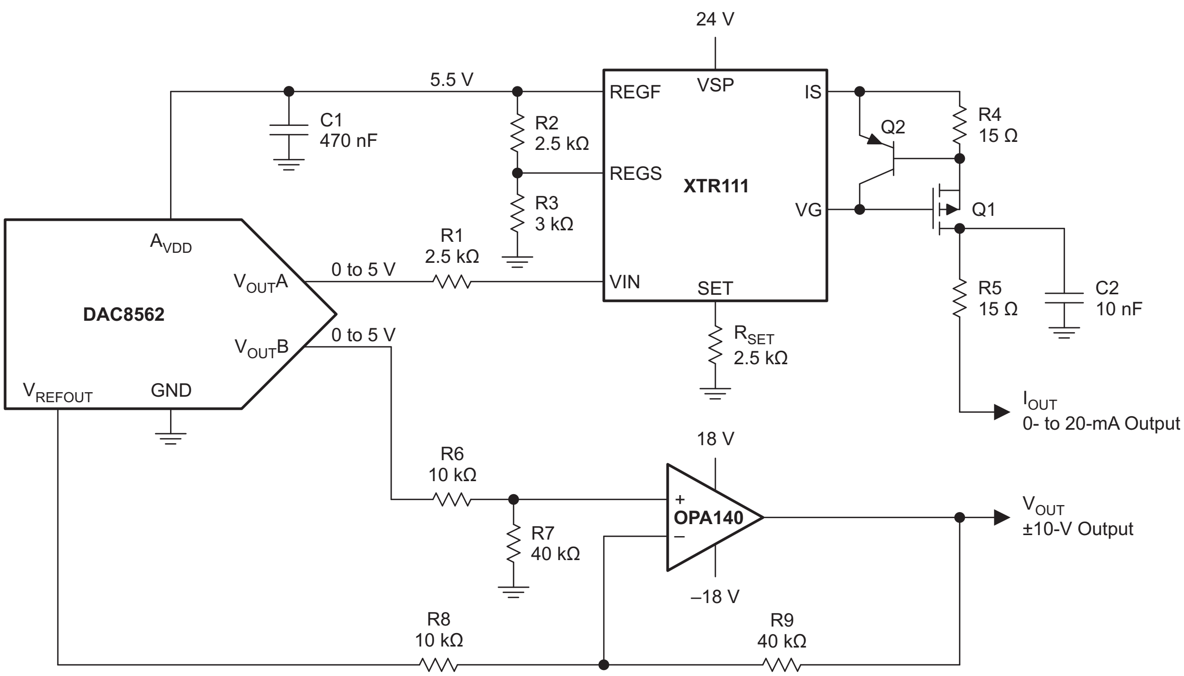
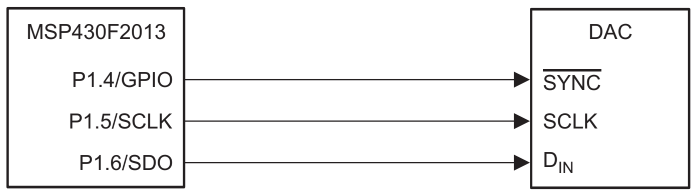


Figure 96. 0- to 20-mA and ±10-V Outputs Using DAC8562

MICROPROCESSOR INTERFACING

DAC756x/DAC816x/DAC856x to an MSP430 USI Interface

Figure 97 shows a serial interface between the DAC756x, DAC816x, or DAC856x and a typical MSP430 USI port such as the one found on the MSP430F2013. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in USICTL1 to provide an efficient means of SPI communication with minimal software overhead. The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on port 1; in this case, port line P1.4 is used. When data are to be transmitted to the DAC756x, DAC816x, or DAC856x, P1.4 is taken low. The USI transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P1.4 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P1.4 is taken high following the completion of the third write cycle.

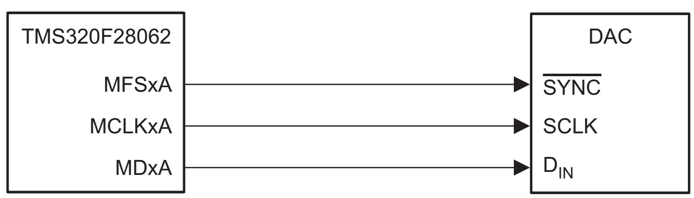


NOTE: Additional pins omitted for clarity.

Figure 97. DAC756x/DAC816x/DAC856x to MSP430 Interface

DAC756x/DAC816x/DAC856x to a TMS320 McBSP Interface

Figure 98 shows an interface between the DAC756x, DAC816x, or DAC856x and any TMS320 series DSP from Texas Instruments with a multi-channel buffered serial port (McBSP). Serial data are shifted out on the rising edge of the serial clock and are clocked into the DAC756x, DAC816x, or DAC856x on the falling edge of the SCLK signal.

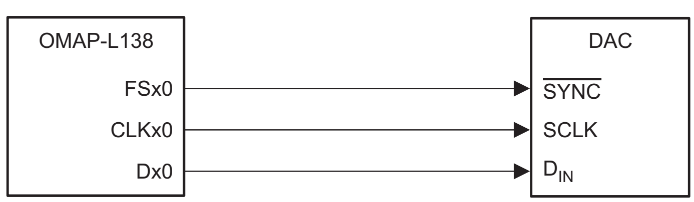


NOTE: Additional pins omitted for clarity.

Figure 98. DAC756x/DAC816x/DAC856x to TMS320 McBSP Interface

DAC756x/DAC816x/DAC856x to an OMAP-L1x Processor

Figure 99 shows a serial interface between the DAC756x/DAC816x/DAC856x and the OMAP-L138. The transmit clock CLKx0 of the L138 drives SCLK of the DAC756x, DAC816x, or DAC856x, and the data transmit (Dx0) output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from the frame sync transmit (FSx0) line, similar to the TMS320 interface.



NOTE: Additional pins omitted for clarity.

Figure 99. DAC756x/DAC816x/DAC856x to OMAP-L1x Processor

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC756x, DAC816x, and DAC856x offer single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. As a result of the single ground pin of the DAC756x, DAC816x, and DAC856x, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system. The power applied to AV_{DD} should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, AV_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1-μF to 10-μF capacitor and 0.1-μF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100-μF electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed to essentially low-pass filter the supply and remove the high-frequency noise.

PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1 LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is less than 1 LSB, the DAC is said to be monotonic.

Full-Scale Error

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code (0xFFFF). Ideally, the output should be V_{REF} – 1 LSB or 2 × V_{REF} – 1 LSB, depending on the DAC voltage gain. The full-scale error is expressed in percent of full-scale range (% FSR).

Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of ppm of FSR/°C.

Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an n-bit DAC, these values are usually given as the values matching with code 0 and $2^n – 1$.

Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (% FSR).

Gain Temperature Coefficient

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

Least-Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by 2^n, where n is the resolution of the converter.

Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains constant for each step increase (or decrease) in the input code.

Most-Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

Offset Error

The offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes (code 512 and code 65,024). Because the offset error is defined by a straight line, it can have a negative or positive value. Offset error is measured in mV.

Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in μV/°C.

Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. INL is measured in LSBs.

Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

Zero-Code Error

The zero-code error is defined as the DAC output voltage, when all 0s are loaded into the DAC register. Zero-code error is a measure of the difference between actual output voltage and ideal output voltage (0 V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in μV/°C.

DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

Channel-to-Channel Crosstalk

Crosstalk in a multi-channel DAC is defined as a glitch coupled onto the output of a channel (victim) when the output of an adjacent channel (agressor) has a full-scale transition. It is calculated as the total area under the measured glitch on the victim channel at mid-scale code. It is expressed in nV-s.

Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel at mid-scale. It is expressed in LSB.

Code Change/Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolt-seconds (nV-s), and is measured when the digital input code is changed by 1 LSB at the major carry transition.

DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at mid-scale while filtering the output voltage within a band of 0.1 Hz to 10 Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage (V_{PP}).

DAC Output Noise Density

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density ($nV/\sqrt{Hz}$). It is measured by setting the DAC to mid-scale and measuring noise at the output.

Digital Feedthrough

Digital feedthrough is defined as the impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all 0s to all 1s and vice versa.

Output Voltage Settling Time

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.024% FSR (or whatever value is stated) of full-scale range.

Slew Rate

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right) \quad (7)$$

Where $\Delta V_{OUT}(t)$ is the output produced by the amplifier as a function of time t.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DAC7562SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7562SDGST	ACTIVE	MSOP	DGS	10	250	TBD	Call TI	Call TI	
DAC7562SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC7562SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC7563SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7563SDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7563SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC7563SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8162SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8162SDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8162SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8162SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8163SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8163SDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8163SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8163SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8562SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
DAC8562SDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8562SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8562SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8563SDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8563SDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC8563SDSCR	ACTIVE	SON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8563SDSCT	ACTIVE	SON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

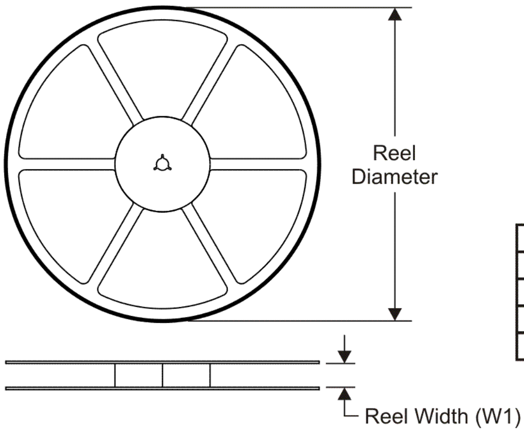
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

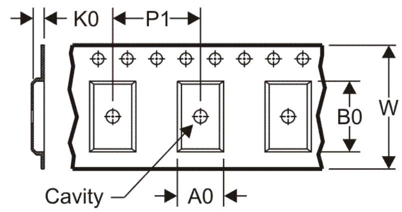
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

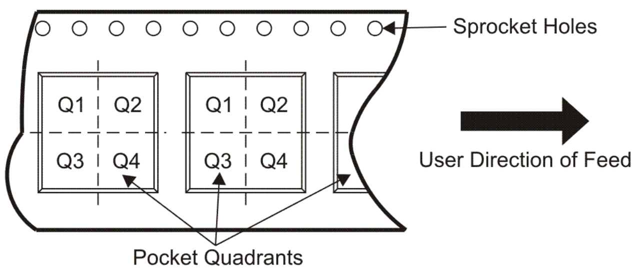


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

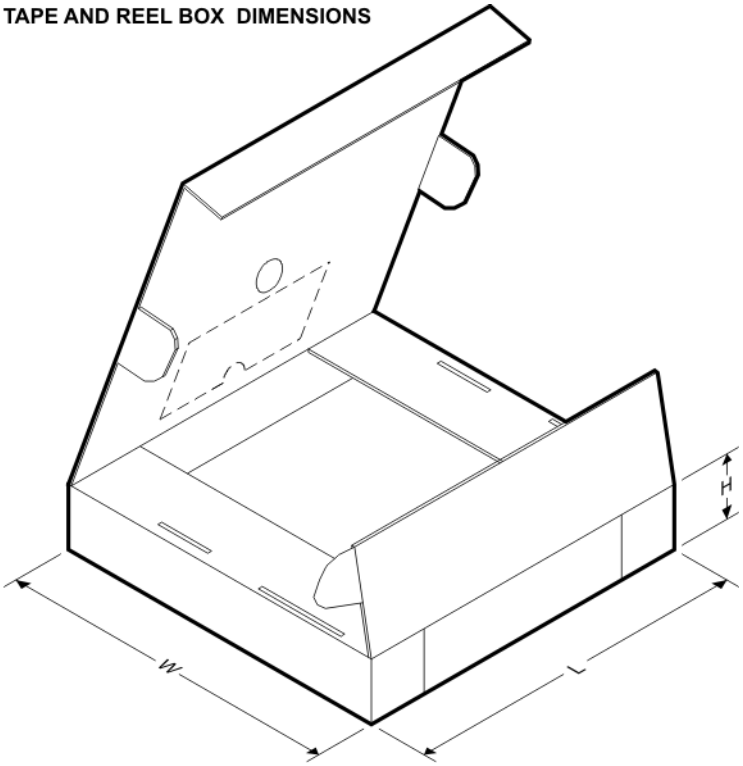


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7562SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7562SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7563SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563SDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162SDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162SDSCT	SON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8163SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163SDSCT	SON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8562SDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8562SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562SDSCT	SON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8563SDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8563SDSCR	SON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8563SDSCT	SON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

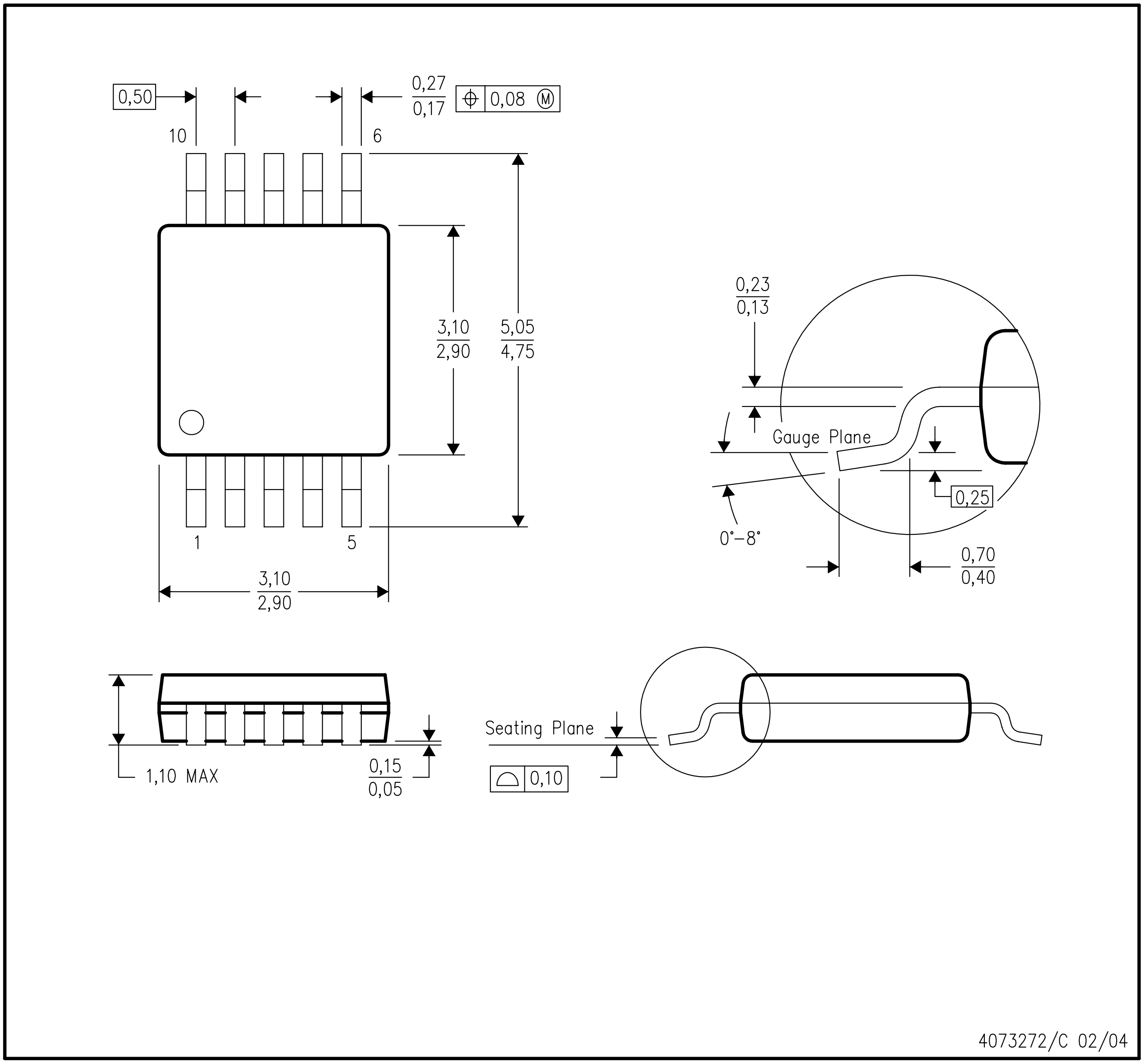


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7562SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC7562SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC7563SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC7563SDGST	MSOP	DGS	10	250	203.0	203.0	35.0
DAC7563SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC8162SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC8162SDGST	MSOP	DGS	10	250	203.0	203.0	35.0
DAC8162SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC8162SDSCT	SON	DSC	10	250	190.5	212.7	31.8
DAC8163SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC8163SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC8163SDSCT	SON	DSC	10	250	190.5	212.7	31.8
DAC8562SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC8562SDGST	MSOP	DGS	10	250	203.0	203.0	35.0
DAC8562SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC8562SDSCT	SON	DSC	10	250	190.5	212.7	31.8

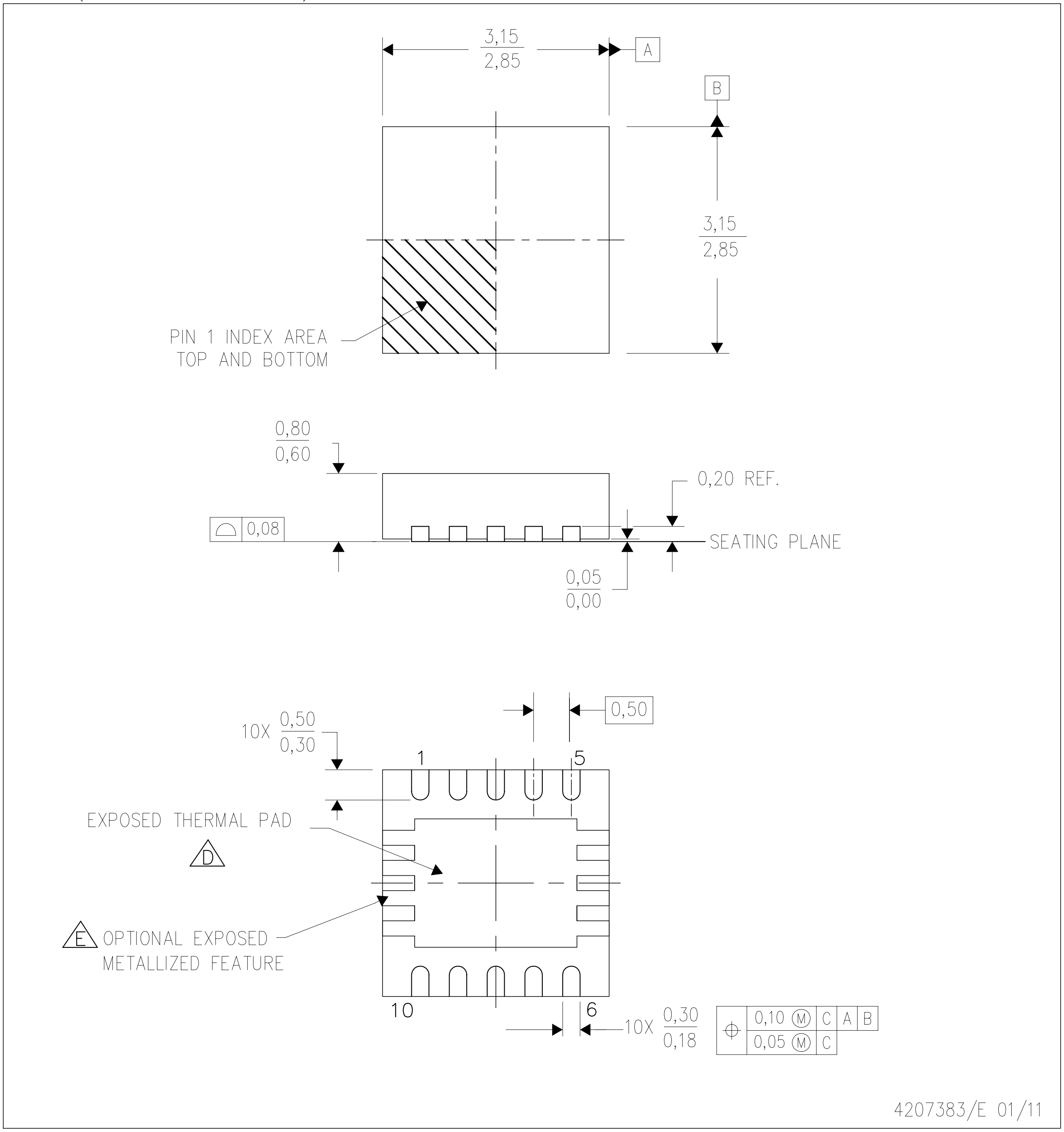
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8563SDGSR	MSOP	DGS	10	2500	346.0	346.0	35.0
DAC8563SDSCR	SON	DSC	10	3000	346.0	346.0	29.0
DAC8563SDSCT	SON	DSC	10	250	190.5	212.7	31.8

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

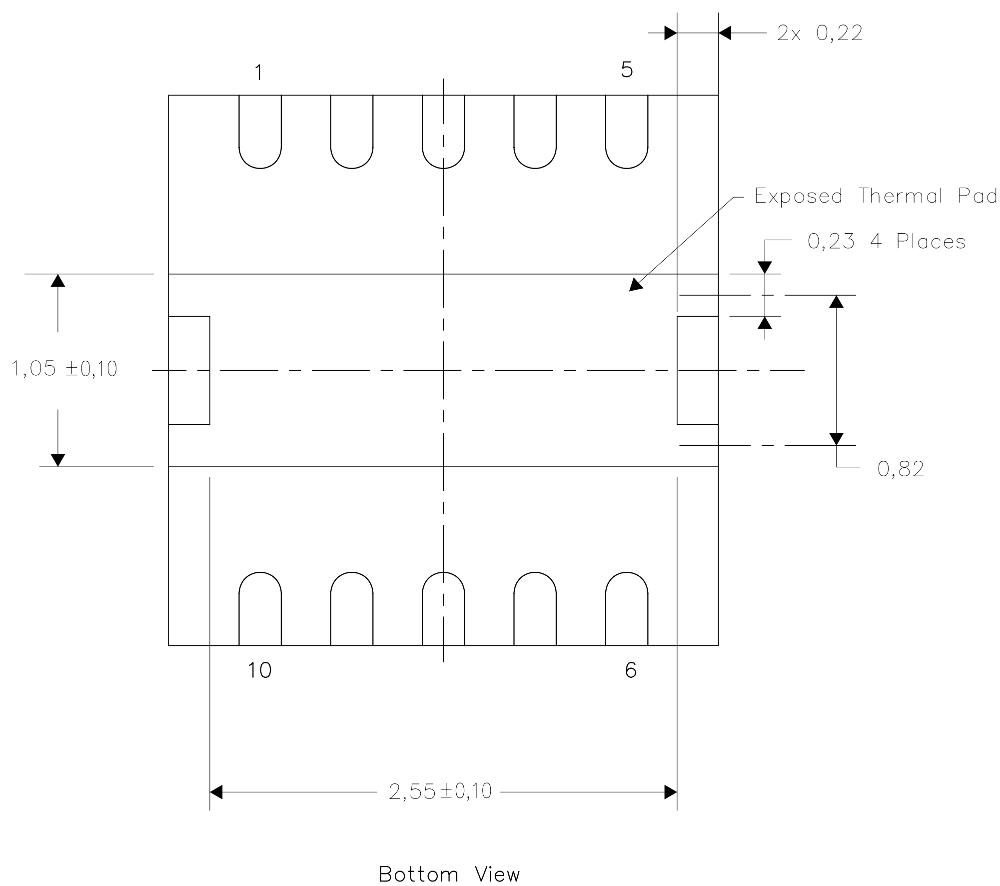
DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

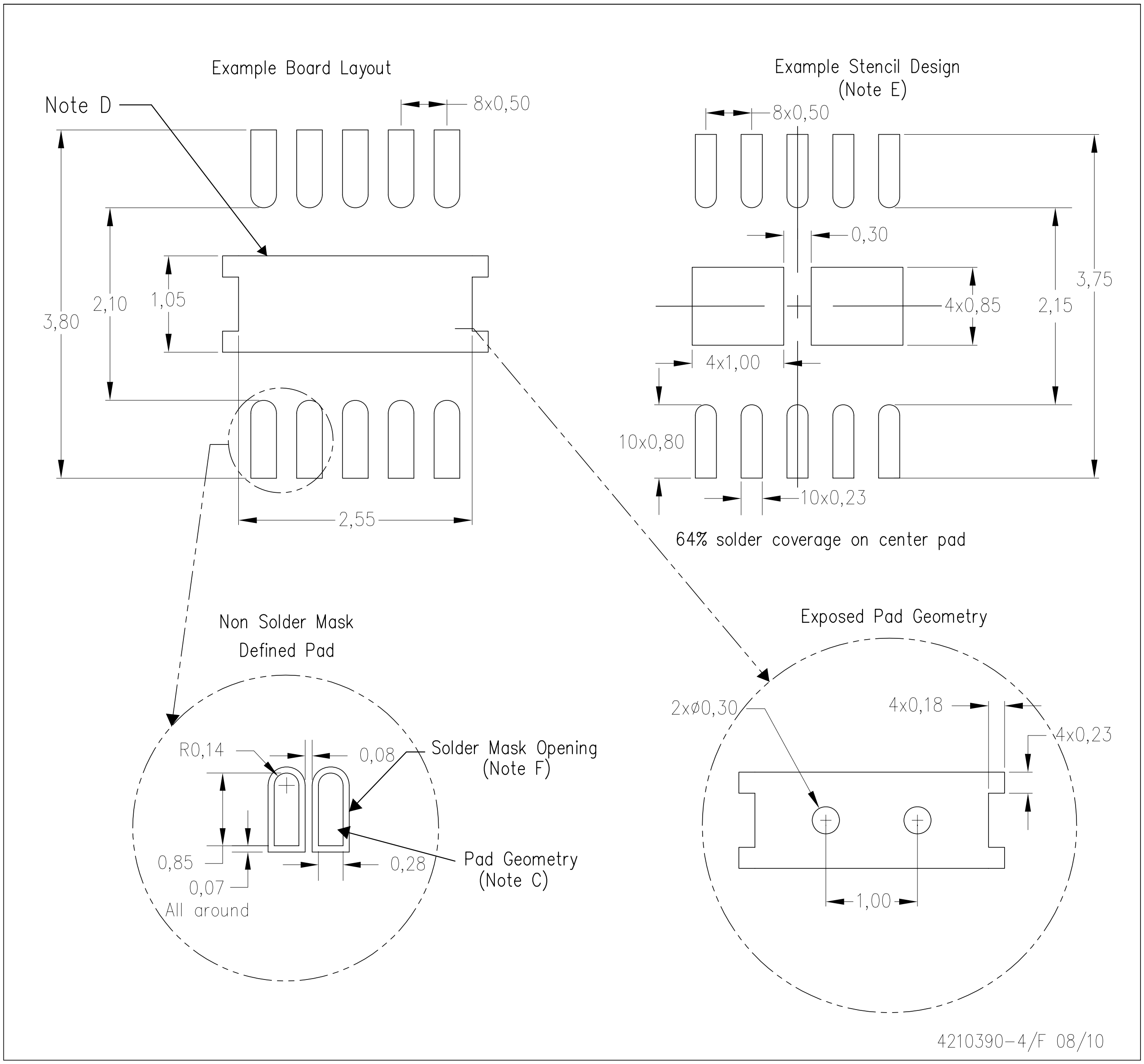


Exposed Thermal Pad Dimensions

4210391-4/F 04/11

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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