

### FEATURES

- 12-bit accuracy in an 8-lead PDIP and SOIC package
- Fast serial data input
- Double data buffers
- Low  $\pm 1/2$  LSB maximum INL and  $\pm 1$  LSB maximum DNL
- Maximum gain error: 2 LSB
- Low  $\pm 5$  ppm/ $^{\circ}$ C maximum tempco
- ESD resistant
- Low cost
- Available in die form

### APPLICATIONS

- Autocalibration systems
- Process control and industrial automation
- Programmable amplifiers and attenuators
- Digitally controlled filters

### GENERAL DESCRIPTION

The DAC8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-lead PDIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC8043 is ideal for applications where PC board space is at a premium. In addition, improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the LD input pin.

### FUNCTIONAL BLOCK DIAGRAM

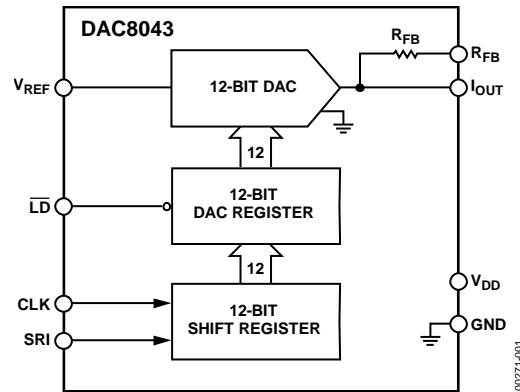


Figure 1.

Data in the DAC register is converted to an output current by the digital-to-analog converter (DAC).

The fast interface timing of the DAC8043 may reduce timing design considerations while minimizing microprocessor wait states. For applications requiring an asynchronous clear function or more versatile microprocessor interface logic, refer to the [AD5443](#).

Operating from a single 5 V power supply, the DAC8043 is the ideal low power, small size, high performance solution to many application problems. It is available in a PDIP package that is compatible with auto-insertion equipment. There is also a 16-lead SOIC package available.

### Rev. E

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## TABLE OF CONTENTS

Features .....	1	Typical Performance Characteristics .....	7
Applications.....	1	Terminology.....	9
Functional Block Diagram .....	1	Digital Section.....	10
General Description .....	1	General Circuit Information.....	10
Revision History .....	2	Equivalent Circuit Analysis .....	11
Specifications.....	3	Dynamic Performance.....	11
Electrical Characteristics .....	3	Applications Information .....	12
Wafer Test Limits.....	4	Application Tips .....	12
Absolute Maximum Ratings.....	5	Interfacing to the MC6800.....	14
Caution .....	5	DAC8043 Interface to the 8085.....	14
Thermal Resistance .....	5	DAC8043 to the 68000 Interface.....	14
ESD Caution.....	5	Outline Dimensions .....	15
Pin Configuration and Function Descriptions.....	6	Ordering Guide .....	16

## REVISION HISTORY

### 1/11—Rev. D to Rev. E

Updated Format.....	Universal
Added SOIC_W Models.....	Universal
Added Table 5.....	6
Updated Outline Dimensions .....	15
Changes to Ordering Guide .....	15

### 3/03—Data Sheet Changed from Rev. C to Rev. D.

Deleted 8-Lead CIRDIP and 16-Lead Wide-Body SOL.....	Universal
Figures renumbered .....	Universal
Changes to Absolute Maximum Ratings .....	4
Changes to Ordering Guide .....	4
Deleted to Dice Characteristics .....	4
Updated Outline Dimensions .....	11

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 5\text{ V}$ ;  $V_{REF} = 10\text{ V}$ ;  $I_{OUT} = \text{GND} = 0\text{ V}$ ;  $T_A = \text{full temperature range specified under the Absolute Maximum Ratings, unless otherwise noted.}$

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity <sup>1</sup>	INL	DAC8043G DAC8043F			±½	LSB
Differential Nonlinearity <sup>2</sup>	DNL				1	LSB
Gain Error <sup>3</sup>	$G_{FSE}$	$T_A = 25^\circ\text{C}$ $T_A = \text{full temperature range, all grades}$			±1	LSB
Gain Tempco ( $\Delta\text{Gain}/\Delta\text{Temp}$ ) <sup>4</sup>	$TC_{GFS}$				2	LSB
Power Supply Rejection Ratio ( $\Delta\text{Gain}/\Delta V_{DD}$ )	PSRR	$\Delta V_{DD} = \pm 5\%$		±0.0006	±0.002	ppm/°C
Output Leakage Current <sup>5</sup>	$I_{LKG}$	$T_A = 25^\circ\text{C}$ $T_A = \text{full temperature range}$			±5	nA
Zero Scale Error <sup>6, 7</sup>	$I_{ZSE}$	$T_A = 25^\circ\text{C}$ $T_A = \text{full temperature range}$			±25	nA
Input Resistance <sup>8</sup>	$R_{IN}$		7	11	15	kΩ
AC PERFORMANCE						
Output Current						
Settling Time <sup>4, 9</sup>	$t_s$	$T_A = 25^\circ\text{C}, V_{REF} = 0\text{ V}$		0.25	1	μs
Digital-to-Analog Glitch Energy <sup>4, 10</sup>	Q	$I_{OUT}$ load = 100 Ω, $C_{EXT} = 13\text{ pF}$ , DAC register loaded alternately with all 0s and all 1s		2	20	nVs
Feedthrough Error ( $V_{REF}$ to $I_{OUT}$ ) <sup>4, 11</sup>	FT	$V_{REF} = 20\text{ V p-p @ } f = 10\text{ kHz}$ , digital input = 0000 0000 0000		0.7	1	mV p-p
Total Harmonic Distortion <sup>4</sup>	THD	$T_A = 25^\circ\text{C}$ $V_{REF} = 6\text{ V rms @ } 1\text{ kHz}$ , DAC register loaded with all 1s		-85		dB
Output Noise Voltage Density <sup>4, 12</sup>	$e_n$	10 Hz to 100 kHz between $R_{FB}$ and $I_{OUT}$			17	nV/√Hz
DIGITAL INPUTS						
Digital Input						
High	$V_{IN}$		2.4			V
Low	$V_{IL}$				0.8	V
Input Leakage Current <sup>13</sup>	$I_{IL}$	$V_{IN} = 0\text{ V to } +5\text{ V}$			±1	μA
Input Capacitance <sup>4, 11</sup>	$C_{IN}$	$V_{IN} = 0\text{ V}$			8	pF
ANALOG OUTPUTS						
Output Capacitance <sup>4</sup>	$C_{OUT}$	Digital inputs = $V_{IH}$ Digital inputs = $V_{IL}$			110 80	pF pF
TIMING CHARACTERISTICS <sup>4, 14</sup>						
Data Setup Time	$t_{DS}$	$T_A = \text{full temperature range}$	40			ns
Data Hold Time	$t_{DH}$	$T_A = \text{full temperature range}$	80			ns
Clock Pulsewidth High	$t_{CH}$	$T_A = \text{full temperature range}$	90			ns
Clock Pulsewidth Low	$t_{CL}$	$T_A = \text{full temperature range}$	120			ns
Load Pulsewidth	$t_{LD}$	$T_A = \text{full temperature range}$	120			ns
LSB Clock Into Input Register to Load DAC Register Time	$t_{ASB}$	$T_A = \text{full temperature range}$	0			ns

# DAC8043

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage	$V_{DD}$		4.75	5	5.25	V
Supply Current	$I_{DD}$	Digital inputs = $V_{IH}$ or $V_{IL}$ Digital inputs = 0 V or $V_{DD}$			500 100	$\mu$ A $\mu$ A

<sup>1</sup>  $\pm 1/2$  LSB =  $\pm 0.012\%$  of full scale.

<sup>2</sup> All grades are monotonic to 12 bits over temperature.

<sup>3</sup> Using internal feedback resistor.

<sup>4</sup> Guaranteed by design and not tested.

<sup>5</sup> Applies to  $I_{OUT}$ ; all digital inputs = 0 V.

<sup>6</sup>  $V_{REF} = 10$  V; all digital inputs = 0 V.

<sup>7</sup> Calculated from worst-case  $R_{REF}$ :  $I_{ZSE}$  (in LSBs) =  $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$ .

<sup>8</sup> Absolute temperature coefficient is less than 300 ppm/ $^{\circ}$ C.

<sup>9</sup>  $I_{OUT}$  load = 100  $\Omega$ ,  $C_{EXT} = 13$  pF, digital input = 0 V to  $V_{DD}$  or  $V_{DD}$  to 0 V. Extrapolated to  $1/2$  LSB;  $t_s$  = propagation delay ( $t_{PD}$ ) +  $9\tau$  where  $\tau$  = measured time constant of the final RC decay.

<sup>10</sup>  $V_{REF} = 0$  V, all digital inputs = 0 V to  $V_{DD}$  or  $V_{DD}$  to 0 V.

<sup>11</sup> All digit inputs = 0 V.

<sup>12</sup> Calculations from  $e_n = \sqrt{4KTRB}$

where:

$K$  = Boltzmann constant,  $J/^{\circ}$ K,

$R$  = resistance,  $\Omega$ ,

$T$  = resistor temperature,  $^{\circ}$ K,

$B$  = bandwidth, Hz.

<sup>13</sup> Digital inputs are CMOS gates;  $I_{IN}$  is typically 1 nA at 25 $^{\circ}$ C.

<sup>14</sup> Tested at  $V_{IN} = 0$  V or  $V_{DD}$ .

## WAFER TEST LIMITS

$V_{DD} = 5$  V,  $V_{REF} = 10$  V;  $I_{OUT} = GND = 0$  V,  $T_A = 25^{\circ}$ C.

Table 2.

Parameter <sup>1</sup>	Symbol	Conditions	DAC8043GBC Limit			Unit
			Min	Typ	Max	
STATIC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL				$\pm 1$	LSB
Differential Nonlinearity	DNL				$\pm 1$	LSB
Gain Error	$G_{FSE}$	Using internal feedback resistor			$\pm 2$	LSB
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD} = \pm 5\%$			$\pm 0.002$	%/%
Output Leakage Current ( $I_{OUT}$ )	$I_{LKG}$	Digital inputs = $V_{IL}$			$\pm 5$	nA
REFERENCE INPUT						
Input Resistance	$R_{IN}$		7		15	k $\Omega$
DIGITAL INPUTS						
Digital Input High	$V_{IH}$		2.4			V
Digital Input Low	$V_{IL}$				0.8	V
Input Leakage Current	$I_{IL}$	$V_{IN} = 0$ V to $V_{DD}$			$\pm 1$	$\mu$ A
POWER SUPPLY						
Supply Current	$I_{DD}$	Digital inputs = $V_{IN}$ or $V_{IL}$ Digital inputs = 0 V or $V_{DD}$			500 100	$\mu$ A $\mu$ A

<sup>1</sup> Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult a factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +8 V
$V_{REF}$ to GND	$\pm 18$ V
$V_{RFB}$ to GND	$\pm 18$ V
Digital Input Voltage Range	-0.3 V to $V_{DD} + 0.3$ V
$V_{IOUT}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
FP Version	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
GP Version	$0^\circ\text{C}$ to $70^\circ\text{C}$
Junction Temperature	$150^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

- Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal except  $V_{REF}$  and  $R_{FB}$ .
- The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Use proper antistatic handling procedures.
- Absolute Maximum Ratings apply to both packaged devices and dice. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead PDIP	96	37	$^\circ\text{C}/\text{W}$
16-Lead SOIC	92	27	$^\circ\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# DAC8043

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

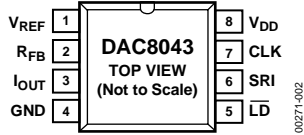
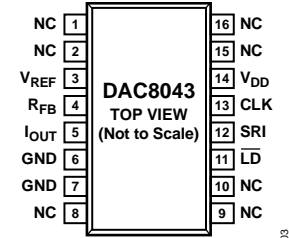


Figure 2. 8-Lead PDIP



NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 3. 16-Lead Wide-Body SOIC

Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Description
8-Lead PDIP	16-Lead SOIC		
1	3	$V_{REF}$	DAC Reference Voltage Input Pin.
2	4	$R_{FB}$	DAC Feedback Resistor Pin. This pin establishes voltage output for the DAC by connecting to an external amplifier output.
3	5	$I_{OUT}$	DAC Current Output.
4	6, 7	GND	Ground Pin.
5	11	$\overline{LD}$	Load Strobe, Level-Sensitive Digital Input. Transfers shift-register data to DAC register while active low.
6	12	SRI	12-Bit Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
7	13	CLK	Serial Clock Input. Positive-edge clocks data into shift register.
8	14	$V_{DD}$	Positive Power Supply Input.
	1, 2, 8, 9, 10, 15, 16	NC	Do Not Connect to These Pins.

# TYPICAL PERFORMANCE CHARACTERISTICS

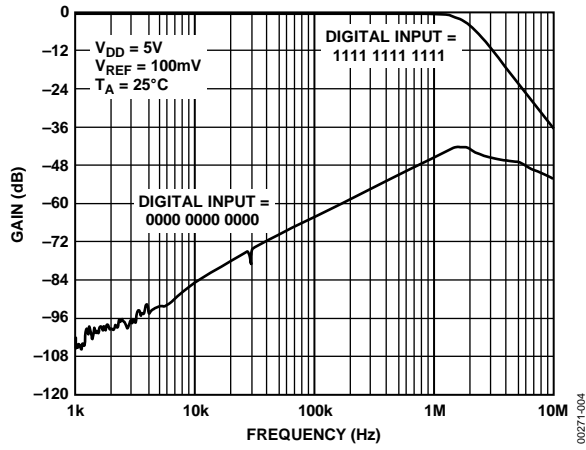


Figure 4. Gain vs. Frequency (Output Amplifier: OP42)

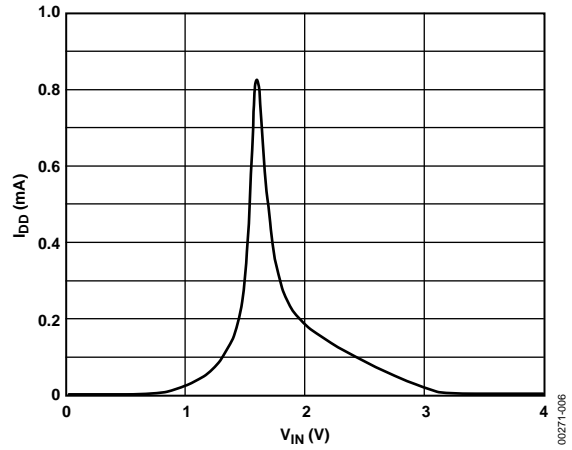


Figure 6. Supply Current vs. Logic Input Voltage

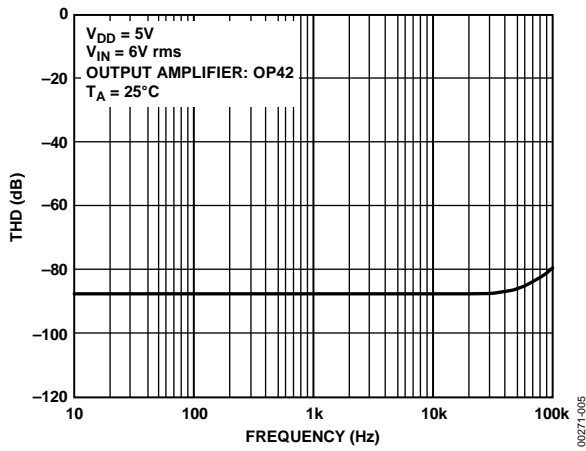


Figure 5. Total Harmonic Distortion vs. Frequency (Multiplying Mode)

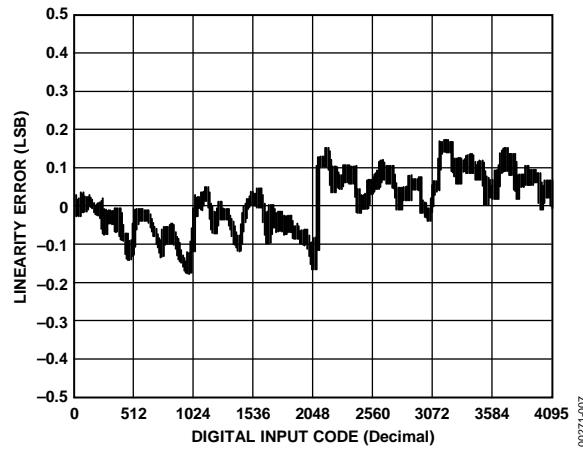


Figure 7. Linearity Error vs. Digital Input Code

# DAC8043

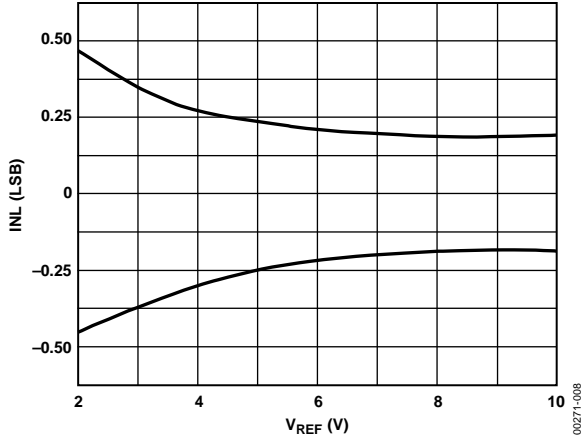


Figure 8. Linearity Error vs. Reference Voltage

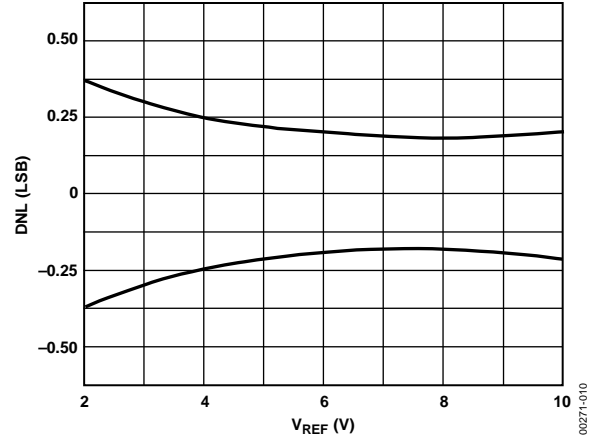


Figure 10. DNL Error vs. Reference Voltage

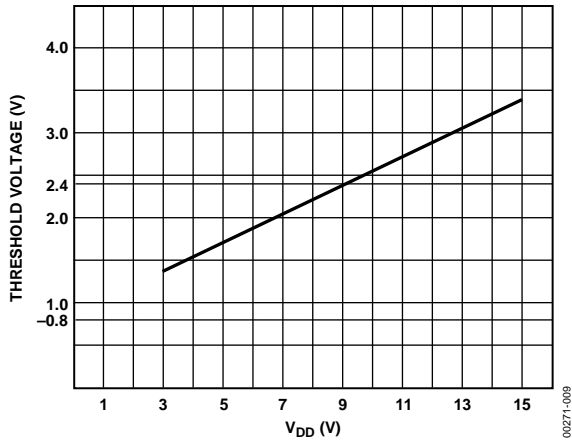


Figure 9. Logic Threshold Voltage vs. Supply Voltage



## TERMINOLOGY

### Integral Nonlinearity (INL)

This is the single most important DAC specification. Analog Devices, Inc., measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs.

Refer to the [Analog Devices Glossary of EE Terms](#) for additional digital-to-analog converter definitions.

### Interface Logic Information

The DAC8043 has been designed for ease of operation. The timing diagram (see Figure 12) illustrates the input register loading sequence. Note that the most significant bit (MSB) is loaded first.

Once the input register is full, the data is transferred to the DAC register by taking  $\overline{LD}$  momentarily low.

# DAC8043

## DIGITAL SECTION

The digital inputs of the DAC8043 (SRI,  $\overline{\text{LD}}$ , and CLK) are TTL compatible. The input voltage levels affect the amount of current drawn from the supply; peak supply current occurs as the digital input ( $V_{\text{IN}}$ ) passes through the transition region (see Figure 6). Maintaining the digital input voltage levels as close as possible to the  $V_{\text{DD}}$  and GND supplies minimizes supply current consumption.

The digital inputs of the DAC8043 have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry. Figure 11 shows the input protection diodes and series resistor; this input structure is duplicated on each digital input. High voltage static charges applied to the inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes were designed to clamp the inputs to well below dangerous levels during static discharge conditions.

## GENERAL CIRCUIT INFORMATION

The DAC8043 is a 12-bit multiplying digital-to-analog converter (DAC) with a very low temperature coefficient. It contains an R-2R resistor ladder network, data input, control logic, and two data registers.

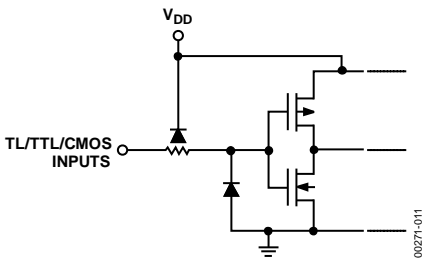


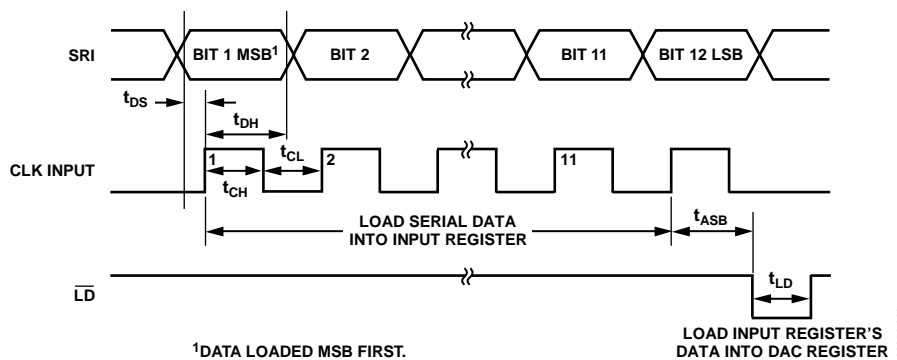
Figure 11. Digital Input Protection

The digital circuitry forms an interface in which serial data can be loaded under microprocessor control into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

A simplified circuit of the DAC8043 is shown in Figure 13, which has an inverted R-2R ladder network consisting of silicon-chrome, highly stable (50 ppm/°C) thin-film resistors, and twelve pairs of NMOS current-steering switches.

These switches steer binarily weighted currents into either  $I_{\text{OUT}}$  or GND; this yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at  $V_{\text{REF}}$  equal to R. The  $V_{\text{REF}}$  input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings section.

The twelve output current-steering NMOS FET switches are in series with each R-2R resistor; they can introduce bit errors if all are of the same  $R_{\text{ON}}$  resistance value. They were designed so that the switch on resistance is binarily scaled so that the voltage drop across each switch remains constant. If, for example, Switch S1 of Figure 13 was designed with an on resistance of 10  $\Omega$ , Switch S2 for 20  $\Omega$ , and so on, a constant 5 mV drop would be maintained across each switch.



<sup>1</sup>DATA LOADED MSB FIRST.

Figure 12. Write Cycle Timing Diagram

To further ensure accuracy across the full temperature range, permanently on MOS switches were included in series with the feedback resistor and the terminating resistor of the R-2R ladder. The simplified DAC circuit, Figure 13, shows the location of the series switches. These series switches are equivalently scaled to two times Switch S1 (MSB) and to Switch S12 (LSB), respectively, to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or  $R_{FEEDBACK}$  (such as incoming inspection),  $V_{DD}$  must be present to turn on these series switches.

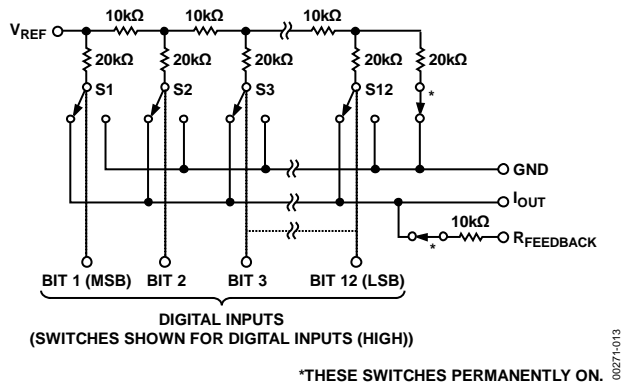


Figure 13. Simplified DAC Circuit

## EQUIVALENT CIRCUIT ANALYSIS

Figure 14 shows an equivalent analog circuit for the DAC8043. The  $(D \times V_{REF})/R$  current source is code dependent and is the current generated by the DAC. The current source,  $I_{LKG}$ , consists of surface and junction leakages and doubles approximately every 10°C.  $C_{OUT}$  is the output capacitance; it is the result of the N-channel MOS switches and varies from 80 pF to 110 pF, depending on the digital input code.  $R_O$  is the equivalent output resistance that also varies with digital input code. R is the nominal R-2R resistor ladder resistance.

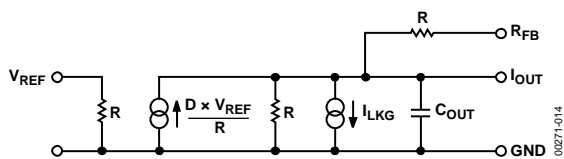


Figure 14. Equivalent Analog Circuit

## DYNAMIC PERFORMANCE

### Output Impedance

The output resistance of the DAC8043, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the  $I_{OUT}$  terminal, may be between 10 kΩ (the feedback resistor alone when all digital inputs are low) and 7.5 kΩ (the feedback resistor in parallel with approximately 30 kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be

affected by these variations. This variation is best illustrated by using the circuit of Figure 15 and the following equation:

$$V_{ERROR} = V_{OS} \left( 1 + \frac{R_{FB}}{R_O} \right)$$

where:

- $R_O$  is a function of the digital code and
- = 10 kΩ for more than four bits of Logic 1.
- = 30 kΩ for any single bit of Logic 1.

Therefore, the offset gain varies as follows:

At Code 0011 1111 1111,

$$V_{ERROR1} = V_{OS} \left( 1 + \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega} \right) = 2 V_{OS}$$

At Code 0100 0000 0000,

$$V_{ERROR2} = V_{OS} \left( 1 + \frac{10 \text{ k}\Omega}{30 \text{ k}\Omega} \right) = 4/3 V_{OS}$$

The error difference is  $2/3 V_{OS}$ .

Because one LSB has a weight (for  $V_{REF} = 10 \text{ V}$ ) of 2.4 mV for the DAC8043, it is clearly important that  $V_{OS}$  be minimized, either by using the amplifier's nulling pins or an external nulling network or by selecting an amplifier with inherently low  $V_{OS}$ . Amplifiers with sufficiently low  $V_{OS}$  include OP77, OP07, OP27, and OP42.

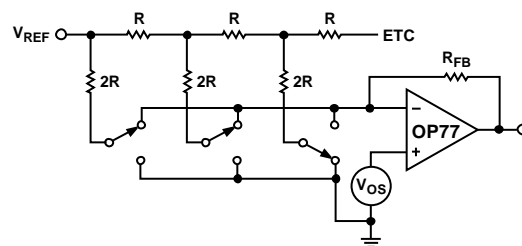


Figure 15. Simplified Circuit

The gain and phase stability of the output amplifier, board layout, and power supply decoupling all affect the dynamic performance. The use of a small compensation capacitor may be required when high speed operational amplifiers are used. It may be connected across the feedback resistor of the amplifier to provide the necessary phase compensation to critically damp the output. The output capacitance of the DAC8043 and the  $R_{FB}$  resistor form a pole that must be outside the amplifier's unity gain crossover frequency.

The considerations when using high speed amplifiers are:

1. Phase compensation (see Figure 16 and Figure 17).
2. Power supply decoupling at the device socket and the use of proper grounding techniques.

## APPLICATIONS INFORMATION

### APPLICATION TIPS

In most applications, linearity depends upon the potential of the I<sub>OUT</sub> and GND pins being equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figure 16 and Figure 17). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than 200 μV (less than 10% of 1 LSB).

The noninverting input of the operational amplifier should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V<sub>DD</sub> power supply should have a low noise level with no transients greater than 17 V.

### Unipolar Operation (2-Quadrant)

The circuits shown in Figure 16 and Figure 17 may be used with an ac or dc reference voltage. The output of the circuit ranges between 0 V and approximately -V<sub>REF</sub> (4095/4096), depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 6. The limiting parameters for the V<sub>REF</sub> range are the maximum input voltage range of the op amp or ±25 V, whichever is lowest.

Gain error may be trimmed by adjusting R<sub>1</sub>, as shown in Figure 17. The DAC register must first be loaded with all 1s. R<sub>1</sub> may then be adjusted until V<sub>OUT</sub> = -V<sub>REF</sub> (4095/4096). In the case of an adjustable V<sub>REF</sub>, R<sub>1</sub> and R<sub>2</sub> may be omitted, with V<sub>REF</sub> adjusted to yield the desired full-scale output.

In most applications, the DAC8043's negligible zero-scale error and very low gain error permit the elimination of the trimming components (R<sub>1</sub> and the external R<sub>2</sub>) without adversely affecting on circuit performance.

**Table 6. Unipolar Code Table<sup>1,2</sup>**

Digital Input MSB	LSB	Nominal Analog Output (V <sub>OUT</sub> as Shown in Figure 16 and Figure 17)
1111	1111 1111	$-V_{REF} \left( \frac{4095}{4096} \right)$
1000	0000 0001	$-V_{REF} \left( \frac{2049}{4096} \right)$
1000	0000 0000	$-V_{REF} \left( \frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0111	1111 1111	$-V_{REF} \left( \frac{2047}{4096} \right)$
0000	0000 0001	$-V_{REF} \left( \frac{1}{4096} \right)$
0000	0000 0000	$-V_{REF} \left( \frac{0}{4096} \right) = 0$

<sup>1</sup> Nominal full scale for Figure 16 and Figure 17 circuits is given by

$$FS = -V_{REF} \left( \frac{4095}{4096} \right)$$

<sup>2</sup> Nominal LSB magnitude for Figure 16 and Figure 17 circuits is given by

$$LSB = V_{REF} \left( \frac{1}{4096} \right) \text{ or } V_{REF} (2^{-n})$$

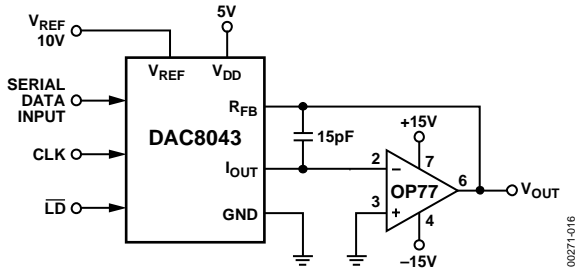


Figure 16. Unipolar Operation with High Accuracy Op Amp (2-Quadrant)

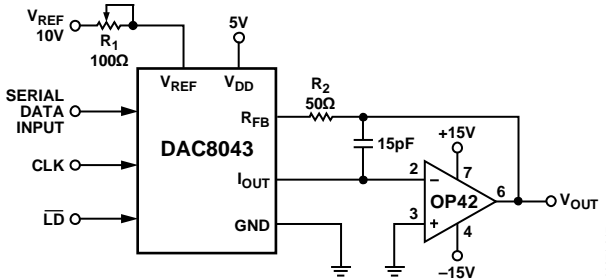


Figure 17. Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)

## Bipolar Operation (4-Quadrant)

Figure 19 details a suggested circuit for bipolar, or offset binary, operation. Table 7 shows the digital input to analog output relationship. The circuit uses offset binary coding. Twos complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

**Table 7. Bipolar (Offset Binary) Code Table<sup>1,2</sup>**

Digital Input	Nominal Analog Output
MSB      LSB	(V <sub>OUT</sub> as Shown in Figure 19)
1111 1111 1111	$+V_{REF} \left( \frac{2047}{2048} \right)$
1000 0000 0001	$+V_{REF} \left( \frac{1}{2048} \right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF} \left( \frac{1}{2048} \right)$
0000 0000 0001	$-V_{REF} \left( \frac{2047}{2048} \right)$
0000 0000 0000	$-V_{REF} \left( \frac{2048}{2048} \right)$

<sup>1</sup> Nominal full scale for Figure 19 circuits is given by

$$FS = V_{REF} \left( \frac{2047}{2048} \right)$$

<sup>2</sup> Nominal LSB magnitude for Figure 19 circuits is given by

$$LSB = V_{REF} \left( \frac{1}{2048} \right)$$

Resistors R<sub>3</sub>, R<sub>4</sub>, and R<sub>5</sub> must be selected to match within 0.01%, and they all must be of the same (preferably metal foil) type to ensure temperature coefficient matching. Mismatching between R<sub>3</sub> and R<sub>4</sub> causes offset and full-scale errors, while an R<sub>5</sub> to R<sub>4</sub> and R<sub>3</sub> mismatch results in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R<sub>1</sub> until V<sub>OUT</sub> = 0 V. R<sub>1</sub> and R<sub>2</sub> may be omitted, adjusting the ratio of R<sub>3</sub> to R<sub>4</sub> to yield V<sub>OUT</sub> = 0 V. Full

scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V<sub>REF</sub> or the value of R<sub>5</sub> until the desired V<sub>OUT</sub> is achieved.

## Analog/Digital Division

The transfer function for the DAC8043 connected in the multiplying mode, as shown in Figure 16, Figure 17, and Figure 19, is

$$V_O = -V_{IN} \left( \frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A<sub>X</sub> assumes a value of 1 for an on bit and 0 for an off bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier, as shown in Figure 18 and becomes

$$V_O = \left( \frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The previous transfer function is the division of an analog voltage (V<sub>REF</sub>) by a digital word. The amplifier goes to the rails with all bits off because division by zero is infinity. With all bits on the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, Bit 12, on.

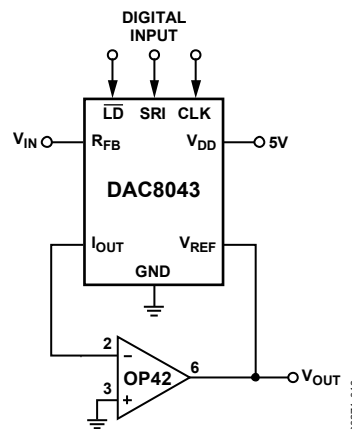


Figure 18. Analog/Digital Divider

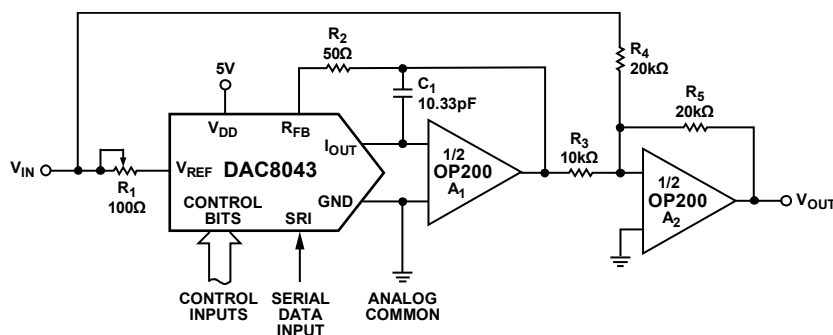


Figure 19. Bipolar Operation (4-Quadrant, Offset Binary)

# DAC8043

## INTERFACING TO THE MC6800

As shown in Figure 20, the DAC8043 may be interfaced to the MC6800 by successively executing memory write instructions while manipulating the data between writes, so that each write presents the next bit.

In this example, the most significant bits are found in the 0000 and 0001 memory locations. The four MSBs are found in the lower half of 0000 and the eight LSBs in 0001. The data is taken from the DB<sub>7</sub> line.

The serial data loading is triggered by the CLK pulse, which is asserted by a decoded memory write to the 2000 memory location, R/W, and Φ2. A write to address location 4000 transfers data from the input register to the DAC register.

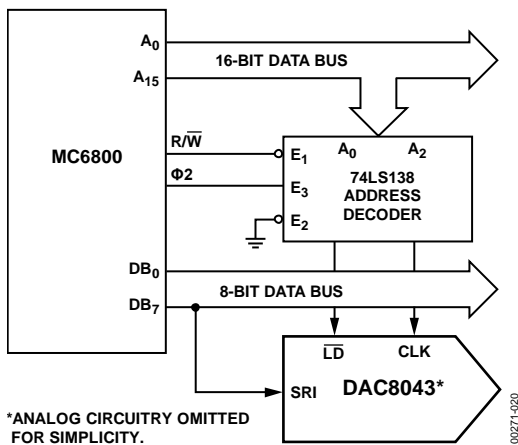


Figure 20. DAC8043 to MC6800 Interface

## DAC8043 INTERFACE TO THE 8085

The interface of the DAC8043 to the 8085 microprocessor is shown in Figure 21. Note that the SOD line of the microprocessor is used to present data serially to the DAC.

Data is clocked into the DAC8043 by executing memory write instructions. The clock input is generated by decoding Address 8000 and WR. Data is loaded into the DAC register with a memory write instruction to Address A000.

Serial data supplied to the DAC8043 must be present in the right-justified format in Register H and Register L of the microprocessor.

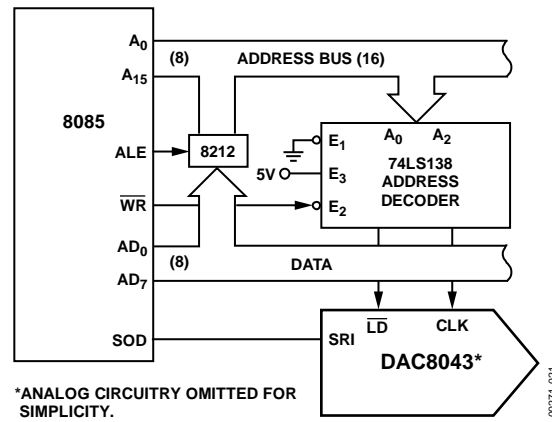


Figure 21. DAC8043 to 8085 Interface

## DAC8043 TO THE 68000 INTERFACE

The interface of the DAC8043 to the 68000 microprocessor is shown in Figure 22. Serial data to the DAC is taken from one of the microprocessor's data bus lines.

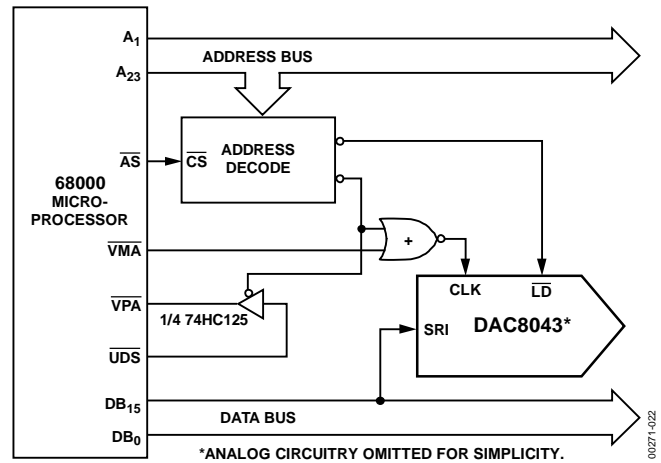
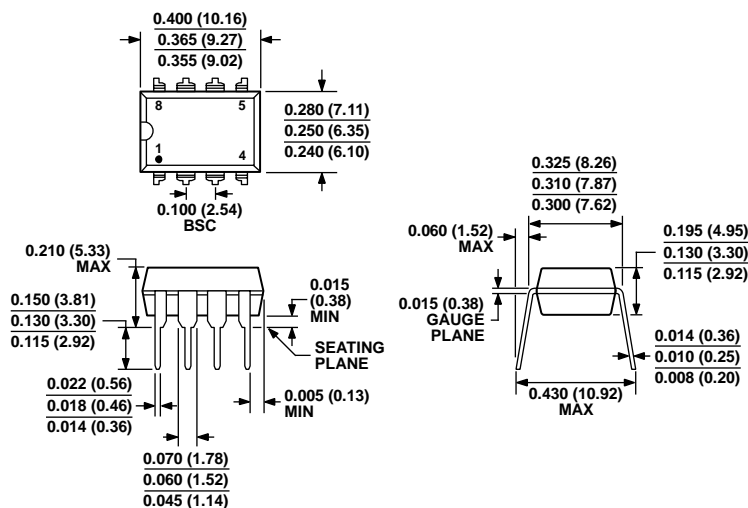


Figure 22. DAC8043 to 68000 Microprocessor Interface

# OUTLINE DIMENSIONS

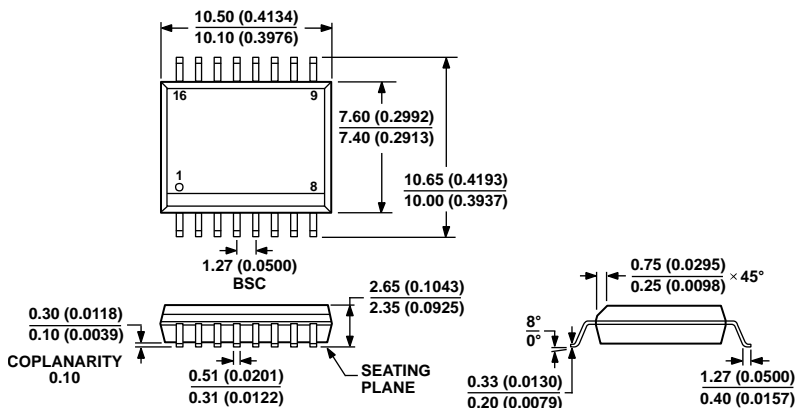


COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 23. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 16-Lead Standard Small Outline Package [SOIC\_W] Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

# DAC8043

## ORDERING GUIDE

Model <sup>1, 2</sup>	Relative Accuracy	Temperature Range	Package Description	Package Option
DAC8043FP	±1 LSB	−40°C to +85°C	8-Lead PDIP	N-8
DAC8043FPZ	±1 LSB	−40°C to +85°C	8-Lead PDIP	N-8
DAC8043FSZ	±1 LSB	−40°C to +85°C	16-Lead SOIC_W	RW-16
DAC8043GP	±½ LSB	0°C to 70°C	8-Lead PDIP	N-8
DAC8043GPZ	±½ LSB	0°C to 70°C	8-Lead PDIP	N-8

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> All commercial and industrial temperature range parts are available with burn-in.