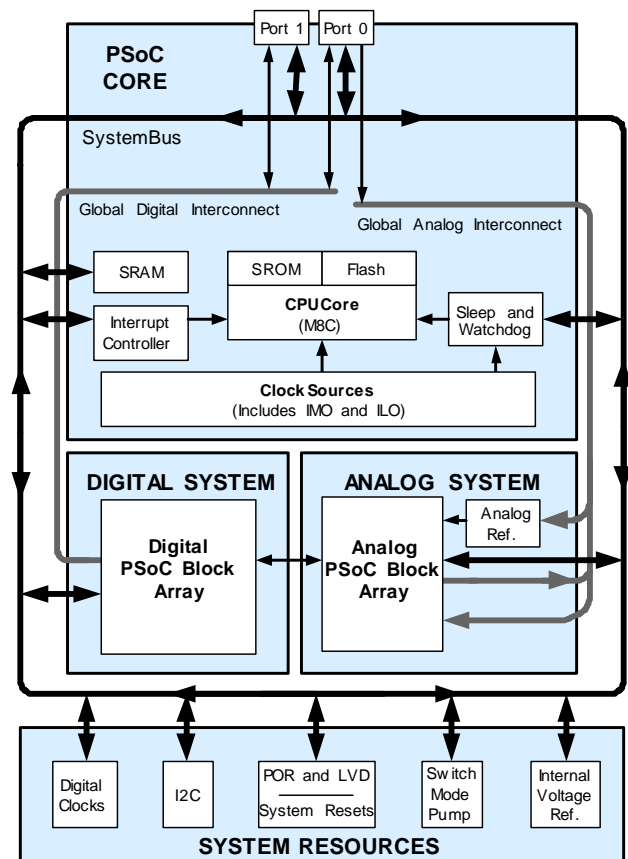


Features

- Powerful Harvard-architecture processor:
 - M8C processor speeds up to 24 MHz
 - Low power at high speed
 - Operating voltage: 2.4 V to 5.25 V
 - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
 - Industrial temperature range: -40 °C to +85 °C
- Advanced peripherals (PSoC[®] blocks):
 - Four analog type “E” PSoC blocks provide:
 - Two comparators with digital to analog converter (DAC) references
 - Single or dual 10-Bit 8-to-1 analog to digital converter (ADC)
 - Four digital PSoC blocks provide:
 - 8- to 32-bit timers and counters, 8- and 16-bit pulse-width modulators (PWMs)
 - CRC and PRS modules
 - Full duplex UART, SPI[™] master or slave: Connectable to all general-purpose I/O (GPIO) pins
 - Complex peripherals by combining blocks
- Flexible on-chip memory:
 - 4 KB flash program storage 50,000 erase/write cycles
 - 256 bytes SRAM data storage
 - In-system serial programming (ISSP)
 - Partial flash updates
 - Flexible protection modes
 - EEPROM emulation in flash
- Complete development tools:
 - Free development software (PSoC Designer[™])
 - Full-featured, in-circuit emulator (ICE) and programmer
 - Full-speed emulation
 - Complex breakpoint structure
 - 128-KB trace memory
- Precision, programmable clocking:
 - Internal ±2.5% 24- / 48-MHz main oscillator
 - Internal low-speed, low-power oscillator for watchdog and sleep functionality
- Programmable pin configurations:
 - 25-mA sink, 10-mA source on all GPIOs
 - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs
 - Up to eight analog inputs on all GPIOs
 - Configurable interrupt on all GPIOs

- Additional system resources:
 - I²C master, slave and multi-master to 400 kHz
 - Watchdog and sleep timers
 - User-configurable low-voltage detection (LVD)
 - Integrated supervisory circuit
 - On-chip precision voltage reference

Logic Block Diagram



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PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture allows you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as shown in Figure 1, consists of four main areas: the Core, the System Resources, the Digital System, and the Analog System. Configurable global bus resources allow the combining of all device resources into a complete custom system. Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 GPIO are also included. The GPIO provide access to the global digital and analog interconnects.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO), and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks or I²C functionality for implementing an I²C master, slave, MultiMaster, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, an SMP that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The digital system consists of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global bus that can route any signal to any pin. This frees designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators and analog-to-digital conversion up to 10 bits of precision.

Digital System

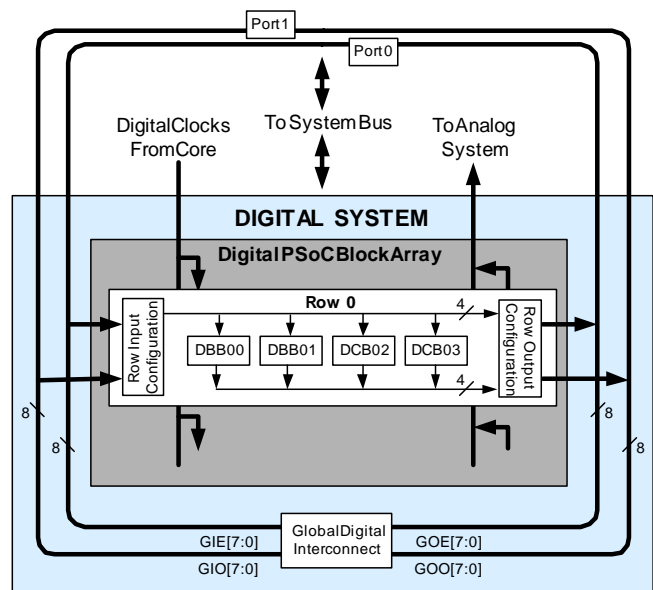
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to two)
- SPI master and slave
- I²C slave, master, multi-master (one available as a system resource)
- Cyclical redundancy checker/generator (8-bit)
- IrDA (up to two)
- Pseudo random sequence generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global bus that can route any signal to any pin. The busses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides an optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Figure 1. Digital System Block Diagram



Analog System

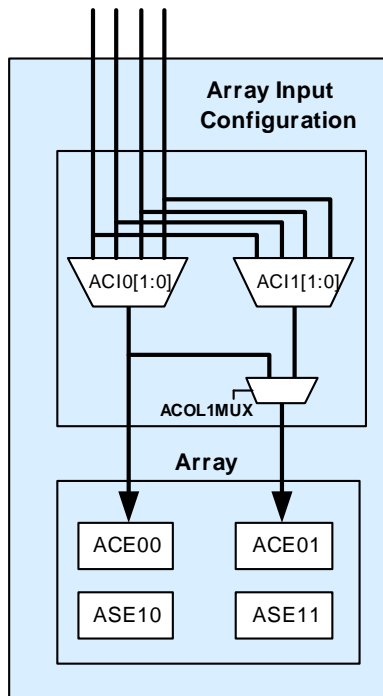
The analog system consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in [Table 1 on page 5](#).

Figure 2. CY8C21x23 Analog System Block Diagram



Additional System Resources

System resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I²C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|------------------|-------------|--------------|----------------|---------------|----------------|----------------|-----------------------------|-----------|------------|
| CY8C29x66 | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4 ^[1] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94 | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45 | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6 ^[1] | 1 K | 16 K |
| CY8C21x45 | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6 ^[1] | 512 | 8 K |
| CY8C21x34 | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4 ^[1] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4 ^[1] | 256 | 4 K |
| CY8C20x34 | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3 ^[1,2] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3 ^[1,2] | up to 2 K | up to 32 K |

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for this PSoC device.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at <http://www.cypress.com>.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They can be found at <http://www.cypress.com>.

Development Kits

PSoC Development Kits are available online from Cypress at <http://www.cypress.com> and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at <http://www.cypress.com>. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to <http://www.cypress.com> and refer to CYPros Consultants.

Solutions Library

Visit our growing library of solution focused designs at <http://www.cypress.com>. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at <http://www.cypress.com>. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes

- Limited analog functionality.
- Two analog blocks and one CapSense®.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at <http://www.cypress.com>. PSoC Designer comes with a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices. The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24MHz) operation.

Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36A/66A family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in a 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a "P") is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

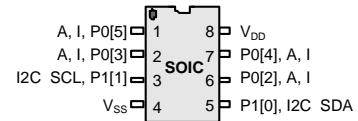
8-Pin Part Pinout

Table 2. Pin Definitions – CY8C21123 8-Pin SOIC

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[5] | Analog column mux input |
| 2 | I/O | I | P0[3] | Analog column mux input |
| 3 | I/O | | P1[1] | I ² C serial clock (SCL), ISSP-SCLK ^[3] |
| 4 | Power | | V _{SS} | Ground connection |
| 5 | I/O | | P1[0] | I ² C serial data (SDA), ISSP-SDATA ^[3] |
| 6 | I/O | I | P0[2] | Analog column mux input |
| 7 | I/O | I | P0[4] | Analog column mux input |
| 8 | Power | | V _{DD} | Supply voltage |

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C21123 8-Pin SOIC



16-Pin Part Pinout

Table 3. Pin Definitions – CY8C21223 16-Pin SOIC

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[7] | Analog column mux input |
| 2 | I/O | I | P0[5] | Analog column mux input |
| 3 | I/O | I | P0[3] | Analog column mux input |
| 4 | I/O | I | P0[1] | Analog column mux input |
| 5 | Power | | SMP | SMP connection to required external components |
| 6 | Power | | V _{SS} | Ground connection |
| 7 | I/O | | P1[1] | I ² C SCL, ISSP-SCLK ^[3] |
| 8 | Power | | V _{SS} | Ground connection |
| 9 | I/O | | P1[0] | I ² C SDA, ISSP-SDATA ^[3] |
| 10 | I/O | | P1[2] | |
| 11 | I/O | | P1[4] | Optional external clock input (EXTCLK) |
| 12 | I/O | I | P0[0] | Analog column mux input |
| 13 | I/O | I | P0[2] | Analog column mux input |
| 14 | I/O | I | P0[4] | Analog column mux input |
| 15 | I/O | I | P0[6] | Analog column mux input |
| 16 | Power | | V _{DD} | Supply voltage |

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. CY8C21223 16-Pin SOIC

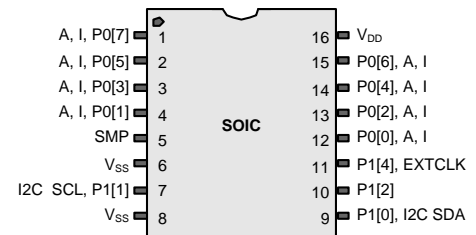
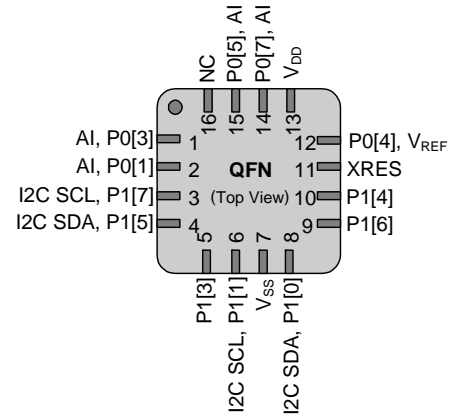


Table 4. Pin Definitions – CY8C21223 16-Pin QFN with no E-Pad^[3]

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P0[3] | Analog column mux input |
| 2 | I/O | I | P0[1] | Analog column mux input |
| 3 | I/O | | P1[7] | I ² C SCL |
| 4 | I/O | | P1[5] | I ² C SDA |
| 5 | I/O | | P1[3] | |
| 6 | I/O | | P1[1] | I ² C SCL, ISSP-SCLK ^[3] |
| 7 | Power | | V _{SS} | Ground connection |
| 8 | I/O | | P1[0] | I ² C SDA, ISSP-SDATA ^[3] |
| 9 | I/O | | P1[6] | |
| 10 | I/O | | P1[4] | EXTCLK |
| 11 | Input | | XRES | Active high external reset with internal pull-down |
| 12 | I/O | I | P0[4] | V _{REF} |
| 13 | Power | | V _{DD} | Supply voltage |
| 14 | I/O | I | P0[7] | Analog column mux input |
| 15 | I/O | I | P0[5] | Analog column mux input |
| 16 | | | NC | No Connection. Pin must be left floating |

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. CY8C21223 16-Pin QFN



Notes

- These are the ISSP pins, which are not high Z at POR (power on reset). See the [PSoC Technical Reference Manual](#) for details.
- The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

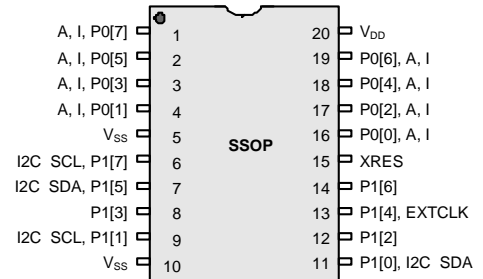
20-Pin Part Pinout

Table 5. Pin Definitions – CY8C21323 20-Pin SSOP

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P0[7] | Analog column mux input |
| 2 | I/O | I | P0[5] | Analog column mux input |
| 3 | I/O | I | P0[3] | Analog column mux input |
| 4 | I/O | I | P0[1] | Analog column mux input |
| 5 | Power | | V _{SS} | Ground connection |
| 6 | I/O | | P1[7] | I ² C SCL |
| 7 | I/O | | P1[5] | I ² C SDA |
| 8 | I/O | | P1[3] | |
| 9 | I/O | | P1[1] | I ² C SCL, ISSP-SCLK ^[3] |
| 10 | Power | | V _{SS} | Ground connection |
| 11 | I/O | | P1[0] | I ² C SDA, ISSP-SDATA ^[3] |
| 12 | I/O | | P1[2] | |
| 13 | I/O | | P1[4] | Optional EXTCLK input |
| 14 | I/O | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull-down |
| 16 | I/O | I | P0[0] | Analog column mux input |
| 17 | I/O | I | P0[2] | Analog column mux input |
| 18 | I/O | I | P0[4] | Analog column mux input |
| 19 | I/O | I | P0[6] | Analog column mux input |
| 20 | Power | | V _{DD} | Supply voltage |

LEGEND A = Analog, I = Input, and O = Output.

Figure 6. CY8C21323 20-Pin SSOP



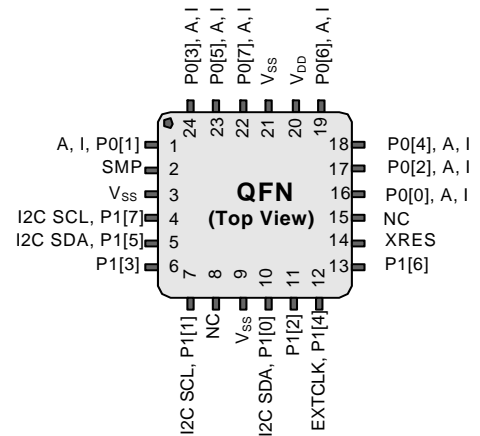
24-Pin Part Pinout

Table 6. Pin Definitions – CY8C21323 24-Pin QFN^[5]

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P0[1] | Analog column mux input |
| 2 | Power | | SMP | SMP connection to required external components |
| 3 | Power | | V _{SS} | Ground connection |
| 4 | I/O | | P1[7] | I ² C SCL |
| 5 | I/O | | P1[5] | I ² C SDA |
| 6 | I/O | | P1[3] | |
| 7 | I/O | | P1[1] | I ² C SCL, ISSP-SCLK ^[3] |
| 8 | | | NC | No connection. Pin must be left floating |
| 9 | Power | | V _{SS} | Ground connection |
| 10 | I/O | | P1[0] | I ² C SDA, ISSP-SDATA ^[3] |
| 11 | I/O | | P1[2] | |
| 12 | I/O | | P1[4] | Optional (EXTCLK) input |
| 13 | I/O | | P1[6] | |
| 14 | Input | | XRES | Active high external reset with internal pull-down |
| 15 | | | NC | No connection. Pin must be left floating |
| 16 | I/O | I | P0[0] | Analog column mux input |
| 17 | I/O | I | P0[2] | Analog column mux input |
| 18 | I/O | I | P0[4] | Analog column mux input |
| 19 | I/O | I | P0[6] | Analog column mux input |
| 20 | Power | | V _{DD} | Supply voltage |
| 21 | Power | | V _{SS} | Ground connection |
| 22 | I/O | I | P0[7] | Analog column mux input |
| 23 | I/O | I | P0[5] | Analog column mux input |
| 24 | I/O | I | P0[3] | Analog column mux input |

LEGEND A = Analog, I = Input, and O = Output.

Figure 7. CY8C21323 24-Pin QFN



Note

- The center pad on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

Register Reference

This section lists the registers of the CY8C21x23 PSoC device. For detailed register information, refer the [PSoC Technical Reference Manual](#).

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 7. Register Conventions

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines the bank you are currently in. When the XOI bit is set, you are in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 8. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | | D0 | |
| | 11 | | | 51 | | | 91 | | | D1 | |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | | D3 | |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 8. Register Map Bank 0 Table: User Space (continued)

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|------|--------------|--------|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | | D8 | |
| | 19 | | | 59 | | | 99 | | | D9 | |
| | 1A | | | 5A | | | 9A | | | DA | |
| | 1B | | | 5B | | | 9B | | | DB | |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|-----------|--------------|--------|---------|--------------|--------|-----------|--------------|--------|
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | ADC0_TR | E5 | RW |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | ADC1_TR | E6 | RW |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CLK_CR3 | 6B | RW | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | FLS_PR1 | FA | RW |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x23 PSoC device. For up to date electrical specifications, check if you have the latest datasheet by visiting the web at <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted.

Refer to [Table 24 on page 25](#) for the electrical specifications on the IMO using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

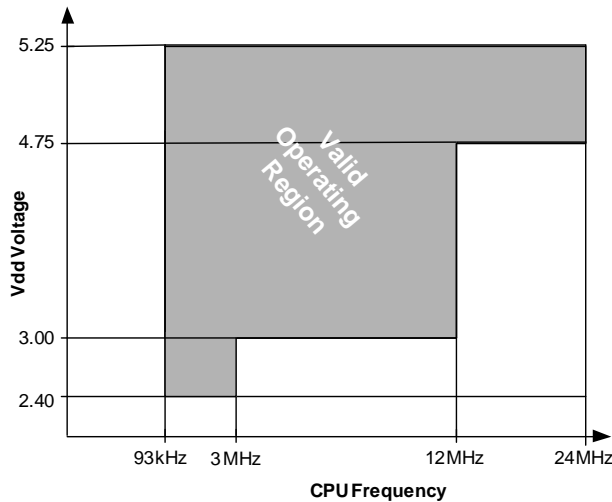
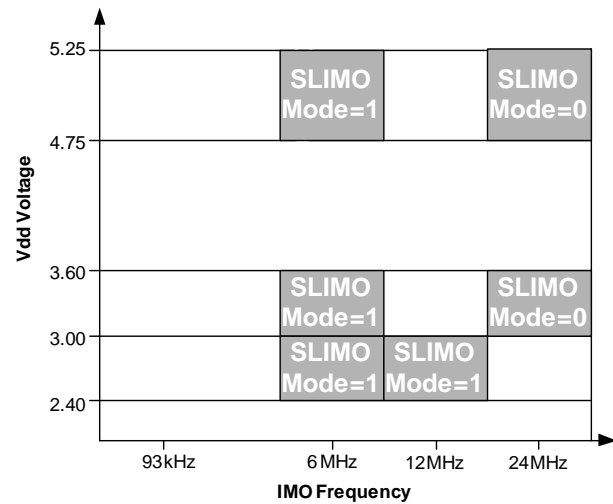


Figure 11. Voltage versus IMO Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|---|-------------------|-----|-------------------|--------------------|--|
| T_{STG} | Storage temperature | -55 | - | +100 | $^{\circ}\text{C}$ | Higher storage temperatures reduce data retention time. Recommended storage temperature is $+25\text{ }^{\circ}\text{C} \pm 25\text{ }^{\circ}\text{C}$. Extended duration storage temperatures higher than $65\text{ }^{\circ}\text{C}$ degrade reliability. |
| $T_{BAKETEMP}$ | Bake temperature | - | 125 | See package label | $^{\circ}\text{C}$ | |
| $t_{BAKETIME}$ | Bake time | See package label | - | 72 | Hours | |
| T_A | Ambient temperature with power applied | -40 | - | +85 | $^{\circ}\text{C}$ | |
| V_{DD} | Supply voltage on V_{DD} relative to V_{SS} | -0.5 | - | +6.0 | V | |
| V_{IO} | DC input voltage | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| V_{IOZ} | DC voltage applied to tristate | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| I_{MIO} | Maximum current into any port pin | -25 | - | +50 | mA | |
| ESD | Electro static discharge voltage | 2000 | - | - | V | Human body model ESD |
| LU | Latch-up current | - | - | 200 | mA | |

Operating Temperature

Table 11. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|--|
| T _A | Ambient temperature | -40 | - | +85 | °C | |
| T _J | Junction temperature | -40 | - | +100 | °C | The temperature rise from ambient to junction is package specific. See Table 36 on page 35 . You must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

[Table 12](#) lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, 3.0 V to 3.6 V and $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, or 2.4 V to 3.0 V and $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 12. DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|--------------------------|------------------|--------------------------|-------|--|
| V _{DD} | Supply voltage | 2.40 | - | 5.25 | V | See DC POR and LVD specifications, Table 19 on page 21 . |
| I _{DD} | Supply current, IMO = 24 MHz | - | 3 | 4 | mA | Conditions are V _{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSClk doubler disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 0.366 kHz |
| I _{DD3} | Supply current, IMO = 6 MHz | - | 1.2 | 2 | mA | Conditions are V _{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz |
| I _{DD27} | Supply current, IMO = 6 MHz | - | 1.1 | 1.5 | mA | Conditions are V _{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz |
| I _{SB27} | Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range. | - | 2.6 | 4 | µA | V _{DD} = 2.55 V, 0 °C to 40 °C |
| I _{SB} | Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. | - | 2.8 | 5 | µA | V _{DD} = 3.3 V, $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ |
| V _{REF} | Reference voltage (bandgap) | 1.28 | 1.30 | 1.32 | V | Trimmed for appropriate V _{DD} . V _{DD} = 3.0 V to 5.25 V |
| V _{REF27} | Reference voltage (bandgap) | 1.16 | 1.30 | 1.330 | V | Trimmed for appropriate V _{DD} . V _{DD} = 2.4 V to 3.0 V |
| AGND | Analog ground | V _{REF} - 0.003 | V _{REF} | V _{REF} + 0.003 | V | |

DC GPIO Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|--|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High output level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget. |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget. |
| I _{OH} | High level source current | 10 | – | – | mA | V _{OH} = V _{DD} - 1.0 V, see the limitations of the total current in the note for V _{OH} |
| I _{OL} | Low level sink current | 25 | – | – | mA | V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL} |
| V _{IL} | Input low level | – | – | 0.8 | V | V _{DD} = 3.0 to 5.25 |
| V _{IH} | Input high level | 2.1 | – | – | V | V _{DD} = 3.0 to 5.25 |
| V _H | Input hysteresis | – | 60 | – | mV | |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C |

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$. Typical parameters apply to 2.7 V at 25 °C and are for design guidance only.

Table 14. 2.7-V DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|---|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High output level | V _{DD} - 0.4 | – | – | V | I _{OH} = 2.5 mA (6.25 Typ), V _{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I _{OH} budget). |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 10 mA, V _{DD} = 2.4 to 3.0 V (90 mA maximum combined I _{OL} budget). |
| I _{OH} | High level source current | 2.5 | – | – | mA | V _{OH} = V _{DD} - 0.4 V, see the limitations of the total current in the note for V _{OH} |
| I _{OL} | Low level sink current | 10 | – | – | mA | V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL} |
| V _{IL} | Input low level | – | – | 0.75 | V | V _{DD} = 2.4 to 3.0 |
| V _{IH} | Input high level | 2.0 | – | – | V | V _{DD} = 2.4 to 3.0 |
| V _H | Input hysteresis | – | 60 | – | mV | |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C |

DC Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. 5-V DC Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|-----|-----|--------------|--------------------------------|--|
| V_{OSOA} | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| TCV_{OSOA} | Average input offset voltage drift | – | 10 | – | $\mu\text{V}/^{\circ}\text{C}$ | |
| I_{EBOA} | Input leakage current (port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 μA |
| C_{INOA} | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| V_{CMOA} | Common mode voltage range | 0.0 | – | $V_{DD} - 1$ | V | |
| G_{OLOA} | Open loop gain | 80 | – | – | dB | |
| I_{SOA} | Amplifier supply current | – | 10 | 30 | μA | |

Table 16. 3.3-V DC Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|-----|-----|--------------|--------------------------------|--|
| V_{OSOA} | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| TCV_{OSOA} | Average input offset voltage drift | – | 10 | – | $\mu\text{V}/^{\circ}\text{C}$ | |
| I_{EBOA} | Input leakage current (port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 μA |
| C_{INOA} | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| V_{CMOA} | Common mode voltage range | 0 | – | $V_{DD} - 1$ | V | |
| G_{OLOA} | Open loop gain | 80 | – | – | dB | |
| I_{SOA} | Amplifier supply current | – | 10 | 30 | μA | |

Table 17. 2.7V DC Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|-----|-----|--------------|--------------------------------|--|
| V_{OSOA} | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| TCV_{OSOA} | Average input offset voltage drift | – | 10 | – | $\mu\text{V}/^{\circ}\text{C}$ | |
| I_{EBOA} | Input leakage current (port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 μA |
| C_{INOA} | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| V_{CMOA} | Common mode voltage range | 0 | – | $V_{DD} - 1$ | V | |
| G_{OLOA} | Open loop gain | 80 | – | – | dB | |
| I_{SOA} | Amplifier supply current | – | 10 | 30 | μA | |

DC Switch Mode Pump Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

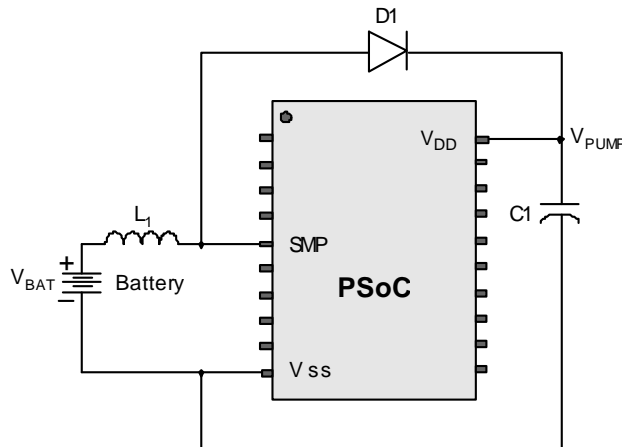
Table 18. DC Switch Mode Pump (SMP) Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------|---|-------------|-------------|-------------|----------------|---|
| V_{PUMP5V} | 5 V output voltage from pump | 4.75 | 5.0 | 5.25 | V | Configuration of footnote. ^[6] Average, neglecting ripple. SMP trip voltage is set to 5.0 V. |
| V_{PUMP3V} | 3.3 V output voltage from pump | 3.00 | 3.25 | 3.60 | V | Configuration of footnote. ^[6] Average, neglecting ripple. SMP trip voltage is set to 3.25 V. |
| V_{PUMP2V} | 2.6 V output voltage from pump | 2.45 | 2.55 | 2.80 | V | Configuration of footnote. ^[6] Average, neglecting ripple. SMP trip voltage is set to 2.55 V. |
| I_{PUMP} | Available output current $V_{BAT} = 1.8\text{ V}, V_{PUMP} = 5.0\text{ V}$ $V_{BAT} = 1.5\text{ V}, V_{PUMP} = 3.25\text{ V}$ $V_{BAT} = 1.3\text{ V}, V_{PUMP} = 2.55\text{ V}$ | 5 8 8 | – – – | – – – | mA mA mA | Configuration of footnote. ^[6] SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V. |
| V_{BAT5V} | Input voltage range from battery | 1.8 | – | 5.0 | V | Configuration of footnote. ^[6] SMP trip voltage is set to 5.0 V. |
| V_{BAT3V} | Input voltage range from battery | 1.0 | – | 3.3 | V | Configuration of footnote. ^[6] SMP trip voltage is set to 3.25 V. |
| V_{BAT2V} | Input voltage range from battery | 1.0 | – | 2.8 | V | Configuration of footnote. ^[6] SMP trip voltage is set to 2.55 V. |
| $V_{BATSTART}$ | Minimum input voltage from battery to start pump | 1.2 | – | – | V | Configuration of footnote. ^[6] $0\text{ }^{\circ}\text{C} \leq T_A \leq 100$. 1.25 V at $T_A = -40\text{ }^{\circ}\text{C}$. |
| ΔV_{PUMP_Line} | Line regulation (over V_i range) | – | 5 | – | % V_O | Configuration of footnote. ^[6] V_O is the “ V_{DD} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21. |
| ΔV_{PUMP_Load} | Load regulation | – | 5 | – | % V_O | Configuration of footnote. ^[6] V_O is the “ V_{DD} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21. |
| ΔV_{PUMP_Ripple} | Output voltage ripple (depends on cap/load) | – | 100 | – | mVpp | Configuration of footnote. ^[6] Load is 5 mA. |
| E_3 | Efficiency | 35 | 50 | – | % | Configuration of footnote. ^[6] Load is 5 mA. SMP trip voltage is set to 3.25 V. |
| E_2 | Efficiency | 35 | 80 | – | % | For $I_{load} = 1\text{ mA}$, $V_{PUMP} = 2.55\text{ V}$, $V_{BAT} = 1.3\text{ V}$, 10 uH inductor, 1 uF capacitor, and Schottky diode. |
| F_{PUMP} | Switching frequency | – | 1.3 | – | MHz | |
| DC_{PUMP} | Switching duty cycle | – | 50 | – | % | |

Note

6. $L_1 = 2\text{ mH}$ inductor, $C_1 = 10\text{ mF}$ capacitor, $D_1 =$ Schottky diode. Refer to Figure 12 on page 21.

Figure 12. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC POR and LVD Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|---|------|------|----------------------|-------|--|
| V_{PPOR0} | V_{DD} value for PPOR trip PORLEV[1:0] = 00b | – | 2.36 | 2.40 | V | V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog. |
| V_{PPOR1} | PORLEV[1:0] = 01b | – | 2.82 | 2.95 | V | |
| V_{PPOR2} | PORLEV[1:0] = 10b | – | 4.55 | 4.70 | V | |
| V_{LVD0} | V_{DD} value for LVD trip VM[2:0] = 000b | 2.40 | 2.45 | 2.51 ^[7] | V | |
| V_{LVD1} | VM[2:0] = 001b | 2.85 | 2.92 | 2.99 ^[8] | V | |
| V_{LVD2} | VM[2:0] = 010b | 2.95 | 3.02 | 3.09 | V | |
| V_{LVD3} | VM[2:0] = 011b | 3.06 | 3.13 | 3.20 | V | |
| V_{LVD4} | VM[2:0] = 100b | 4.37 | 4.48 | 4.55 | V | |
| V_{LVD5} | VM[2:0] = 101b | 4.50 | 4.64 | 4.75 | V | |
| V_{LVD6} | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| V_{LVD7} | VM[2:0] = 111b | 4.71 | 4.81 | 4.95 | V | |
| V_{PUMP0} | V_{DD} value for PUMP trip VM[2:0] = 000b | 2.45 | 2.55 | 2.62 ^[9] | V | |
| V_{PUMP1} | VM[2:0] = 001b | 2.96 | 3.02 | 3.09 | V | |
| V_{PUMP2} | VM[2:0] = 010b | 3.03 | 3.10 | 3.16 | V | |
| V_{PUMP3} | VM[2:0] = 011b | 3.18 | 3.25 | 3.32 ^[10] | V | |
| V_{PUMP4} | VM[2:0] = 100b | 4.54 | 4.64 | 4.74 | V | |
| V_{PUMP5} | VM[2:0] = 101b | 4.62 | 4.73 | 4.83 | V | |
| V_{PUMP6} | VM[2:0] = 110b | 4.71 | 4.82 | 4.92 | V | |
| V_{PUMP7} | VM[2:0] = 111b | 4.89 | 5.00 | 5.12 | V | |

Notes

7. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
8. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
9. Always greater than 50 mV above V_{LVD0} .
10. Always greater than 50 mV above V_{LVD3} .

DC Programming Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|---|------------------------|-----|------------------------|-------|--|
| V _{DDP} | V _{DD} for programming and erase | 4.5 | 5.0 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDL} | Low V _{DD} for verify | 2.4 | 2.5 | 2.6 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDHV} | High V _{DD} for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDIWRITE} | Supply voltage for flash write operations | 2.70 | – | 5.25 | V | This specification applies to this device when it is executing internal flash writes |
| I _{DDP} | Supply current during programming or verify | – | 5 | 25 | mA | |
| V _{ILP} | Input low voltage during programming or verify | – | – | 0.8 | V | |
| V _{IHP} | Input high voltage during programming or verify | 2.2 | – | – | V | |
| I _{ILP} | Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor |
| V _{OLV} | Output low voltage during programming or verify | – | – | V _{SS} + 0.75 | V | |
| V _{OHV} | Output high voltage during programming or verify | V _{DD} – 1.0 | – | V _{DD} | V | |
| Flash _{ENPB} | Flash endurance (per block) | 50,000 ^[11] | – | – | – | Erase/write cycles per block |
| Flash _{ENT} | Flash endurance (total) ^[12] | 1,800,000 | – | – | – | Erase/write cycles |
| Flash _{DR} | Flash data retention | 10 | – | – | Years | |

DC I²C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 21. DC I²C Specifications^[13]

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|------------------|-----------------------|-----|------------------------|-------|-----------------------------------|
| V _{ILI2C} | Input low level | – | – | 0.3 × V _{DD} | V | 2.4 V ≤ V _{DD} ≤ 3.6 V |
| | | – | – | 0.25 × V _{DD} | V | 4.75 V ≤ V _{DD} ≤ 5.25 V |
| V _{IHI2C} | Input high level | 0.7 × V _{DD} | – | – | V | 2.4 V ≤ V _{DD} ≤ 5.25 V |

Notes

11. The 50,000 cycle flash endurance per block is guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.

12. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, [Design Aids — Reading and Writing PSoC[®] Flash — AN2015](#) for more information on Flash APIs.

13. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section [DC GPIO Specifications on page 18](#). The I²C GPIO pins also meet the mentioned specs.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 22. 5-V and 3.3-V AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------------|--|--------|------|-------------------------|-------|--|
| F _{IMO24} | IMO frequency for 24 MHz | 23.4 | 24 | 24.6 ^[14,15] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. Refer to Figure 11 on page 16 . SLIMO mode = 0. |
| F _{IMO6} | IMO frequency for 6 MHz | 5.5 | 6 | 6.5 ^[14,15] | MHz | Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 16 . SLIMO mode = 1. |
| F _{CPU1} | CPU frequency (5 V nominal) | 0.0937 | 24 | 24.6 ^[14] | MHz | 12 MHz only for SLIMO mode = 0. |
| F _{CPU2} | CPU frequency (3.3 V nominal) | 0.0937 | 12 | 12.3 ^[15] | MHz | SLIMO Mode = 0. |
| F _{BLK5} | Digital PSoC block frequency (5 V nominal) | 0 | 48 | 49.2 ^[14,16] | MHz | Refer to the section AC Digital Block Specifications on page 26 . |
| F _{BLK33} | Digital PSoC block frequency (3.3 V nominal) | 0 | 24 | 24.6 ^[16] | MHz | |
| F _{32K1} | ILO frequency | 15 | 32 | 64 | kHz | |
| F _{32K_U} | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing. |
| t _{XRST} | External reset pulse width | 10 | – | – | μs | |
| DC _{24M} | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| DC _{ILO} | ILO duty cycle | 20 | 50 | 80 | % | |
| Step _{24M} | 24 MHz trim step size | – | 50 | – | kHz | |
| F _{out48M} | 48 MHz output frequency | 46.8 | 48.0 | 49.2 ^[14,15] | MHz | Trimmed. Using factory trim values. |
| F _{MAX} | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| SR _{POWER_UP} | Power supply slew rate | – | – | 250 | V/ms | V _{DD} slew rate during power-up. |
| t _{POWERUP} | Time from end of POR to CPU executing code | – | 16 | 100 | ms | Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual . |
| t _{jit_IMO} | 24-MHz IMO cycle-to-cycle jitter (RMS) ^[17] | – | 200 | 700 | ps | |
| | 24-MHz IMO long term N cycle-to-cycle jitter (RMS) ^[17] | – | 300 | 900 | ps | N = 32 |
| | 24-MHz IMO period jitter (RMS) ^[17] | – | 100 | 400 | ps | |

Notes

14. 4.75 V < V_{DD} < 5.25 V.

15. 3.0 V < V_{DD} < 3.6 V. Refer to the application note, [Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012](#) for more information on trimming for operation at 3.3 V.

16. See the individual user module datasheets for information on maximum frequencies for user modules.

17. Refer to the application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information on jitter specifications.

Table 23. 2.7-V AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------------|--|-------|-----|-------------------------|-------|--|
| F _{IMO12} | IMO frequency for 12 MHz | 11.5 | 12 | 12.7 ^[18,19] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16 . SLIMO mode = 1. |
| F _{IMO6} | IMO frequency for 6 MHz | 5.5 | 6 | 6.5 ^[18,19] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16 . SLIMO mode = 1. |
| F _{CPU1} | CPU frequency (2.7 V nominal) | 0.093 | 3 | 3.15 ^[18] | MHz | 24 MHz only for SLIMO mode = 0. |
| F _{BLK27} | Digital PSoC block frequency (2.7 V nominal) | 0 | 12 | 12.5 ^[18,19] | MHz | Refer to the section AC Digital Block Specifications on page 26 . |
| F _{32K1} | ILO frequency | 8 | 32 | 96 | kHz | |
| F _{32K_U} | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing. |
| t _{XRST} | External reset pulse width | 10 | – | – | μs | |
| DC _{ILO} | ILO duty cycle | 20 | 50 | 80 | % | |
| F _{MAX} | Maximum frequency of signal on row input or row output | – | – | 12.3 | MHz | |
| SR _{POWER_UP} | Power supply slew rate | – | – | 250 | V/ms | V _{DD} slew rate during power-up. |
| t _{POWERUP} | Time from end of POR to CPU executing code | – | 16 | 100 | ms | Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual . |
| t _{jit_IMO} | 12-MHz IMO cycle-to-cycle jitter (RMS) ^[20] | – | 400 | 1000 | ps | |
| | 12-MHz IMO long term N cycle-to-cycle jitter (RMS) ^[20] | – | 600 | 1300 | ps | N = 32 |
| | 12-MHz IMO period jitter (RMS) ^[20] | – | 100 | 500 | ps | |

Notes

 18. 2.4 V < V_{DD} < 3.0 V.

 19. Refer to the application note [Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012](#) for more information on maximum frequency for user modules.

 20. Refer to the application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information on jitter specifications.

AC General Purpose I/O Specifications

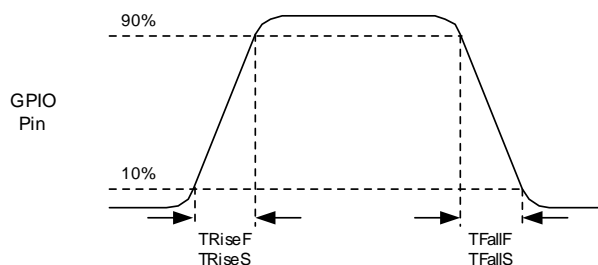
Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 24. 5-V and 3.3-V AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|-----|-----|-----|-------|--|
| F_{GPIO} | GPIO operating frequency | 0 | – | 12 | MHz | Normal strong mode |
| t_{RiseF} | Rise time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 3 | – | 18 | ns | $V_{\text{DD}} = 4.5\text{ V to }5.25\text{ V}$, 10% to 90% |
| t_{FallF} | Fall time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 2 | – | 18 | ns | $V_{\text{DD}} = 4.5\text{ V to }5.25\text{ V}$, 10% to 90% |
| t_{RiseS} | Rise time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 10 | 27 | – | ns | $V_{\text{DD}} = 3\text{ V to }5.25\text{ V}$, 10% to 90% |
| t_{FallS} | Fall time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 10 | 22 | – | ns | $V_{\text{DD}} = 3\text{ V to }5.25\text{ V}$, 10% to 90% |

Table 25. 2.7-V AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|-----|-----|-----|-------|---|
| F_{GPIO} | GPIO operating frequency | 0 | – | 3 | MHz | Normal strong mode |
| t_{RiseF} | Rise time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 6 | – | 50 | ns | $V_{\text{DD}} = 2.4\text{ V to }3.0\text{ V}$, 10% to 90% |
| t_{FallF} | Fall time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 6 | – | 50 | ns | $V_{\text{DD}} = 2.4\text{ V to }3.0\text{ V}$, 10% to 90% |
| t_{RiseS} | Rise time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 18 | 40 | 120 | ns | $V_{\text{DD}} = 2.4\text{ V to }3.0\text{ V}$, 10% to 90% |
| t_{FallS} | Fall time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 18 | 40 | 120 | ns | $V_{\text{DD}} = 2.4\text{ V to }3.0\text{ V}$, 10% to 90% |

Figure 13. GPIO Timing Diagram

AC Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Table 26. 5-V and 3.3-V AC Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units |
|--------------------|---|-----|-----|-----|-------|
| t_{COMP1} | Comparator mode response time, 50 mVpp signal centered on Ref | – | – | 100 | ns |
| t_{COMP2} | Comparator mode response time, 2.5 V input, 0.5 V overdrive | – | – | 300 | ns |

Table 27. 2.7-V AC Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units |
|--------------------|---|-----|-----|-----|-------|
| t_{COMP1} | Comparator mode response time, 50 mVpp signal centered on Ref | – | – | 600 | ns |
| t_{COMP2} | Comparator mode response time, 1.5 V input, 0.5 V overdrive | – | – | 300 | ns |

AC Digital Block Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Unit | Notes |
|-------------------|--|--------------------|-----|------|------|---|
| All functions | Block input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| Timer | Input clock frequency | | | | | |
| | No capture, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | No capture, $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| | With capture | – | – | 24.6 | MHz | |
| | Capture pulse width | 50 ^[21] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | No enable input, $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| | With enable input | – | – | 24.6 | MHz | |
| | Enable input pulse width | 50 ^[21] | – | – | ns | |
| Dead Band | Kill pulse width | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 ^[21] | – | – | ns | |
| | Disable mode | 50 ^[21] | – | – | ns | |
| | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| CRCPRS (PRS Mode) | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| CRCPRS (CRC Mode) | Input clock frequency | – | – | 24.6 | MHz | |
| SPIM | Input clock frequency | – | – | 8.2 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock (SCLK) frequency | – | – | 4.1 | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_negated between transmissions | 50 ^[21] | – | – | ns | |
| Transmitter | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75\text{ V}$, 2 stop bits | – | – | 49.2 | MHz | |
| | $V_{DD} \geq 4.75\text{ V}$, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| Receiver | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75\text{ V}$, 2 stop bits | – | – | 49.2 | MHz | |
| | $V_{DD} \geq 4.75\text{ V}$, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |

Note

21. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 29. 2.7-V AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|---------------------|-----|------|-------|---|
| All functions | Block input clock frequency | – | – | 12.7 | MHz | 2.4 V < V _{DD} < 3.0 V. |
| Timer | Capture pulse width | 100 ^[22] | – | – | ns | |
| | Input clock frequency, with or without capture | – | – | 12.7 | MHz | |
| Counter | Enable input pulse width | 100 | – | – | ns | |
| | Input clock frequency, no enable input | – | – | 12.7 | MHz | |
| | Input clock frequency, enable input | – | – | 12.7 | MHz | |
| Dead band | Kill pulse width: | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 100 | – | – | ns | |
| | Disable mode | 100 | – | – | ns | |
| | Input clock frequency | – | – | 12.7 | MHz | |
| CRCPRS (PRS mode) | Input clock frequency | – | – | 12.7 | MHz | |
| CRCPRS (CRC mode) | Input clock frequency | – | – | 12.7 | MHz | |
| SPIM | Input clock frequency | – | – | 6.35 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock (SCLK) frequency | – | – | 4.1 | MHz | |
| | Width of SS_ Negated between transmissions | 100 | – | – | ns | |
| Transmitter | Input clock frequency | – | – | 12.7 | MHz | The baud rate is equal to the input clock frequency divided by 8. |
| Receiver | Input clock frequency | – | – | 12.7 | MHz | The baud rate is equal to the input clock frequency divided by 8. |

Note

22. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F _{OSCEXT} | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High period | 20.6 | – | 5300 | ns | |
| – | Low period | 20.6 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | μs | |

Table 31. 3.3-V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-------|-----|------|-------|---|
| F _{OSCEXT} | Frequency with CPU clock divide by 1 | 0.093 | – | 12.3 | MHz | Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| F _{OSCEXT} | Frequency with CPU clock divide by 2 or greater | 0.186 | – | 24.6 | MHz | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| – | High period with CPU clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 41.7 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | μs | |

Table 32. 2.7-V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-------|-----|-------|-------|--|
| F _{OSCEXT} | Frequency with CPU clock divide by 1 | 0.093 | – | 6.06 | MHz | Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| F _{OSCEXT} | Frequency with CPU clock divide by 2 or greater | 0.186 | – | 12.12 | MHz | If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| – | High period with CPU clock divide by 1 | 83.4 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 83.4 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | μs | |

AC Programming Specifications

Table 33 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|---------------------|-------|---|
| t_{RSCLK} | Rise time of SCLK | 1 | – | 20 | ns | |
| t_{FSCLK} | Fall time of SCLK | 1 | – | 20 | ns | |
| t_{SSCLK} | Data set up time to falling edge of SCLK | 40 | – | – | ns | |
| t_{HSCLK} | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| F_{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | |
| t_{ERASEB} | Flash erase time (block) | – | 10 | – | ms | |
| t_{WRITE} | Flash block write time | – | 80 | – | ms | |
| t_{DSCLK3} | Data out delay from falling edge of SCLK | – | – | 50 | ns | $3.0 \leq V_{DD} \leq 3.6$. |
| t_{DSCLK2} | Data out delay from falling edge of SCLK | – | – | 70 | ns | $2.4 \leq V_{DD} \leq 3.0$. |
| $t_{ERASEALL}$ | Flash erase time (bulk) | – | 20 | – | ms | Erase all blocks and protection fields at once. |
| $t_{PROGRAM_HOT}$ | Flash block erase + flash block write time | – | – | 180 ^[24] | ms | $0\text{ }^{\circ}\text{C} \leq T_j \leq 100\text{ }^{\circ}\text{C}$. |
| $t_{PROGRAM_COLD}$ | Flash block erase + flash block write time | – | – | 360 ^[24] | ms | $-40\text{ }^{\circ}\text{C} \leq T_j \leq 0\text{ }^{\circ}\text{C}$. |

AC I²C Specifications

Table 34 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 34. AC Characteristics of the I²C SDA and SCL Pins for $V_{CC} \geq 3.0\text{ V}$

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|----------------|--|---------------|-----|---------------------|-----|---------------|
| | | Min | Max | Min | Max | |
| F_{SCL2C} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HDSTA2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs |
| t_{LOW2C} | Low period of the SCL clock | 4.7 | – | 1.3 | – | μs |
| t_{HIGH2C} | High period of the SCL clock | 4.0 | – | 0.6 | – | μs |
| $t_{SUSTA2C}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | μs |
| $t_{HDDAT2C}$ | Data hold time | 0 | – | 0 | – | μs |
| $t_{SUDAT2C}$ | Data setup time | 250 | – | 100 ^[23] | – | ns |
| $t_{SUSTOI2C}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | μs |
| t_{BUFI2C} | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | μs |
| t_{SPI2C} | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

Notes

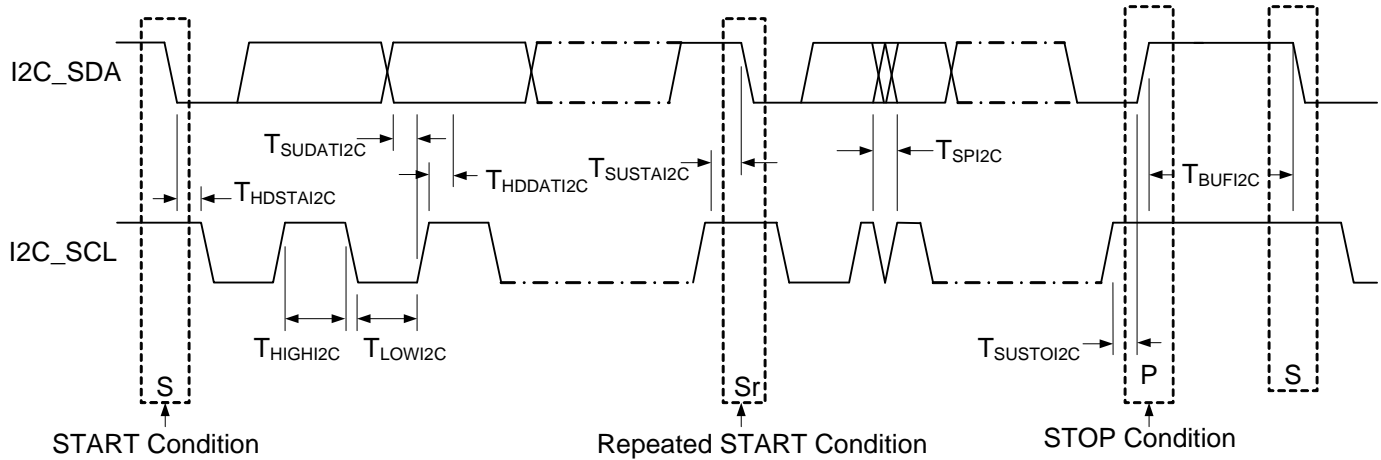
23. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250\text{ ns}$ must then be met. This automatically becomes the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250\text{ ns}$ (according to the standard-mode I²C-bus specification) before the SCL line is released.

24. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, [Design Aids — Reading and Writing PSoC[®] Flash – AN2015](#) for more information on Flash APIs.

Table 35. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode Not Supported)

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|-----------------------|--|---------------|-----|-----------|-----|-------|
| | | Min | Max | Min | Max | |
| F _{SCL I2C} | SCL clock frequency | 0 | 100 | – | – | kHz |
| t _{HDSTAI2C} | Hold time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | – | – | μs |
| t _{LOWI2C} | Low period of the SCL clock | 4.7 | – | – | – | μs |
| t _{HIGHI2C} | High period of the SCL clock | 4.0 | – | – | – | μs |
| t _{SUSTAI2C} | Setup time for a repeated START condition | 4.7 | – | – | – | μs |
| t _{HDDATI2C} | Data hold time | 0 | – | – | – | μs |
| t _{SUDATI2C} | Data setup time | 250 | – | – | – | ns |
| t _{SUSTOI2C} | Setup time for STOP condition | 4.0 | – | – | – | μs |
| t _{BUF I2C} | Bus free time between a STOP and START condition | 4.7 | – | – | – | μs |
| t _{SPI2C} | Pulse width of spikes are suppressed by the input filter. | – | – | – | – | ns |

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



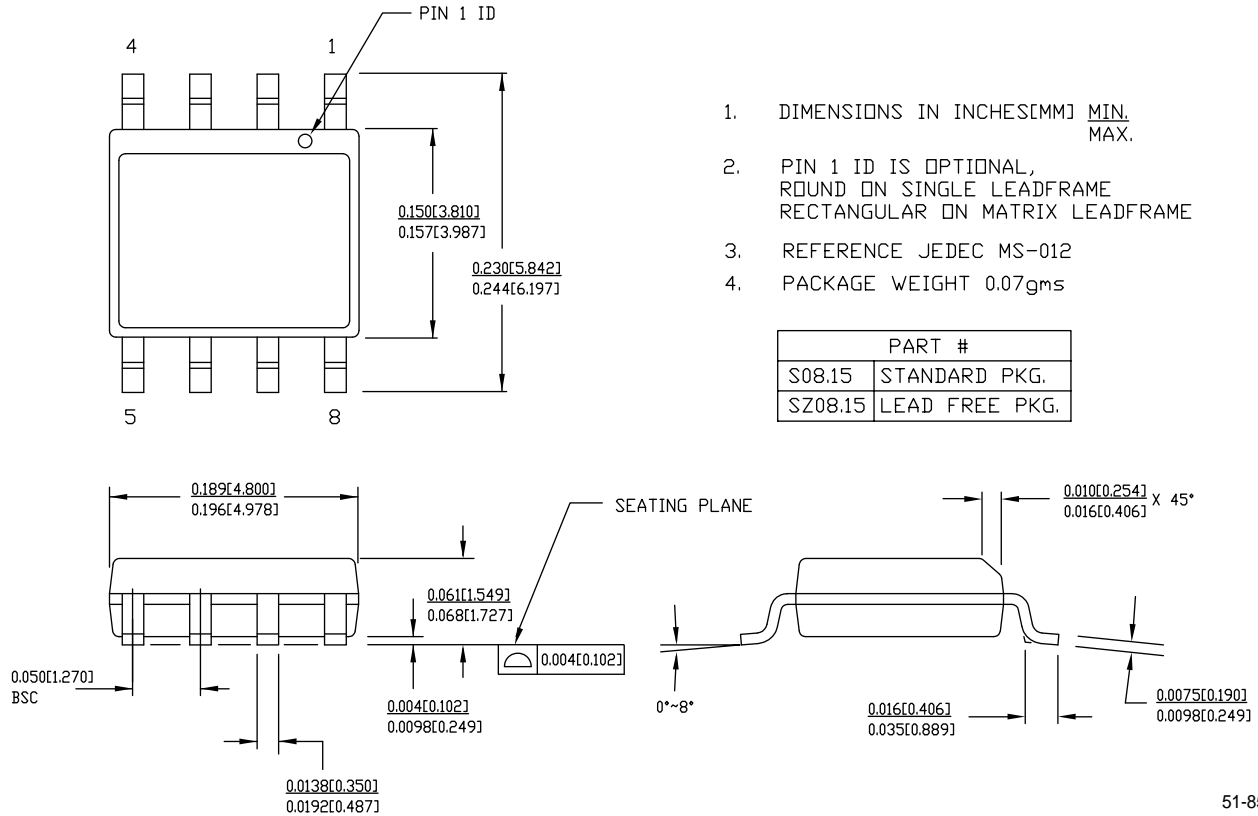
Packaging Information

This section illustrates the packaging specifications for the CY8C21x23 PSoC device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

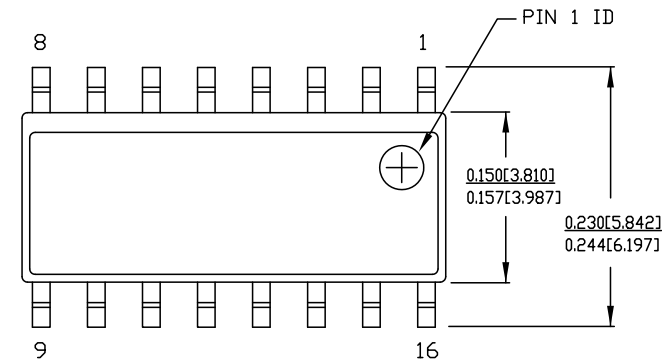
Packaging Dimensions

Figure 15. 8-Pin (150-Mil) SOIC



51-85066 *E

Figure 16. 16-Pin (150-Mil) SOIC



DIMENSIONS IN INCHES[MM] MIN. MAX.
 REFERENCE JEDEC MS-012
 PACKAGE WEIGHT 0.15gms

| PART # | |
|---------|----------------|
| S16.15 | STANDARD PKG. |
| SZ16.15 | LEAD FREE PKG. |

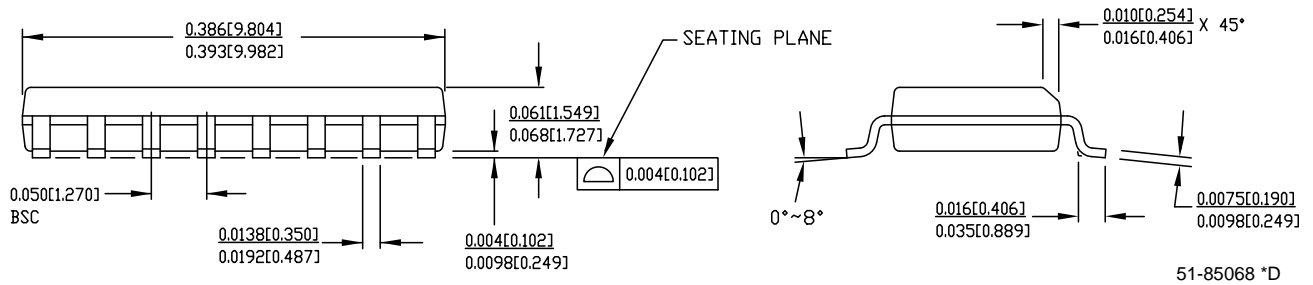
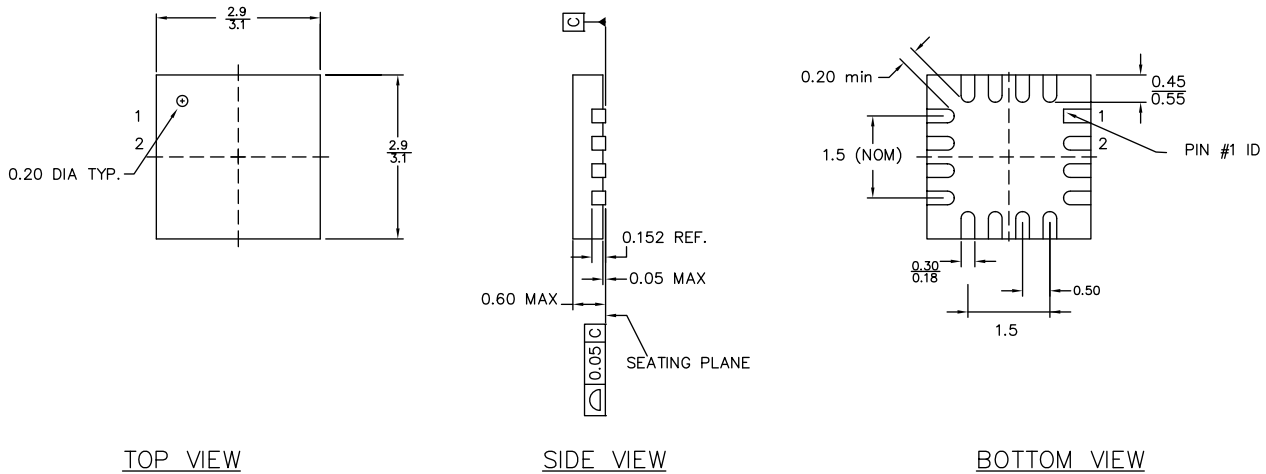


Figure 17. 16-Pin QFN with no E-Pad



TOP VIEW

SIDE VIEW

BOTTOM VIEW

| PART NO. | DESCRIPTION |
|----------|-------------|
| LG16A | LEAD-FREE |
| LD16A | STANDARD |

NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN. MAX.

001-09116 *F

Figure 18. 20-Pin (210-Mil) SSOP

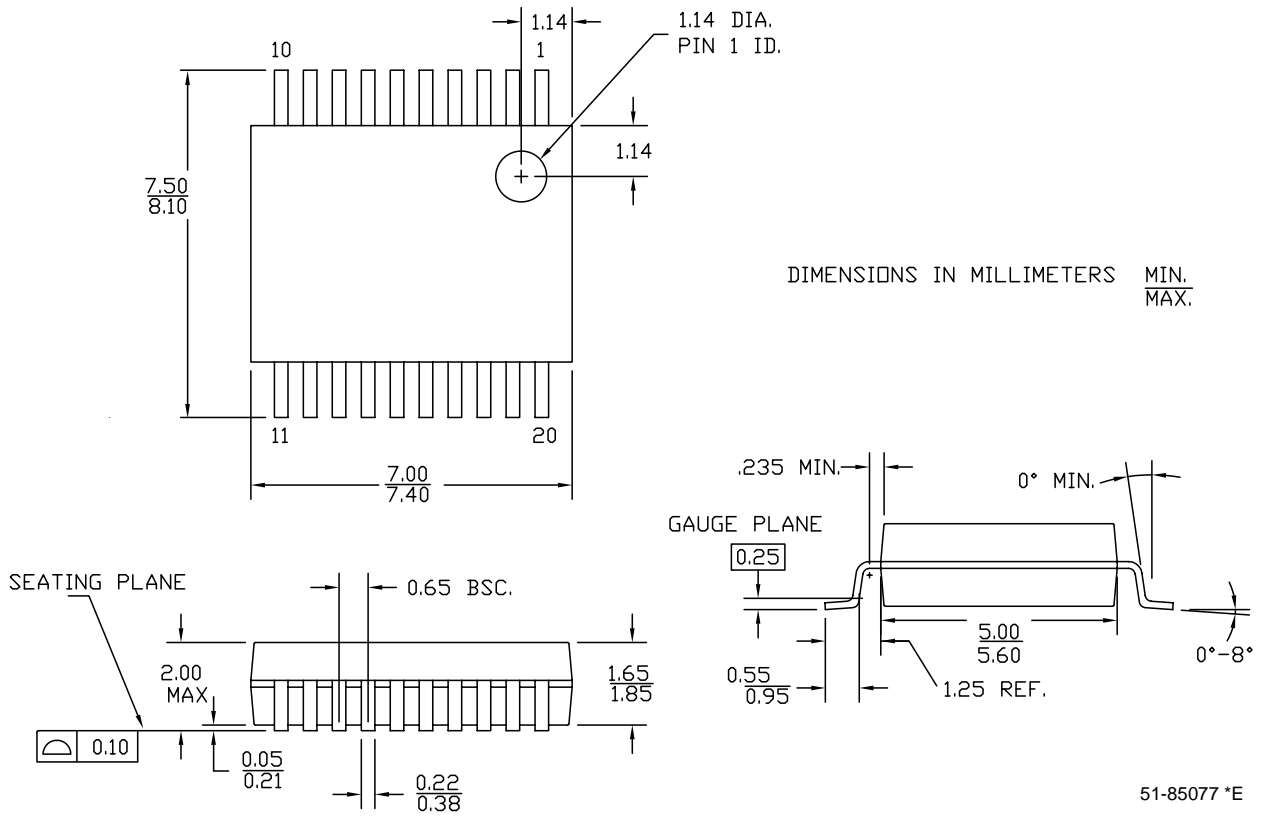
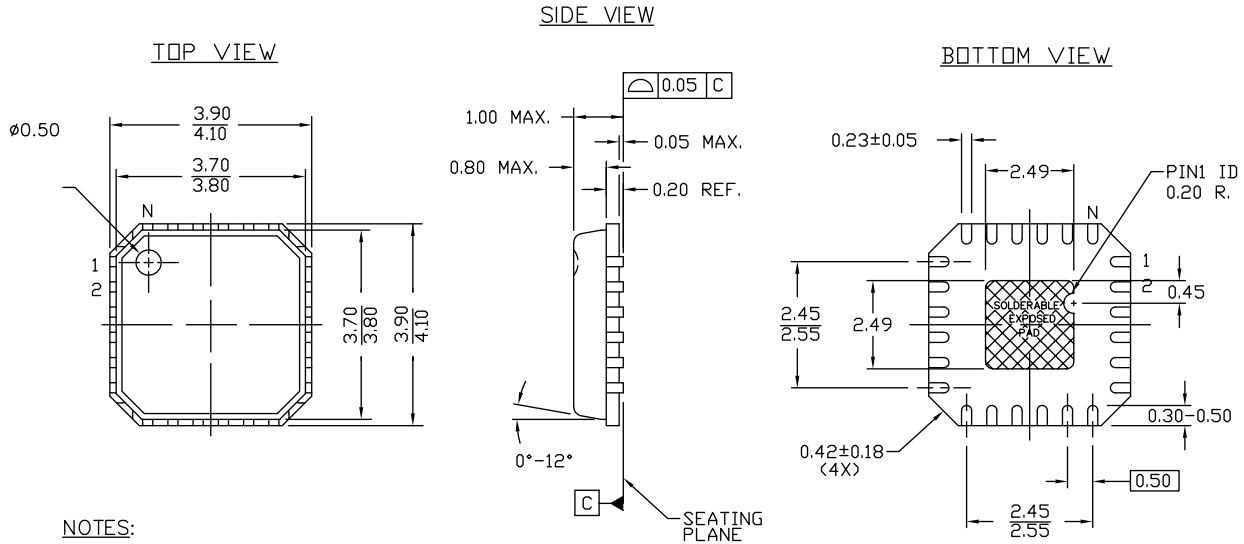



Figure 19. 24-Pin (4 x 4) QFN



NOTES:

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF24A | STANDARD |
| LY24A | LEAD FREE |

51-85203 *C

Important Note For information on the preferred dimensions for mounting QFN packages, refer the application note, Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages available at <http://www.amkor.com>. Note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances
Table 36. Thermal Impedances per Package

| Package | Typical θ_{JA} [25] |
|----------------------------|----------------------------|
| 8-pin SOIC | 186 °C/W |
| 16-pin SOIC | 125 °C/W |
| 16-pin QFN | 46 °C/W |
| 20-pin SSOP | 117 °C/W |
| 24-pin QFN ^[26] | 40 °C/W |

Solder Reflow Specifications

Table 37 shows the solder reflow temperature limits that must not be exceeded.

Table 37. Solder Reflow Specifications

| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5$ °C |
|-------------|------------------------------------|---------------------------------|
| 8-pin SOIC | 260 °C | 30 seconds |
| 16-pin SOIC | 260 °C | 30 seconds |
| 16-pin QFN | 260 °C | 30 seconds |
| 20-pin SSOP | 260 °C | 30 seconds |
| 24-pin QFN | 260 °C | 30 seconds |

Notes

25. $T_J = T_A + \text{POWER} \times \theta_{JA}$

26. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at <http://www.amkor.com>.

27. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5 °C with Sn-Pb or 245+/-5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

The following table lists the CY8C21x23 PSoC device's key package features and ordering codes.

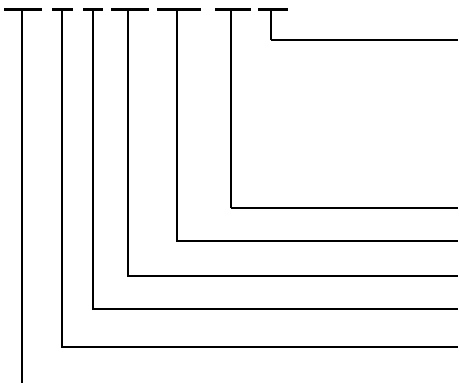
Table 38. CY8C21x23 PSoC Device Key Features and Ordering Information

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital PSoC Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---------------------------------------|-------------------|---------------|-------------|------------------|-------------------|---------------------|---------------|------------------|---------------|----------------|----------|
| 8-Pin (150-Mil) SOIC | CY8C21123-24SXI | 4 K | 256 | No | -40 °C to +85 °C | 4 | 4 | 6 | 4 | 0 | No |
| 8-Pin (150-Mil) SOIC (Tape and Reel) | CY8C21123-24SXIT | 4 K | 256 | No | -40 °C to +85 °C | 4 | 4 | 6 | 4 | 0 | No |
| 16-Pin (150-Mil) SOIC | CY8C21223-24SXI | 4 K | 256 | Yes | -40 °C to +85 °C | 4 | 4 | 12 | 8 | 0 | No |
| 16-Pin (150-Mil) SOIC (Tape and Reel) | CY8C21223-24SXIT | 4 K | 256 | Yes | -40 °C to +85 °C | 4 | 4 | 12 | 8 | 0 | No |
| 16-Pin (3 x 3) QFN with no E-Pad | CY8C21223-24LGXI | 4 K | 256 | No | -40 °C to +85 °C | 4 | 4 | 12 | 8 | 0 | Yes |
| 20-Pin (210-Mil) SSOP | CY8C21323-24PVXI | 4 K | 256 | No | -40 °C to +85 °C | 4 | 4 | 16 | 8 | 0 | Yes |
| 20-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21323-24PVXIT | 4 K | 256 | No | -40 °C to +85 °C | 4 | 4 | 16 | 8 | 0 | Yes |
| 24-Pin (4 x 4) QFN | CY8C21323-24LFXI | 4 K | 256 | Yes | -40 °C to +85 °C | 4 | 4 | 16 | 8 | 0 | Yes |
| 24-Pin (4 x 4) QFN (Tape and Reel) | CY8C21323-24LFXIT | 4 K | 256 | Yes | -40 °C to +85 °C | 4 | 4 | 16 | 8 | 0 | Yes |

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 21 xxx-24xx



Package Type: SX = SOIC Pb-Free
 PVX = SSOP Pb-Free
 LFX/LGX = QFN Pb-Free

Thermal Rating: C = Commercial
 I = Industrial
 E = Extended

Speed: 24 MHz
 Part Number
 Family Code
 Technology Code: C = CMOS
 Marketing Code: 8 = Cypress PSoC
 Company ID: CY = Cypress

Acronyms

Acronyms Used

Table 39 lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

| Acronym | Description | Acronym | Description |
|---------|---|---------|---|
| AC | alternating current | PCB | printed circuit board |
| ADC | analog-to-digital converter | PGA | programmable gain amplifier |
| API | application programming interface | POR | power on reset |
| CMOS | complementary metal oxide semiconductor | PPOR | precision power on reset |
| CPU | central processing unit | PRS | pseudo-random sequence |
| CRC | cyclic redundancy check | PSoC® | Programmable System-on-Chip |
| CT | continuous time | PWM | pulse width modulator |
| DAC | digital-to-analog converter | QFN | quad flat no leads |
| DC | direct current | SC | switched capacitor |
| EEPROM | electrically erasable programmable read-only memory | SLIMO | slow IMO |
| GPIO | general purpose I/O | SMP | switch mode pump |
| ICE | in-circuit emulator | SOIC | small-outline integrated circuit |
| IDE | integrated development environment | SPI™ | serial peripheral interface |
| ILO | internal low speed oscillator | SRAM | static random access memory |
| IMO | internal main oscillator | SROM | supervisory read only memory |
| I/O | input/output | SSOP | shrink small-outline package |
| IrDA | infrared data association | UART | universal asynchronous receiver / transmitter |
| ISSP | in-system serial programming | USB | universal serial bus |
| LVD | low voltage detect | WDT | watchdog timer |
| MCU | microcontroller unit | XRES | external reset |
| MIPS | million instructions per second | | |

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 (001-17397)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at <http://www.amkor.com>.

Document Conventions

Units of Measure

Table 40 lists the units of measures.

Table 40. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-------------------------|
| dB | decibels | mH | millihenry |
| °C | degree Celsius | μH | microhenry |
| μF | microfarad | μs | microsecond |
| pF | picofarad | ms | millisecond |
| kHz | kilohertz | ns | nanosecond |
| MHz | megahertz | ps | picosecond |
| rt-Hz | root hertz | μV | microvolt |
| kΩ | kilohm | mV | millivolt |
| Ω | ohm | mVpp | millivolts peak-to-peak |
| μA | microampere | V | volt |
| mA | milliampere | W | watt |
| nA | nanoampere | mm | millimeter |
| pA | pikoampere | % | percent |

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

| | |
|---|---|
| active high | <ol style="list-style-type: none"> 1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | <ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |

Glossary (continued)

| | |
|-------------------------------|--|
| bias | <ol style="list-style-type: none"> 1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | <ol style="list-style-type: none"> 1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | <ol style="list-style-type: none"> 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none"> 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |

Glossary (continued)

| | |
|---------------------------------|--|
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| External Reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| Flash | An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none"> 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V _{DD} and provides an interrupt to the system when V _{DD} falls lower than a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |

Glossary (continued)

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| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the slave device . |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | <ol style="list-style-type: none">1. A disturbance that affects a signal and that may distort the information carried by the signal.2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| Phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| Power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset. |
| PSoC [®] | Cypress Semiconductor's PSoC [®] is a registered trademark and Programmable System-on-Chip [™] is a trademark of Cypress. |
| PSoC Designer [™] | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |

Glossary (continued)

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| serial | <ol style="list-style-type: none"> 1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | <ol style="list-style-type: none"> 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V_{DD} | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V. |
| V_{SS} | A name for a power net meaning "voltage source." The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Document History Page

| Document Title: CY8C21123, CY8C21223, CY8C21323 PSoC [®] Programmable System-on-Chip™ | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number:38-12022 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 133248 | NWJ | See ECN | New silicon and document (Revision **). |
| *A | 208900 | NWJ | See ECN | Add new part, new package and update all ordering codes to Pb-free. |
| *B | 212081 | NWJ | See ECN | Expand and prepare Preliminary version. |
| *C | 227321 | CMS Team | See ECN | Update specs., data, format. |
| *D | 235973 | SFV | See ECN | Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table. |
| *E | 290991 | HMT | See ECN | Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs. |
| *F | 301636 | HMT | See ECN | DC Chip-Level Specification changes. Update links to new CY.com Portal. |
| *G | 324073 | HMT | See ECN | Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final. |
| *H | 2588457 | KET/HMI/AESA | 10/22/2008 | New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram. |
| *I | 2618175 | OGNE/PYRS | 12/09/08 | Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated 'Development Tools' and 'Designing with PSoC Designer' sections on pages 5 and 6 |
| *J | 2682782 | MAXK/AESA | 04/03/2009 | Corrected 16 COL pinout. |
| *K | 2699713 | MAXK | 04/29/09 | Minor ECN to correct paragraph style of 16 COL Pinout. No change in content. |
| *L | 2762497 | JVY | 09/11/2009 | Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F _{IMO6} and T _{WRITE} specifications. Replaced T _{RAMP} time specification with SR _{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I _{OH} , I _{OL} , DC _{ILO} , F _{32K_U} , T _{POWERUP} , T _{ERASEALL} , T _{PROGRAM_HOT} , and T _{PROGRAM_COLD} specifications.. |
| *M | 2792630 | TTO | 10/26/2009 | Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin. |
| *N | 2901653 | NJF | 03/30/2010 | Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents . Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added T _{BAKETEMP} and T _{BAKETIME} parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions |
| *O | 2928895 | YJI | 05/06/2010 | No technical updates. Included with EROS spec. |
| *P | 3044869 | NJF | 10/01/2010 | Added PSoC Device Characteristics table . Added DC I ² C Specifications table. Added F _{32K_U} max limit. Added T _{jit_IMO} specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I ² C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update. |
| *Q | 3263669 | YJI | 05/23/2011 | Updated 16-pin SOIC and 20-pin SSOP package diagrams. Updated Development Tool Selection and Designing with PSoC Designer sections. |

| Document Title: CY8C21123, CY8C21223, CY8C21323 PSoc® Programmable System-on-Chip™ Document Number:38-12022 | | | | |
|--|---------|-----------|------------|---|
| *R | 3383787 | GIR | 09/26/2011 | The text "Pin must be left floating" is included under Description of NC pin in Table 6 on page 11 . Updated Table 37 on page 35 for improved clarity. |
| *S | 3558729 | RJVB | 03/22/2012 | Updated 16-pin SOIC package. |
| *T | 3598261 | LURE/XZNG | 04/24/2012 | Changed the PWM description string from "8- to 32-bit" to "8- and 16-bit". |
| *U | 3649990 | BVI/YLIU | 06/19/2012 | Updated description of NC pin as "No Connection. Pin must be left floating" |

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