CY7C4255V, CY7C4265V
CY7C4275V, CY7C4285V

8 K/16 K/32 K/64 K × 18 Low Voltage Deep Sync FIFOs

Features

- 3.3 V operation for low power consumption and easy integration into low voltage systems
- High speed, low power, first-in first-out (FIFO) memories
- 8 K × 18 (CY7C4255V)
- 16 K × 18 (CY7C4265V)
- 32 K × 18 (CY7C4275V)
- 64 K × 18 (CY7C4285V)
- 0.35 micron CMOS for optimum speed and power
- High speed 100 MHz operation (10 ns read/write cycle times)
- Low power
  - I_{CC} = 30 mA
  - I_{SB} = 4 mA
- Fully asynchronous and simultaneous read and write operation
- Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags
- Retransmit function
- Output Enable ($\overline{OE}$) pin
- Independent read and write enable pins
- Supports free running 50% duty cycle clock inputs
- Width Expansion Capability
- Depth Expansion Capability
- 64-pin 10×10 STQFP
- Pin compatible density upgrade to CY7C42X5V-ASC families
- Pin compatible 3.3 V solutions for CY7C4255/65/75/85V

Functional Description

The CY7C4255/65/75/85V are high speed, low power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin and functionally compatible to the CY7C42X5V Synchronous FIFO family. The CY7C4255/65/75/85V can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin (WEN).

When WEN is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While WEN is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin (REN). In addition, the CY7C4255/65/75/85V have an output enable pin (OE). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read or write applications. Clock frequencies up to 67 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

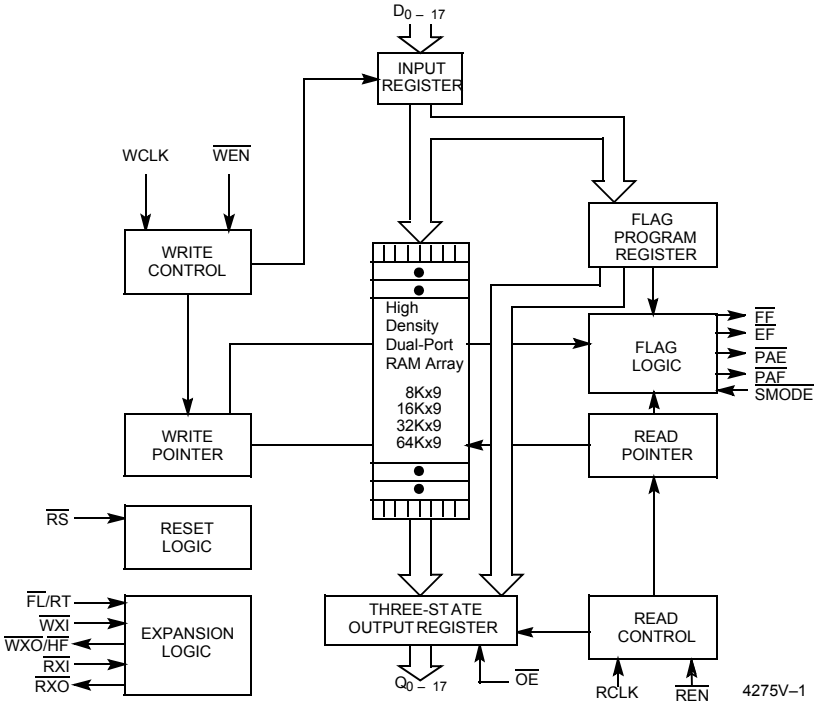
Depth expansion is possible using the cascade input (WXI, RXI), cascade output (WXO, RXO), and First Load (FL) pins. The WXO and RXO pins are connected to the WXI and RXI pins of the next device, and the WXO and RXO pins of the last device must be connected to the WXI and RXI pins of the first device. The FL pin of the first device is tied to VSS and the FL pin of all the remaining devices must be tied to VCC .

Selection Guide

Parameter		7C4255/65/75/85V-10	7C4255/65/75/85V-15
Maximum Frequency (MHz)		100	66.7
Maximum Access Time (ns)		8	10
Minimum Cycle Time (ns)		10	15
Minimum Data or Enable Setup (ns)		3.5	4
Minimum Data or Enable Hold (ns)		0	0
Maximum Flag Delay (ns)		8	10
Active Power Supply Current (I_{CC1}) (mA)	Commercial	30	30
	Industrial		35

Parameter	CY7C4255V	CY7C4265V	CY7C4275V	CY7C4285V
Density	8 K × 18	16 K × 18	32 K × 18	64 K × 18
Package	64-pin 10×10 TQFP	64-pin 10×10 TQFP	64-pin 10×10 TQFP	64-pin 10×10 TQFP

Logic Block Diagram



Contents

Pinouts

Figure 1. Pin Diagram - 64-pin STQFP

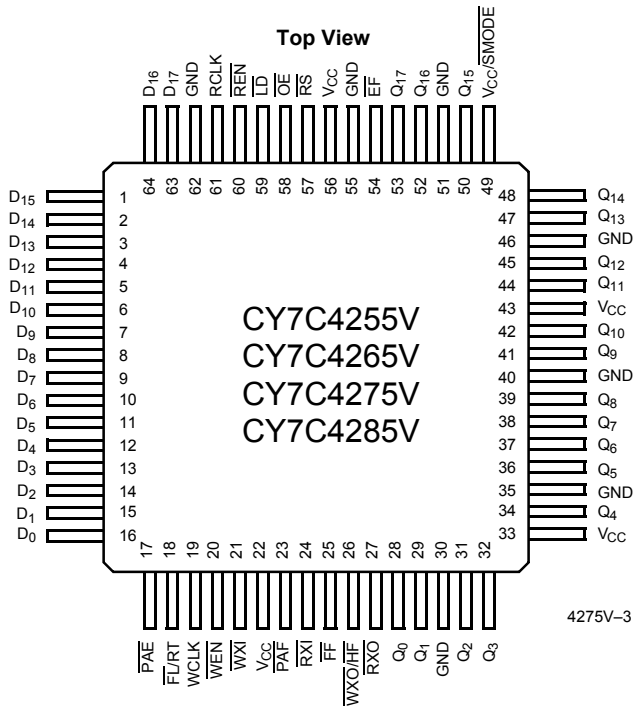


Table 1. Pin Definitions - CY7C4255/65/75/85V 64-pin STQFP

Signal Name	Description	IO	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus.
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus.
$\overline{WEN}$	Write Enable	I	Enables the WCLK input.
$\overline{REN}$	Read Enable	I	Enables the RCLK input.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual Mode Pin: Single device or width expansion – Half Full status flag Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}. It is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}. It is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (Q_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}$/RT	First Load/ Retransmit	I	Dual Mode Pin: Cascaded – The first device in the daisy chain has $\overline{FL}$ tied to V_{SS}; all other devices have $\overline{FL}$ tied to V_{CC}. In standard mode or width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS} . Retransmit function is also available in standalone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device Not Cascaded – Tied to V_{SS}
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device Not Cascaded – Tied to V_{SS}
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power up.
$\overline{OE}$	Output Enable	I	When OE is LOW, the FIFO's data outputs drive the bus to which they are connected. If OE is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual Mode Pin: Asynchronous Almost Empty/Almost Full flags – tied to V_{CC} Synchronous Almost Empty/Almost Full flags – tied to V_{SS} (Almost Empty synchronized to RCLK, Almost Full synchronized to WCLK.)

Functional Description

The CY7C4255/65/75/85V provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see Table 3 on page 7). The Half Full flag shares the WXO pin. This flag is valid in the standalone and width expansion configurations. In the depth expansion, this pin provides the expansion out (WXO) information that is used to signal the next FIFO when it is to be activated.

The Empty and Full flags are synchronous, that is, they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags remain valid from one clock cycle to the next. The Almost Empty/Almost Full flags become synchronous if the V_{CC}/SMODE is tied to V_{SS}. All configurations are fabricated using an advanced 0.35 µ CMOS technology. Input ESD protection is greater than 2001 V, and latch-up is prevented by the use of guard rings.

Architecture

The CY7C4255/65/75/85V consists of an array of 8K/16K/32K/64K words of 18 bits each (implemented by a dual port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN, WEN, RS), and flags (EF, PAE, HF, PAF, FF). The CY7C4255/65/75/85V also includes the control signals WXI, RXI, WXO, RXO for depth expansion.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. For the FIFO to reset to its default state, the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory is presented on the Q_{0-17} outputs. New data is presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is deasserted. When $\overline{OE}$ is enabled (LOW), data in the output register is available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function only outputs data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and under flow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C4255/65/75/85V devices contain two 16-bit offset registers. Data present on D_{0-15} during a program write determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see Table 3 on page 7). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D_{0-15} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see Table 2). All offset registers do not have to be written at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW. Then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Table 2. Write Offset Register

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C4255/65/75/85V devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if V_{CC}/SMODE is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) goes LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) goes LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, that is, it is exclusively updated by each rising edge of RCLK.

Note
1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C4255/65/75/85V features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in section Programming on page 6) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ is asserted, signifying that the FIFO is either Almost Full or Almost Empty. See Table 3 for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Table 3. Flag Truth Table

Number of Words in FIFO				$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
7C4255V – 8 K × 18	7C4265V – 16 K × 18	7C4275V – 32 K × 18	7C4285V – 64 K × 18					
0	0	0	0	H	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	1 to n[2]	H	H	H	L	H
(n+1) to 4096	(n+1) to 8192	(n+1) to 16384	(n+1) to 32768	H	H	H	H	H
4097 to (8192–(m+1))	8193 to (16384 –(m+1))	16385 to (32768–(m+1))	32769 to (65536 –(m+1))	H	H	L	H	H
(8192–m)[3] to 8192	(16384–m)[3] to 16384	(32768–m)[3] to 32767	(65536–m)[3] to 65535	H	L	L	H	H
8192	16384	32768	65536	L	L	L	H	H

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

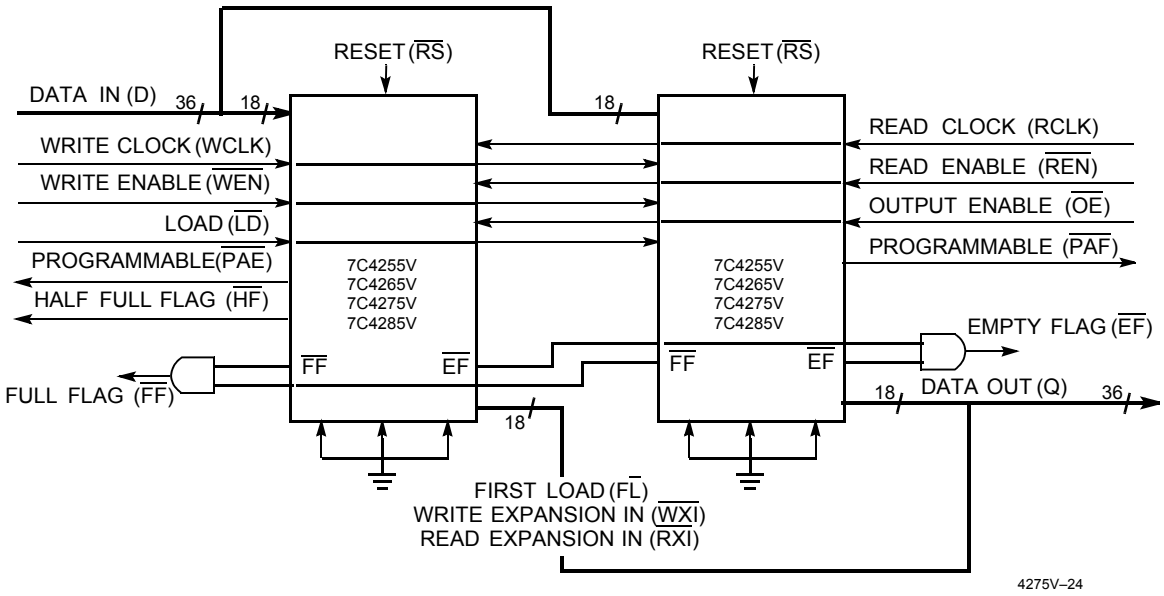
The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also. The full depth of the FIFO can be repeatedly retransmitted.

Width Expansion Configuration

The CY7C4255/65/75/85V can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode, all control line inputs are common and all flags are available. Empty (Full) flags must be created by ANDing the Empty (Full) flags of every FIFO. The $\overline{PAE}$ and $\overline{PAF}$ flags can be detected from any one device. This technique avoids reading data from, or writing data to the FIFO that is “staggered” by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 2 on page 8 demonstrates a 36-word width by using two CY7C4255/65/75/85Vs.

Notes
2. n = Empty Offset (Default Values: CY7C4255/65/75/85V n = 127).
3. m = Full Offset (Default Values: CY7C4255/65/75/85V n = 127).

Figure 2. Block Diagram of 8 K/16 K/32 K/64 K × 18 Low Voltage Synchronous FIFO Memory in Width Expansion Configuration

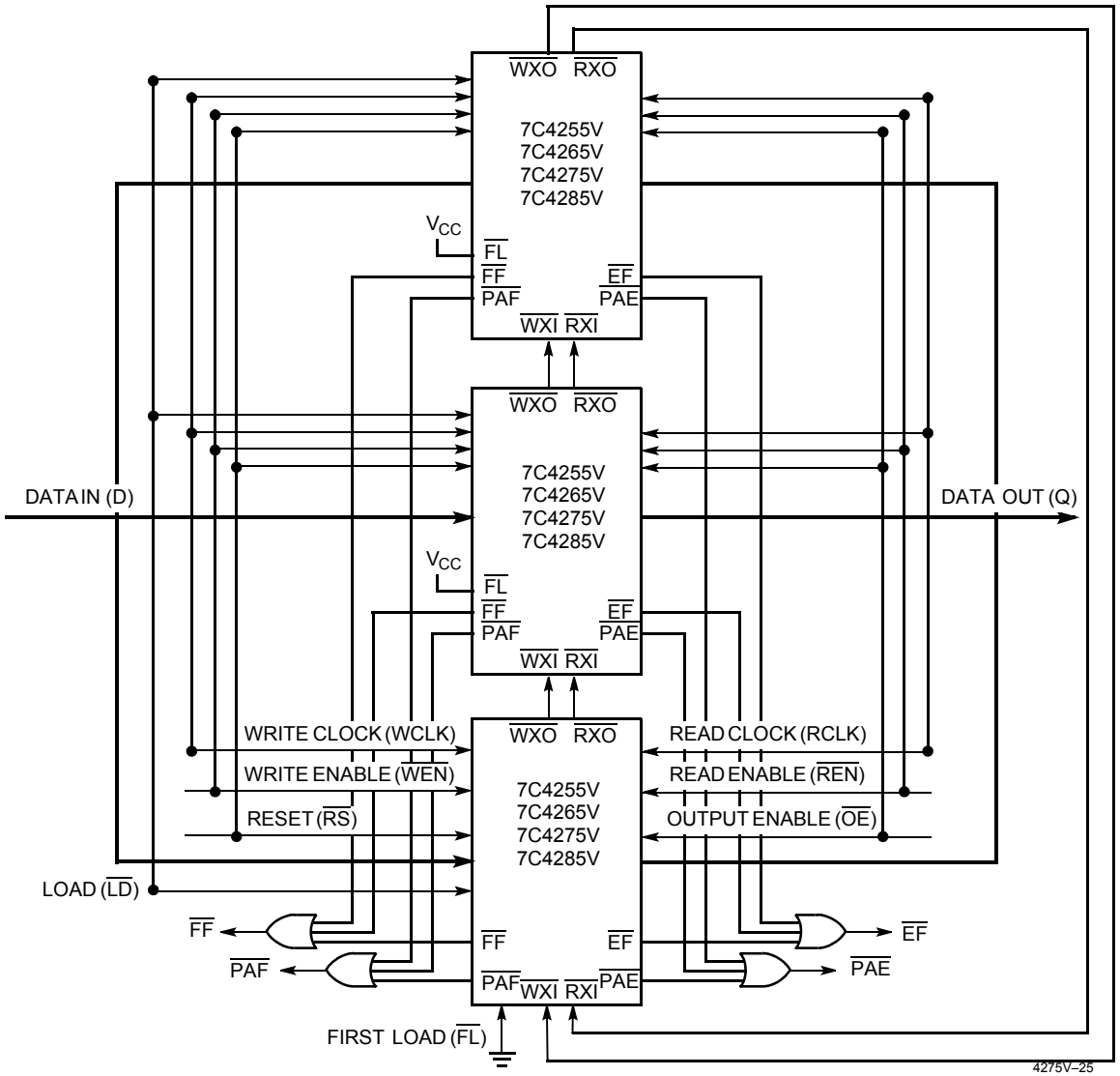


Depth Expansion Configuration (with Programmable Flags)

The CY7C4255/65/75/85V can easily be adapted to applications requiring more than 8 K/16 K/32 K/64 K words of buffering. Figure 3 on page 9 shows Depth Expansion using three CY7C4255/65/75/85Vs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

Figure 3. Block Diagram of 8 K/16 K/32 K/64 K × 18 Low Voltage Synchronous FIFO Memory with Programmable Flags in Depth Expansion Configuration



Maximum Ratings

Exceeding maximum ratings[4] may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential..... –0.5 V to V_{CC} + 0.5 V

DC Voltage Applied to Outputs in High Z State ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001 V (per MIL–STD–883, Method 3015)

Latch-Up Current..... > 200 mA

Operating Range

Range	AmbientTemperature	V_{CC}[5]
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial[6]	–40 °C to +85 °C	3.3 V ± 300 mV

Electrical Characteristics

Over the Operating Range [7]

Parameter	Description	Test Conditions		7C4255/85V-10		7C4255/65/75/85V-15		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –1.0 mA V_{CC} = 3.0 V. I_{OH} = –2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4.0 mA V_{CC} = 3.0 V, I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}[8]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[8]	Input LOW Voltage			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max		–10	+10	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	µA
I_{CC1}[9]	Active Power Supply Current		Commercial		30		30	mA
			Industrial				35	mA
I_{SB}[10]	Average Standby Current		Commercial		4		4	mA
			Industrial				4	mA

Capacitance

Parameter[11]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes

4. The Voltage on any input or IO pin cannot exceed the power pin during power up.
5. V_{CC} range for commercial –10 ns is 3.3 V ± 150 mV.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.
8. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
9. Input signals switch from 0 V to 3 V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.
10. All inputs = V_{CC} – 0.2 V, except RCLK and WCLK (which are at frequency = 0 MHz), and $\overline{FL}$/RT which is at V_{SS}. All outputs are unloaded.
11. Tested initially and after any design changes that may affect these parameters.

Figure 4. AC Test Loads and Waveforms (–15) [12, 13]

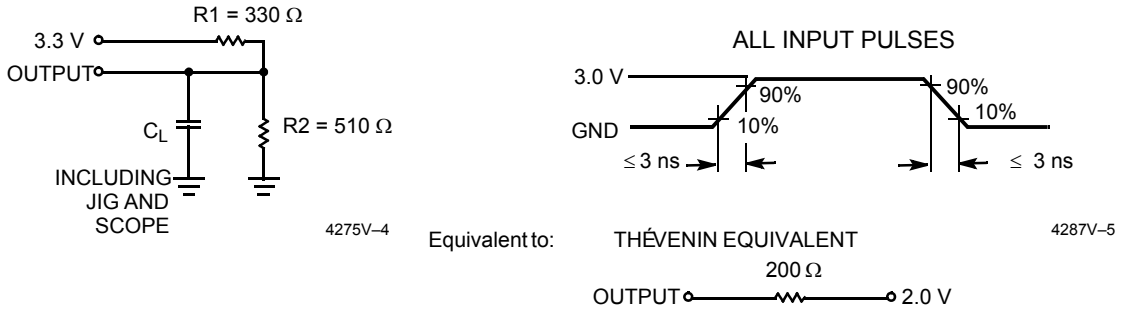
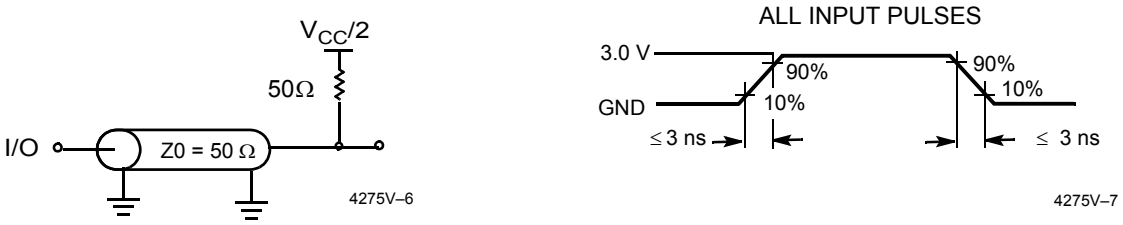


Figure 5. AC Test Loads and Waveforms (–10)



Notes
12. C_L = 30 pF for all AC parameters except for t_{OHZ}.
13. C_L = 5 pF for t_{OHZ}.

Switching Characteristics

Over the Operating Range

Parameter	Description	7C4255/85V-10		7C4255/65/75/85V-15		Unit
		Min	Max	Min	Max	
t_S	Clock Cycle Frequency		100		66.7	MHz
t_A	Data Access Time	2	8	2	10	ns
t_{CLK}	Clock Cycle Time	10		15		ns
t_{CLKH}	Clock HIGH Time	4.5		6		ns
t_{CLKL}	Clock LOW Time	4.5		6		ns
t_{DS}	Data Setup Time	3.5		4		ns
t_{DH}	Data Hold Time	0		0		ns
t_{ENS}	Enable Setup Time	3.5		4		ns
t_{ENH}	Enable Hold Time	0		0		ns
t_{RS}	Reset Pulse Width[14]	10		15		ns
t_{RSR}	Reset Recovery Time	8		10		ns
t_{RSF}	Reset to Flag and Output Time		10		15	ns
t_{PRT}	Retransmit Pulse Width	60		60		ns
t_{RTR}	Retransmit Recovery Time	90		90		ns
t_{OLZ}	Output Enable to Output in Low Z [15]	0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	10	ns
t_{OHZ}	Output Enable to Output in High Z[15]	3	7	3	8	ns
t_{WFF}	Write Clock to Full Flag		8		10	ns
t_{REF}	Read Clock to Empty Flag		8		10	ns
$t_{PAFasynch}$	Clock to Programmable Almost Full Flag[16] (Asynchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		15		16	ns
$t_{PAFsynch}$	Clock to Programmable Almost Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10	ns
$t_{PAEasynch}$	Clock to Programmable Almost Empty Flag[16] (Asynchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		15		16	ns
$t_{PAEsynch}$	Clock to Programmable Almost Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10	ns
t_{HF}	Clock to Half Full Flag		12		16	ns
t_{XO}	Clock to Expansion Out		6		10	ns
t_{XI}	Expansion in Pulse Width	4.5		6.5		ns
t_{XIS}	Expansion in Setup Time	4		5		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5		6		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags (Synchronous Mode only)	10		15		ns

Notes
14. Pulse widths less than minimum values are not allowed.
15. Values guaranteed by design, not currently tested.
16. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write are valid until 5 ns + $t_{PAF(E)}$.

Switching Waveforms

Figure 6. Write Cycle Timing

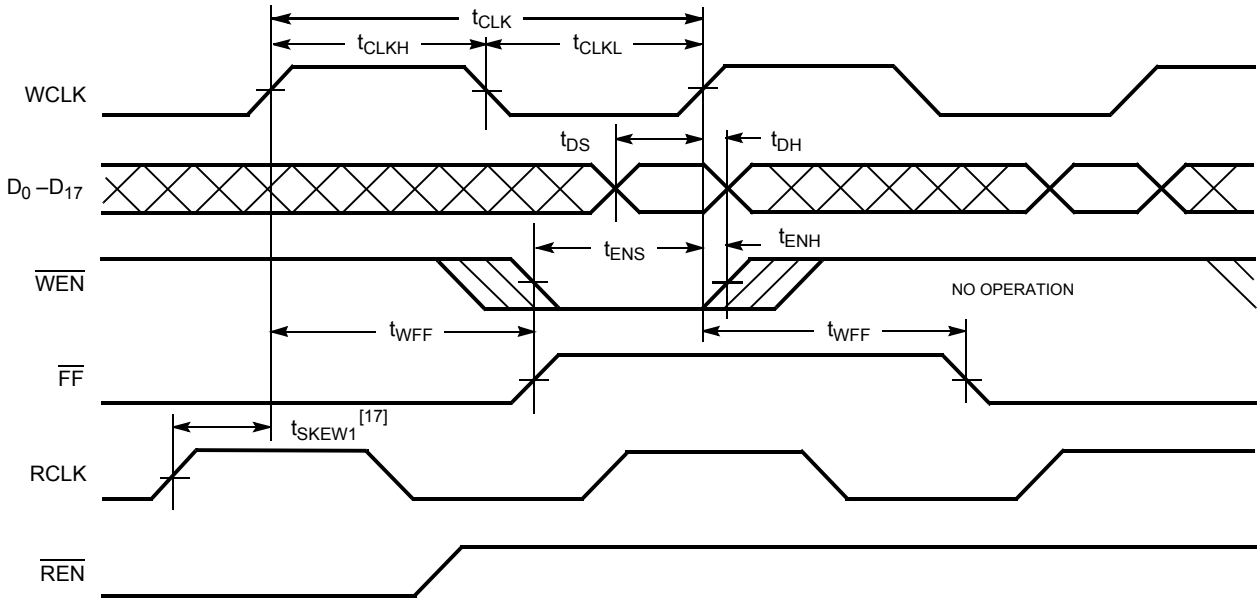
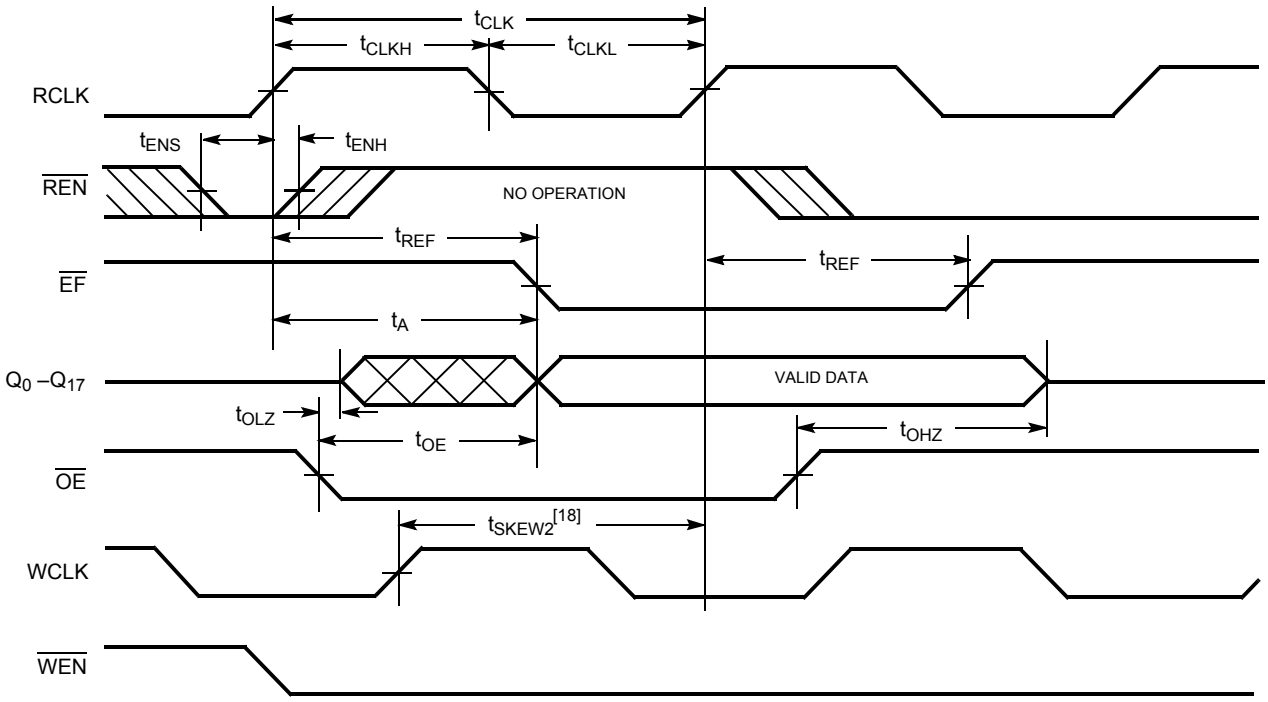


Figure 7. Read Cycle Timing



Notes

17. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK rising edge.
18. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that EF goes HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then EF may not change state until the next RCLK rising edge.

Switching Waveforms *(continued)*

Figure 8. Reset Timing [19]

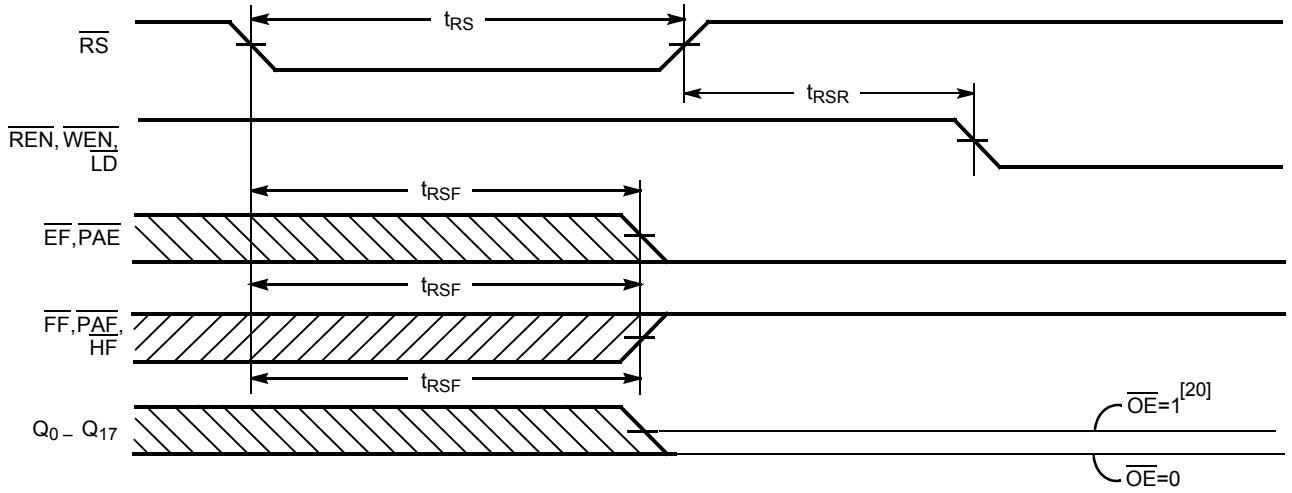
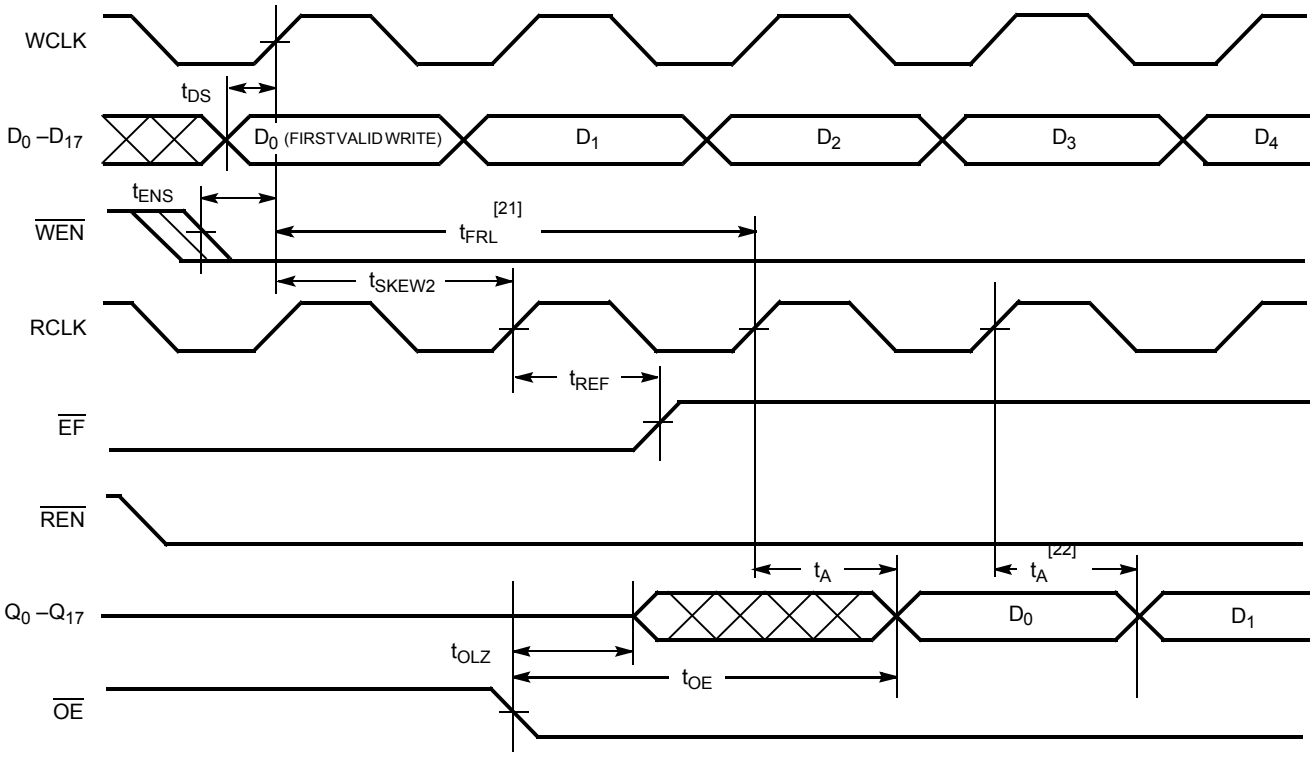


Figure 9. First Data Word Latency after Reset with Simultaneous Read and Write



Notes

19. The clocks (RCLK, WCLK) can be free-running during reset.
20. After reset, the outputs are LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
21. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 × $t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
22. The first word is always available the cycle after $\overline{EF}$ goes HIGH.

Switching Waveforms *(continued)*

Figure 10. Empty Flag Timing

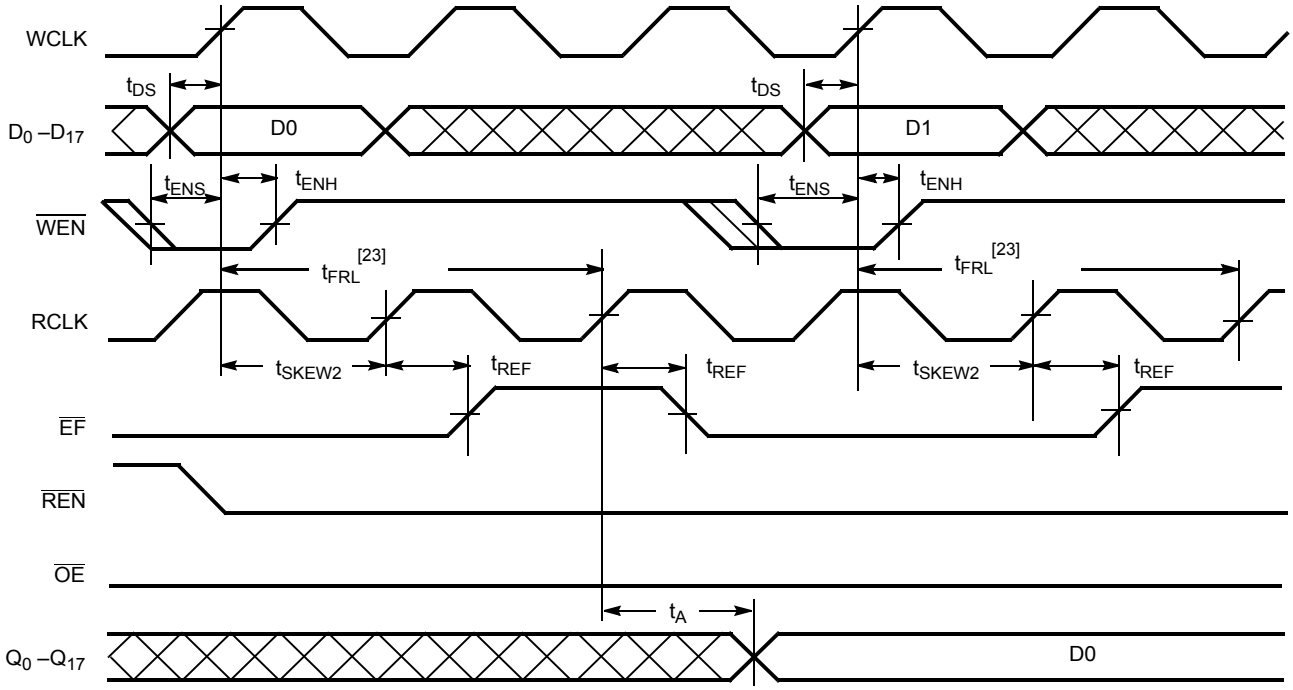
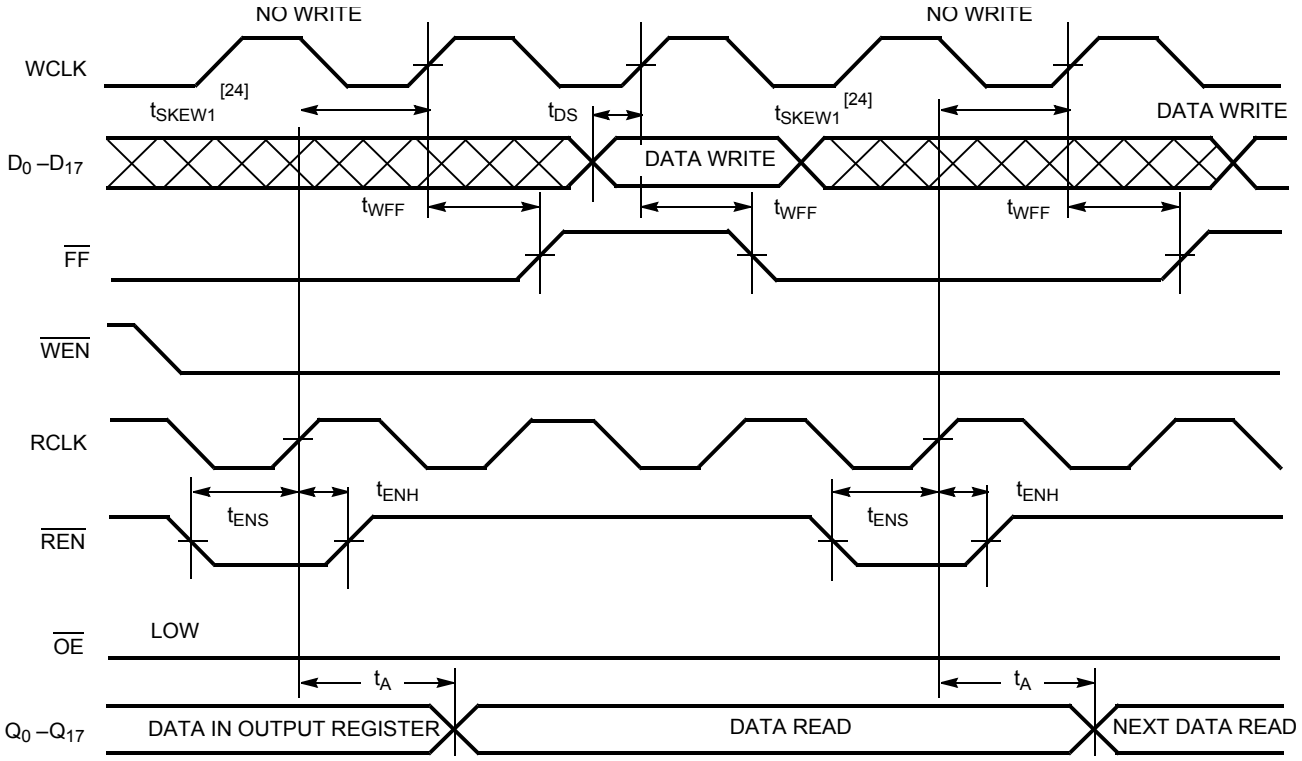


Figure 11. Full Flag Timing



Notes

23. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 × t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
24. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK rising edge.

Switching Waveforms *(continued)*

Figure 12. Half Full Timing

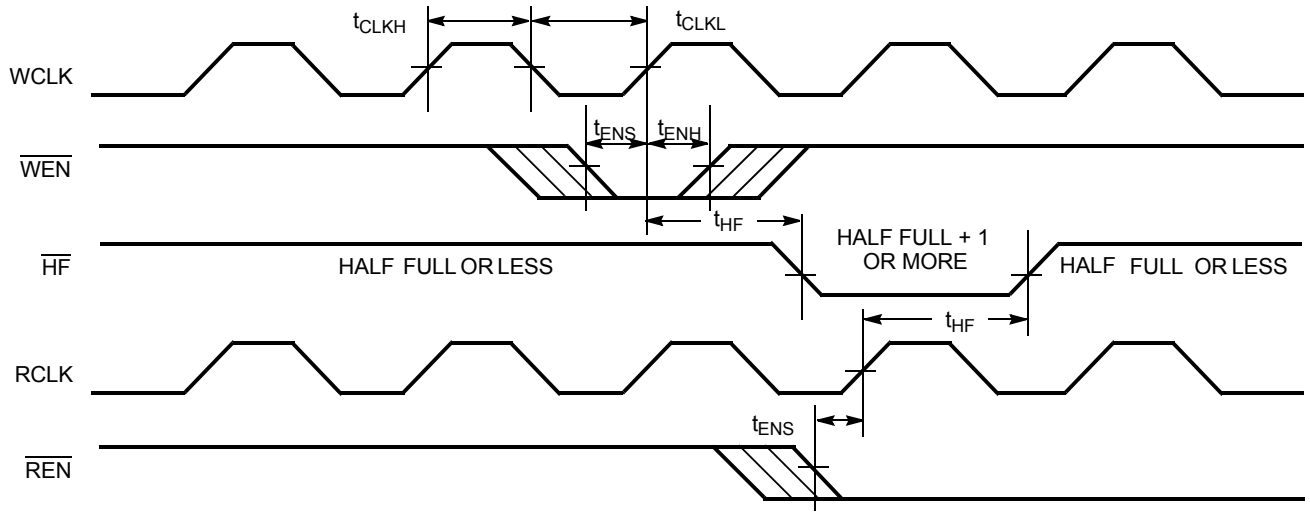
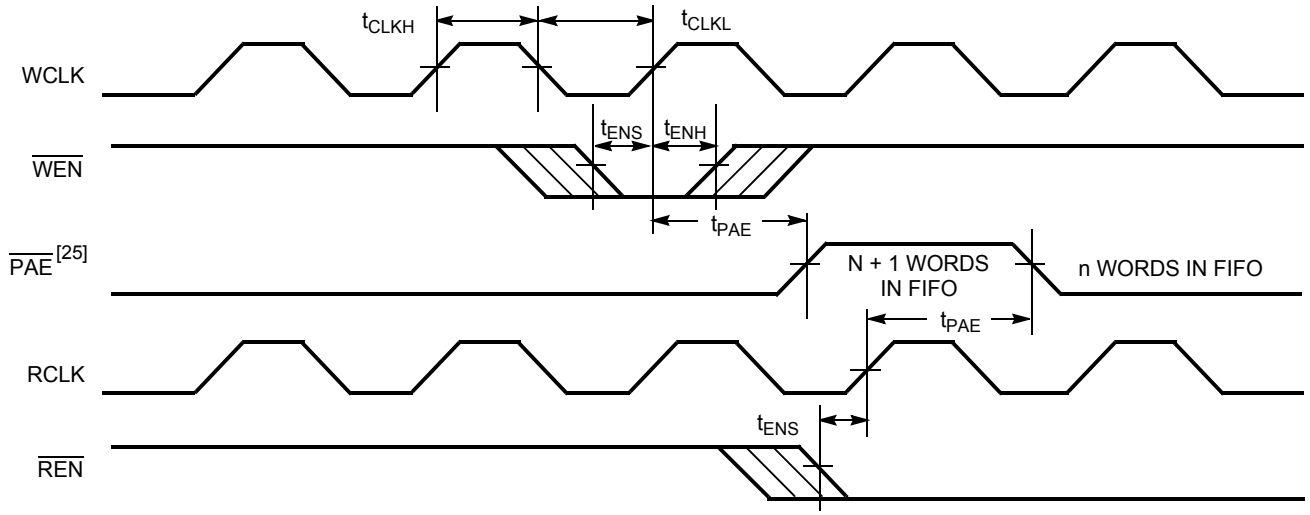


Figure 13. Programmable Almost Empty Flag Timing



Note
25. $\overline{PAE}$ is offset = n. Number of data words into FIFO already = n.

Switching Waveforms *(continued)*

Figure 14. Programmable Almost Empty Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))

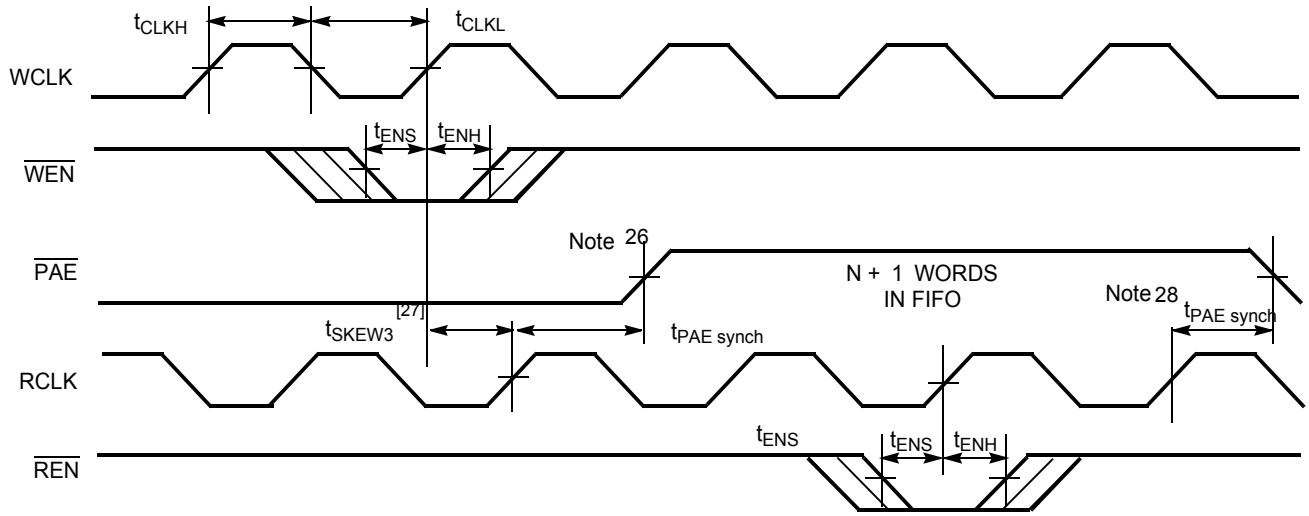
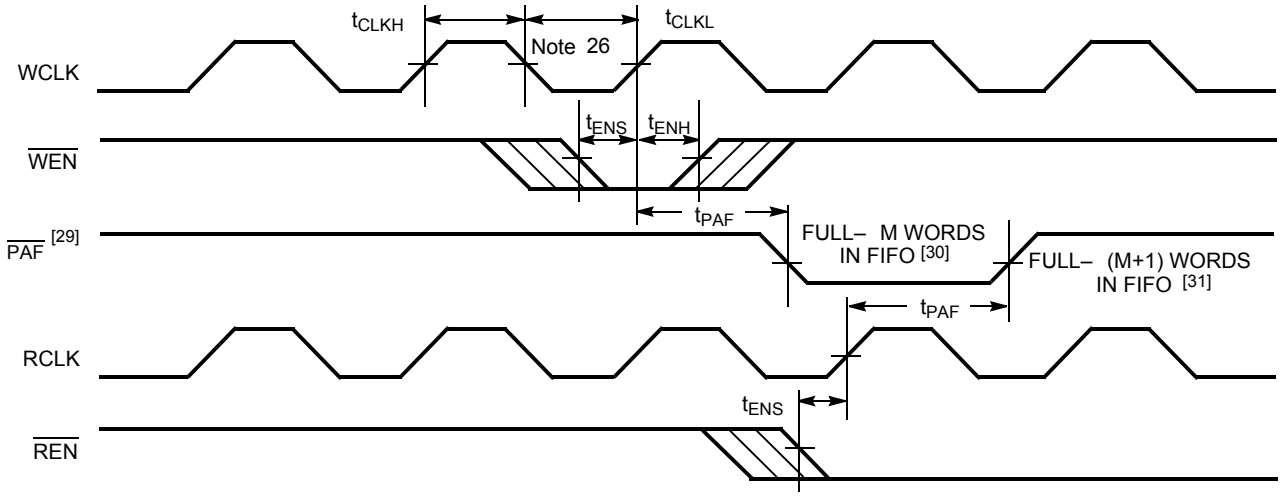


Figure 15. Programmable Almost Full Flag Timing



Notes

26. PAF offset = m. Number of data words written into FIFO already = 8192 – (m + 1) for the CY7C4255V, 16384 – (m + 1) for the CY7C4265V, 32768 – (m + 1) for the CY7C4275V, and 65536 – (m + 1) for the CY7C4285V.
27. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than tSKEW3, then $\overline{PAE}$ may not change state until the next RCLK.
28. If a read is performed on this rising edge of the read clock, there are Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
29. PAF is offset = m.
30. 8192 – m words in CY7C4255V, 16384 – m words in CY7C4265V, 32768 – m words in CY7C4275V, and 65536 – m words in CY7C4285V.
31. 8192 – (m + 1) words in CY7C4255V, 16384 – (m + 1) words in CY7C4265V, 32768 – (m + 1) words in CY7C4275V, and 65536 – (m + 1) words in CY7C4285V.

Switching Waveforms *(continued)*

Figure 16. Programmable Almost Full Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))

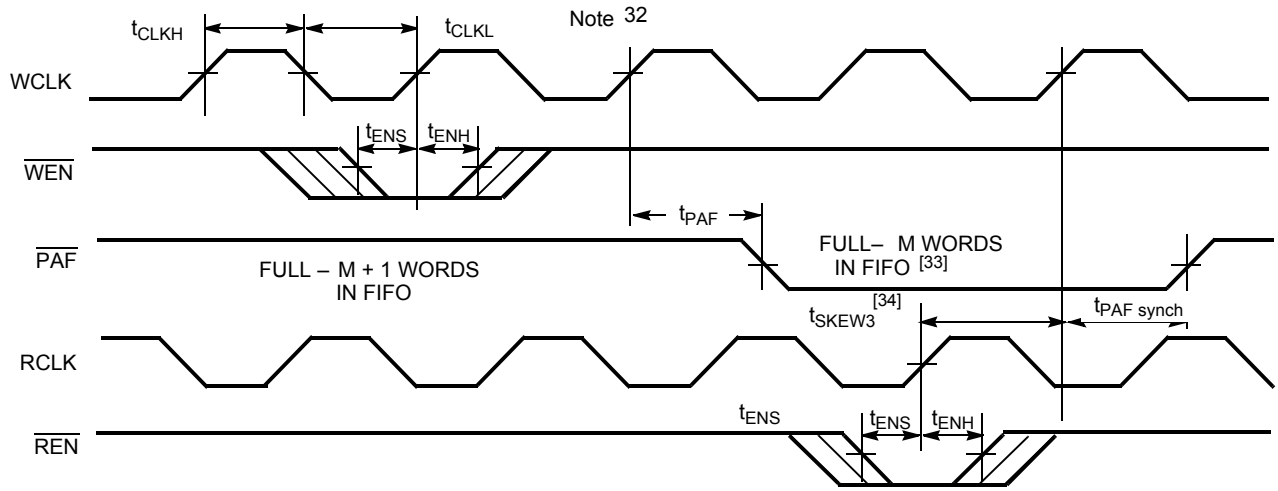
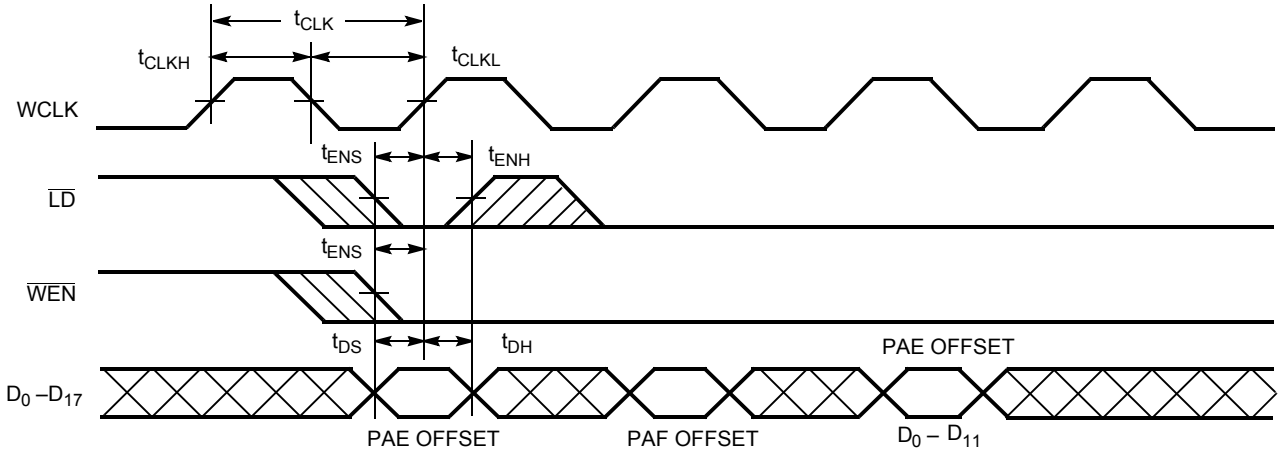


Figure 17. Write Programmable Registers



Notes

32. If a write is performed on this rising edge of the write clock, there are Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
33. 8192 – m words in CY7C4255V, 16384 – m words in CY7C4265V, 32768 – m words in CY7C4275V, and 65536 – m words in CY7C4285V.
34. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{PAF}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.

Switching Waveforms *(continued)*

Figure 18. Read Programmable Registers

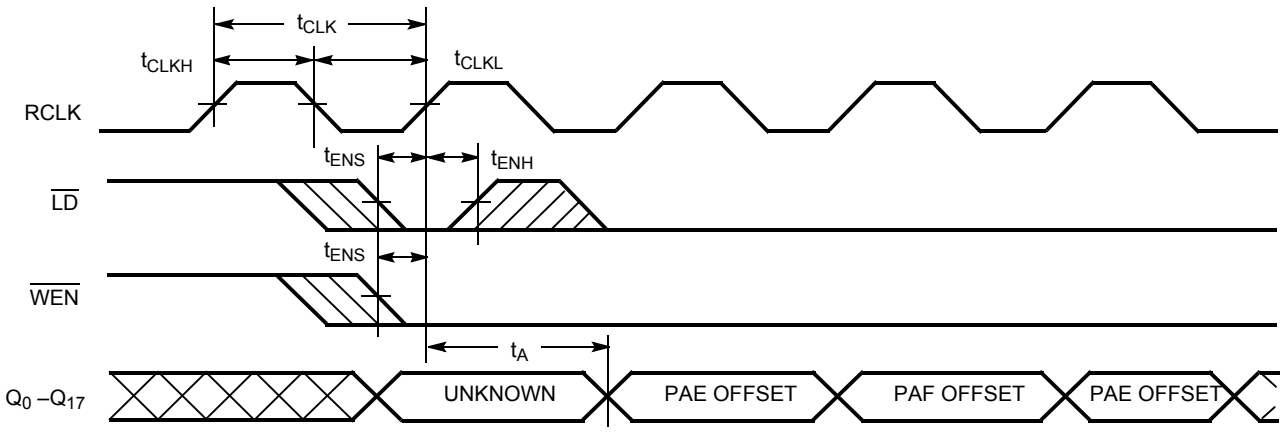


Figure 19. Write Expansion Out Timing

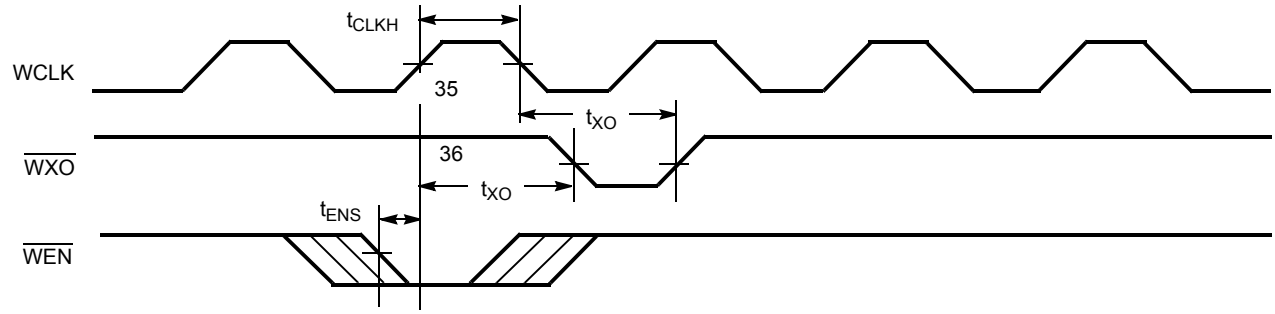


Figure 20. Read Expansion Out Timing

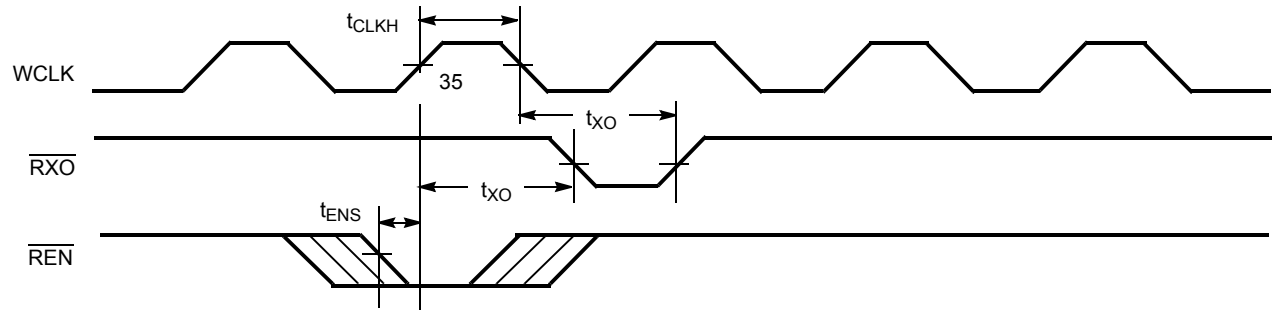
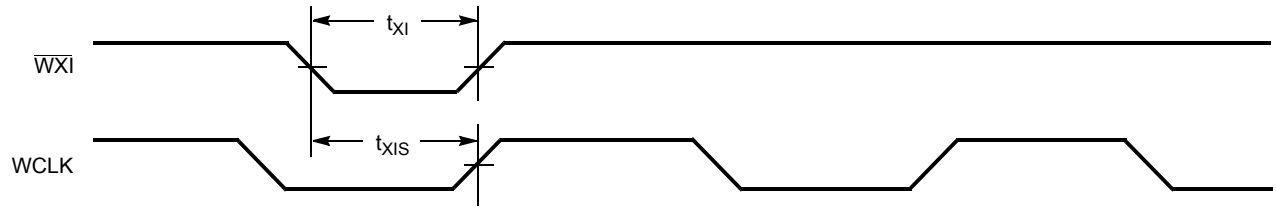


Figure 21. Write Expansion In Timing



Notes
35. Read from Last Physical Location.
36. Write to Last Physical Location.

Switching Waveforms *(continued)*

Figure 22. Read Expansion In Timing

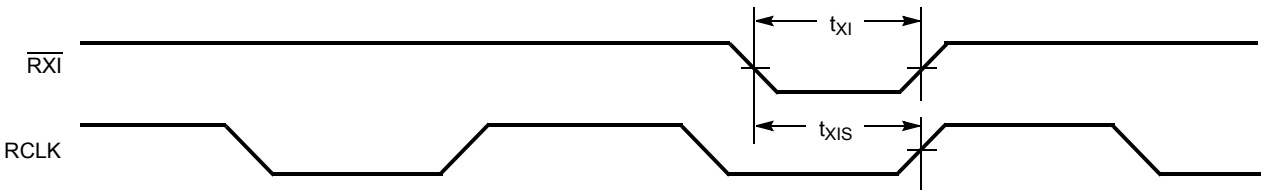
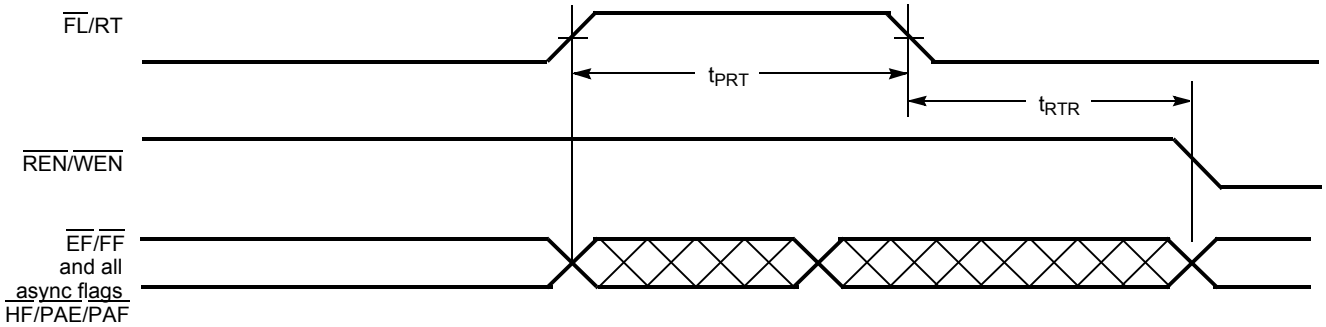


Figure 23. Retransmit Timing [37, 38, 39]

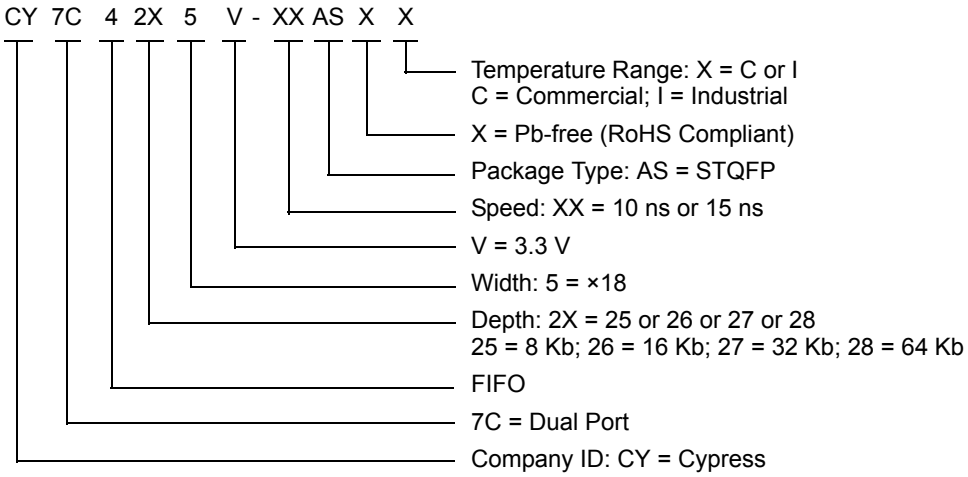


Notes
37. Clocks are free-running in this case.
38. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags are valid at t_{RTR}.
39. For the synchronous PAE and PAF flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Ordering Information

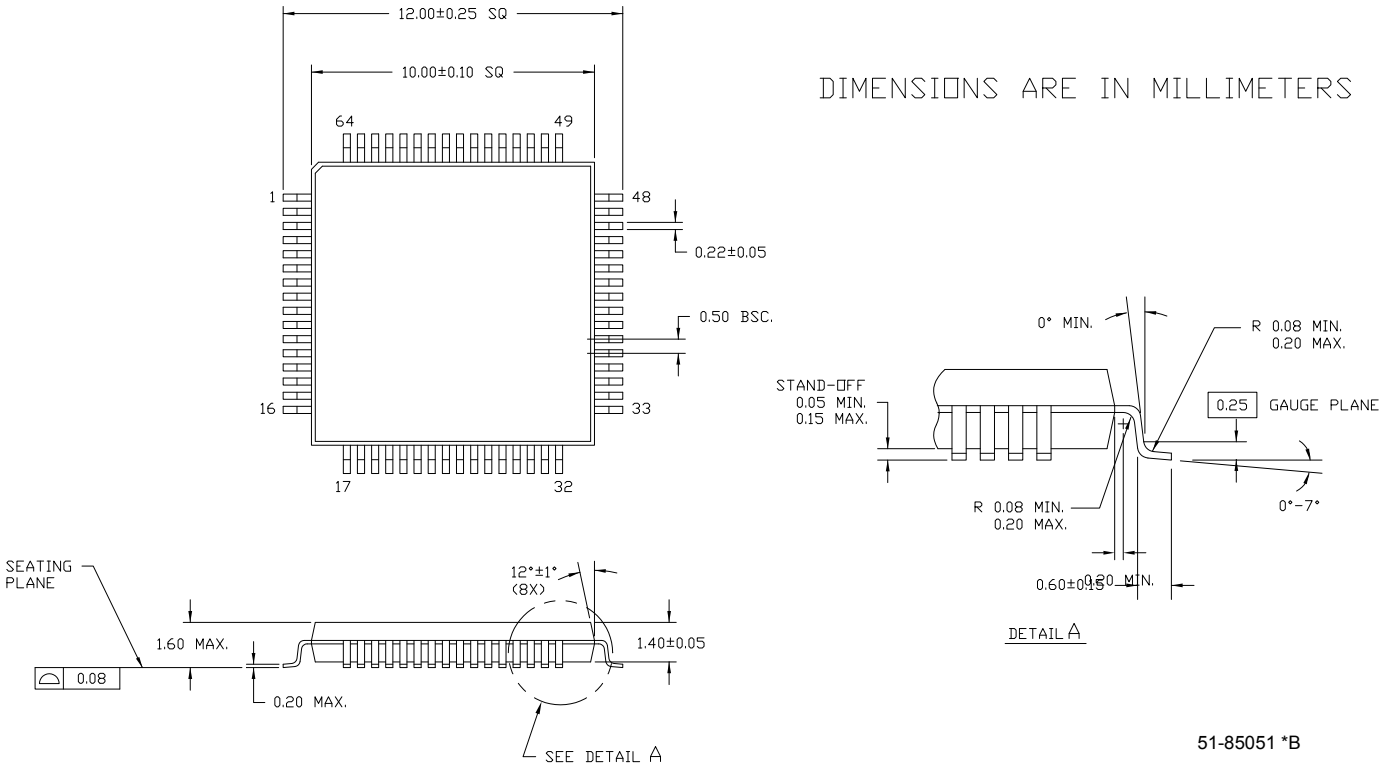
8 K × 18 Low-Voltage Deep Sync FIFO				
Speed (ns)	**Ordering Code**	**Package Diagram**	**Package Type**	**Operating Range**
10	CY7C4255V–10ASC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Commercial
	CY7C4255V–10ASXC		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	
15	CY7C4255V–15ASC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Commercial
	CY7C4255V–15ASXC		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	
	CY7C4255V–15ASXI	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	Industrial
	CY7C4255V–15ASI		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	
16 K × 18 Low-Voltage Deep Sync FIFO				
Speed (ns)	**Ordering Code**	**Package Diagram**	**Package Type**	**Operating Range**
15	CY7C4265V–15ASC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Commercial
32 K × 18 Low-Voltage Deep Sync FIFO				
Speed (ns)	**Ordering Code**	**Package Diagram**	**Package Type**	**Operating Range**
15	CY7C4275V–15ASC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Commercial
	CY7C4275V–15ASXC		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	
64 K × 18 Low-Voltage Deep Sync FIFO				
Speed (ns)	**Ordering Code**	**Package Diagram**	**Package Type**	**Operating Range**
10	CY7C4285V–10ASC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Commercial
	CY7C4285V–10ASXC		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	
15	CY7C4285V–15ASXC	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	Commercial
	CY7C4285V–15ASC		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	
	CY7C4285V–15ASI	51-85051	64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm)	Industrial
	CY7C4285V–15ASXI		64-pin Thin Quad Flat Pack (10 × 10 × 1.4 mm) (Pb-free)	

Ordering Code Definitions



Package Diagram

Figure 24. 64-pin Thin Plastic Quad Flat Pack (10 × 10 × 1.4 mm)



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
FIFO	first-in first-out
I/O	input/output
$\overline{OE}$	output enable
$\overline{REN}$	read enable
RCLK	read clock
RT	Retransmit
$\overline{RS}$	Reset
TQFP	thin quad flat pack
WCLK	write clock
$\overline{WEN}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
ms	milli seconds
mV	milli Volts
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

Document History Page

Document Title: CY7C4255V/CY7C4265V/CY7C4275V/CY7C4285V 8 K/16 K/32 K/64 K × 18 Low Voltage Deep Sync FIFOs Document Number: 38-06012				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	106473	SZV	09/10/01	Change from Spec number: 38-00654 to 38-06012
*A	122264	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	2556036	VKN/AESA	08/22/2008	Updated ordering information and data sheet template.
*C	2896039	RAME	03/19/2010	Added Contents Updated package diagram Removed inactive parts from Ordering information table Updated links in Sales, Solutions and Legal Information
*D	3123000	ADMU	12/31/2010	Removed speed bin -25 Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.

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