

# 1-Mbit (128 K × 8) Static RAM

## Features

- Pin- and function-compatible with CY7C109B/CY7C1009B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA}$  at 10 ns
- Low CMOS standby power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  options
- CY7C109D available in Pb-free 32-pin 400-Mil wide Molded SOJ and 32-pin TSOP I packages. CY7C1009D available in Pb-free 32-pin 300-Mil wide Molded SOJ package

## Functional Description [1]

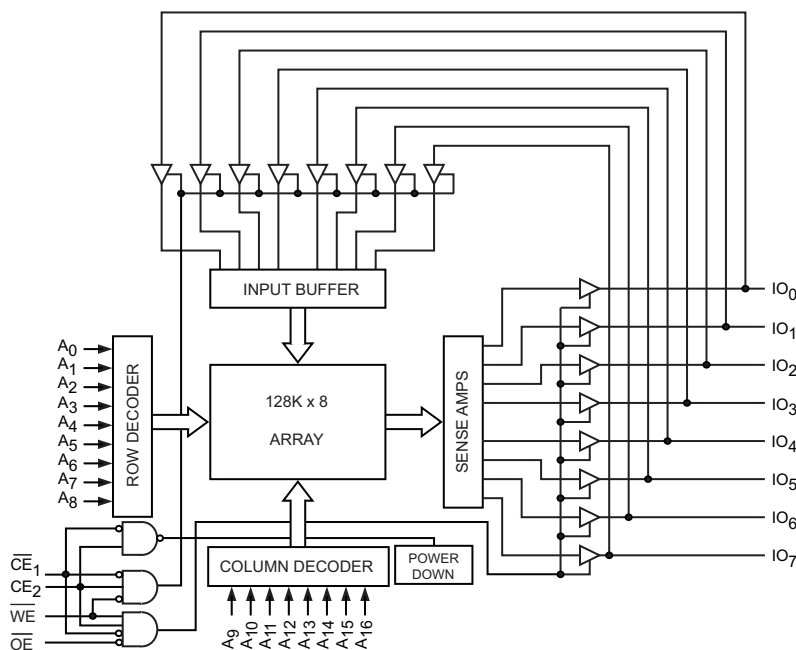
The CY7C109D/CY7C1009D is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW),
- Outputs are disabled ( $\overline{OE}$  HIGH),
- When the write operation is active ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $WE$  LOW)

Write to the device by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and Chip Enable Two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Read from the device by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable Two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

## Logic Block Diagram



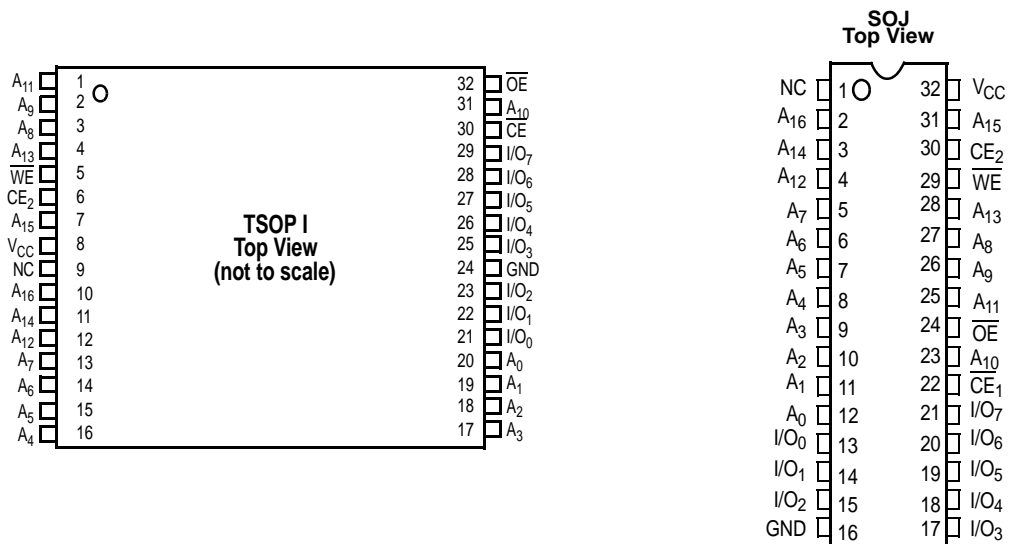
### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configuration [2]



## Selection Guide

	<b>CY7C109D-10</b> <b>CY7C1009D-10</b>	<b>Unit</b>
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	3	mA

**Note**

2. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND <sup>[3]</sup>...-0.5 V to +6.0 V  
 DC Voltage Applied to Outputs in High-Z State <sup>[3]</sup>.....-0.5 V to V<sub>CC</sub> + 0.5 V

DC Input Voltage <sup>[3]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001 V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40°C to +85°C	5 V ± 0.5 V	10 ns

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	7C109D-10 7C1009D-10		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>max</sub> = 1/t <sub>RC</sub>	100 MHz	80	mA
			83 MHz	72	mA
			66 MHz	58	mA
			40 MHz	37	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub>		10	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3 V, or CE <sub>2</sub> ≤ 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0		3	mA

**Note**

3. V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.

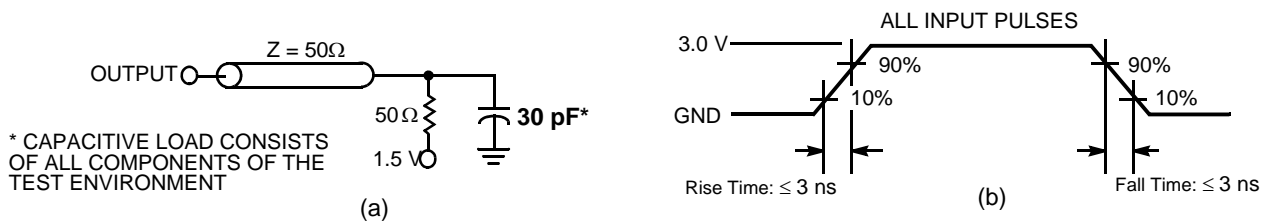
### Capacitance [4]

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

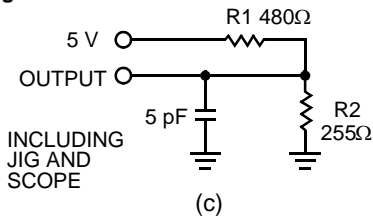
### Thermal Resistance [4]

Parameter	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	TSOP I	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	56.29	50.72	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		40.53	38.14	16.21	°C/W

### AC Test Loads and Waveforms [5]



#### High-Z characteristics:



#### Notes

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

### Switching Characteristics (Over the Operating Range) <sup>[6]</sup>

Parameter	Description	7C109D-10 7C1009D-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[7]}$	$V_{CC}$ (typical) to the first access	100		$\mu$ s
$t_{RC}$	Read Cycle Time	10		ns
$t_{AA}$	Address to Data Valid		10	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		10	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[8, 9]</sup>		5	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[9]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[8, 9]</sup>		5	ns
$t_{PU}^{[10]}$	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		ns
$t_{PD}^{[10]}$	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		10	ns
<b>Write Cycle <sup>[11, 12]</sup></b>				
$t_{WC}$	Write Cycle Time	10		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	7		ns
$t_{AW}$	Address Set-Up to Write End	7		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		ns
$t_{SD}$	Data Set-Up to Write End	6		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8, 9]</sup>		5	ns

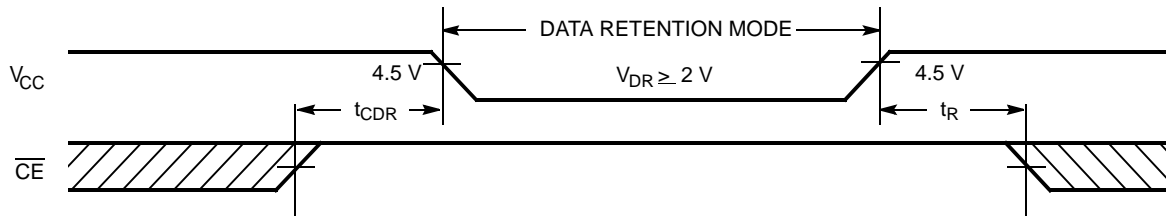
#### Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
7.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed
8.  $t_{HZOE}$ ,  $t_{HZCE}$  and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms <sup>[5]</sup>" on page 5. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** (Over the Operating Range)

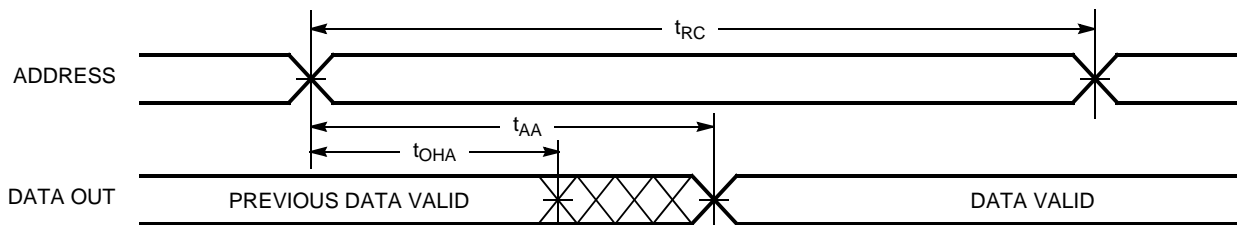
Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	$V_{CC} = V_{DR} = 2.0\text{ V}$ ,	2.0		V
$I_{CCDR}$	Data Retention Current	$CE_1 \geq V_{CC} - 0.3\text{ V}$ or $CE_2 \leq 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$		3	mA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[13]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

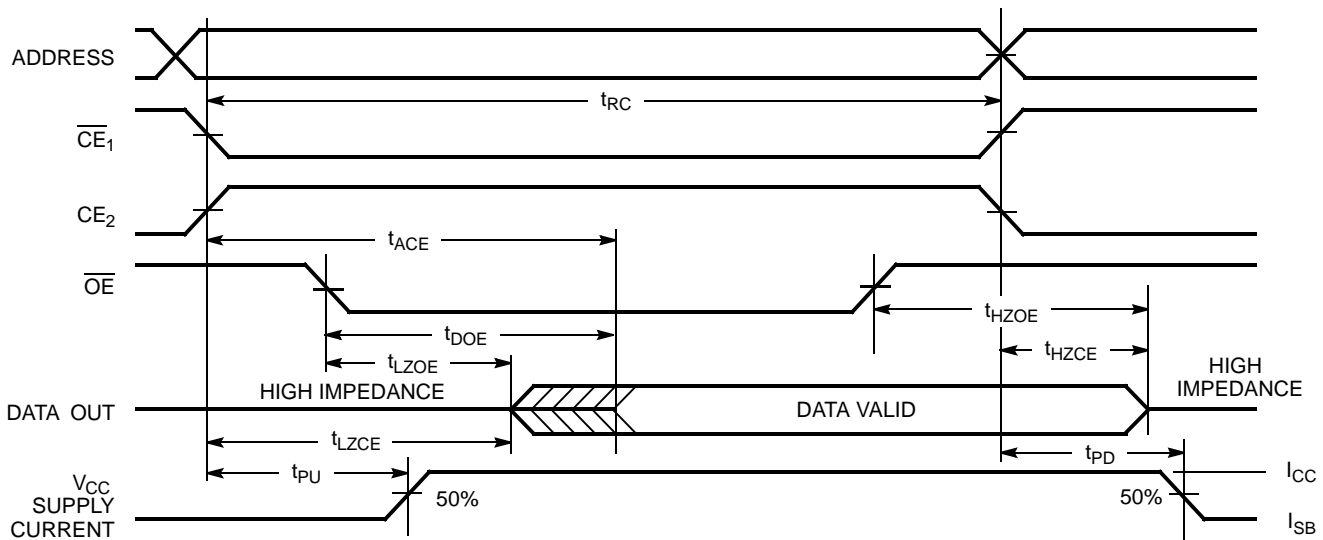


**Switching Waveforms**

**Figure 1. Read Cycle No. 1 (Address Transition Controlled)** [14, 15]



**Figure 2. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [15, 16]



**Notes**

- 13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .
- 14. Device is continuously selected.  $\overline{OE}$ ,  $CE_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 3. Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [17, 18]

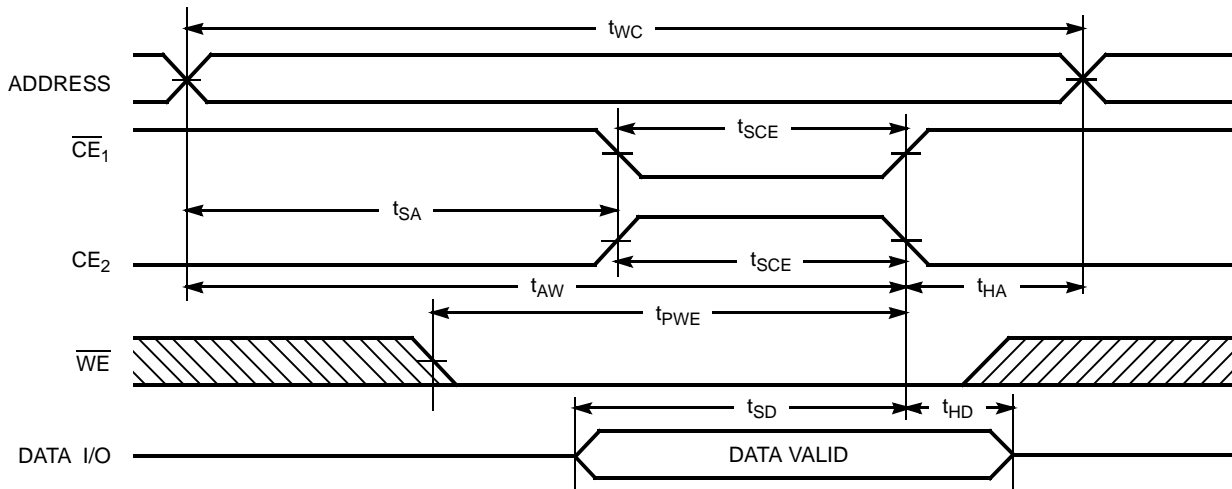
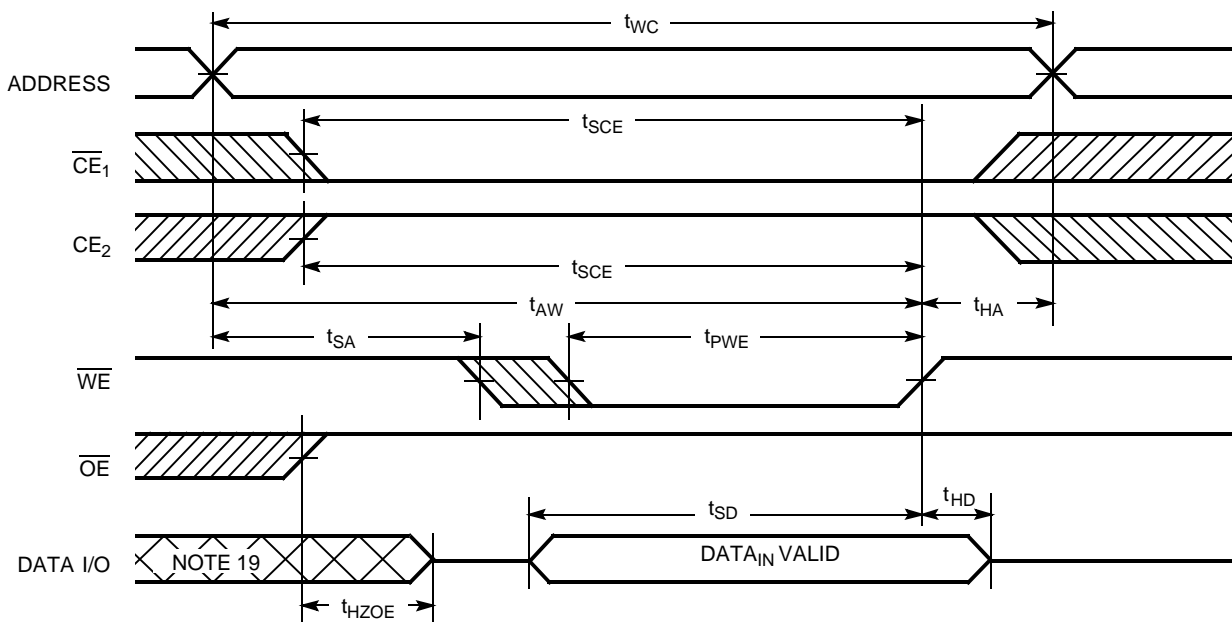


Figure 4. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [17, 18]



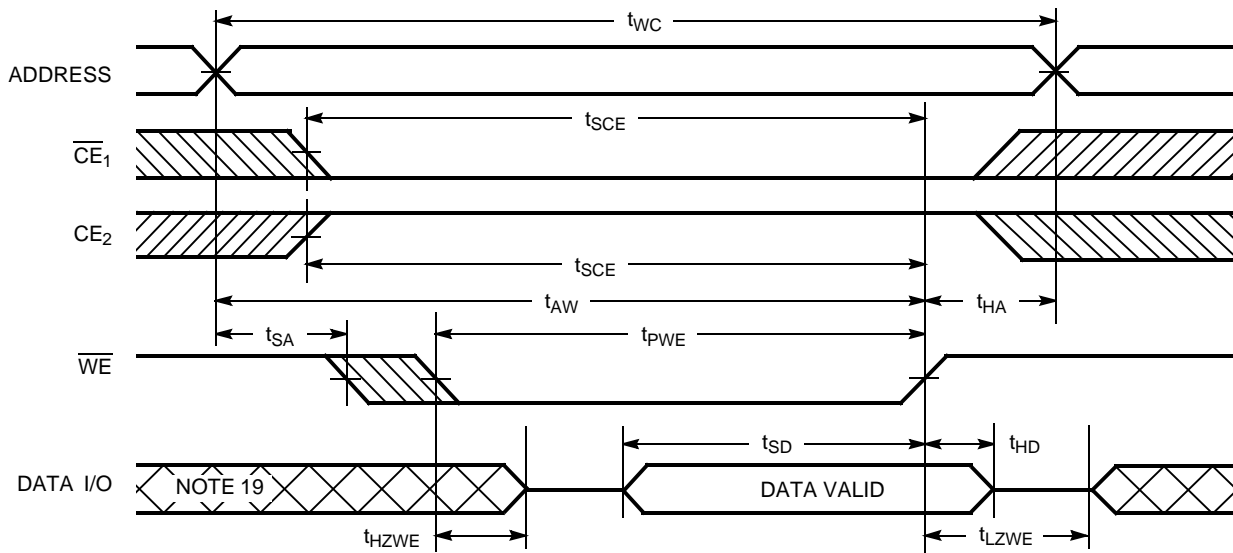
Notes

- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 19. During this period the I/Os are in the output state and input signals should not be applied.



Switching Waveforms (continued)

Figure 5. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [12, 18]



Truth Table

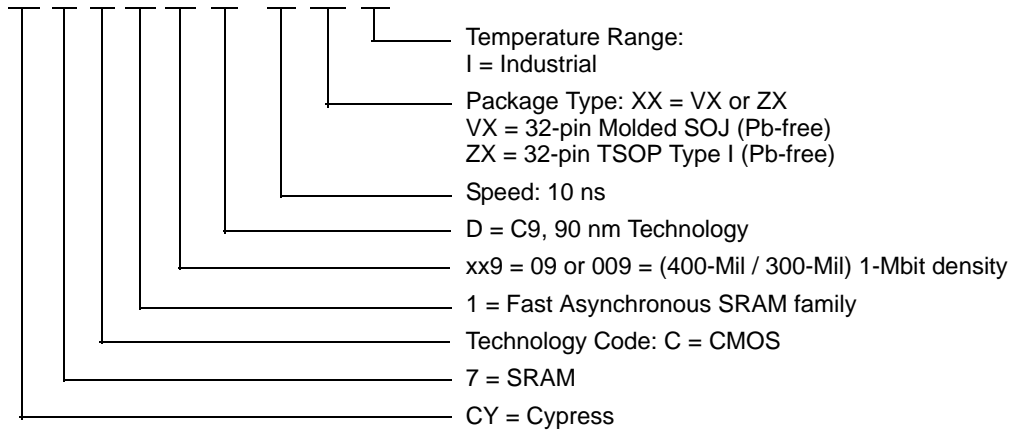
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C109D-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C109D-10ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY7C1009D-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	

## Ordering Code Definitions

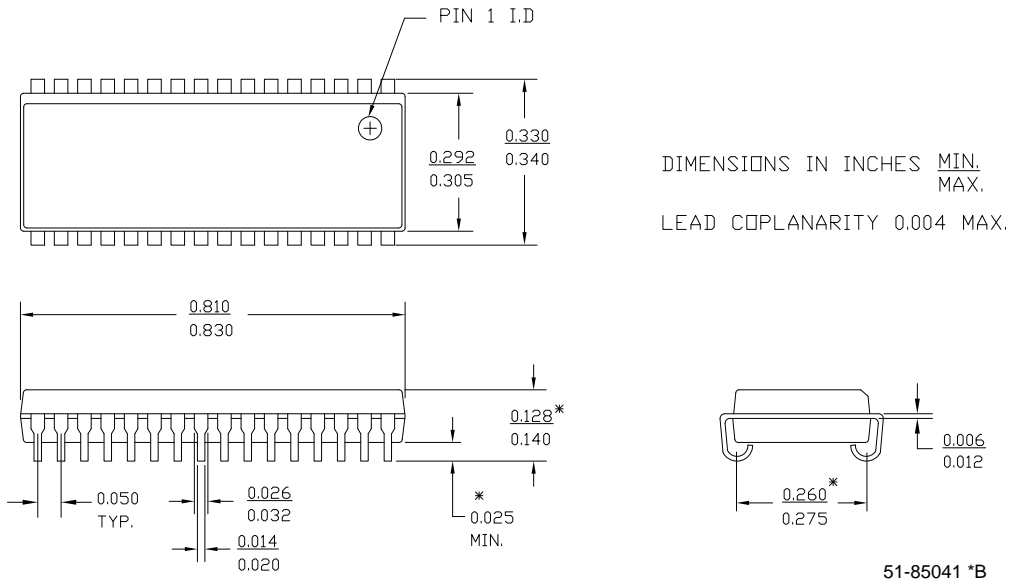
CY 7 C 1 xx9 D - 10 XX I



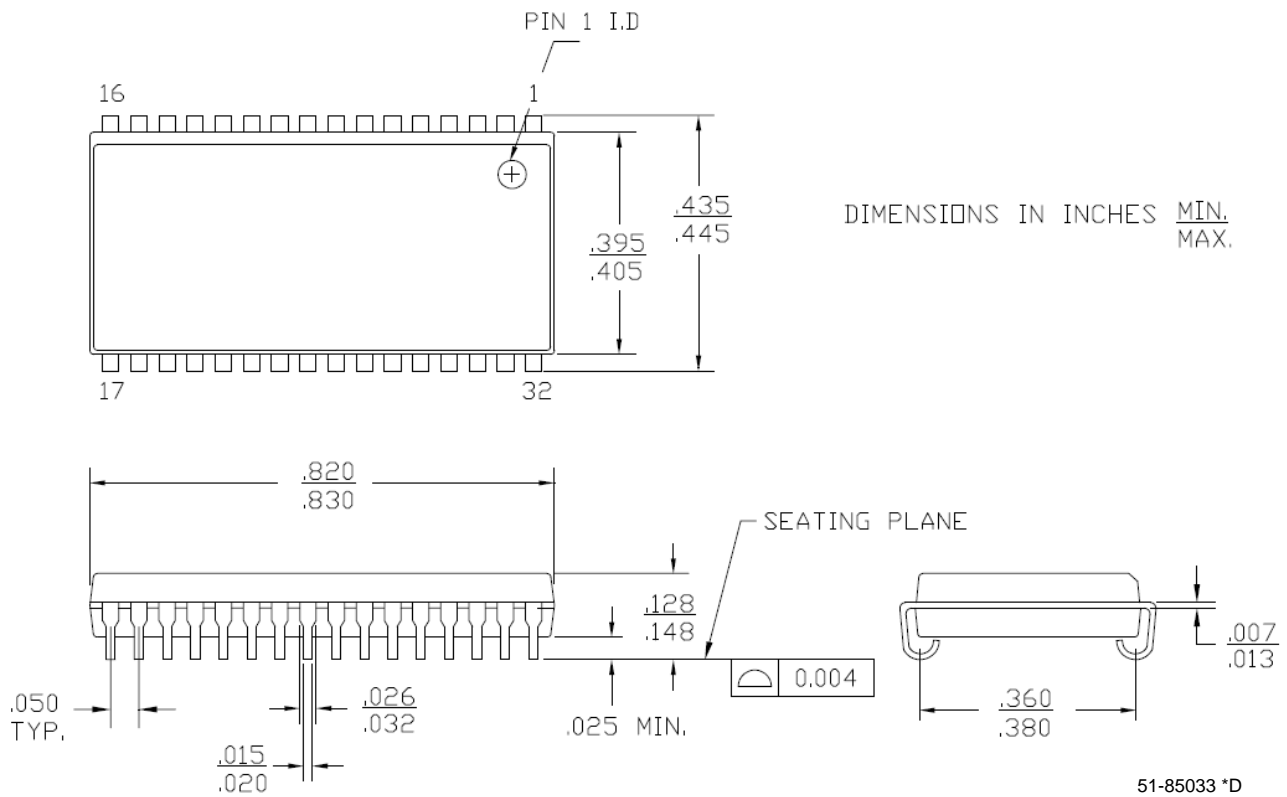
Please contact your local Cypress sales representative for availability of these parts.

**Package Diagrams**

**Figure 6. 32-pin (300-Mil) Molded SOJ, 51-85041**

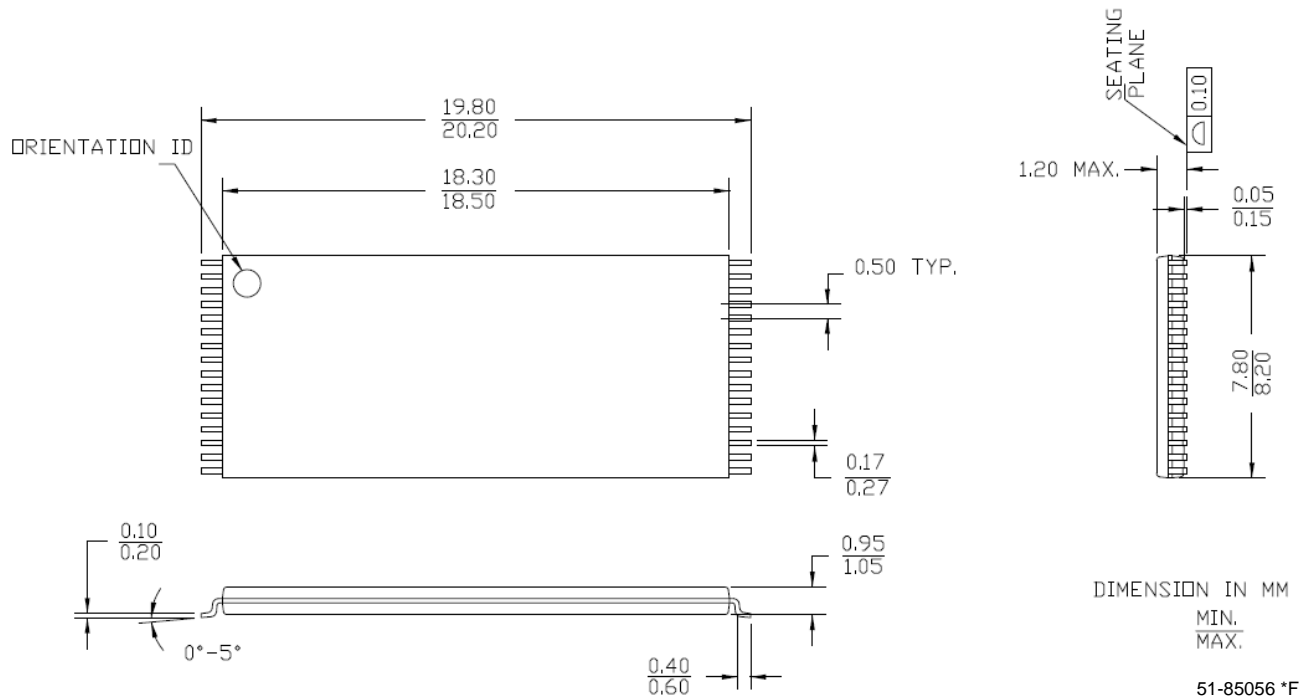


**Figure 7. 32-pin (400-Mil) Molded SOJ, 51-85033**



**Package Diagrams** (continued)

**Figure 8. 32-pin Thin Small Outline Package Type I (8 × 20 mm), 51-85056**



**Acronyms**

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

## Document History Page

Document Title: CY7C109D/CY7C1009D, 1-Mbit (128 K × 8) Static RAM				
Document Number: 38-05468				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics Table Shaded Ordering Information
*C	See ECN	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2 V to V <sub>CC</sub> +1 V in footnote #3
*E	802877	See ECN	VKN	Changed I <sub>CC</sub> spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3104943	12/08/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*G	3220123	04/08/2011	PRAS	Updated template and styles as per current Cypress standards. Added Acronyms and units of measure. Updated package diagrams: 51-85033 to *D 51-85056 to *F

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