

# 2M x 8 Static RAM

## Features

- High speed
  - $t_{AA} = 10, 12 \text{ ns}$
- Low active power
  - 990 mW (max.)
- Operating voltages of  $3.3 \pm 0.3V$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free and non Pb-free 54-pin TSOP II, non Pb-free 60-ball fine-pitch ball grid array (FBGA) package

## Functional Description

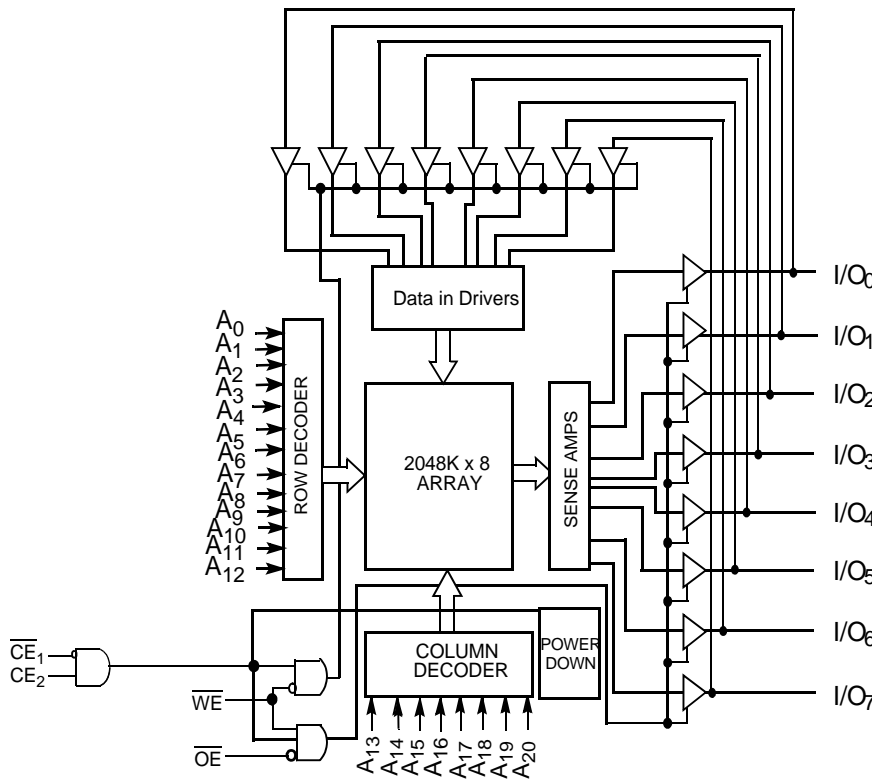
The CY7C1069AV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking  $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW.

Reading from the device is accomplished by enabling the chip ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) as well as forcing the Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 60-ball fine-pitch ball grid array (FBGA) package.

## Logic Block Diagram



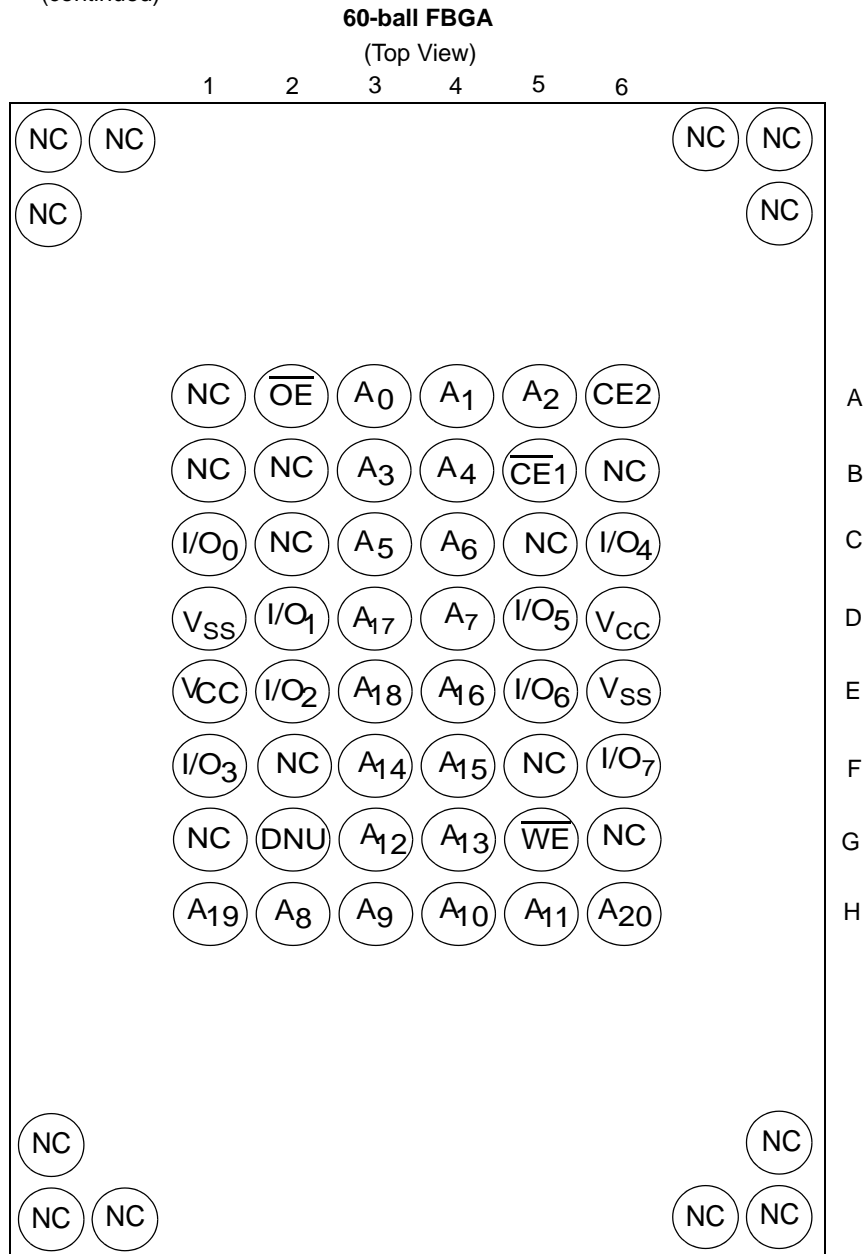
## Pin Configurations<sup>[1, 2]</sup>

TSOP II Top View			
NC	1	54	NC
V <sub>CC</sub>	2	53	V <sub>SS</sub>
NC	3	52	NC
I/O <sub>6</sub>	4	51	I/O <sub>5</sub>
V <sub>SS</sub>	5	50	V <sub>CC</sub>
I/O <sub>7</sub>	6	49	I/O <sub>4</sub>
A <sub>4</sub>	7	48	A <sub>5</sub>
A <sub>3</sub>	8	47	A <sub>6</sub>
A <sub>2</sub>	9	46	A <sub>7</sub>
A <sub>1</sub>	10	45	A <sub>8</sub>
A <sub>0</sub>	11	44	A <sub>9</sub>
NC	12	43	NC
$\overline{CE}_1$	13	42	$\overline{OE}$
V <sub>CC</sub>	14	41	V <sub>SS</sub>
$\overline{WE}$	15	40	DNU
$CE_2$	16	39	A <sub>20</sub>
A <sub>19</sub>	17	38	A <sub>10</sub>
A <sub>18</sub>	18	37	A <sub>11</sub>
A <sub>17</sub>	19	36	A <sub>12</sub>
A <sub>16</sub>	20	35	A <sub>13</sub>
A <sub>15</sub>	21	34	A <sub>14</sub>
I/O <sub>0</sub>	22	33	I/O <sub>3</sub>
V <sub>CC</sub>	23	32	V <sub>SS</sub>
I/O <sub>1</sub>	24	31	I/O <sub>2</sub>
NC	25	30	NC
V <sub>SS</sub>	26	29	V <sub>CC</sub>
NC	27	28	NC

**Selection Guide**

	-10	-12	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	275	260	mA
Maximum CMOS Standby Current	50	50	mA

**Pin Configurations<sup>[1, 2]</sup>(continued)**



**Notes:**

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[3]</sup> .... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- DC Input Voltage<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

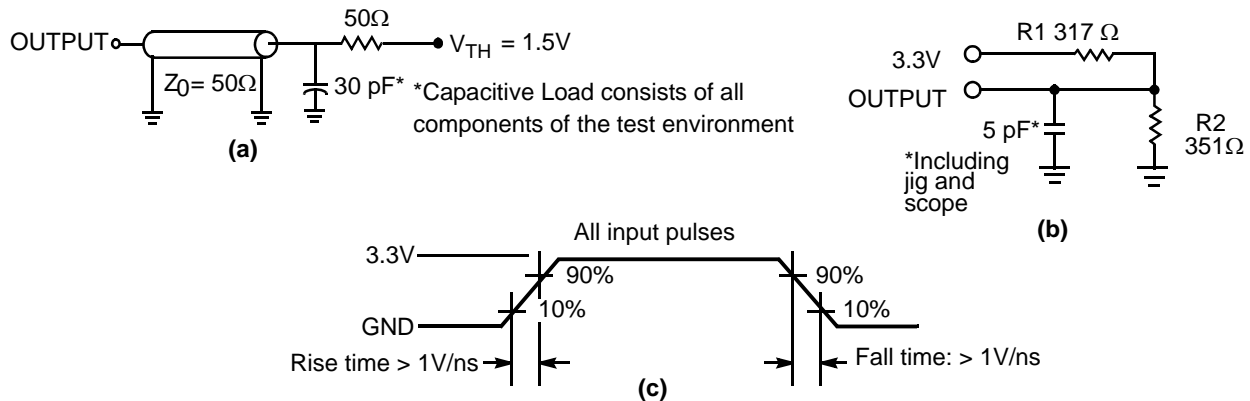
**DC Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		275		260	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	CE <sub>2</sub> ≤ V <sub>IL</sub> , Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		70		70	mA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	CE <sub>2</sub> ≤ 0.3V, Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		50		50	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	TSOP II	FBGA	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	6	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	10	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**



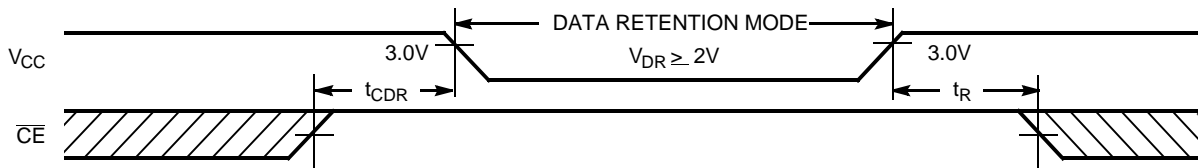
**Notes:**

3. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0V). As soon as 1ms (T<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation can begin including reduction in V<sub>DD</sub> to the data retention (V<sub>CCDR</sub>, 2.0V) voltage.

AC Switching Characteristics Over the Operating Range [7]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[8]</sup>	1		1		ms
$t_{RC}$	Read Cycle Time	10		12		ns
$t_{AA}$	Address to Data Valid		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Data Valid		10		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[9]</sup>	1		1		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[9]</sup>		5		6	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to High-Z <sup>[9]</sup>		5		6	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Power-up <sup>[10]</sup>	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to Power-down <sup>[10]</sup>		10		12	ns
<b>Write Cycle<sup>[10, 11]</sup></b>						
$t_{WC}$	Write Cycle Time	10		12		ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Write End	7		8		ns
$t_{AW}$	Address Set-up to Write End	7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		ns
$t_{SD}$	Data Set-up to Write End	5.5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[9]</sup>		5		6	ns

Data Retention Waveform

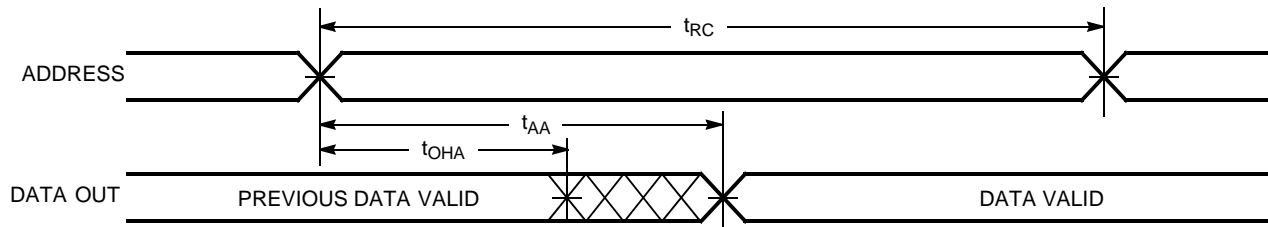


Notes:

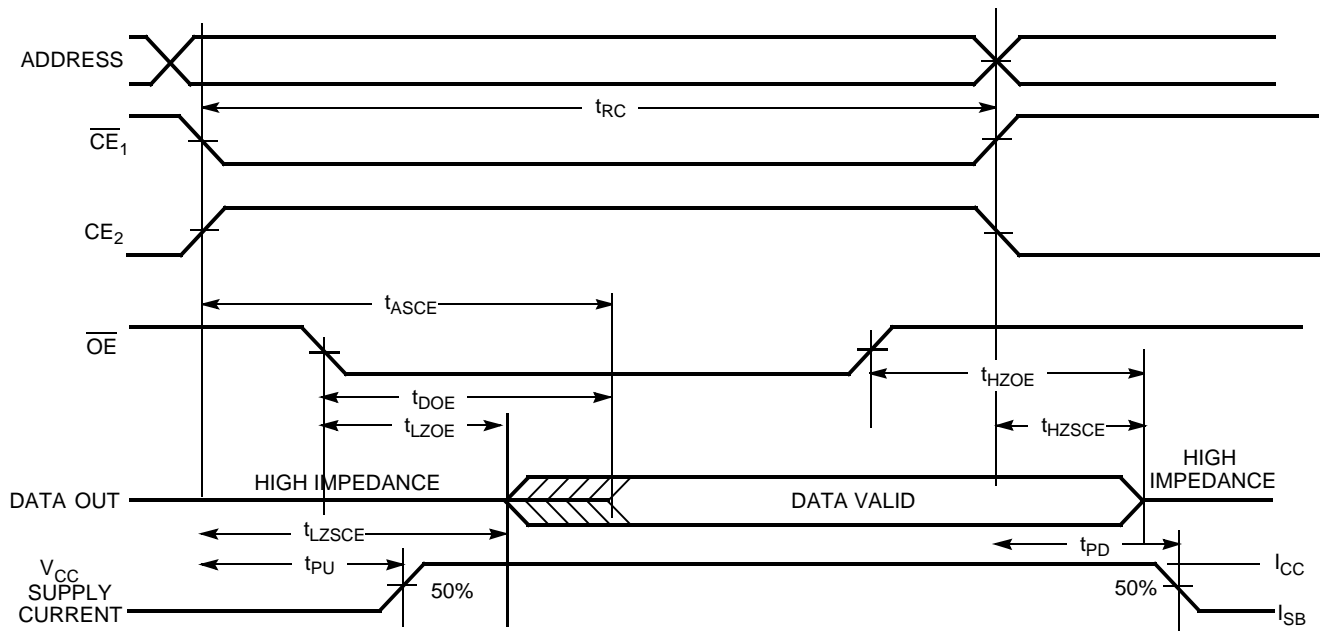
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{power}$  time has to be provided initially before a Read/Write operation is started.
- $t_{HZOE}$ ,  $t_{HZSCE}$ ,  $t_{HZWE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ , and  $t_{LZWE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW/ $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW along with  $CE_2$  HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

#### Read Cycle No. 1<sup>[13, 14]</sup>

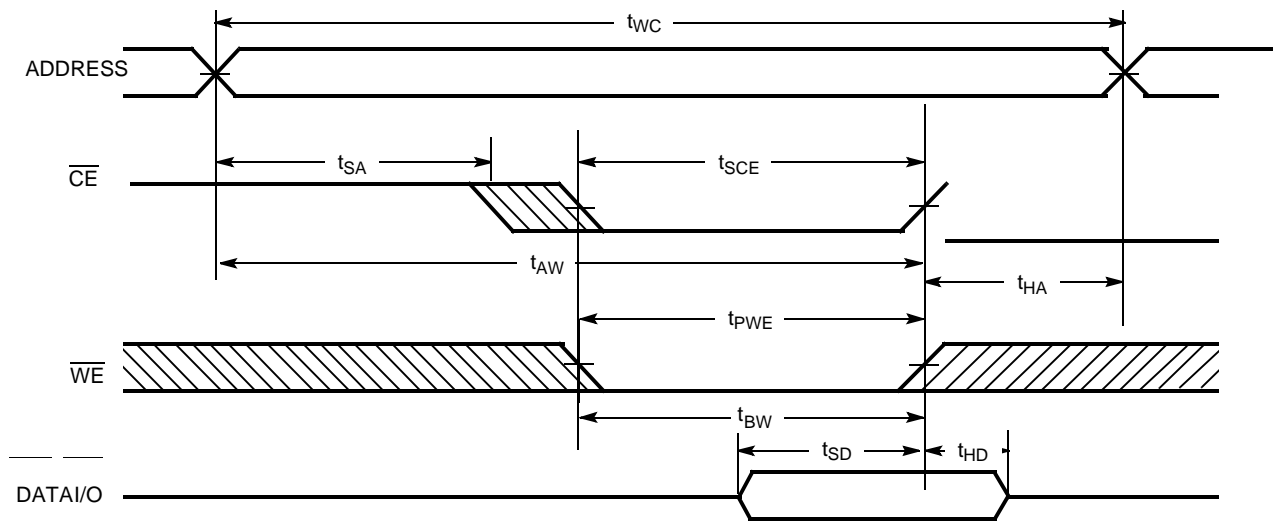
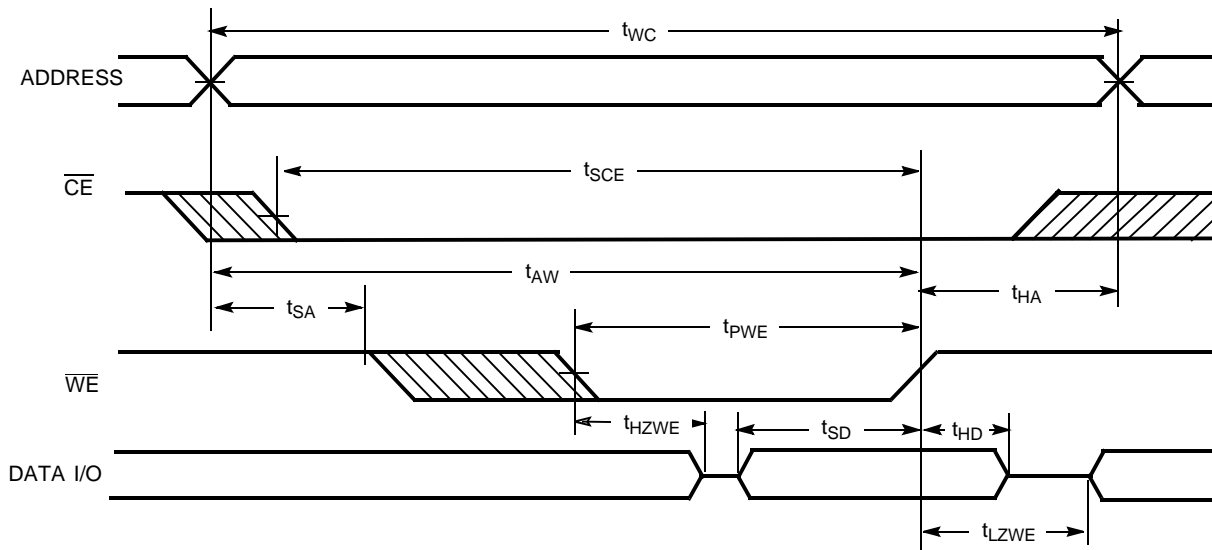


#### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[14, 15]</sup>



**Notes:**

- 13. Device is continuously selected.  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 14.  $\overline{WE}$  is HIGH for Read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  Controlled)<sup>[16, 17, 18]</sup>**

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16, 17, 18]</sup>**

**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read All Bits	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write All Bits	Active ( $I_{CC}$ )
L	H	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Notes:**

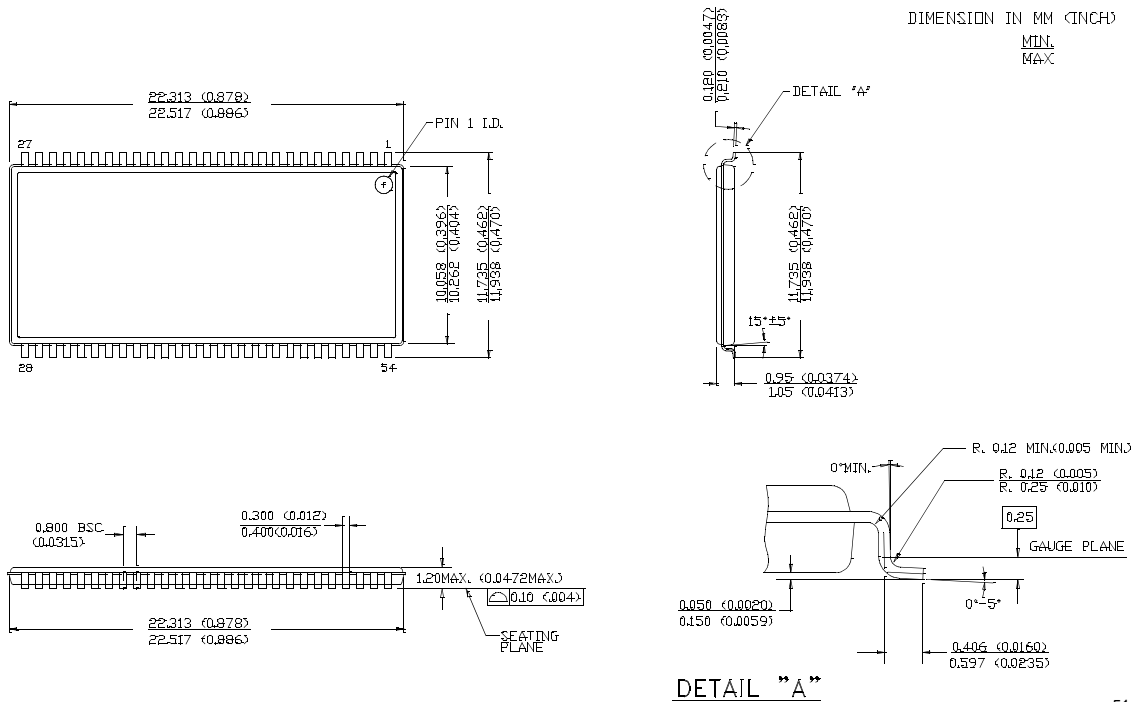
16. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
17. If  $\overline{CE}_1$  goes HIGH/ $\overline{CE}_2$  LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
18.  $\overline{CE}$  above is defined as a combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . It is active low.

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069AV33-10ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069AV33-10ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-10BAC	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
	CY7C1069AV33-10ZI	51-85160	54-pin TSOP II	Industrial
	CY7C1069AV33-10ZXI		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-10BAI	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
12	CY7C1069AV33-12ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069AV33-12ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-12BAC	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
	CY7C1069AV33-12ZI	51-85160	54-pin TSOP II	Industrial
	CY7C1069AV33-12ZXI		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-12BAI	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	

**Package Diagrams**

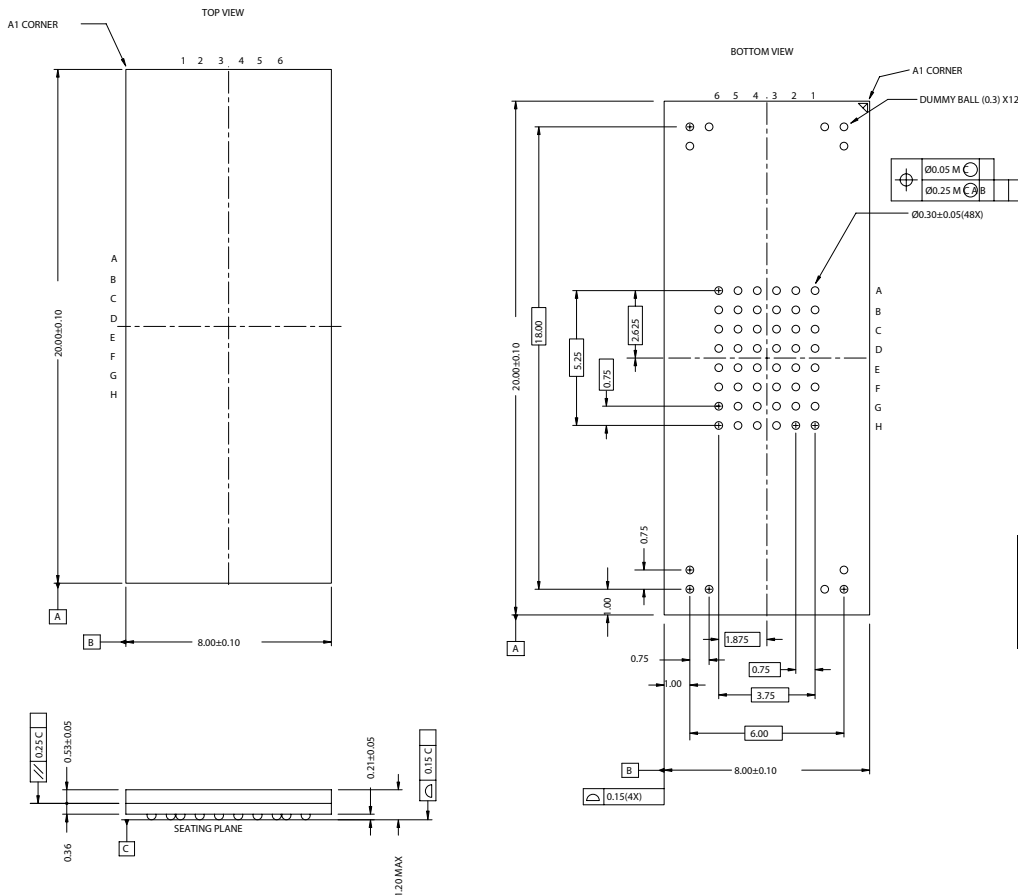
**54-pin TSOP II (51-85160)**



51-85160-\*\*

Package Diagrams (continued)

60-ball FBGA (8 mm x 20 mm x 1.2 mm) (51-85162)



DIMENSIONS IN MM

PART #	
BA60A	STANDARD PKG.
BK60A	LEAD FREE PKG.

PKG WEIGHT: 0.30 gms

51-85162-\*D

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**Document History Page**

Document Title: CY7C1069AV33 2M x 8 Static RAM				
Document Number: 38-05255				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15-ns bin
*B	117990	08/30/02	DFP	Added 8-ns bin Changing I <sub>CC</sub> for 8, 10, 12 bins t <sub>power</sub> changed from 1 μs to 1 ms Load Cap Comment changed (for Tx line load) t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin #'s (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> ) Removed hz < lz comments
*C	120385	11/13/02	DFP	Final Data Sheet Added note 4 to "AC Test Loads and Waveforms" and note 7 to t <sub>pu</sub> and t <sub>pd</sub> Updated Input/Output Caps (for 48BGA only) to 8 pf/10 pf and for the 54-pin TSOP to 6/8 pf
*D	124441	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded the 48fBGA product offering information
*E	403984	See ECN	NXR	Changed the Logic Block Diagram On page # 1 Added notes under Pin Configuration Changed the Package diagram of 51-85162 from Rev *A to Rev *D Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Updated the Ordering Information
*F	492137	See ECN	NXR	Removed 8 ns speed bin from product offering Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information