

## Features

- 3.3 V operation (3.0 V–3.6 V)
- High speed
  - $t_{AA} = 15$  ns
- CMOS for optimum speed/power
- Low Active Power
  - 576 mW (max)
- Low CMOS Standby Power
  - 1.80 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 400-mil SOJ
- Available in a 48-ball Mini BGA package

## Functional Description<sup>[1]</sup>

The CY7C1021BNV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

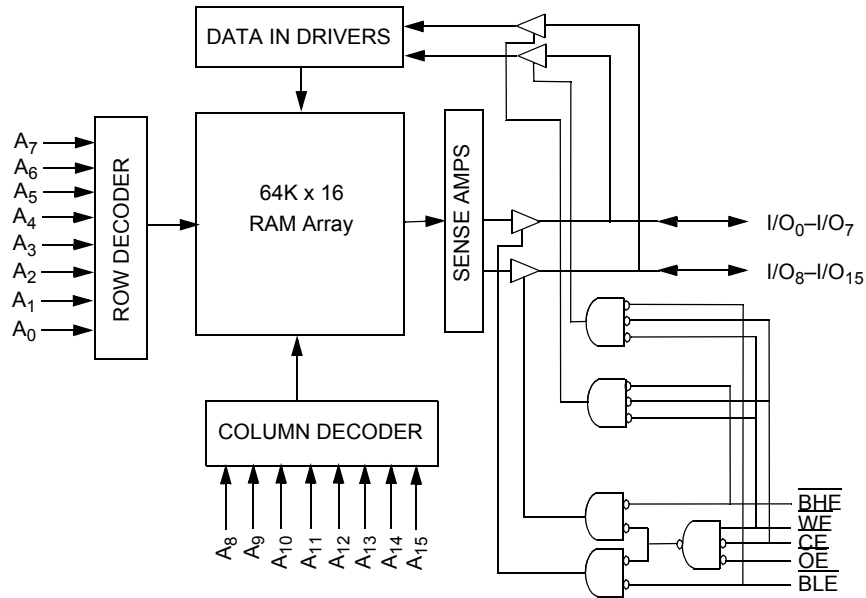
The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and WE LOW).

The CY7C1021BNV33 is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and 48-ball mini BGA packages.

### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

Logic Block Diagram



Selection Guide

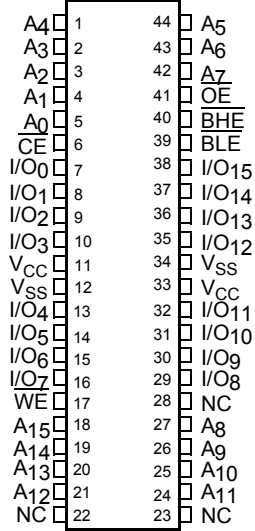
	<b>-15</b>
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	160
Maximum CMOS Standby Current (mA)	0.5

## Contents

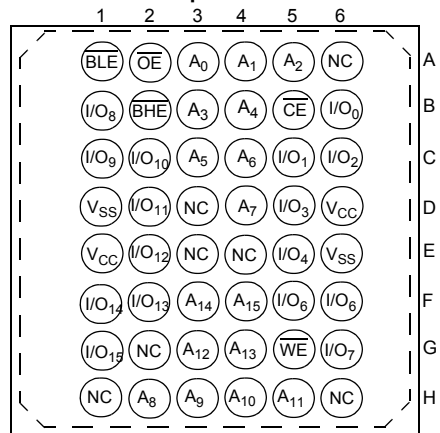
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Pin Configurations

SOJ / TSOP II  
Top View



Mini BGA  
Top View



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with  
 Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> ... -0.5 V to +4.6 V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage<sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V  
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... > 2001 V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V ± 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	–	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0$ mA	–	0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$ V	V
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$	–	160	mA
$I_{SB1}$	Automatic CE Power Down Current —TTL Inputs	Max $V_{CC}$ , $CE \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	–	40	mA
$I_{SB2}$	Automatic CE Power Down Current —CMOS Inputs	Max $V_{CC}$ , $CE \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$	–	500	μA

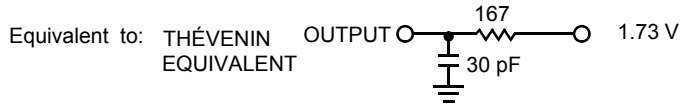
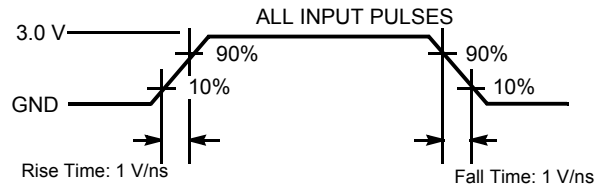
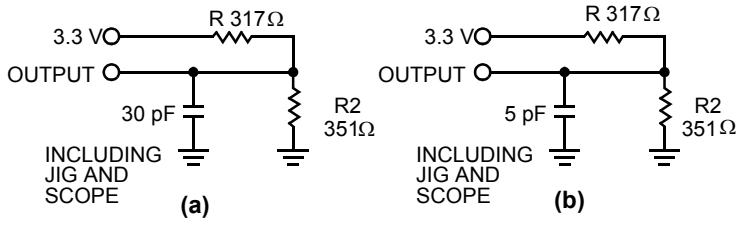
## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25$ °C, $f = 1$ MHz	6	pF
$C_{OUT}$	Output Capacitance		8	pF

### Notes

- Minimum voltage is -2.0 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



## Switching Characteristics<sup>[4]</sup>

Over the Operating Range

Parameter	Description	-15		Unit
		Min	Max	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	15	–	ns
$t_{AA}$	Address to Data Valid	–	15	ns
$t_{OHA}$	Data Hold from Address Change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid	–	15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>	–	7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>	–	7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down	–	15	ns
$t_{DBE}$	Byte Enable to Data Valid	–	7	ns
$t_{LZBE}$	Byte Enable to Low Z	0	–	ns
$t_{HZBE}$	Byte Disable to High Z	–	7	ns
<b>WRITE CYCLE<sup>[7]</sup></b>				
$t_{WC}$	Write Cycle Time	15	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10	–	ns
$t_{AW}$	Address Set-Up to Write End	10	–	ns
$t_{HA}$	Address Hold from Write End	0	–	ns
$t_{SA}$	Address Set-Up to Write Start	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10	–	ns
$t_{SD}$	Data Set-Up to Write End	8	–	ns
$t_{HD}$	Data Hold from Write End	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>	–	7	ns
$t_{BW}$	Byte Enable to End of Write	9	–	ns

### Notes

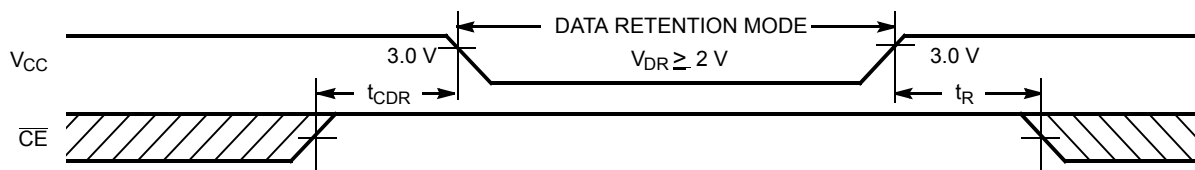
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of [AC Test Loads and Waveforms on page 6](#). Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}$  /  $\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}$  /  $\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

### Data Retention Characteristics

Over the Operating Range (L version only)

Parameter	Description	Conditions <sup>[8]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $CE \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	100	$\mu\text{A}$
$t_{CDR}^{[9]}$	Chip Deselect to Data Retention Time		0	–	ns
$t_R^{[10]}$	Operation Recovery Time		15	–	ns

### Data Retention Waveform



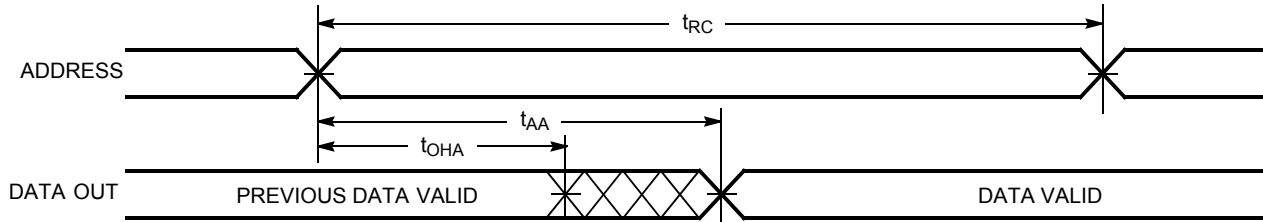
**Notes**

- 8. No input may exceed  $V_{CC} + 0.5\text{ V}$ .
- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10.  $t_r \leq 3\text{ ns}$  for the -12 and -15 speeds.  $t_r \leq 5\text{ ns}$  for the -20 and slower speeds.

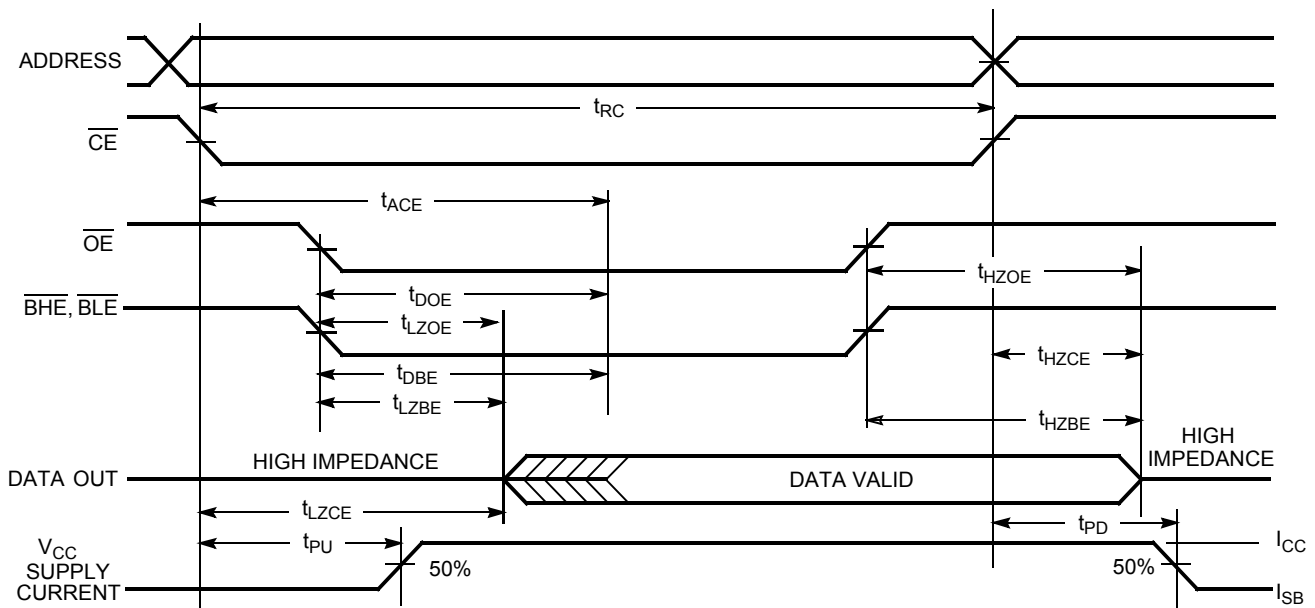


### Switching Waveforms

#### Read Cycle No. 1<sup>[11, 12]</sup>



#### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[12, 13]</sup>

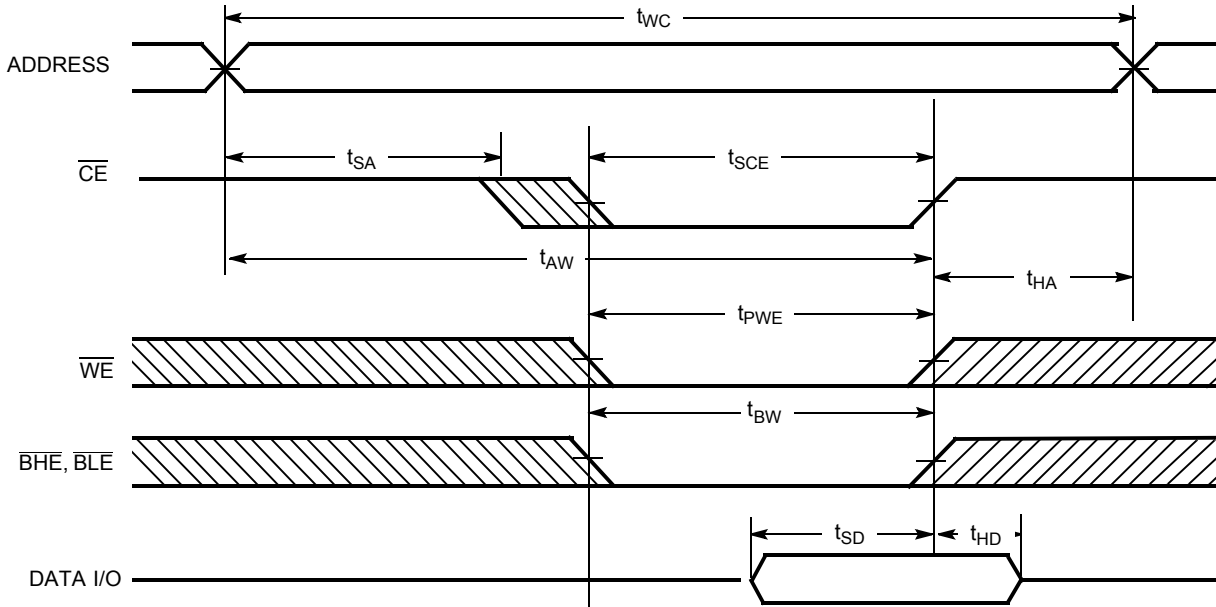


**Notes**

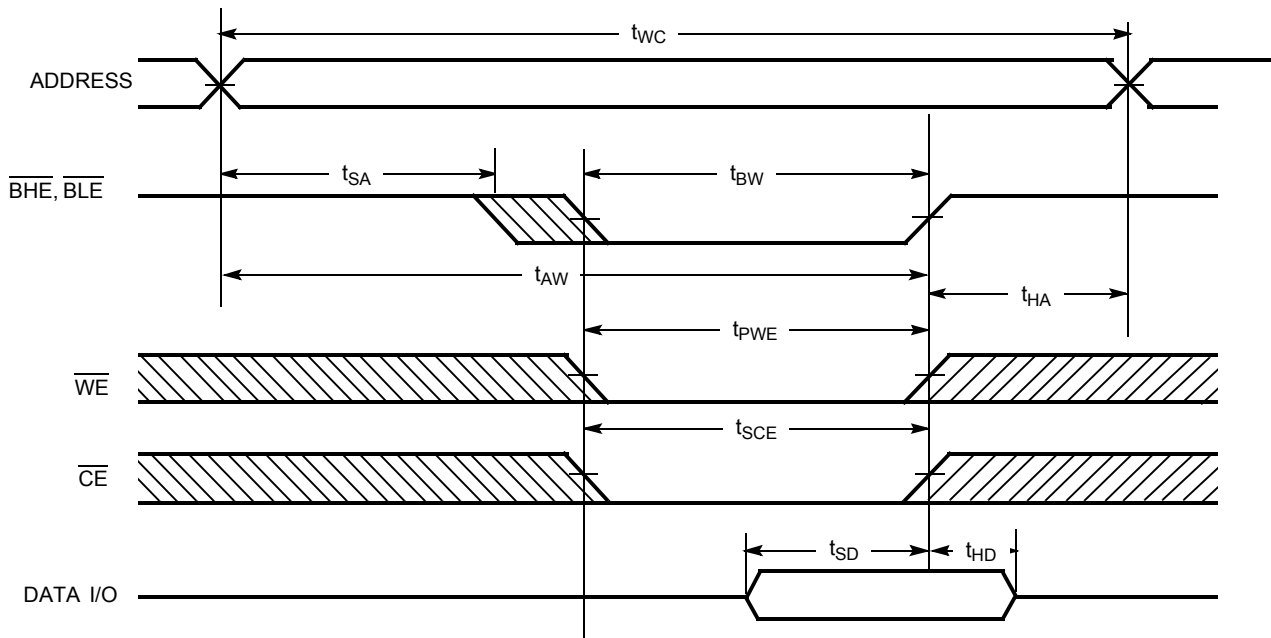
- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms(continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>



Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)

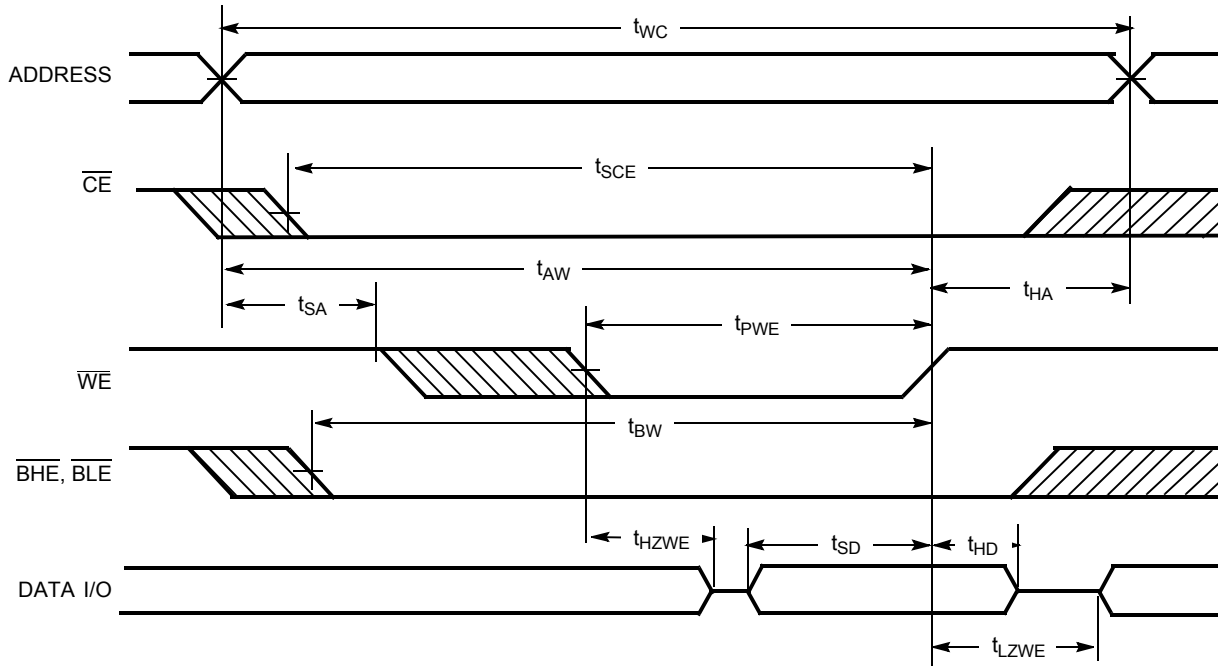


Notes

- 14. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

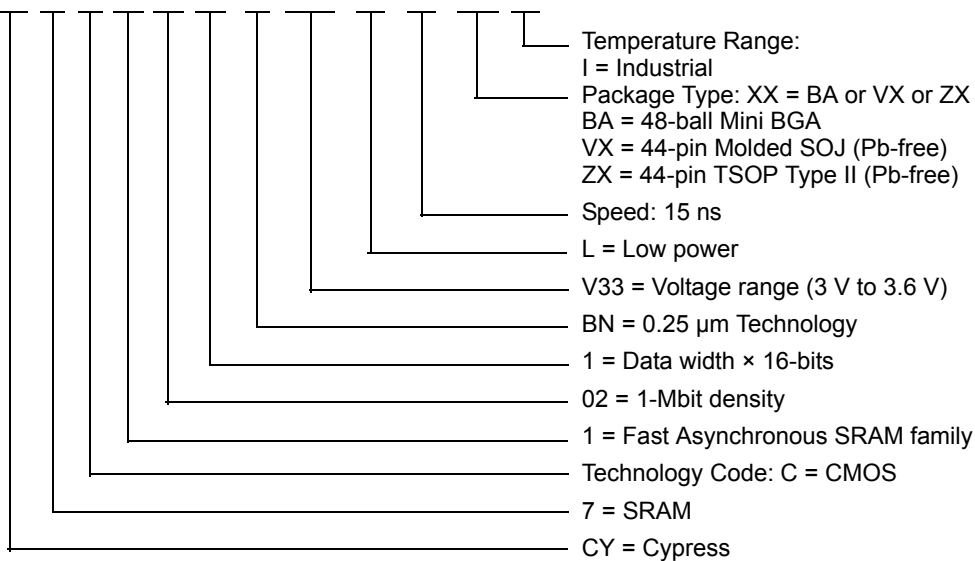
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

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Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1021BNV33L-15BAI	51-85096	48-ball Mini BGA (7 mm × 7 mm)	Industrial
	CY7C1021BNV33L-15VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021BNV33L-15ZXI	51-85087	44-pin TSOP Type II (Pb-free)	

**Ordering Code Definitions**

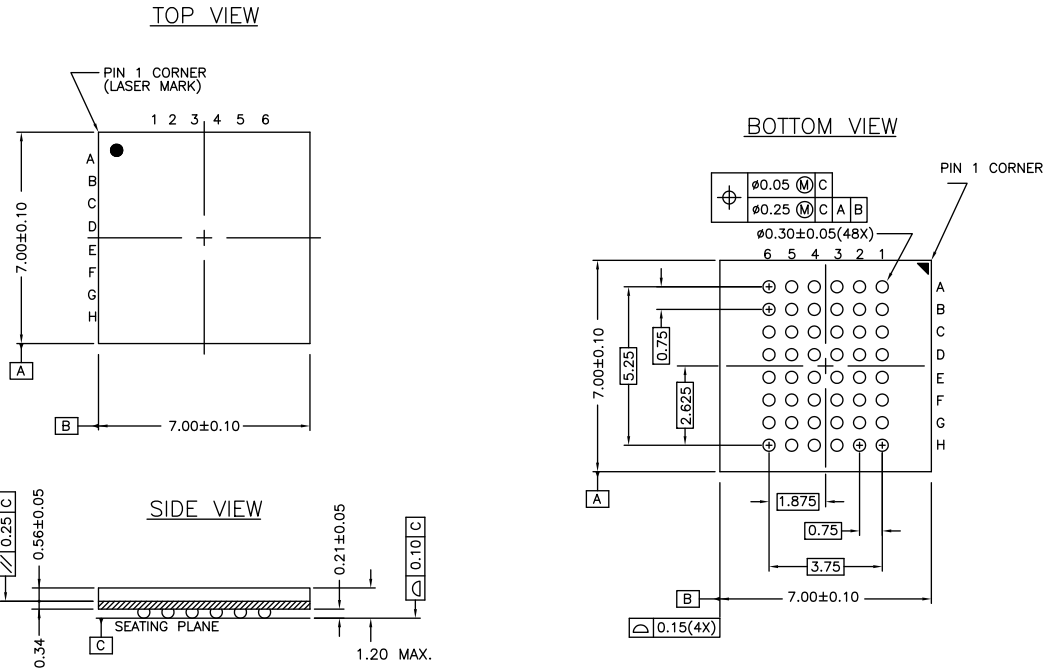
CY 7 C 1 02 1 BN V33 L - 15 XX I



Please contact local sales representative regarding availability of these parts.

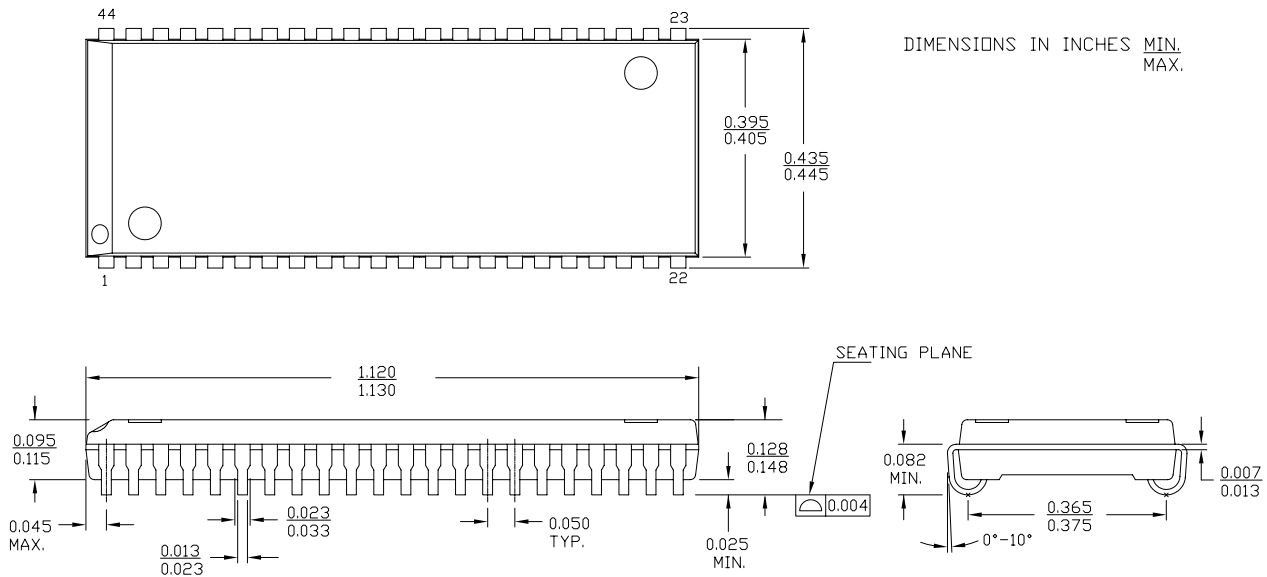
Package Diagrams

Figure 1. 48-ball FBGA (7 mm × 7 mm × 1.2 mm), 51-85096



51-85096 \*1

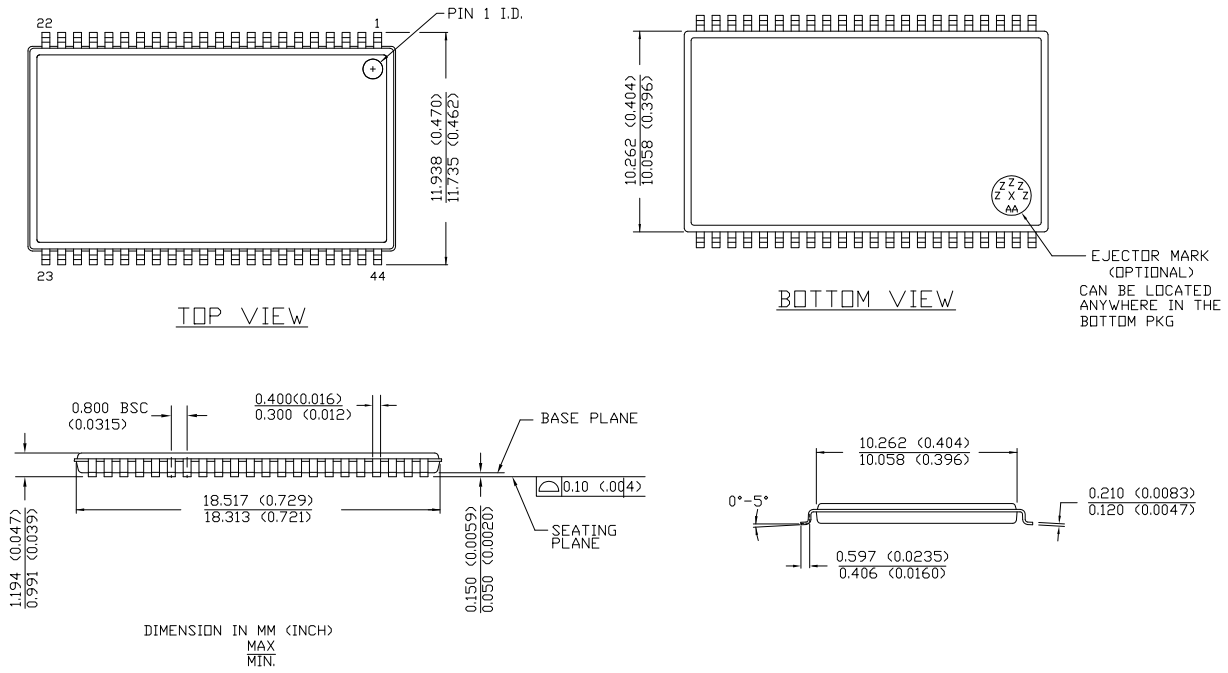
Figure 2. 44-pin (400-Mil) Molded SOJ, 51-85082



51-85082 \*C

Package Diagrams(continued)

Figure 3. 44-pin TSOP Type II, 51-85087



51-85087 °C

### Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
FBGA	Fine-Pitch Ball Grid Array
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
TSOP	thin small-outline package
$\overline{WE}$	write enable

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
$\mu$ s	micro seconds
$\Omega$	ohms
V	Volts
$\mu$ A	micro Amperes
mA	milli Amperes
mm	milli meter
MHz	Mega Hertz
pF	pico Farad
$^{\circ}$ C	degree Celcius
%	percent
mW	milli Watts
W	Watts

## Document History Page

Document Title: CY7C1021BNV33 64 K × 16 Static RAM Document Number: 001-06433				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423847	See ECN	NXR	New Data Sheet
*A	2897061	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*B	3109897	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a>
*C	3103073	03/08/2011	PRAS	Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.



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