128K x 8 Static RAM

Features

- **Pin and function compatible with CY7C1019BV33**
- **High speed**
  - **— t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Data retention at 2.0V**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**
- **Available in Pb-free and non Pb-free 48-ball VFBGA, 32-pin TSOP II and 400-mil SOJ package**

Functional Description

The CY7C1019CV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.
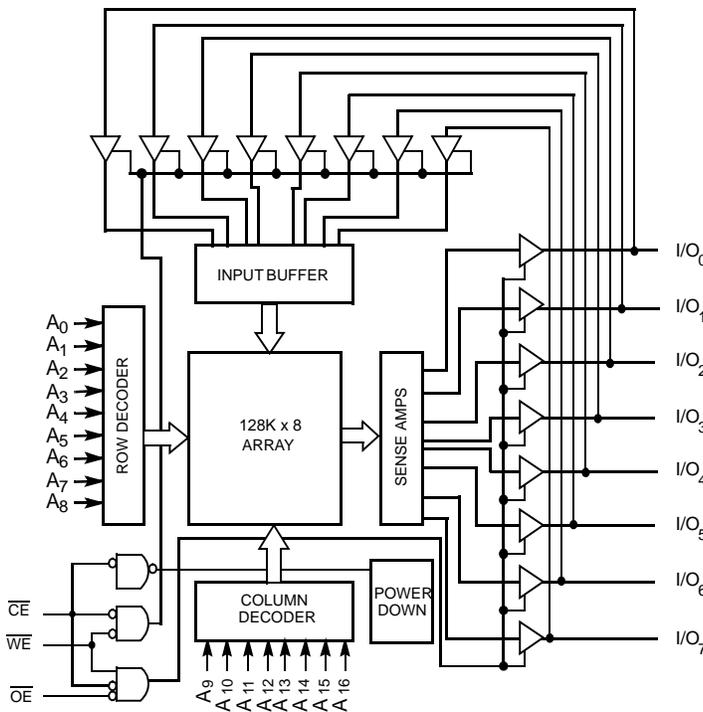
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A$_0$ through A$_{16}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).
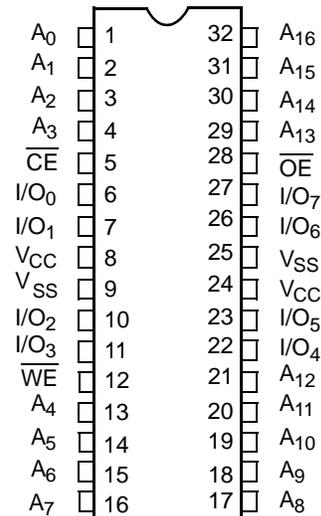
The CY7C1019CV33 is available in Standard 48-ball FBGA, 32-pin TSOP II and 400-mil-wide SOJ packages
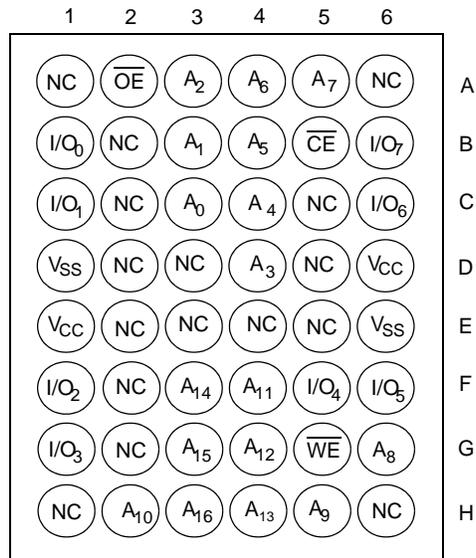
Logic Block Diagram

Pin Configuration

SOJ/TSOP II
Top View

Revised August 3, 2006

Pin Configuration[1]

48-ball VFBGA
(Top View)

	1	2	3	4	5	6	
A	NC	$\overline{OE}$	A_2	A_6	A_7	NC	
B	I/O$_0$	NC	A_1	A_5	$\overline{CE}$	I/O$_7$	
C	I/O$_1$	NC	A_0	A_4	NC	I/O$_6$	
D	V$_{SS}$	NC	NC	A_3	NC	V$_{CC}$	
E	V$_{CC}$	NC	NC	NC	NC	V$_{SS}$	
F	I/O$_2$	NC	A_{14}	A_{11}	I/O$_4$	I/O$_5$	
G	I/O$_3$	NC	A_{15}	A_{12}	$\overline{WE}$	A_8	
H	NC	A_{10}	A_{16}	A_{13}	A_9	NC	

Selection Guide

	-10	-12	-15	Unit
Maximum Access Time	10	12	15	ns
Maximum Operating Current	80	75	70	mA
Maximum Standby Current	5	5	5	mA

Note:
1. NC pins are not connected on the die.

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied...−55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... −0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[2] ....−0.5V to V_{CC} + 0.5V

DC Input Voltage[2]................................−0.5V to V_{CC} + 0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage...>2001V
(per MIL-STD-883, Method 3015)

Latch-up Current..>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V $\pm$ 10%
Industrial	−40°C to +85°C	3.3V $\pm$ 10%

Electrical Characteristics Over the Operating Range
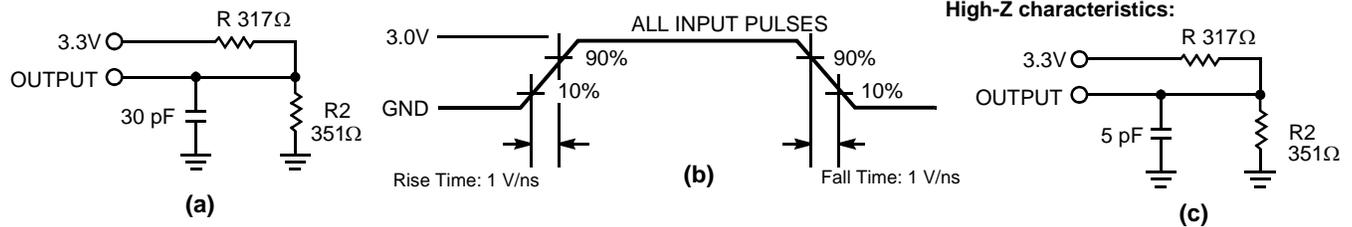
Parameter	Description	Test Conditions	−10 Min.	−10 Max.	−12 Min.	−12 Max.	−15 Min.	−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$	−1	+1	−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled	−1	+1	−1	+1	−1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		80		75		70	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		15		15		15	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq$ 0.3V, f = 0		5		5		5	mA

Capacitance[3]

| Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
2. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]

(a)

(b)

Rise Time: 1 V/ns   Fall Time: 1 V/ns

High-Z characteristics:

(c)

Switching Characteristics Over the Operating Range[5]
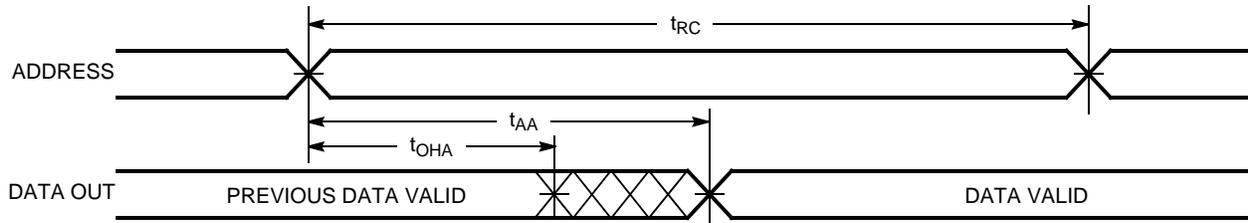
| Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		5		6		7	ns
t_{PU}[8]	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}[8]	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
Write Cycle[9, 10]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t_{AW}	Address Set-Up to Write End	8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		5		6		7	ns
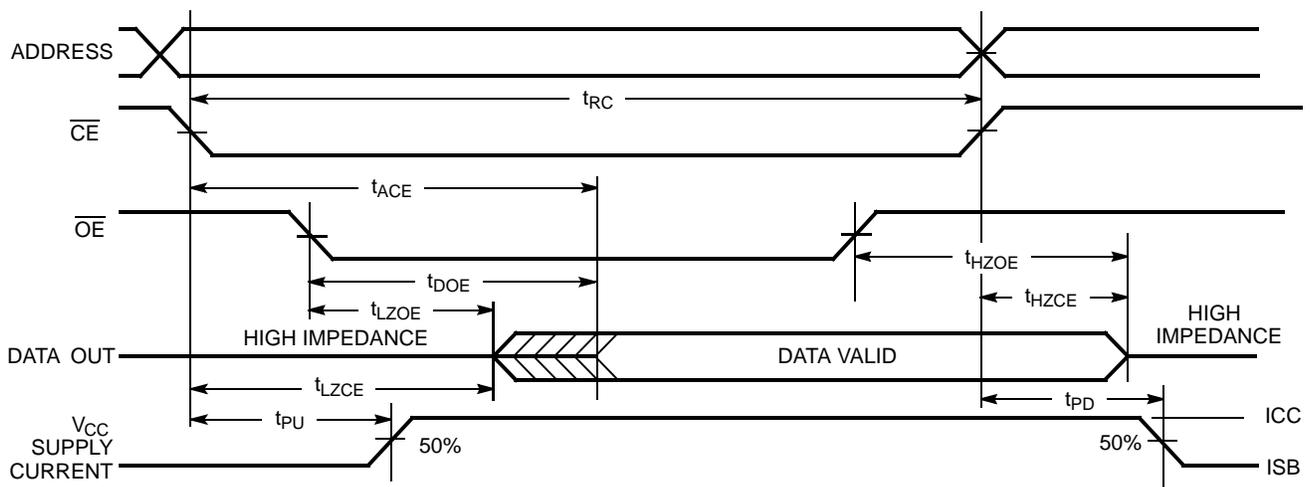
Notes:
4. AC characteristics (except High-Z) for all speeds are tested using the Thevenin load shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. This parameter is guaranteed by design and is not tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

[+] Feedback

Switching Waveforms
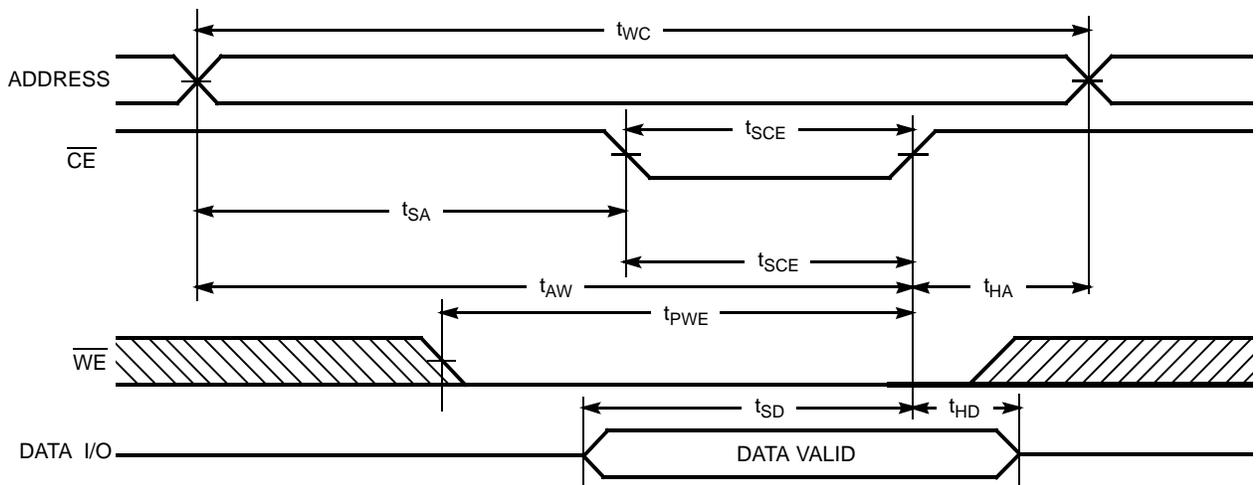
Read Cycle No. 1[11, 12]

Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]

### Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]
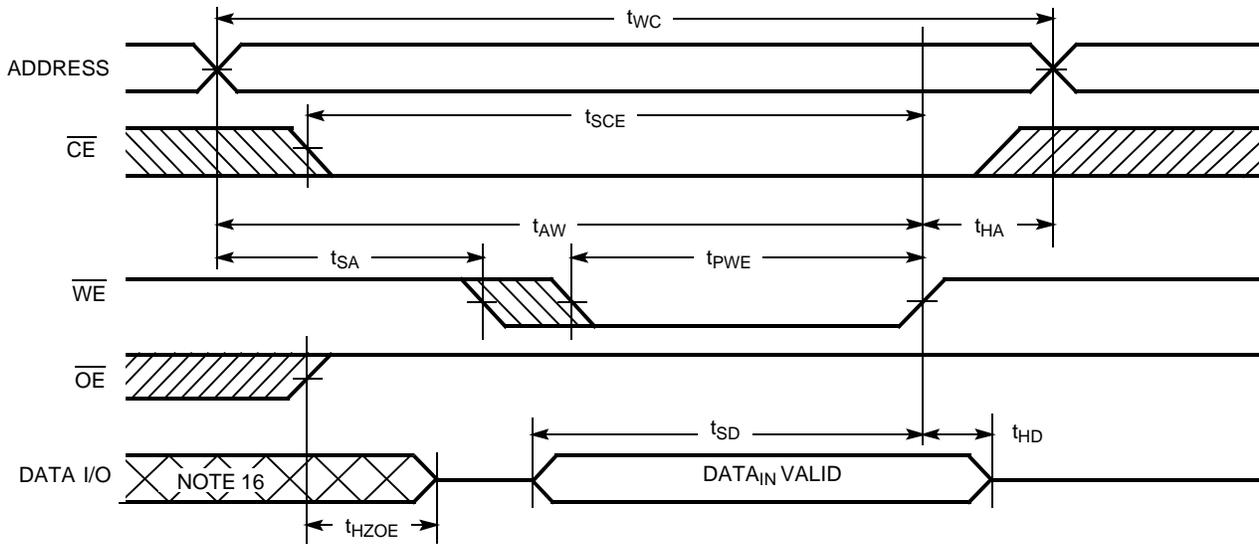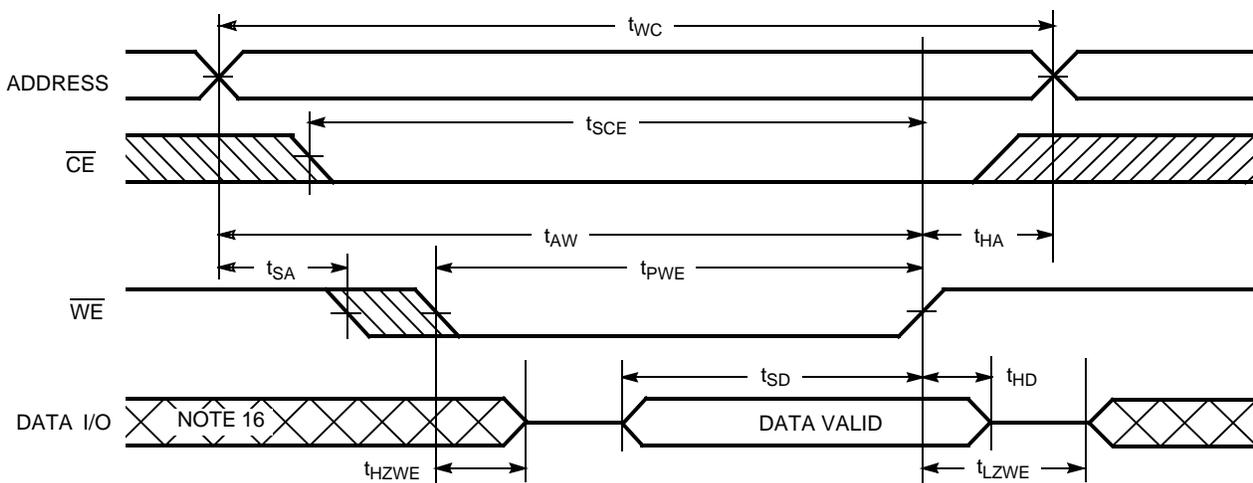
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)[14, 15]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[15]

Truth Table

| $\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O$_0$–I/O$_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})
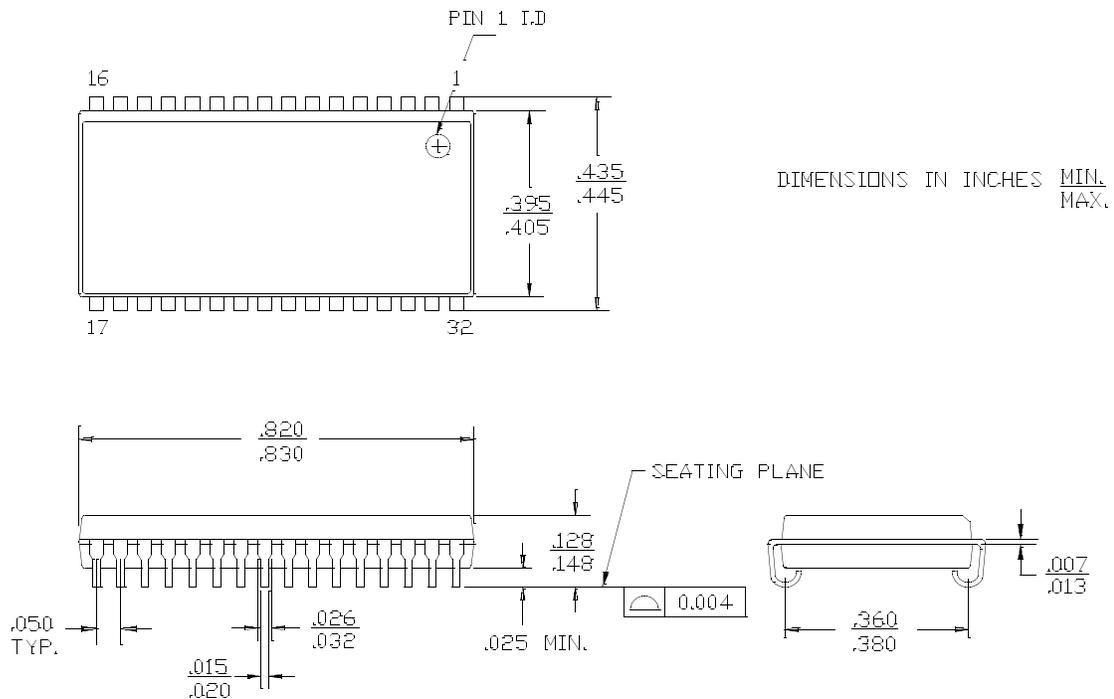
Note:
16. During this period the I/Os are in the output state and input signals should not be applied.

Ordering Information

| Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019CV33-10VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-10ZXC	51-85095	32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-10ZXI		32-pin TSOP II (Pb-Free)	Industrial
12	CY7C1019CV33-12VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-12ZC	51-85095	32-pin TSOP II	
	CY7C1019CV33-12ZXC		32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-12VI	51-85033	32-pin 400-Mil Molded SOJ	Industrial
	CY7C1019CV33-12BVXI	51-85150	48-ball VFBGA (Pb-Free)	
15	CY7C1019CV33-15VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-15VXC	51-85033	32-pin 400-Mil Molded SOJ (Pb-Free)	
	CY7C1019CV33-15ZXC	51-85095	32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-15ZXI	51-85095	32-pin TSOP II (Pb-Free)	Industrial
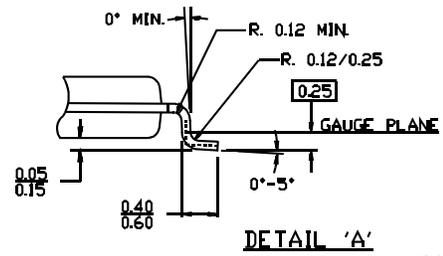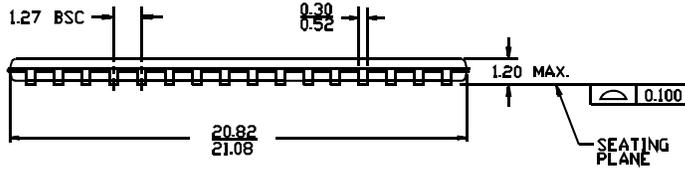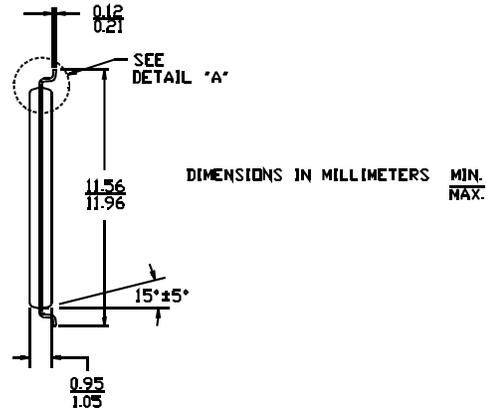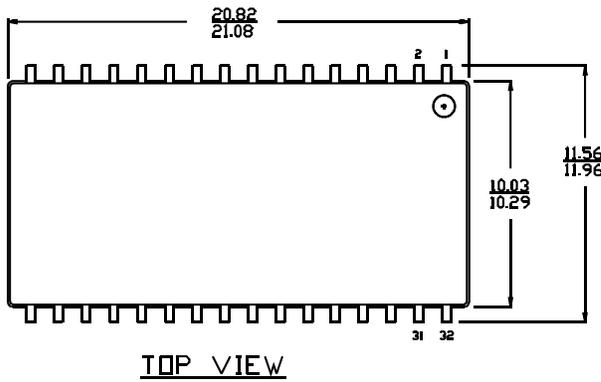
Package Diagrams

32-pin (400-Mil) Molded SOJ (51-85033)

51-85033-*B

[+] Feedback

Package Diagrams (continued)
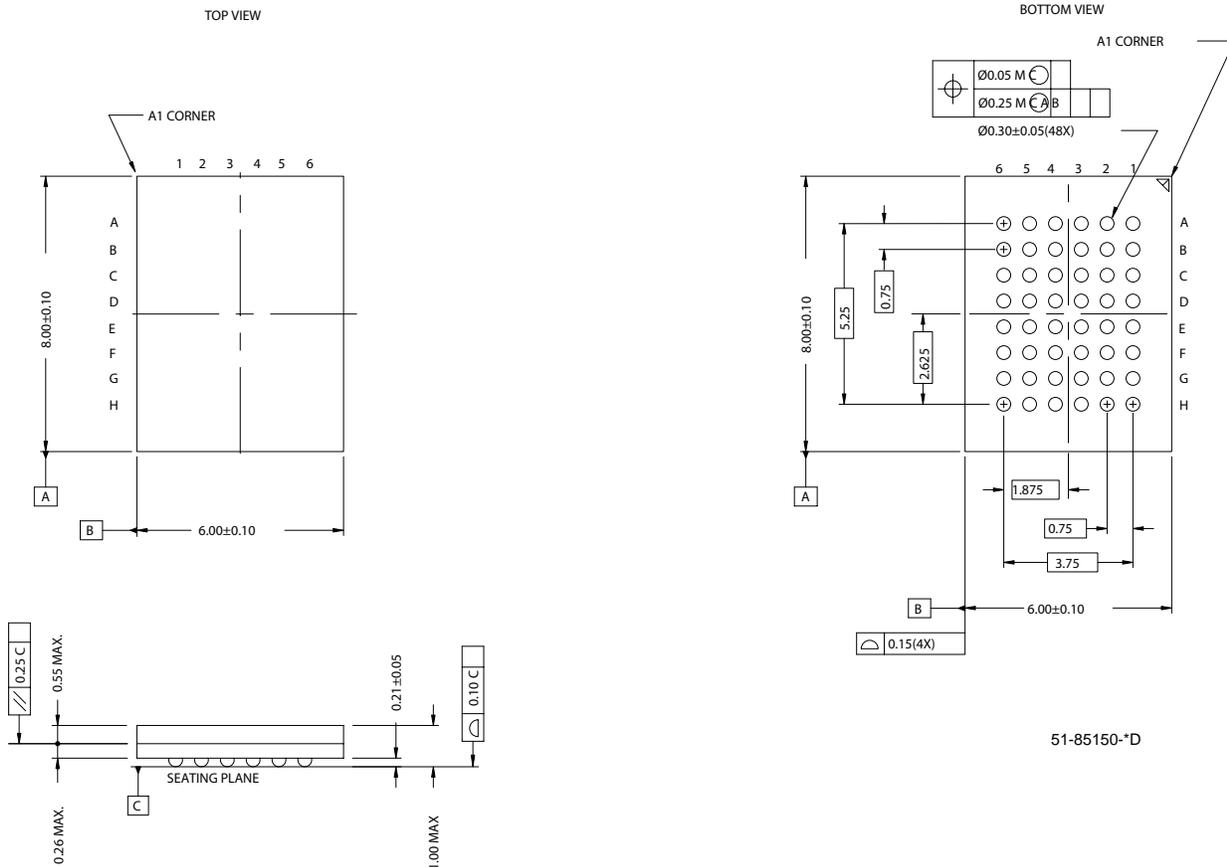
32-pin TSOP II (51-85095)

TOP VIEW

DETAIL 'A'

51-85095-**

Package Diagrams (continued)

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)

TOP VIEW

BOTTOM VIEW

A1 CORNER

A1 CORNER

A1 CORNER

Ø0.05 M C

Ø0.25 M C A B

Ø0.30±0.05(48X)

51-85150-*D

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Document History Page

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109245	12/16/01	HGK	New Data Sheet
*A	113431	04/10/02	NSL	AC Test Loads split based on speed
*B	115047	08/01/02	HGK	Added TSOP II Package and I Temp. Improved I_{CC} limits
*C	119796	10/11/02	DFP	Updated standby current from 5 nA to 5 mA
*D	123030	12/17/02	DFP	Updated Truth Table to reflect single Chip Enable option
*E	419983	See ECN	NXR	Added 48-ball VFBGA Package Added lead-free parts in Ordering Information Table Replaced Package Name column with Package Diagram in the Ordering Information Table
*F	493543	See ECN	NXR	Removed 8 ns speed bin from Product offering Added note #1 on page #2 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information

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Document Number: 38-05130

[+] Feedback