

2-Mbit (128K x 16) Static RAM

Features

- Pin-and function-compatible with CY7C1011CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns (Industrial)}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- Data Retention at 2.0 V
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Lead-Free 44-pin TSOP II, and 48-ball VFBGA

Functional Description

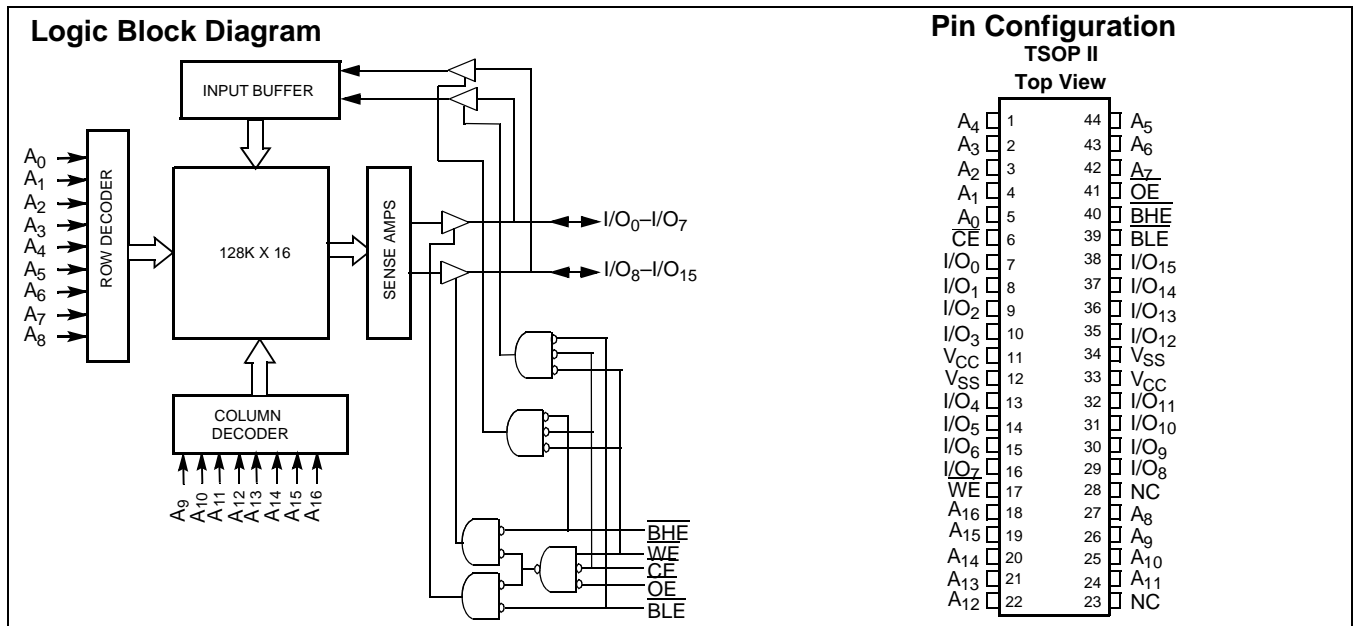
The CY7C1011DV33 is a high-performance CMOS Static RAM organized as 128K words by 16 bits.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1011DV33 is available in standard Lead-Free 44-pin TSOP II with center power and ground pinout, as well as 48-ball fine-pitch ball grid array (VFBGA) packages



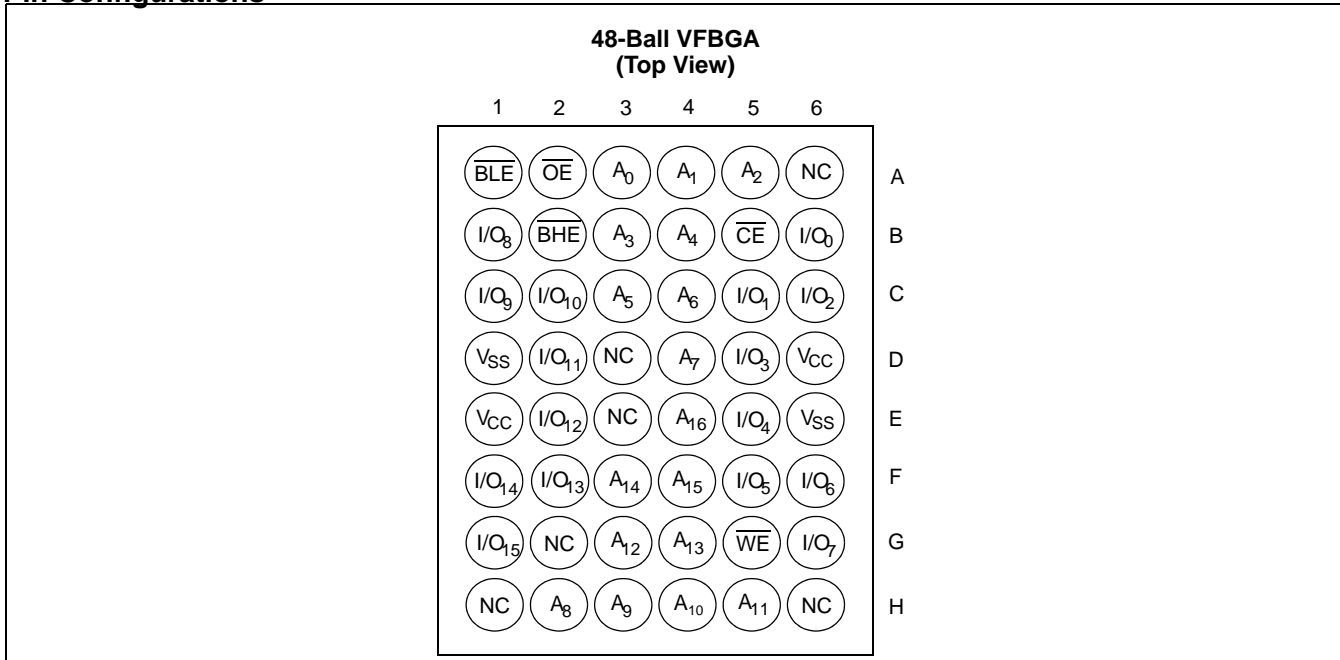
Note

1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com

Selection Guide

| | -10 | Unit |
|------------------------------|------------|-------------|
| Maximum Access Time | 10 | ns |
| Maximum Operating Current | 90 | mA |
| Maximum CMOS Standby Current | 10 | mA |

Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V_{CC} to Relative GND^[3] -0.3V to +4.6V
- DC Voltage Applied to Outputs in High-Z State^[3] -0.3V to V_{CC} +0.3V
- DC Input Voltage^[3]..... -0.3V to V_{CC} +0.3V

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C | 3.3V ± 0.3V |

DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -10 | | Unit |
|------------------|--|---|---------|-----------------------|------|
| | | | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[2] | | -0.3 | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | -1 | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., f = f _{MAX} = 1/t _{RC} | 100 MHz | 90 | mA |
| | | | 83 MHz | 80 | |
| | | | 66 MHz | 70 | |
| | | | 40 MHz | 60 | |
| I _{SB1} | Automatic CE Power-down Current —TTL Inputs | Max. V _{CC} , CE ≥ V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 20 | mA |
| I _{SB2} | Automatic CE Power-down Current —CMOS Inputs | Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | | 10 | mA |

Capacitance^[3]

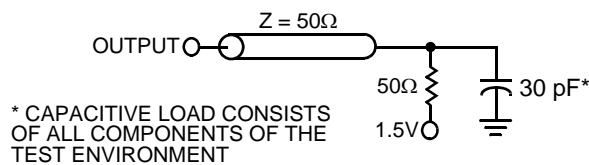
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|-------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | 8 | pF |
| C _{OUT} | I/O Capacitance | | 8 | pF |

Notes

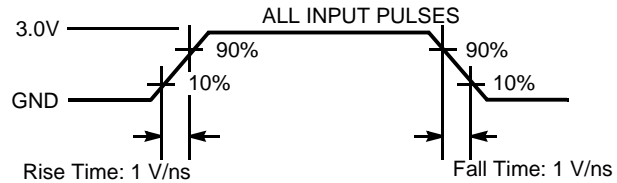
2. V_{IL} (min.) = -2.0V and V_{IH}(max) = V_{CC} +2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance^[3]

| Parameter | Description | Test Conditions | TSOP II | VFBGA | Unit |
|---------------|--|---|---------|-------|----------------------|
| Θ_{JA} | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board | 50.66 | 27.89 | $^{\circ}\text{C/W}$ |
| Θ_{JC} | Thermal Resistance (Junction to Case) | | 17.17 | 14.74 | $^{\circ}\text{C/W}$ |

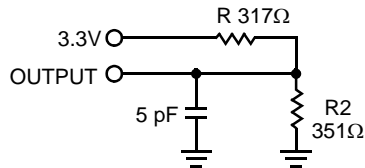
AC Test Loads and Waveforms^[4]


(a)



(b)

High-Z characteristics:



(c)

AC Switching Characteristics Over the Operating Range^[5]

| Parameter | Description | -10 | | Unit |
|--------------------------|--|------|------|---------------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| $t_{\text{power}}^{[6]}$ | V_{CC} (typical) to the first access | 100 | | μs |
| t_{RC} | Read Cycle Time | 10 | | ns |
| t_{AA} | Address to Data Valid | | 10 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 10 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 5 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[7, 8] | | 5 | ns |
| t_{LZCE} | \overline{CE} LOW to Low-Z ^[8] | 3 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High-Z ^[7, 8] | | 5 | ns |
| t_{PU} | \overline{CE} LOW to Power-up | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power-down | | 10 | ns |

Notes

- AC characteristics (except High-Z) are tested using the load conditions shown in (a). High-Z characteristics are tested for all speeds using the test load shown in (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
- t_{HZOE} , t_{HZCE} , t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE} , and t_{HZWE} is less than t_{LZWE} for any given device.

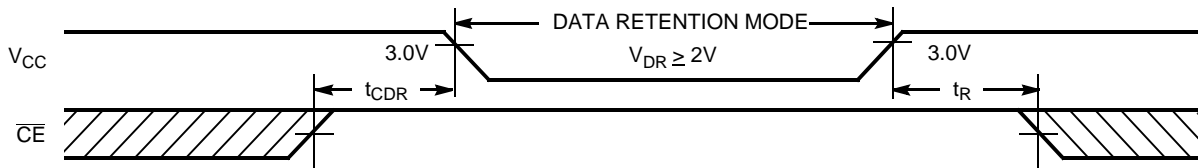
AC Switching Characteristics Over the Operating Range^[5] (continued)

| Parameter | Description | -10 | | Unit |
|--------------------------------------|---|------|------|------|
| | | Min. | Max. | |
| t _{DBE} | Byte Enable to Data Valid | | 5 | ns |
| t _{LZBE} | Byte Enable to Low-Z | 0 | | ns |
| t _{HZBE} | Byte Disable to High-Z | | 6 | ns |
| Write Cycle^[9, 10] | | | | |
| t _{WC} | Write Cycle Time | 10 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 7 | | ns |
| t _{AW} | Address Set-up to Write End | 7 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | ns |
| t _{SA} | Address Set-up to Write Start | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 7 | | ns |
| t _{SD} | Data Set-up to Write End | 5 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low-Z ^[8] | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High-Z ^[7, 8] | | 5 | ns |
| t _{BW} | Byte Enable to End of Write | 7 | | ns |

Data Retention Characteristics Over the Operating Range

| Parameter | Description | Conditions ^[12] | Min. | Max. | Unit |
|---------------------------------|--------------------------------------|--|-----------------|------|------|
| V _{DR} | V _{CC} for Data Retention | | 2.0 | | V |
| I _{CCDR} | Data Retention Current | | | 10 | mA |
| t _{CDR} ^[3] | Chip Deselect to Data Retention Time | V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | 0 | | ns |
| t _R ^[13] | Operation Recovery Time | | t _{RC} | | ns |

Data Retention Waveform

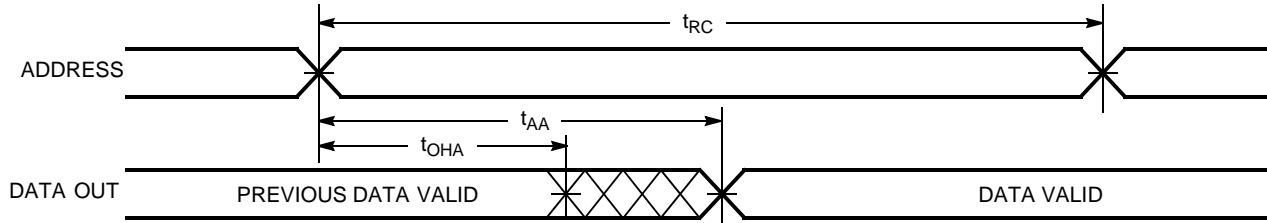


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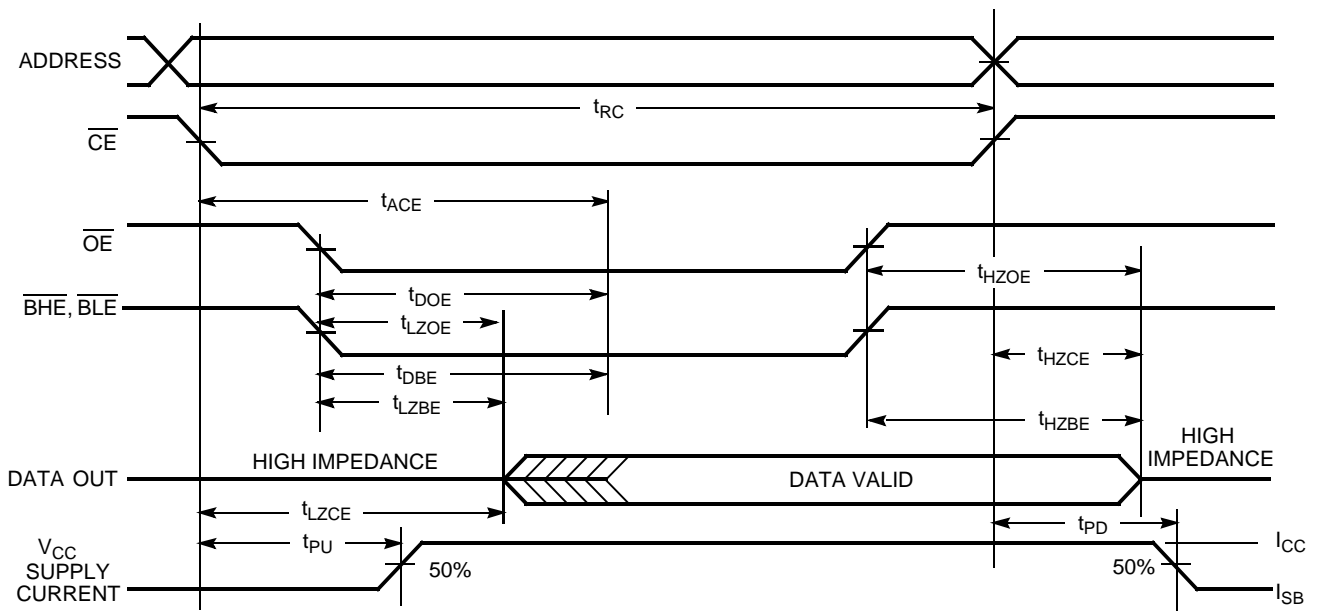
9. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 4 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.
11. Device is continuously selected. OE, CE, BHE and/or BHE = V_{IL}.
12. No input may exceed V_{CC} + 0.3V.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 50 μs or stable at V_{CC(min.)} ≥ 50 μs

Switching Waveforms

Read Cycle No. 1^[11, 14]



Read Cycle No. 2(OE Controlled)^[14, 15]

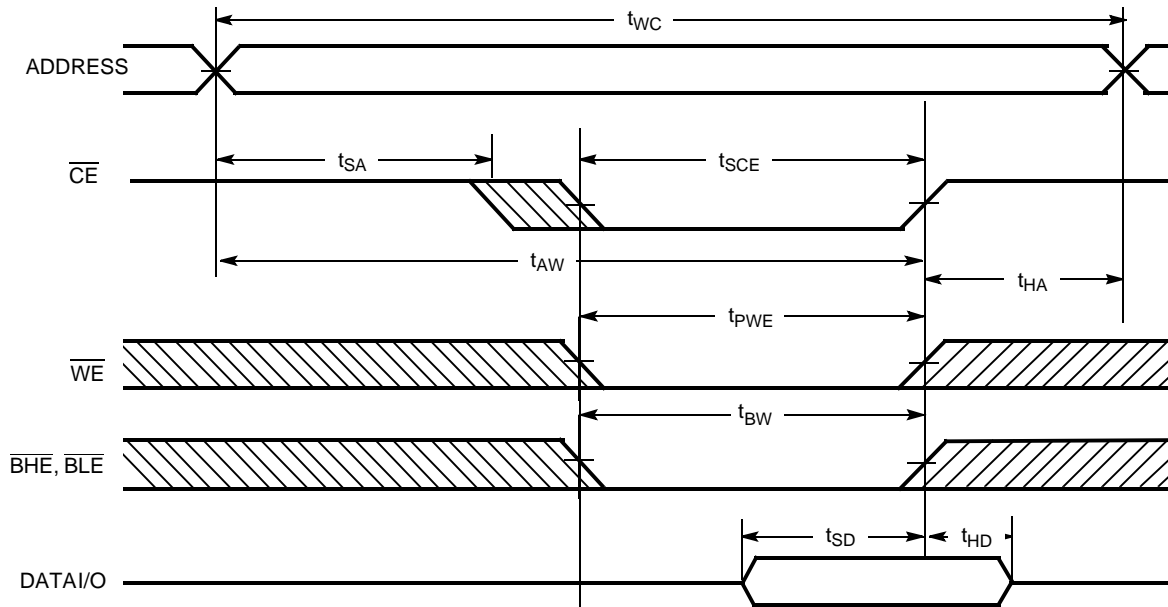


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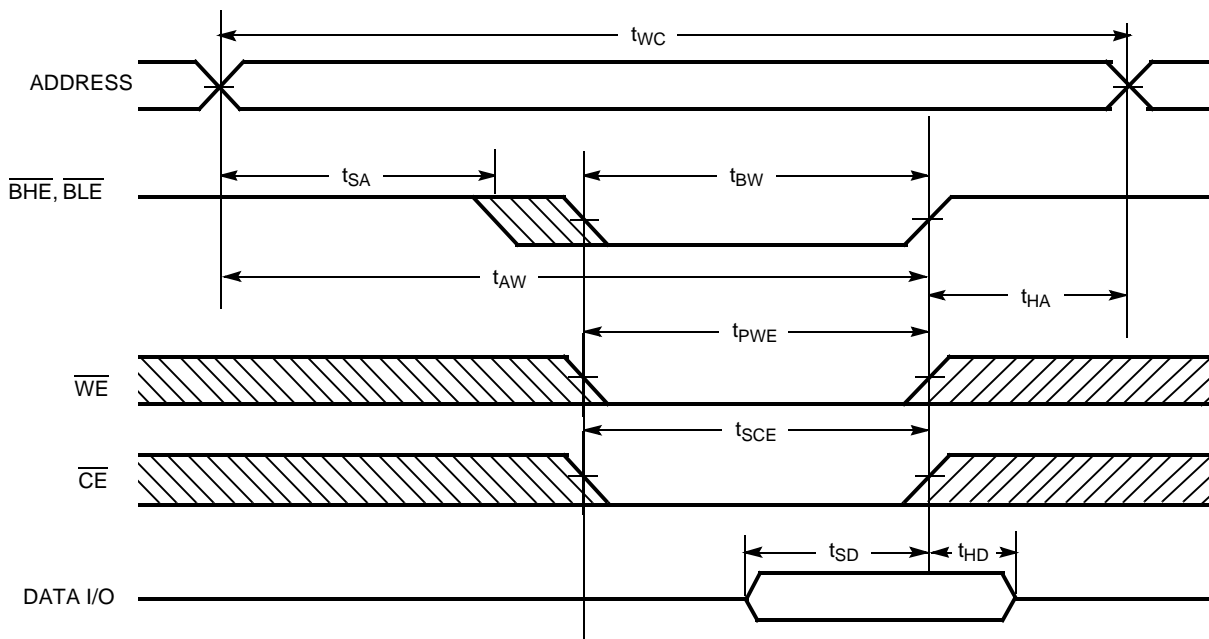
- 14. WE is HIGH for read cycle.
- 15. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[16, 17]



Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

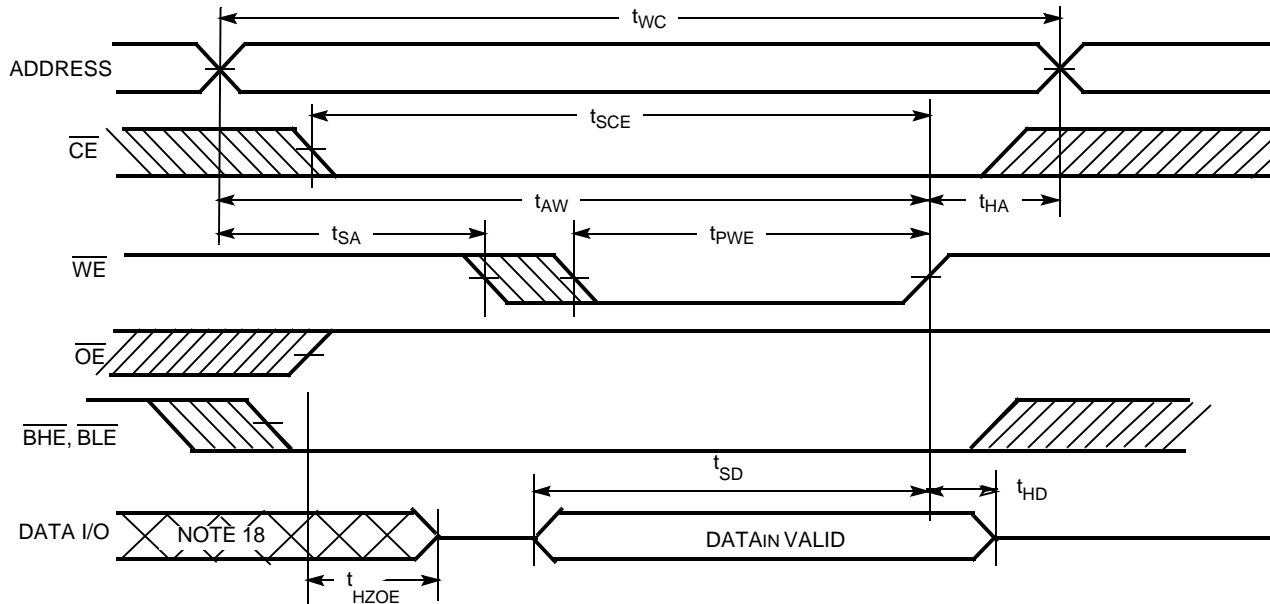


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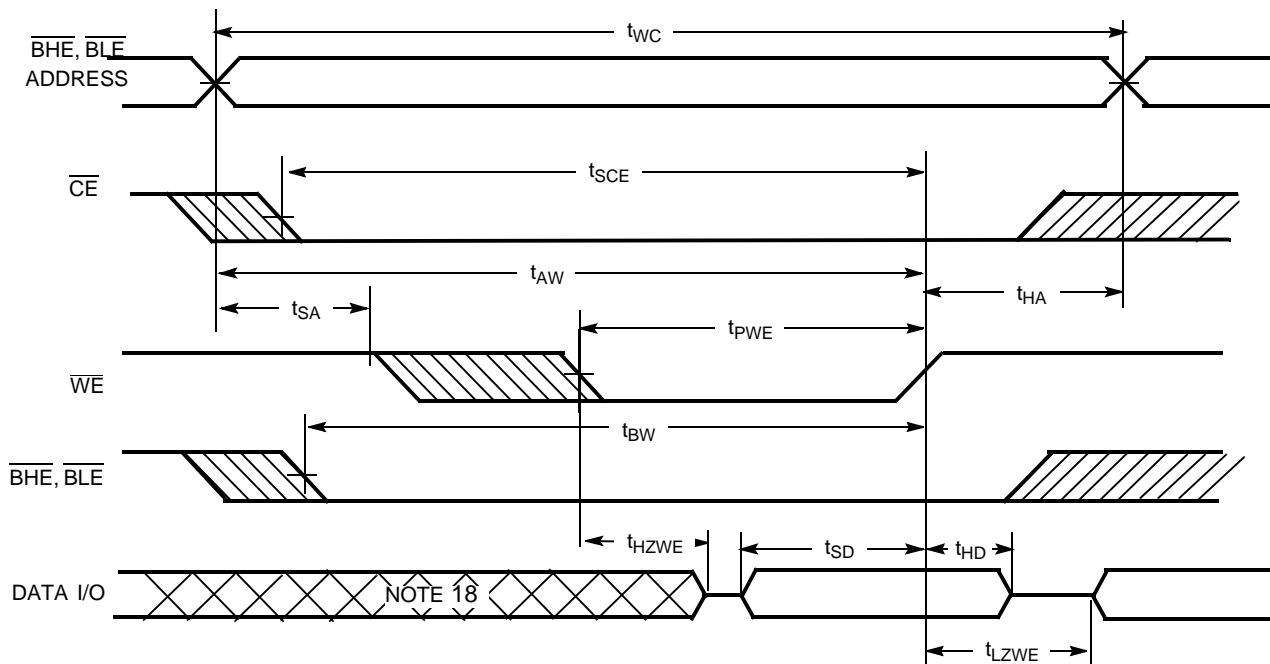
- 16. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[16, 17]



Write Cycle No. 4 (\overline{WE} Controlled, \overline{OE} LOW)



Note
18. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

| CE | OE | WE | BLE | BHE | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|----|----|----|-----|-----|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X | X | X | X | High-Z | High-Z | Power-down | Standby (I _{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read All Bits | Active (I _{CC}) |
| L | L | H | L | H | Data Out | High-Z | Read Lower Bits Only | Active (I _{CC}) |
| L | L | H | H | L | High-Z | Data Out | Read Upper Bits Only | Active (I _{CC}) |
| L | X | L | L | L | Data In | Data In | Write All Bits | Active (I _{CC}) |
| L | X | L | L | H | Data In | High-Z | Write Lower Bits Only | Active (I _{CC}) |
| L | X | L | H | L | High-Z | Data In | Write Upper Bits Only | Active (I _{CC}) |
| L | H | H | X | X | High-Z | High-Z | Selected, Outputs Disabled | Active (I _{CC}) |

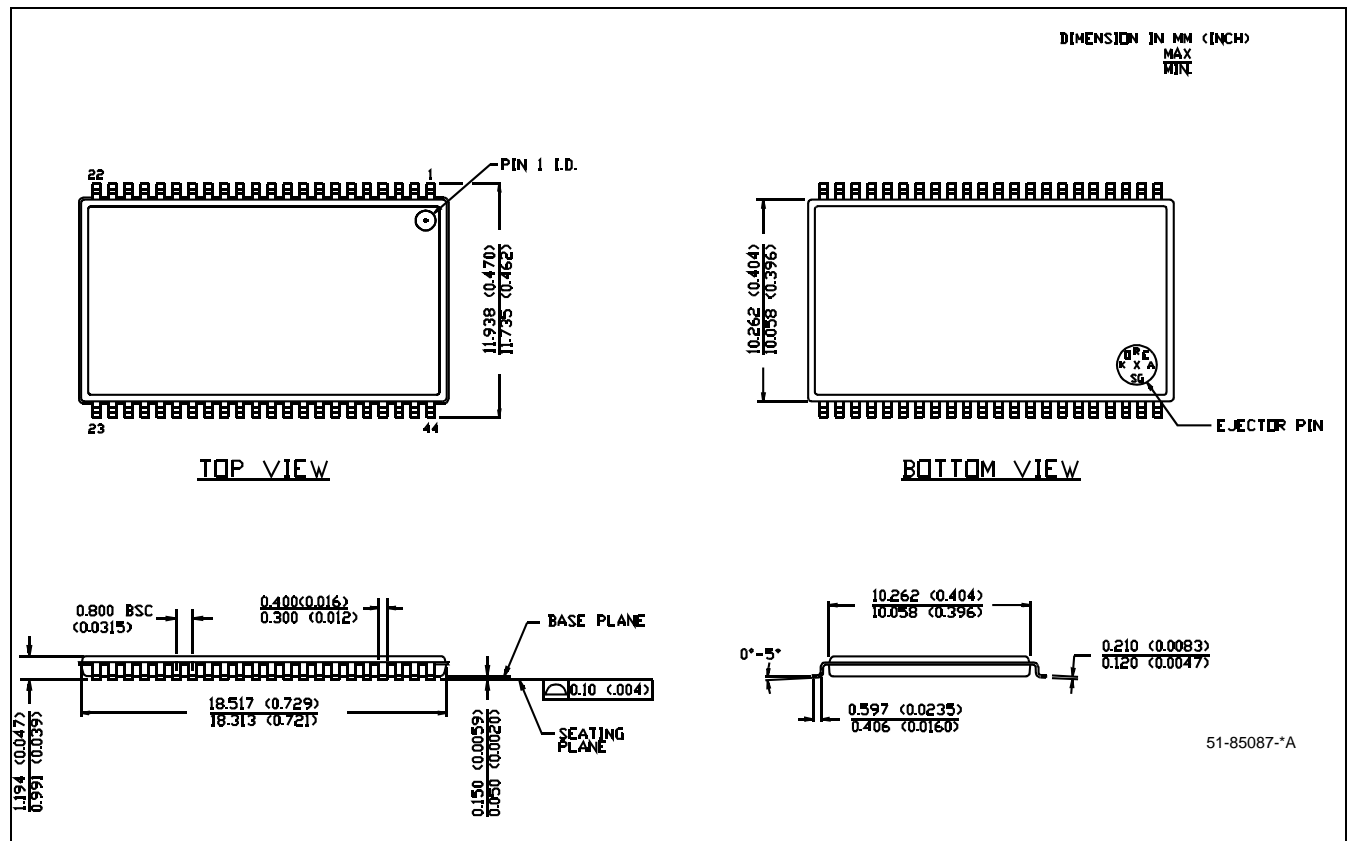
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|-----------------|--------------------------|-----------------|
| 10 | CY7C1011DV33-10ZSXI | 51-85087 | 44-pin TSOP II (Pb-Free) | Industrial |
| | CY7C1011DV33-10BVI | 51-85150 | 48-ball VFBGA | |
| | CY7C1011DV33-10BVXI | | 48-ball VFBGA (Pb-Free) | |

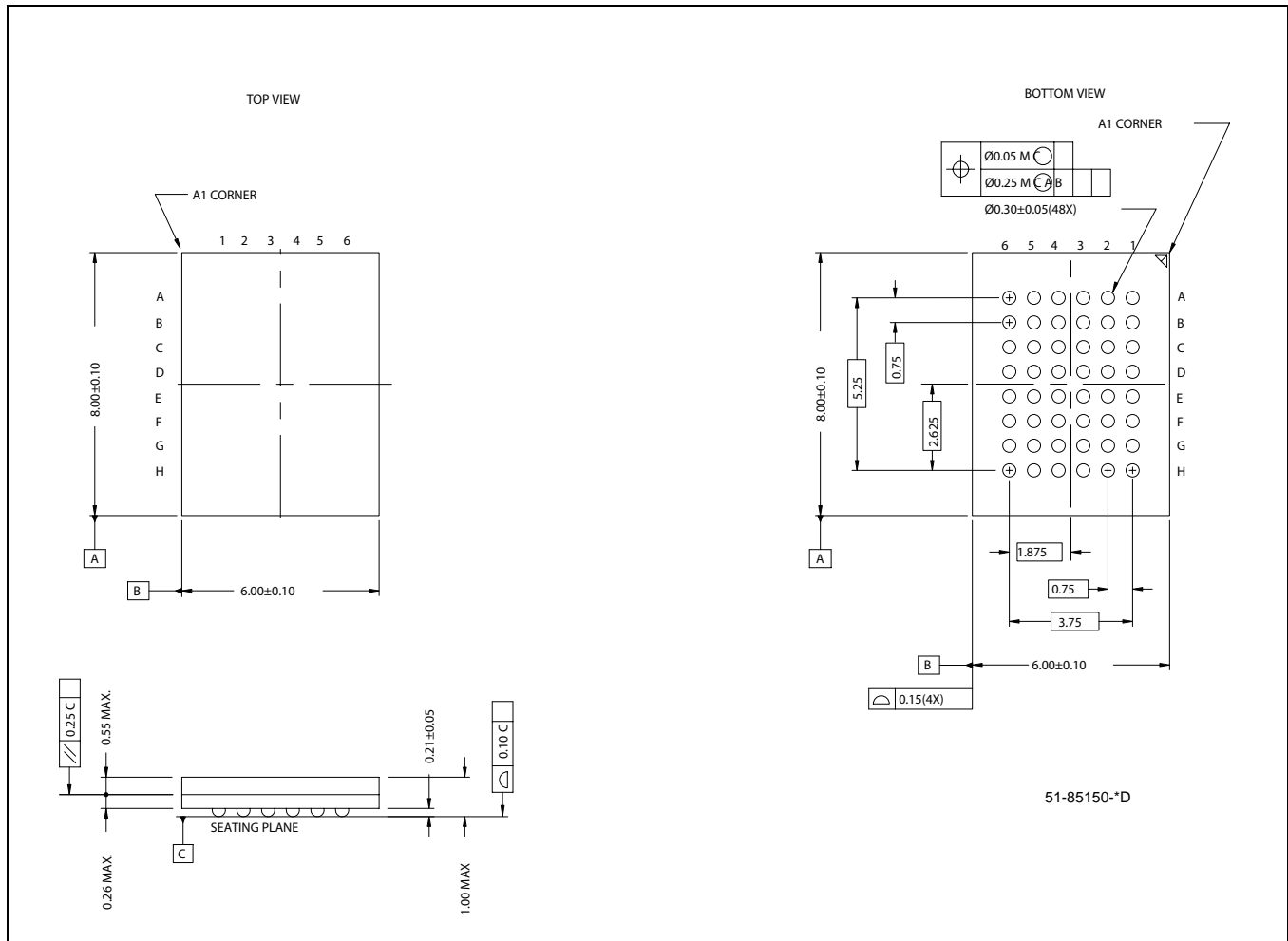
Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 1. 44-Pin TSOP II (51-85087)



Package Diagrams (continued)
 Figure 2. 48-Ball VFBGA (6 x 8 x 1 mm) (51-85150)



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Document History

| Document Title: CY7C1011DV33 2-Mbit (128K x 16)Static RAM | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-05609 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 250650 | See ECN | RKF | New Data Sheet |
| *A | 399070 | See ECN | NXR | <p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed TQFP Package from product offering</p> <p>Removed -15 speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from -0.5 to -0.3V and $V_{CC} +0.5V$ to $V_{CC} +0.3V$</p> <p>Redefined I_{CC} values for Com'l and Ind'l temperature ranges</p> <p>I_{CC} (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively</p> <p>I_{CC} (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12ns speed bins respectively</p> <p>Modified Note# 4 on AC Test Loads</p> <p>Added Static Discharge Voltage and latch-up current spec</p> <p>Added $V_{IH(max)}$ spec in Note# 2</p> <p>Changed reference voltage level for measurement of Hi-Z parameters from ± 500 mV to ± 200 mV</p> <p>Added Data Retention Characteristics Table and footnote on t_R</p> <p>Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram</p> <p>Changed package name for 44-pin TSOP II from Z to ZS</p> <p>Added 8 ns parts in the Ordering Information table</p> <p>Shaded Ordering Information Table</p> |
| *B | 459073 | See ECN | NXR | <p>Converted Preliminary to Final.</p> <p>Removed -8 and -12 Speed bins</p> <p>Removed Commercial Operating Range from product offering.</p> <p>Changed the description of I_{IX} from "Input Load Current" to "Input Leakage Current"</p> <p>Updated the Thermal Resistance table.</p> <p>Changed t_{HZBE} from 5 ns to 6 ns.</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #12.</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p> |
| *C | 480177 | See ECN | VKN | Added -10BVI product ordering code in the Ordering Information table. |