

## Features

- Thin small outline package (TSOP) I package configurable as 512 K × 16 or 1 M × 8 static RAM (SRAM)
- High speed: 45 ns
- Temperature ranges
  - Industrial: -40 °C to +85 °C
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62157DV30
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA (Industrial)
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA), Pb-free 44-pin TSOP II and 48-pin TSOP I packages

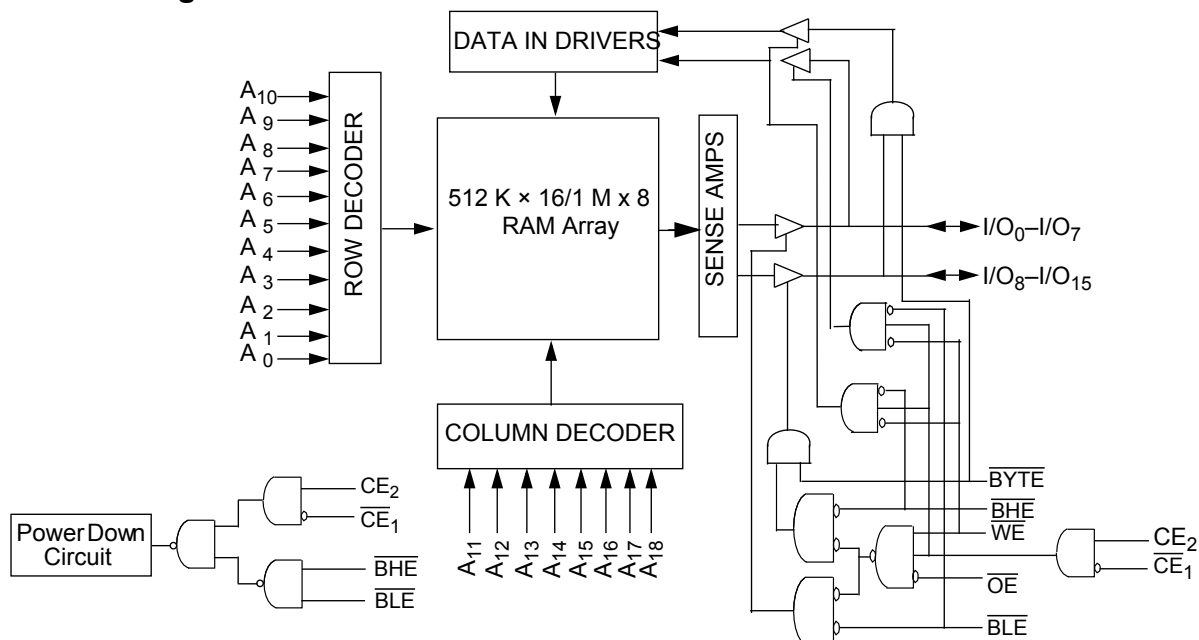
## Functional Description

The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input or output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or a write operation is active ( $CE_1$  LOW,  $CE_2$  HIGH and  $WE$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See Truth Table on page 13 for a complete description of read and write modes.

## Logic Block Diagram



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## Pin Configuration

Figure 1. 48-ball VFBGA (Top View) [1]

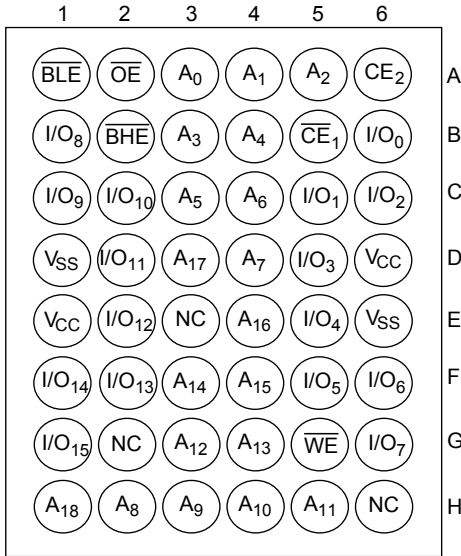


Figure 2. 44-pin TSOP II (Top View) [2]

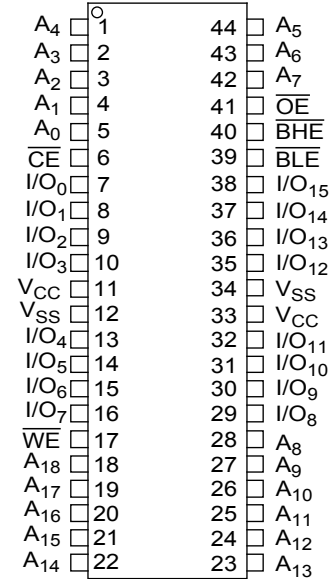


Figure 3. 48-pin TSOP I (512 K × 16/1 M × 8) (Top View) [1, 3]



## Product Portfolio

| Product       | Range              | V <sub>CC</sub> Range (V) |                    |                      | Speed (ns)         | Power Dissipation              |                    |     |    |                                |    |
|---------------|--------------------|---------------------------|--------------------|----------------------|--------------------|--------------------------------|--------------------|-----|----|--------------------------------|----|
|               |                    |                           |                    |                      |                    | Operating I <sub>CC</sub> (mA) |                    |     |    | Standby, I <sub>SB2</sub> (μA) |    |
|               |                    | f = 1 MHz                 |                    | f = f <sub>max</sub> |                    |                                |                    |     |    |                                |    |
| Min           | Typ <sup>[4]</sup> | Max                       | Typ <sup>[4]</sup> | Max                  | Typ <sup>[4]</sup> | Max                            | Typ <sup>[4]</sup> | Max |    |                                |    |
| CY62157EV30LL | Industrial/Auto-A  | 2.2                       | 3.0                | 3.6                  | 45                 | 1.8                            | 3                  | 18  | 25 | 2                              | 8  |
|               | Auto-E             | 2.2                       | 3.0                | 3.6                  | 55                 | 1.8                            | 4                  | 18  | 35 | 2                              | 30 |

### Notes

- NC pins are not connected on the die.
- The 44-pin TSOP II package has only one chip enable ( $\overline{CE}$ ) pin.
- The  $\overline{BYTE}$  pin in the 48-pin TSOP I package must be tied HIGH to use the device as a 512 K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1 M × 8 SRAM by tying the  $\overline{BYTE}$  signal LOW. In the 1 M × 8 configuration, Pin 45 is A19, while BHE, BLE and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used (NC).
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

|   |  |
|---|--|
| Storage Temperature .....   | -65 °C to + 150 °C                     |
| Ambient Temperature with Power Applied .....                          | -55 °C to + 125 °C                     |
| Supply Voltage to Ground Potential .....                              | -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$ V) |
| DC Voltage Applied to Outputs in High Z State <sup>[5, 6]</sup> ..... | -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$ V) |
| DC Input Voltage <sup>[5, 6]</sup> .....                              | -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$ V) |

|   |          |
|---|----------|
| Output Current into Outputs (LOW) .....                   | 20 mA    |
| Static Discharge Voltage (MIL-STD-883, Method 3015) ..... | > 2001 V |
| Latch Up Current .....                                    | > 200 mA |

## Operating Range

| Device        | Range              | Ambient Temperature | V <sub>CC</sub> <sup>[7]</sup> |
|---------------|--------------------|---------------------|--------------------------------|
| CY62157EV30LL | Industrial/ Auto-A | -40 °C to +85 °C    | 2.2 V to 3.6 V                 |
|               | Auto-E             | -40 °C to +125 °C   |                                |

## Electrical Characteristics

Over the Operating Range

| Parameter                       | Description                                   | Test Conditions  | 45 ns (Industrial/ Auto-A) |                    |                       | 55 ns (Auto-E) |                    |                       | Unit |
|---------------------------------|---|--|----------------------------|--------------------|-----------------------|----------------|--------------------|-----------------------|------|
|                                 |   |  | Min                        | Typ <sup>[8]</sup> | Max                   | Min            | Typ <sup>[8]</sup> | Max                   |      |
| V <sub>OH</sub>                 | Output HIGH voltage                           | I <sub>OH</sub> = -0.1 mA  | 2.0                        | -                  | -                     | 2.0            | -                  | -                     | V    |
|                                 |   | I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70 V  | 2.4                        | -                  | -                     | 2.4            | -                  | -                     | V    |
| V <sub>OL</sub>                 | Output LOW voltage                            | I <sub>OL</sub> = 0.1 mA   | -                          | -                  | 0.4                   | -              | -                  | 0.4                   | V    |
|                                 |   | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70 V   | -                          | -                  | 0.4                   | -              | -                  | 0.4                   | V    |
| V <sub>IH</sub>                 | Input HIGH voltage                            | V <sub>CC</sub> = 2.2 V to 2.7 V   | 1.8                        | -                  | V <sub>CC</sub> + 0.3 | 1.8            | -                  | V <sub>CC</sub> + 0.3 | V    |
|                                 |   | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2.2                        | -                  | V <sub>CC</sub> + 0.3 | 2.2            | -                  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>                 | Input LOW voltage                             | V <sub>CC</sub> = 2.2 V to 2.7 V   | -0.3                       | -                  | 0.6                   | -0.3           | -                  | 0.6                   | V    |
|                                 |   | V <sub>CC</sub> = 2.7 V to 3.6 V   | -0.3                       | -                  | 0.8                   | -0.3           | -                  | 0.8                   | V    |
| I <sub>IX</sub>                 | Input leakage current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -1                         | -                  | +1                    | -4             | -                  | +4                    | μA   |
| I <sub>OZ</sub>                 | Output leakage current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -1                         | -                  | +1                    | -4             | -                  | +4                    | μA   |
| I <sub>CC</sub>                 | V <sub>CC</sub> operating supply current      | f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CCmax</sub>  | -                          | 18                 | 25                    | -              | 18                 | 35                    | mA   |
|                                 |   | f = 1 MHz    I <sub>OUT</sub> = 0 mA<br>CMOS levels  | -                          | 1.8                | 3                     | -              | 1.8                | 4                     |      |
| I <sub>SB1</sub> <sup>[9]</sup> | Automatic CE power down current — CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE and WE), V <sub>CC</sub> = 3.60 V | -                          | 2                  | 8                     | -              | 2                  | 30                    | μA   |
| I <sub>SB2</sub> <sup>[9]</sup> | Automatic CE power down current — CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = 3.60 V   | -                          | 2                  | 8                     | -              | 2                  | 30                    | μA   |

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Chip enables (CE<sub>1</sub> and CE<sub>2</sub>), byte enables (BHE and BLE) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the I<sub>SB1</sub>/I<sub>SB2</sub>/I<sub>CCDR</sub> spec. Other inputs can be left floating.

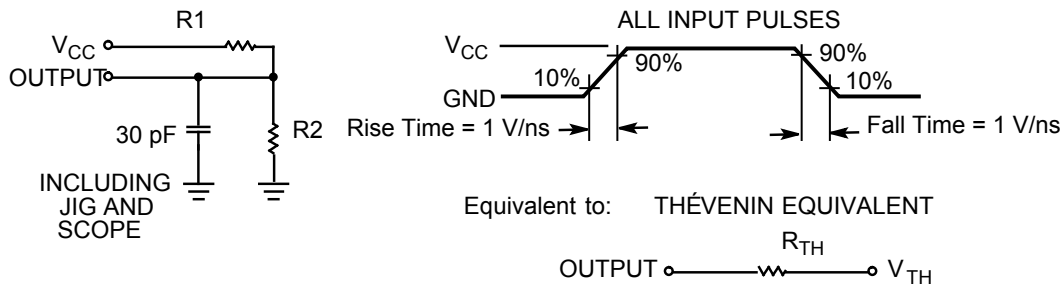
### Capacitance

| Parameter <sup>[10]</sup> | Description        | Test Conditions   | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C <sub>IN</sub>           | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 10  | pF   |
| C <sub>OUT</sub>          | Output capacitance |   | 10  | pF   |

### Thermal Resistance

| Parameter <sup>[10]</sup> | Description                              | Test Conditions  | 48-ball BGA | 44-pin TSOP I | 44-pin TSOP II | Unit |
|---------------------------|--|--|-------------|---------------|----------------|------|
| Θ <sub>JA</sub>           | Thermal resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 72          | 74.88         | 76.88          | °C/W |
| Θ <sub>JC</sub>           | Thermal resistance (Junction to Case)    |  | 8.86        | 8.6           | 13.52          | °C/W |

Figure 4. AC Test Loads and Waveforms



| Parameters      | 2.5 V | 3.0 V | Unit |
|-----------------|-------|-------|------|
| R1              | 16667 | 1103  | Ω    |
| R2              | 15385 | 1554  | Ω    |
| R <sub>TH</sub> | 8000  | 645   | Ω    |
| V <sub>TH</sub> | 1.20  | 1.75  | V    |

**Note**

10. Tested initially and after any design or process changes that may affect these parameters.

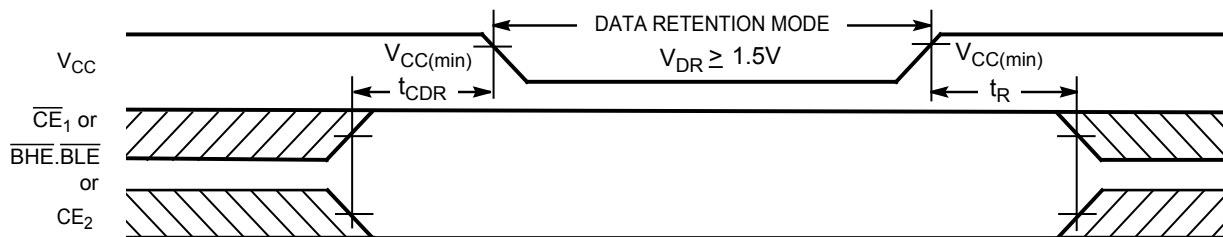
## Data Retention Characteristics

Over the Operating Range

| Parameter                  | Description                          | Conditions  | Min | Typ <sup>[11]</sup> | Max | Unit          |
|----------------------------|--------------------------------------|---|-----|---------------------|-----|---------------|
| $V_{DR}$                   | $V_{CC}$ for data retention          |   | 1.5 | –                   | –   | V             |
| $I_{CCDR}$ <sup>[12]</sup> | Data retention current               | $V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ ,<br>$CE_2 \leq 0.2\text{ V}$ ,<br>( $\overline{BHE}$ and $\overline{BLE}$ ) $\geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ |     |                     |     |               |
|                            |                                      | Industrial/Auto-A   | –   | 2                   | 5   | $\mu\text{A}$ |
|                            |                                      | Auto-E  | –   | –                   | 30  |               |
| $t_{CDR}$ <sup>[13]</sup>  | Chip deselect to data retention time |   | 0   | –                   | –   | ns            |
| $t_R$ <sup>[14]</sup>      | Operation recovery time              |   |     |                     |     |               |
|                            |                                      | CY62157EV30LL-45  | 45  | –                   | –   | ns            |
|                            |                                      | CY62157EV30LL-55  | 55  | –                   | –   |               |

## Data Retention Waveform

Figure 5. Data Retention Waveform <sup>[15]</sup>



### Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
12. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
15.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

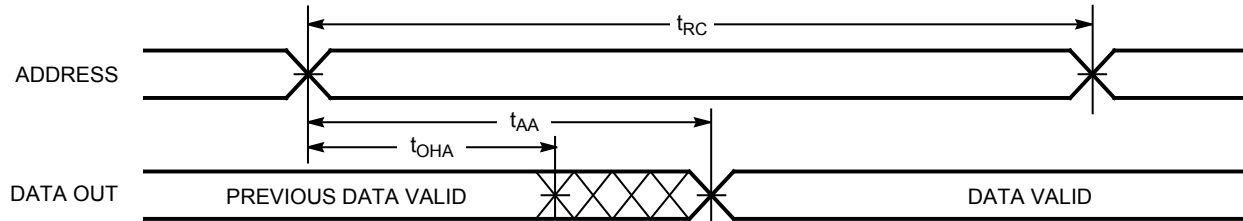
| Parameter <sup>[16, 17]</sup>     | Description   | 45 ns (Industrial/<br>Auto-A) |     | 55 ns (Auto-E) |     | Unit |
|-----------------------------------|---|-------------------------------|-----|----------------|-----|------|
|                                   |   | Min                           | Max | Min            | Max |      |
| <b>Read Cycle</b>                 |   |                               |     |                |     |      |
| $t_{RC}$                          | Read cycle time   | 45                            | –   | 55             | –   | ns   |
| $t_{AA}$                          | Address to data valid   | –                             | 45  | –              | 55  | ns   |
| $t_{OHA}$                         | Data hold from address change                                       | 10                            | –   | 10             | –   | ns   |
| $t_{ACE}$                         | $\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid                 | –                             | 45  | –              | 55  | ns   |
| $t_{DOE}$                         | $\overline{OE}$ LOW to data valid                                   | –                             | 22  | –              | 25  | ns   |
| $t_{LZOE}$                        | $\overline{OE}$ LOW to Low Z <sup>[18]</sup>                        | 5                             | –   | 5              | –   | ns   |
| $t_{HZOE}$                        | $\overline{OE}$ HIGH to High Z <sup>[18, 19]</sup>                  | –                             | 18  | –              | 20  | ns   |
| $t_{LZCE}$                        | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[18]</sup>      | 10                            | –   | 10             | –   | ns   |
| $t_{HZCE}$                        | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z <sup>[18, 19]</sup> | –                             | 18  | –              | 20  | ns   |
| $t_{PU}$                          | $\overline{CE}_1$ LOW and $CE_2$ HIGH to power up                   | 0                             | –   | 0              | –   | ns   |
| $t_{PD}$                          | $\overline{CE}_1$ HIGH and $CE_2$ LOW to power down                 | –                             | 45  | –              | 55  | ns   |
| $t_{DBE}$                         | $\overline{BLE}/\overline{BHE}$ LOW to data valid                   | –                             | 45  | –              | 55  | ns   |
| $t_{LZBE}$                        | $\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[18, 20]</sup>    | 5                             | –   | 10             | –   | ns   |
| $t_{HZBE}$                        | $\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[18, 19]</sup>  | –                             | 18  | –              | 20  | ns   |
| <b>Write Cycle<sup>[21]</sup></b> |   |                               |     |                |     |      |
| $t_{WC}$                          | Write cycle time  | 45                            | –   | 55             | –   | ns   |
| $t_{SCE}$                         | $\overline{CE}_1$ LOW and $CE_2$ HIGH to write end                  | 35                            | –   | 40             | –   | ns   |
| $t_{AW}$                          | Address setup to write end  | 35                            | –   | 40             | –   | ns   |
| $t_{HA}$                          | Address hold from write end   | 0                             | –   | 0              | –   | ns   |
| $t_{SA}$                          | Address setup to write start  | 0                             | –   | 0              | –   | ns   |
| $t_{PWE}$                         | $\overline{WE}$ pulse width   | 35                            | –   | 40             | –   | ns   |
| $t_{BW}$                          | $\overline{BLE}/\overline{BHE}$ LOW to write end                    | 35                            | –   | 40             | –   | ns   |
| $t_{SD}$                          | Data setup to write end   | 25                            | –   | 25             | –   | ns   |
| $t_{HD}$                          | Data hold from write end  | 0                             | –   | 0              | –   | ns   |
| $t_{HZWE}$                        | $\overline{WE}$ LOW to High Z <sup>[18, 19]</sup>                   | –                             | 18  | –              | 20  | ns   |
| $t_{LZWE}$                        | $\overline{WE}$ HIGH to Low Z <sup>[18]</sup>                       | 10                            | –   | 10             | –   | ns   |

### Notes

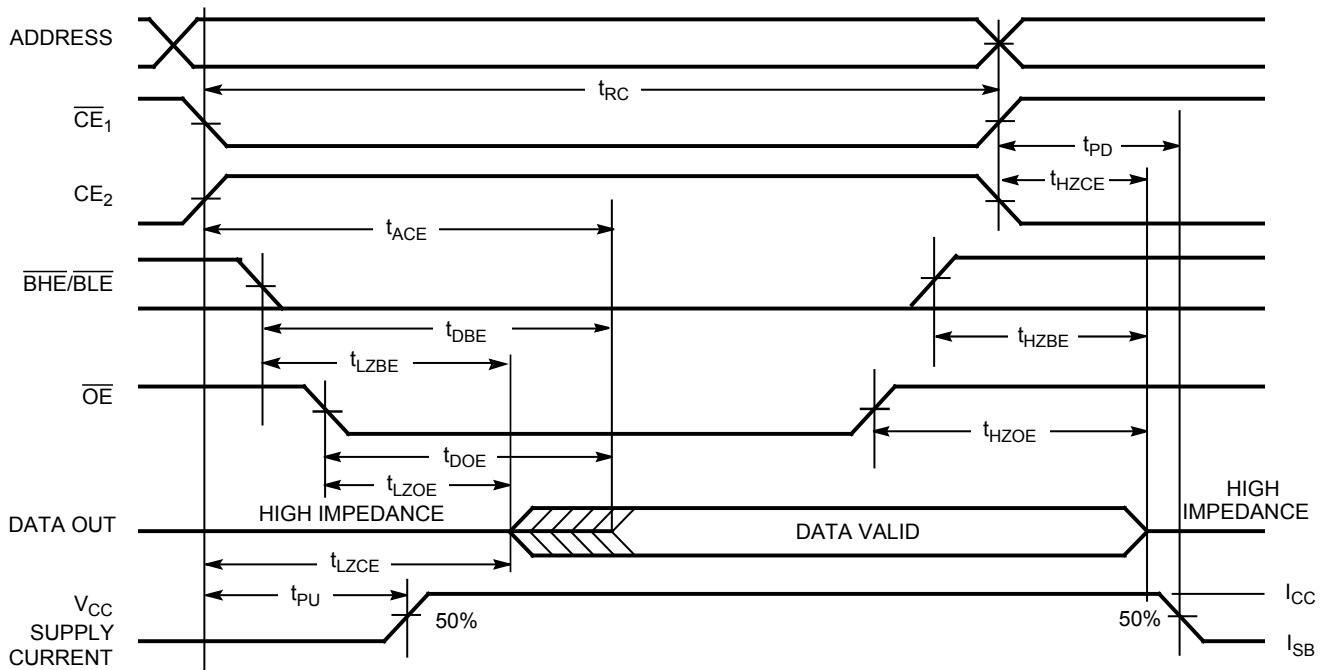
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the Figure 4 on page 5.
17. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
18. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
19.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
20. If both byte enables are toggled together, this value is 10 ns.
21. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle No. 1 (Address Transition Controlled) [22, 23]



### Read Cycle No. 2 ( $\overline{OE}$ Controlled) [23, 24]



#### Notes

22. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .

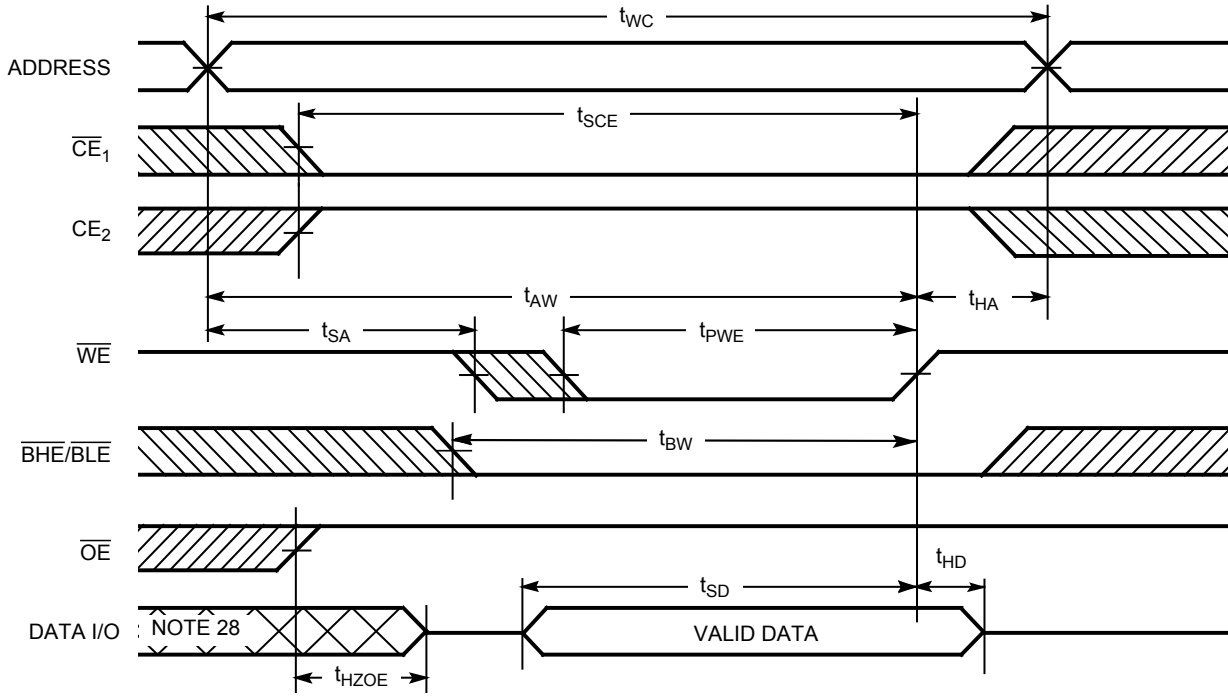
23.  $\overline{WE}$  is HIGH for read cycle.

24. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.



**Switching Waveforms** (continued)

**Write Cycle No. 1 (WE Controlled)** [25, 26, 27]

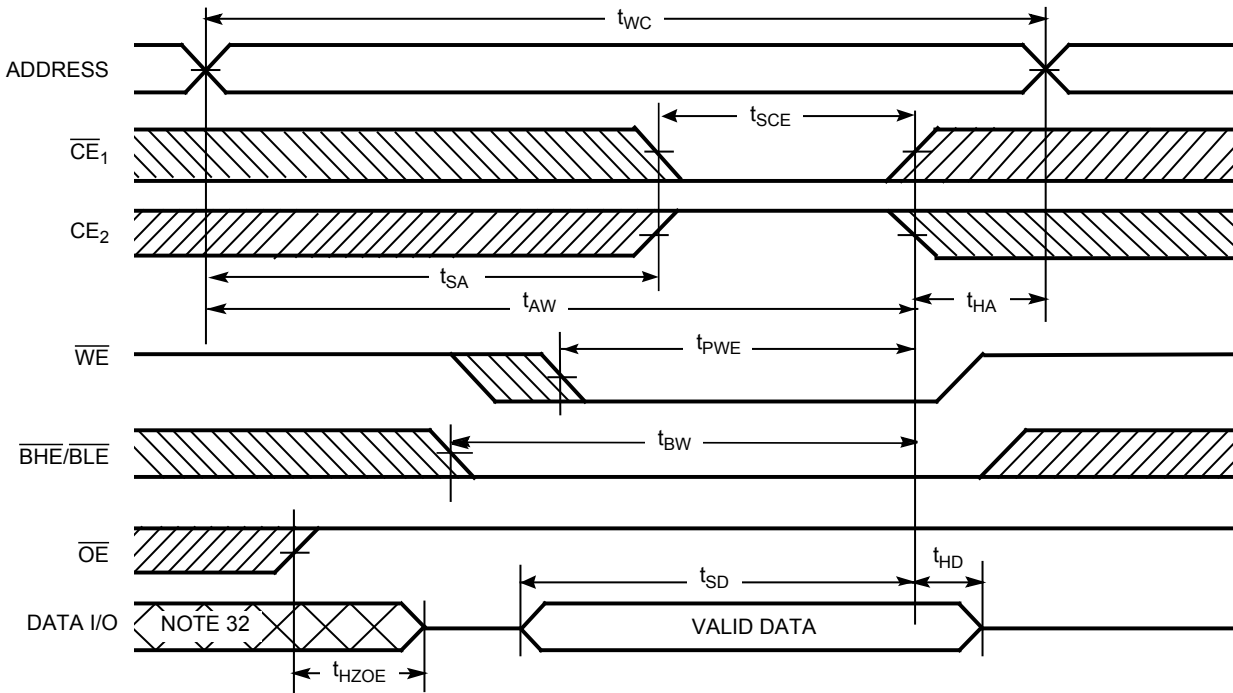


**Notes**

- 25. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 27. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** [29, 30, 31]



**Notes**

29. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

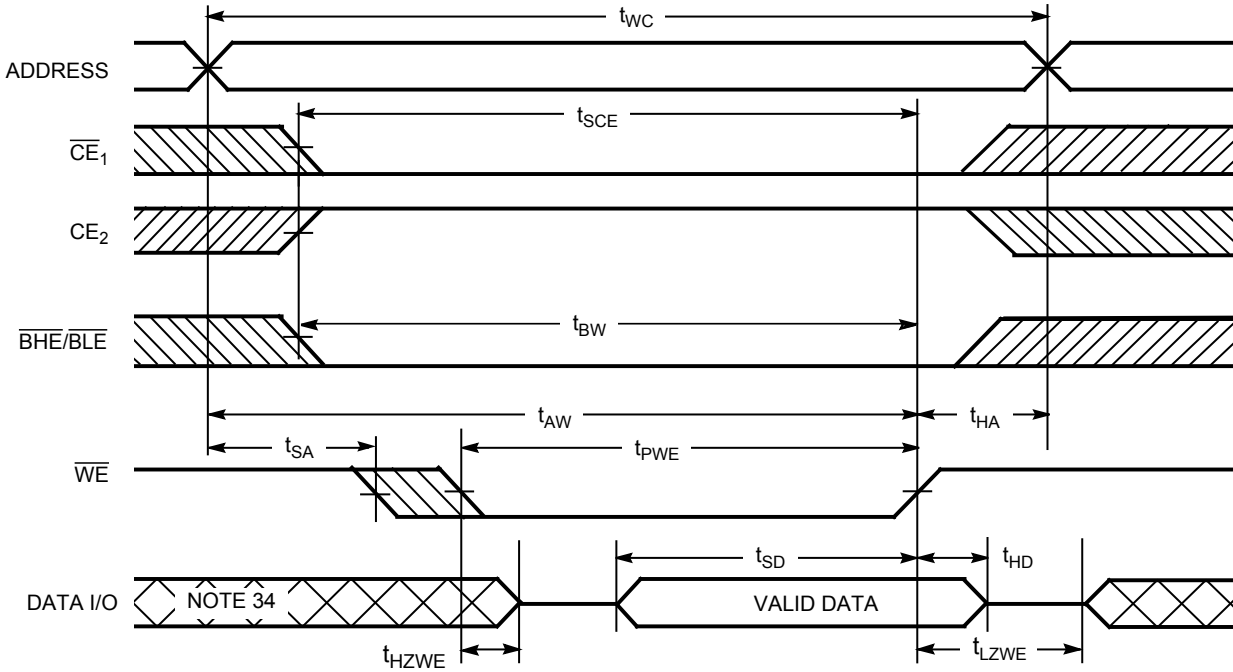
30. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

31. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

32. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [33]

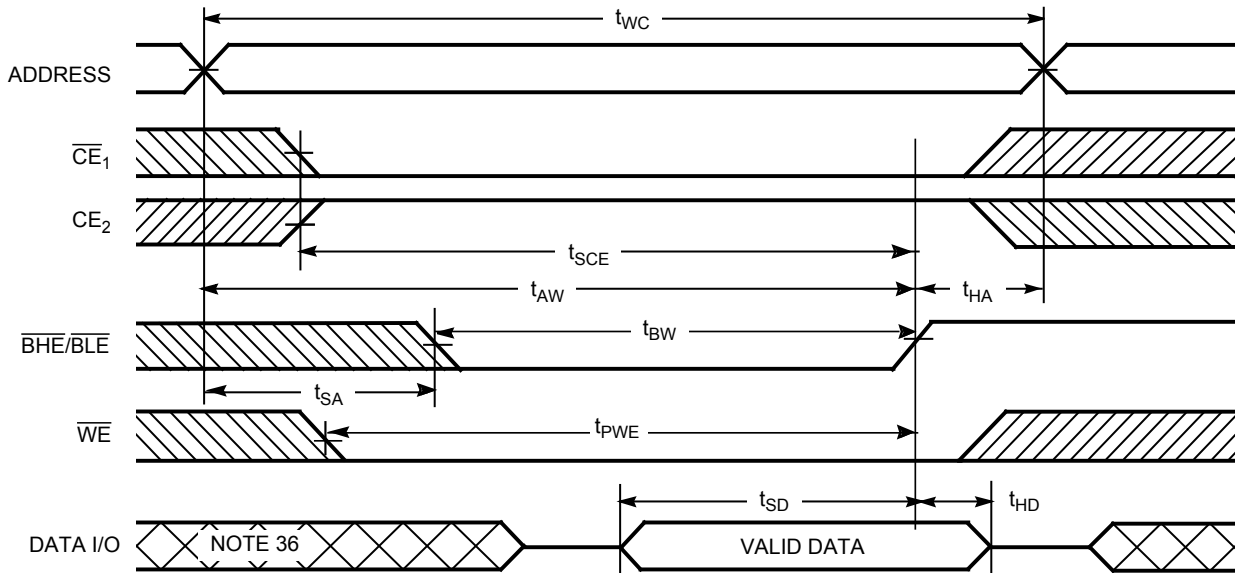


Notes

- 33. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 34. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms** (continued)

**Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [35]**



**Notes**

35. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

36. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

| $\overline{CE}_1$ | $\overline{CE}_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs   | Mode                | Power                      |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------------|
| H                 | X <sup>[37]</sup> | X               | X               | X                | X                | High Z   | Deselect/power down | Standby (I <sub>SB</sub> ) |
| X <sup>[37]</sup> | L                 | X               | X               | X                | X                | High Z   | Deselect/power down | Standby (I <sub>SB</sub> ) |
| X <sup>[37]</sup> | X <sup>[37]</sup> | X               | X               | H                | H                | High Z   | Deselect/power down | Standby (I <sub>SB</sub> ) |
| L                 | H                 | H               | L               | L                | L                | Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )  | Read                | Active (I <sub>CC</sub> )  |
| L                 | H                 | H               | L               | H                | L                | Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>High Z (I/O <sub>8</sub> –I/O <sub>15</sub> ) | Read                | Active (I <sub>CC</sub> )  |
| L                 | H                 | H               | L               | L                | H                | High Z (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ) | Read                | Active (I <sub>CC</sub> )  |
| L                 | H                 | H               | H               | L                | H                | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                 | H                 | H               | H               | H                | L                | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                 | H                 | H               | H               | L                | L                | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                 | H                 | L               | X               | L                | L                | Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )   | Write               | Active (I <sub>CC</sub> )  |
| L                 | H                 | L               | X               | H                | L                | Data In (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>High Z (I/O <sub>8</sub> –I/O <sub>15</sub> )  | Write               | Active (I <sub>CC</sub> )  |
| L                 | H                 | L               | X               | L                | H                | High Z (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>Data In (I/O <sub>8</sub> –I/O <sub>15</sub> )  | Write               | Active (I <sub>CC</sub> )  |

**Note**

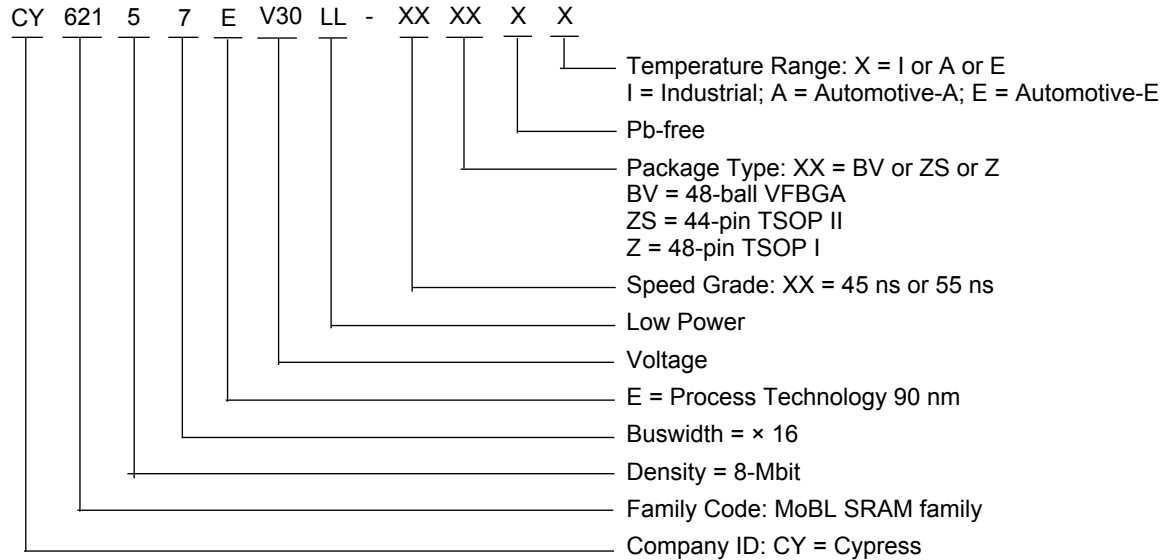
37. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted

**Ordering Information**

| Speed (ns) | Ordering Code        | Package Diagram | Package Type  | Operating Range |
|------------|----------------------|-----------------|---|-----------------|
| 45         | CY62157EV30LL-45BVI  | 51-85150        | 48-ball very fine-pitch ball grid array             | Industrial      |
|            | CY62157EV30LL-45BVXI | 51-85150        | 48-ball very fine-pitch ball grid array (Pb-free)   |                 |
|            | CY62157EV30LL-45ZSXI | 51-85087        | 44-pin thin small outline package type II (Pb-free) |                 |
|            | CY62157EV30LL-45ZXI  | 51-85183        | 48-pin thin small outline package type I (Pb-free)  |                 |
|            | CY62157EV30LL-45BVXA | 51-85150        | 48-ball very fine-pitch ball grid array (Pb-free)   | Automotive-A    |
|            | CY62157EV30LL-45ZSXA | 51-85087        | 44-pin thin small outline package type II (Pb-free) |                 |
|            | CY62157EV30LL-45ZXXA | 51-85183        | 48-pin thin small outline package type I (Pb-free)  |                 |
| 55         | CY62157EV30LL-55ZSXE | 51-85087        | 44-pin thin small outline package type II (Pb-free) | Automotive-E    |
|            | CY62157EV30LL-55ZXXE | 51-85183        | 48-pin thin small outline package type I (Pb-free)  |                 |

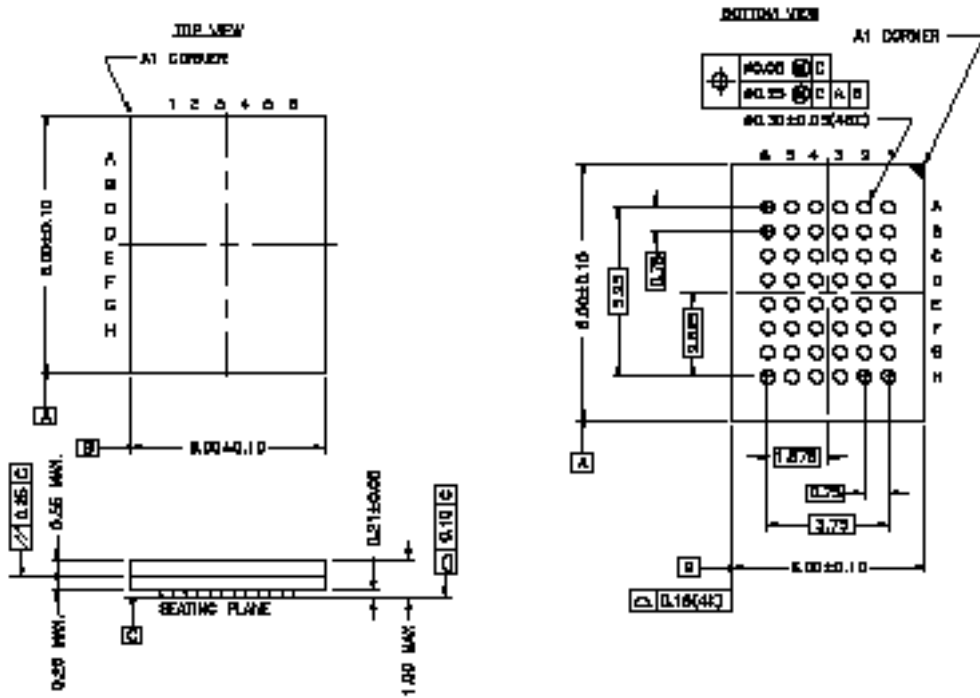
Contact your local Cypress sales representative for availability of these parts.

**Ordering Code Definitions**



Package Diagrams

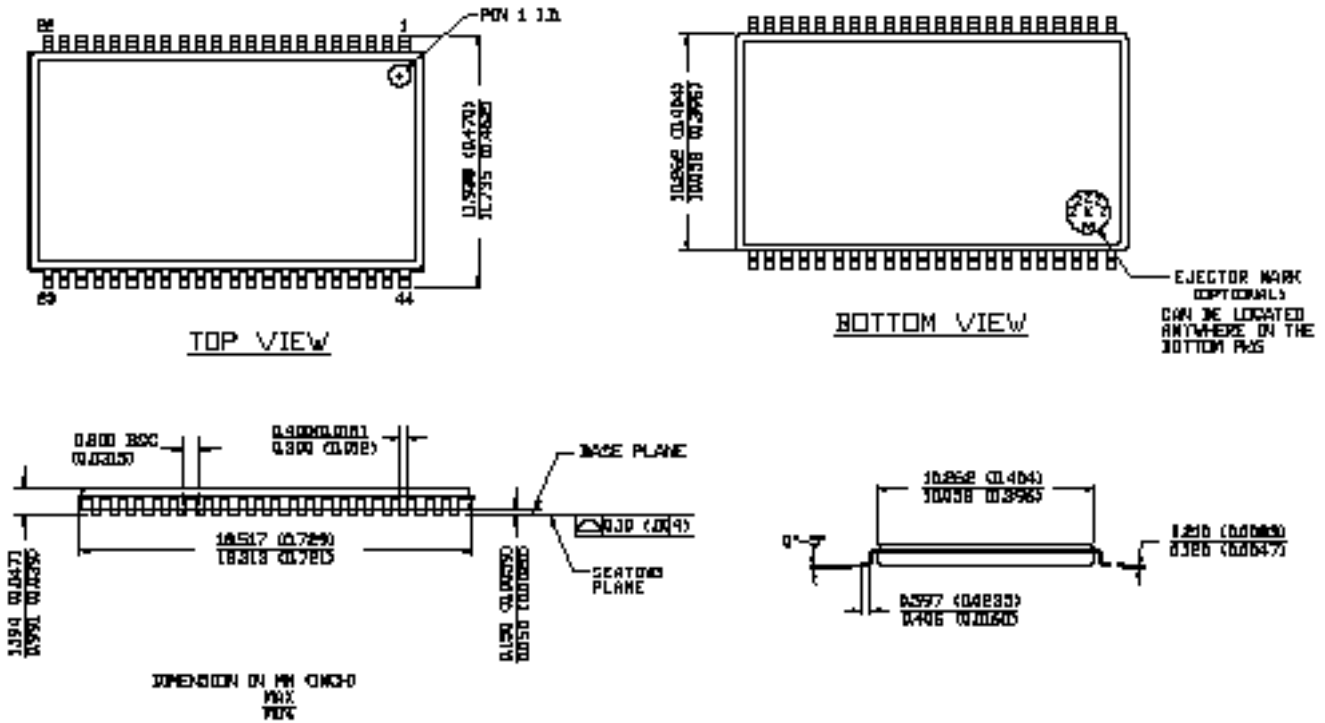
Figure 6. 48-pin VFBGA (6 × 8 × 1 mm) BV48/BZ48, 51-85150



51-85150 \*F

Package Diagrams (continued)

Figure 7. 44-pin TSOP Z44-II, 51-85087

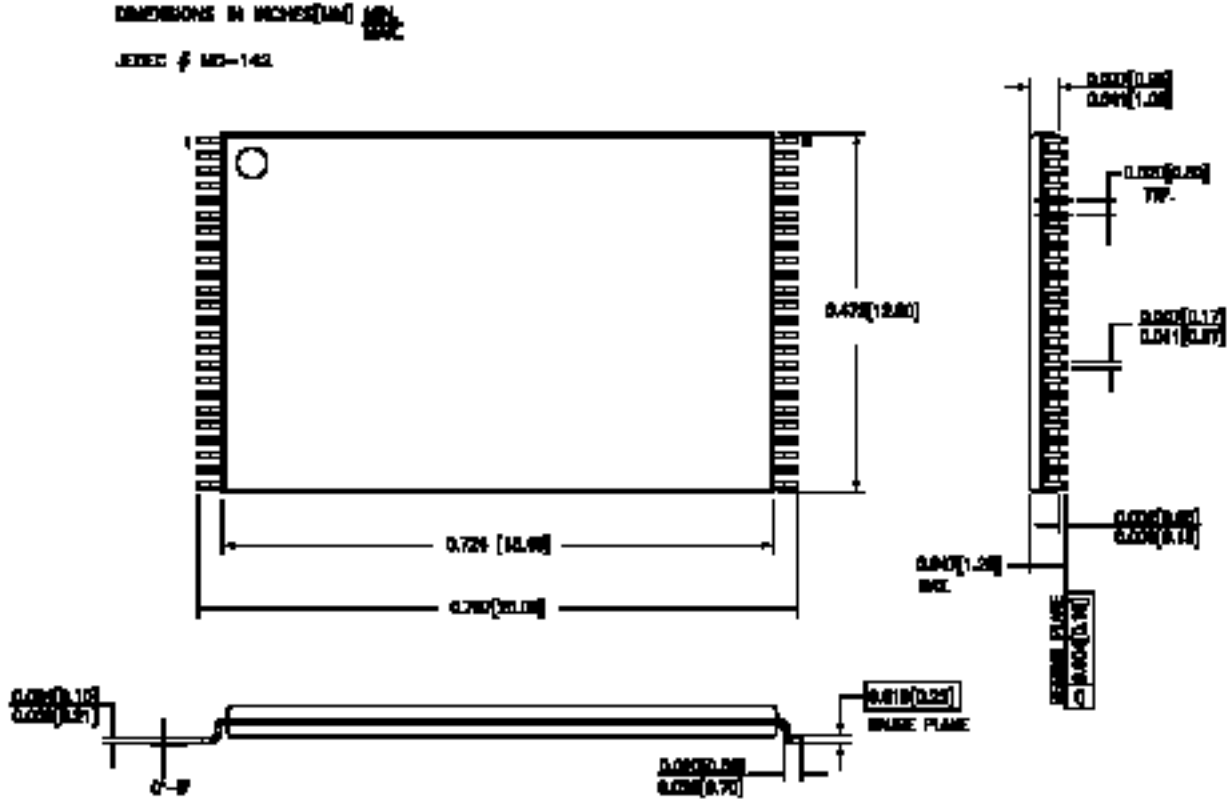


51-85087 \*C



Package Diagrams (continued)

Figure 8. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A, 51-85183



51-85183 \*B

## Acronyms

| Acronym         | Description                             |
|-----------------|---|
| $\overline{CE}$ | chip enable                             |
| CMOS            | complementary metal oxide semiconductor |
| I/O             | input/output                            |
| $\overline{OE}$ | output enable                           |
| RAM             | random access memory                    |
| SRAM            | static random access memory             |
| TSOP            | thin small outline package              |
| VFBGA           | very fine-pitch ball grid array         |
| $\overline{WE}$ | write enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celcius  |
| MHz    | Mega Hertz      |
| μA     | micro Amperes   |
| μs     | micro seconds   |
| mA     | milli Amperes   |
| mm     | milli meter     |
| ns     | nano seconds    |
| Ω      | ohms            |
| %      | percent         |
| pF     | pico Farad      |
| V      | Volts           |
| W      | Watts           |

**Document History Page**

| Document Title: CY62157EV30 MoBL®, 8-Mbit (512 K × 16) Static RAM<br>Document Number: 38-05445 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change   |
| **   | 202940  | AJU             | See ECN         | New Data Sheet  |
| *A   | 291272  | SYT             | See ECN         | <p>Converted from Advance Information to Preliminary</p> <p>Removed 48-TSOP I Package and the associated footnote</p> <p>Added footnote stating 44 TSOP II Package has only one <math>\overline{CE}</math> on Page # 2</p> <p>Changed <math>V_{CC}</math> stabilization time in footnote #7 from 100 <math>\mu</math>s to 200 <math>\mu</math>s</p> <p>Changed <math>I_{CCDR}</math> from 4 to 4.5 <math>\mu</math>A</p> <p>Changed <math>t_{OHA}</math> from 6 to 10 ns for both 35 and 45 ns Speed Bins</p> <p>Changed <math>t_{DOE}</math> from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed <math>t_{HZOE}</math>, <math>t_{HZBE}</math> and <math>t_{HZWE}</math> from 12 and 15 ns to 15 and 18 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed <math>t_{HZCE}</math> from 12 and 15 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed <math>t_{SCE}</math>, <math>t_{AW}</math> and <math>t_{BW}</math> from 25 and 40 ns to 30 and 35 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed <math>t_{SD}</math> from 15 and 20 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively</p> <p>Added Lead-Free Package Information</p>  |
| *B   | 444306  | NXR             | See ECN         | <p>Converted from Preliminary to Final.</p> <p>Changed ball E3 from DNU to NC</p> <p>Removed redundant footnote on DNU.</p> <p>Removed 35 ns speed bin</p> <p>Removed "L" bin</p> <p>Added 48 pin TSOP I package</p> <p>Added Automotive product information.</p> <p>Changed the <math>I_{CC}</math> Typ value from 16 mA to 18 mA and <math>I_{CC}</math> Max value from 28 mA to 25 mA for test condition <math>f = f_{ax} = 1/t_{RC}</math>.</p> <p>Changed the <math>I_{CC}</math> Max value from 2.3 mA to 3 mA for test condition <math>f = 1</math>MHz.</p> <p>Changed the <math>I_{SB1}</math> and <math>I_{SB2}</math> Max value from 4.5 <math>\mu</math>A to 8 <math>\mu</math>A and Typ value from 0.9 <math>\mu</math>A to 2 <math>\mu</math>A respectively.</p> <p>Modified <math>ISB_1</math> test condition to include <math>\overline{BHE}</math>, <math>\overline{BLE}</math></p> <p>Updated Thermal Resistance table.</p> <p>Changed Test Load Capacitance from 50 pF to 30 pF.</p> <p>Added Typ value for <math>I_{CCDR}</math></p> <p>Changed the <math>I_{CCDR}</math> Max value from 4.5 <math>\mu</math>A to 5 <math>\mu</math>A</p> <p>Corrected <math>t_R</math> in Data Retention Characteristics from 100 <math>\mu</math>s to <math>t_{RC}</math> ns.</p> <p>Changed <math>t_{LZOE}</math> from 3 to 5</p> <p>Changed <math>t_{LZCE}</math> from 6 to 10</p> <p>Changed <math>t_{HZCE}</math> from 22 to 18</p> <p>Changed <math>t_{LZBE}</math> from 6 to 5</p> <p>Changed <math>t_{PWE}</math> from 30 to 35</p> <p>Changed <math>t_{SD}</math> from 22 to 25</p> <p>Changed <math>t_{LZWE}</math> from 6 to 10</p> <p>Added footnote #15</p> <p>Updated the ordering Information and replaced the Package Name column with Package Diagram.</p> |
| *C   | 467052  | NXR             | See ECN         | <p>Modified Data sheet to include x8 configurability.</p> <p>Updated the Ordering Information table</p>   |
| *D   | 925501  | VKN             | See ECN         | <p>Removed Automotive-E information</p> <p>Added Preliminary Automotive-A information</p> <p>Added footnote #10 related to <math>I_{SB2}</math> and <math>I_{CCDR}</math></p> <p>Added footnote #15 related AC timing parameters</p>  |
| *E   | 1045801 | VKN             | See ECN         | <p>Converted Automotive-A specs from preliminary to final</p> <p>Updated footnote #9</p>  |

**Document History Page** (continued)

| Document Title: CY62157EV30 MoBL <sup>®</sup> , 8-Mbit (512 K × 16) Static RAM |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Document Number: 38-05445  |         |                 |                 |   |
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change   |
| *F   | 2724889 | NXR/AESA        | 06/26/09        | Added Automotive-E information<br>Included -45ZXA/-55ZSXE/-55ZXE parts in the Ordering Information table  |
| *G   | 2927528 | VKN             | 05/04/2010      | Renamed "DNU" pins as "NC" for 48 TSOP I package<br>Added footnote #24 related to chip enable<br>Updated <a href="#">Package Diagrams</a><br>Added <a href="#">Contents</a><br>Updated links in <a href="#">Sales, Solutions, and Legal Information</a>   |
| *H   | 3110053 | PRAS            | 12/14/2010      | Changed Table Footnotes to Footnotes.<br>Added Ordering Code Definitions.   |
| *I   | 3269771 | RAME            | 05/30/2011      | Updated <a href="#">Functional Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.").<br>Updated <a href="#">Electrical Characteristics</a> .<br>Updated <a href="#">Data Retention Characteristics</a> .<br>Updated <a href="#">Package Diagrams</a> .<br>Added <a href="#">Acronyms and Units of Measure</a> .<br>Updated in new template. |

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