

# 4-Mbit (512 K × 8) Static RAM

## Features

- Very high speed: 45 ns
- Voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62148B
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A (Industrial)
- Ultra low active power
  - Typical active current: 2.0 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC)<sup>[1]</sup> packages

## Functional Description

The CY62148E is a high performance CMOS static RAM organized as 512 K words by 8-bits. This device features

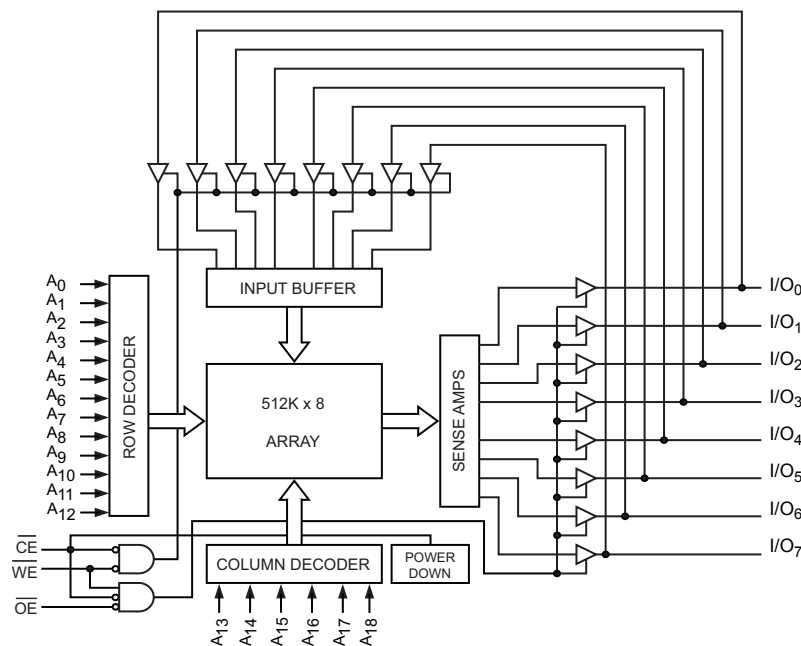
advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), Outputs are disabled ( $\overline{OE}$  HIGH), or during an active Write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

## Logic Block Diagram



### Note

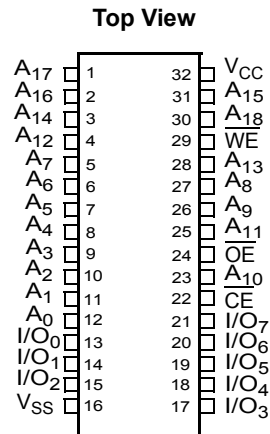
1. SOIC package is available only in 55 ns speed bin.

## Contents

<b>Pin Configurations</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>11</b>
<b>Product Portfolio</b> .....	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>14</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>14</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	14
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>15</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>17</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	17
<b>Data Retention Waveform</b> .....	<b>6</b>	Products .....	17
<b>Switching Characteristics</b> .....	<b>7</b>	PSoC Solutions .....	17
<b>Switching Waveforms</b> .....	<b>8</b>		
<b>Truth Table</b> .....	<b>10</b>		

## Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout



## Product Portfolio

Product		Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
			Min	Typ <sup>[2]</sup>	Max		Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
						f = 1 MHz		f = f <sub>max</sub>				
						Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	
CY62148ELL	TSOP II	Industrial	4.5	5.0	5.5	45	2	2.5	15	20	1	7
CY62148ELL	SOIC	Industrial / Automotive-A	4.5	5.0	5.5	55	2	2.5	15	20	1	7

**Note**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to + 150 °C
Ambient temperature with power applied .....	-55 °C to + 125 °C
Supply voltage to ground potential .....	-0.5 V to 6.0 V ( $V_{CCmax} + 0.5$ V)
DC voltage applied to outputs in high Z state <sup>[3, 4]</sup> .....	-0.5 V to 6.0 V ( $V_{CCmax} + 0.5$ V)

DC input voltage <sup>[3, 4]</sup> .....	-0.5 V to 6.0 V ( $V_{CCmax} + 0.5$ V)
Output current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch-up current .....	> 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[5]</sup>
CY62148E	Industrial / Automotive-A	-40 °C to +85 °C	4.5 V to 5.5 V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			55 ns <sup>[6]</sup>			Unit	
			Min	Typ <sup>[7]</sup>	Max	Min	Typ <sup>[7]</sup>	Max		
V <sub>OH</sub> <sup>[8]</sup>	Output HIGH voltage	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	2.4	-	-	2.4	-	-	V	
		V <sub>CC</sub> = 5.5 V, I <sub>OH</sub> = -0.1 mA	-	-	3.4 <sup>[8]</sup>	-	-	3.4 <sup>[8]</sup>	V	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 2.1 mA	-	-	0.4	-	-	0.4	V	
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.2	-	V <sub>CC</sub> + 0.5	2.2	-	V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	For TSOPII package	-0.5	-	0.8	-	-	-	V
			For SOIC package	-	-	-	-0.5	-	0.6 <sup>[9]</sup>	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	-1	-	+1	µA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-1	-	+1	-1	-	+1	µA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	-	15	20	-	15	20	mA	
		f = 1 MHz	-	2	2.5	-	2	2.5		
I <sub>SB2</sub> <sup>[10]</sup>	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	-	1	7	-	1	7	µA	

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns for I ≤ 30 mA.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V<sub>CC(min)</sub> and 200 µs wait time after V<sub>CC</sub> stabilization.
- SOIC package is available only in 55 ns speed bin.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Please note that the maximum V<sub>OH</sub> limit for this device does not exceed minimum CMOS V<sub>IH</sub> of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.6 V. This is applicable to SOIC package only.
- Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

### Capacitance

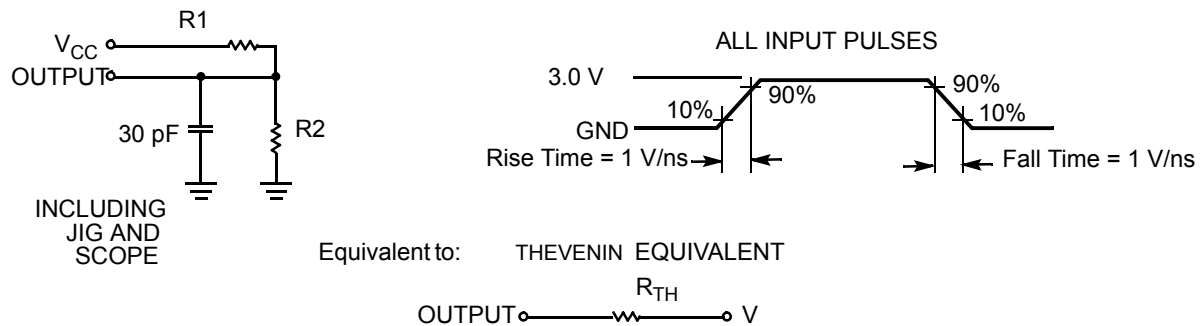
Parameter <sup>[11]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(Typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		10	13	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter <sup>[11]</sup>	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

**Note**

11. Tested initially and after any design or process changes that may affect these parameters.

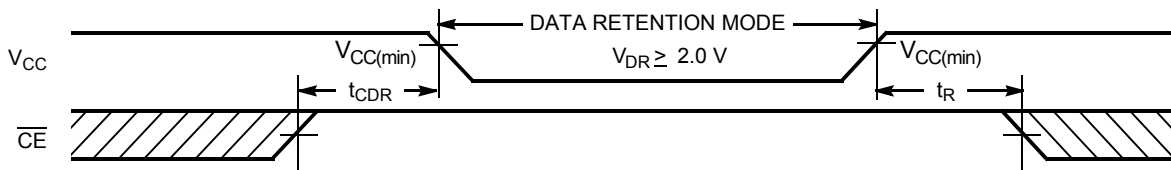
### Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ <sup>[12]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention			2	–	–	V
I <sub>CCDR</sub> <sup>[13]</sup>	Data retention current	V <sub>CC</sub> = V <sub>DR</sub> , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V	Industrial / Automotive-A	–	1	7	μA
t <sub>CDR</sub>	Chip deselect to data retention time			0	–	–	ns
t <sub>R</sub> <sup>[14]</sup>	Operation recovery time	TSOP II		45	–	–	ns
		SOIC		55	–	–	ns

### Data Retention Waveform

Figure 3. Data Retention Waveform



**Notes**

- 12. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- 13. Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
- 14. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> > 100 μs or stable at V<sub>CC(min)</sub> > 100 μs.

## Switching Characteristics

Over the operating range

Parameter <sup>[15]</sup>	Description	45 ns		55 ns <sup>[16]</sup>		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	45	–	55	–	ns
$t_{AA}$	Address to data valid	–	45	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[17]</sup>	5	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[17, 18]</sup>	–	18	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[17]</sup>	10	–	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[17, 18]</sup>	–	18	–	20	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
<b>Write Cycle <sup>[19]</sup></b>						
$t_{WC}$	Write cycle time	45	–	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	40	–	ns
$t_{AW}$	Address setup to write end	35	–	40	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	40	–	ns
$t_{SD}$	Data setup to write end	25	–	25	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[17, 18]</sup>	–	18	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[17]</sup>	10	–	10	–	ns

### Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).
16. SOIC package is available only in 55 ns speed bin.
17. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
18.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

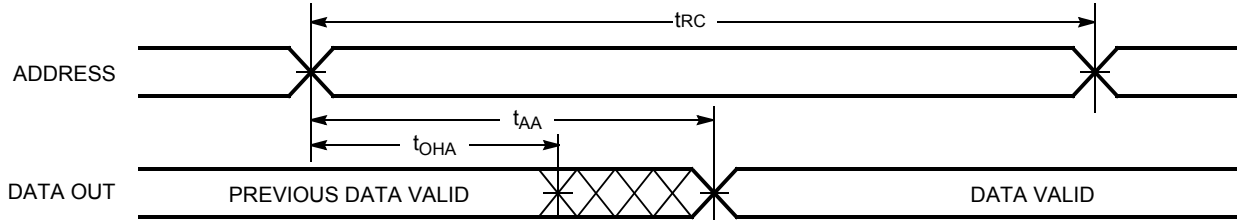


Figure 5. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled) [21, 22]

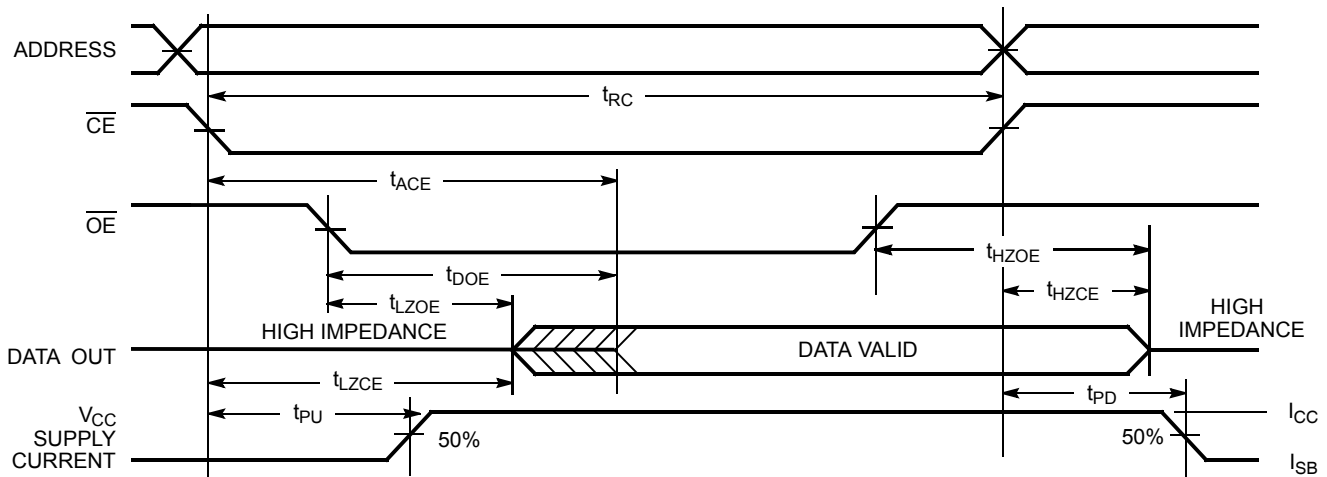
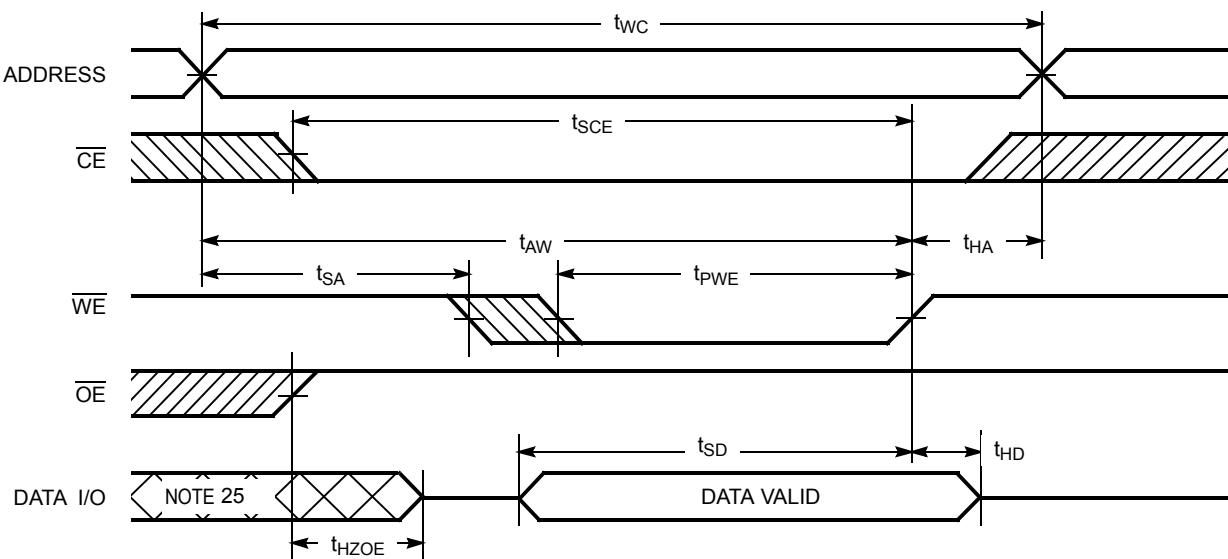


Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write) [23, 24]



### Notes

20. Device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$ .
21.  $\overline{\text{WE}}$  is HIGH for read cycles.
22. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.
23. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
24. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals must not be applied.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [26, 27]

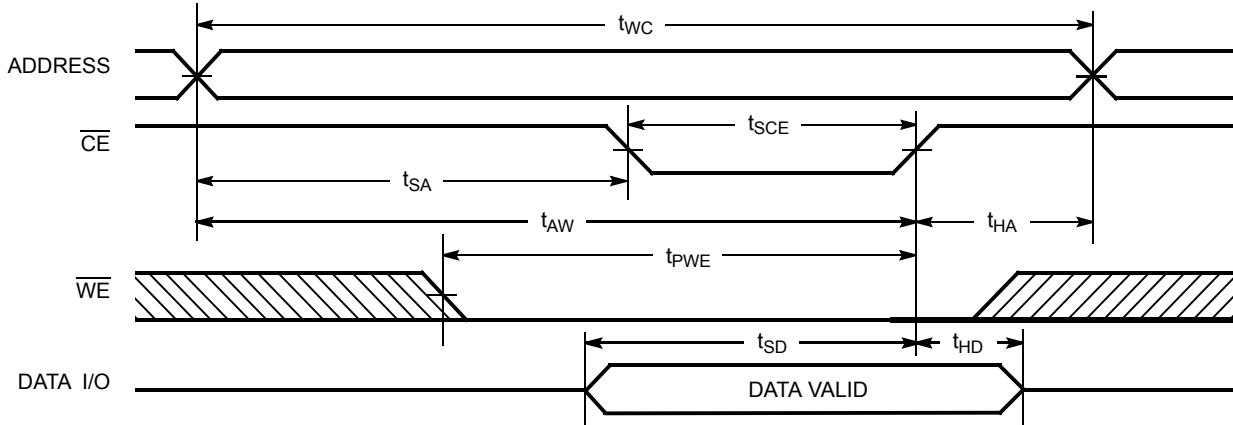
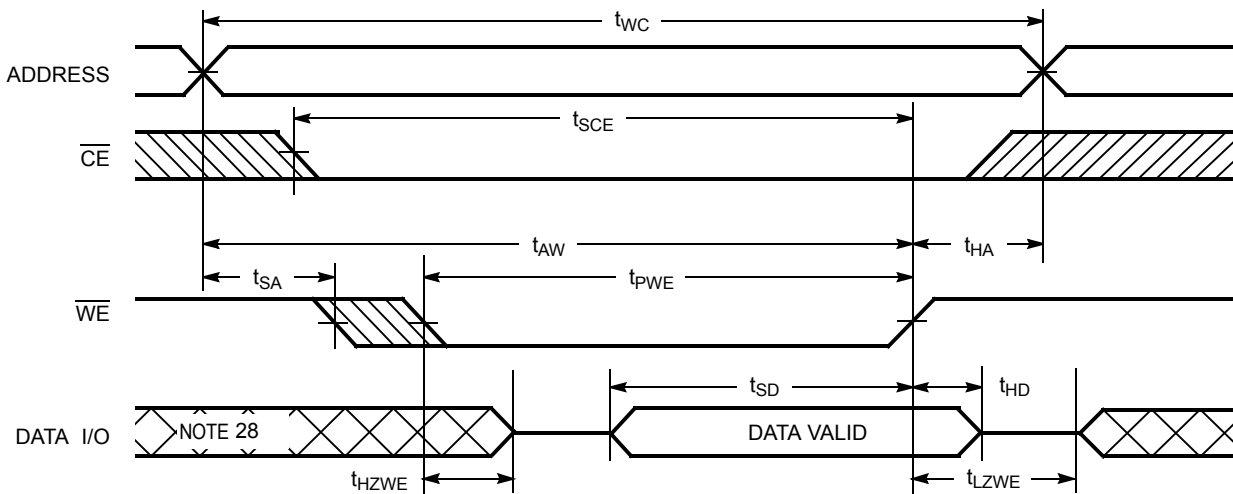


Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [27]



Notes

- 26. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 27. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 28. During this period, the I/Os are in output state and input signals must not be applied.

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [29]	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
L	H	L	Data out	Read	Active ( $I_{CC}$ )
L	L	X	Data in	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

**Note**

29. Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

## Ordering Information

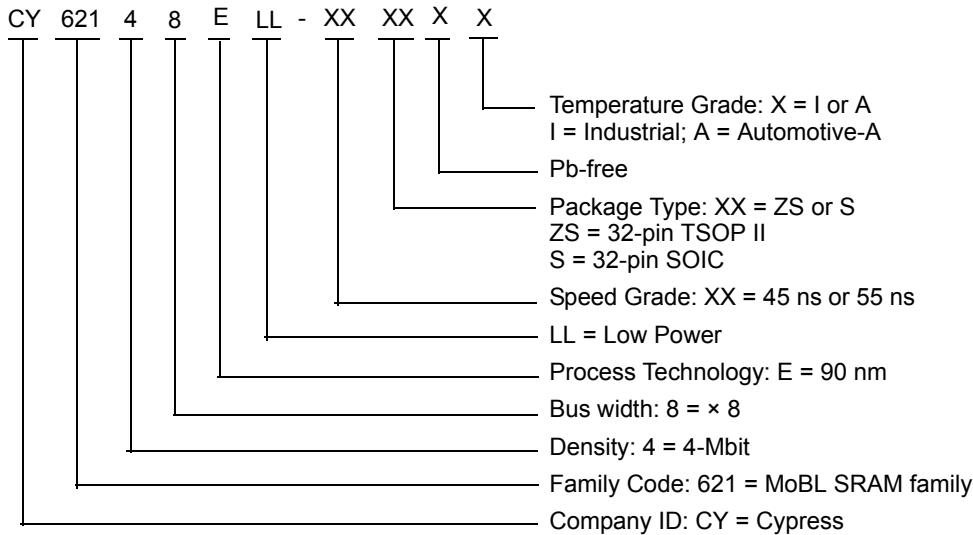
Table 1 lists the CY62148E MoBL® key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>.

Table 1. Key features and Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
	CY62148ELL-45ZSXA	51-85095	32-pin TSOP II (Pb-free)	Automotive-A
55	CY62148ELL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial
	CY62148ELL-55SXA	51-85081	32-pin SOIC (Pb-free)	Automotive-A

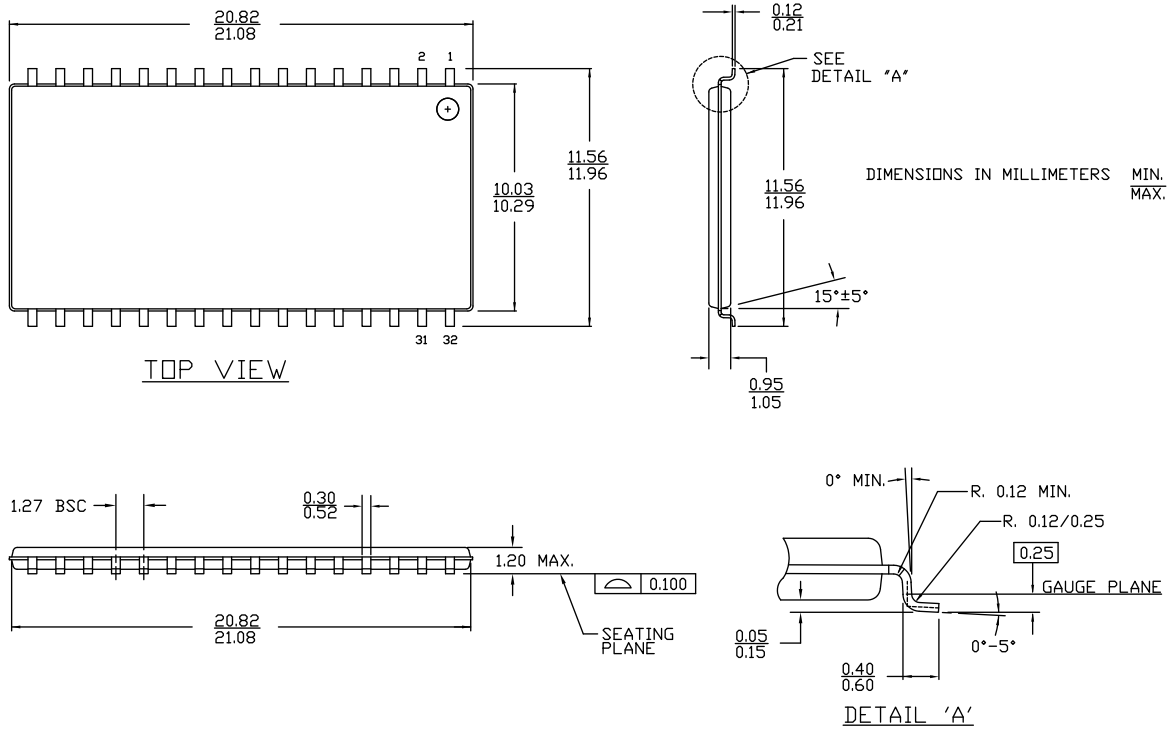
Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



Package Diagrams

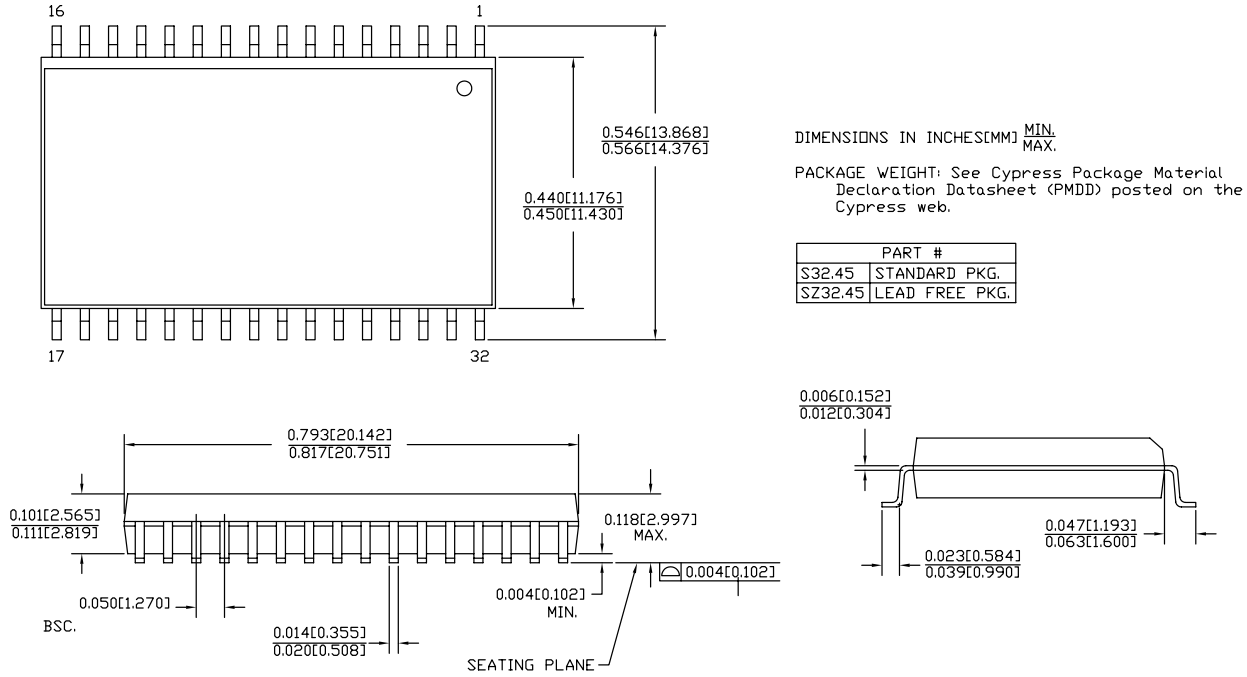
Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 \*B

Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mil) S32.45/SZ32.45 Package Outline, 51-85081



51-85081 \*E

**Acronyms**

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
MoBL	More Battery Life
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY62148E MoBL <sup>®</sup> , 4-Mbit (512 K × 8) Static RAM Document Number: 38-05442				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201580	AJU	01/08/04	New data sheet.
*A	249276	SYT	See ECN	<p>Changed status from Advance Information to Preliminary.</p> <p>Updated <a href="#">Features</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Functional Description</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Pin Configurations</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Operating Range</a> (Updated Note 5 (Changed V<sub>CC</sub> stabilization time from 100 μs to 200 μs)).</p> <p>Updated <a href="#">Data Retention Characteristics</a> (Changed maximum value of I<sub>CCDR</sub> parameter from 2.0 μA to 2.5 μA, changed minimum value of t<sub>R</sub> parameter from 100 μs to t<sub>RC</sub> ns).</p> <p>Updated <a href="#">Switching Characteristics</a> (Changed minimum value of t<sub>OHA</sub> parameter from 6 ns to 10 ns for both 35 ns and 45 ns speed bin, changed maximum value of t<sub>DOE</sub> parameter from 15 ns to 18 ns for 35 ns speed bin, changed maximum value of t<sub>HZOE</sub>, t<sub>HZWE</sub> parameters from 12 ns to 15 ns for 35 ns speed bin and 15 ns to 18 ns for 45 ns speed bin, changed minimum value of t<sub>SCE</sub> parameter from 25 ns to 30 ns for 35 ns speed bin and 40 ns to 35 ns for 45 ns speed bin, changed maximum value of t<sub>HZCE</sub> parameter from 12 ns to 18 ns for 35 ns speed bin and 15 ns to 22 ns for 45 ns speed bin, changed minimum value of t<sub>SD</sub> parameter from 15 ns to 18 ns for 35 ns speed bin and 20 ns to 22 ns for 45 ns speed bin).</p> <p>Updated <a href="#">Ordering Information</a> (Corrected typo in Package Name column, also updated Ordering Codes (to include Pb-free packages)).</p>
*B	414820	ZSD	See ECN	<p>Changed status from Preliminary to Final</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Updated <a href="#">Features</a> (Removed 35 ns speed bin).</p> <p>Updated <a href="#">Pin Configurations</a> (Removed the Note "DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application." and its reference).</p> <p>Updated <a href="#">Product Portfolio</a> (Removed 35 ns speed bin).</p> <p>Updated <a href="#">Maximum Ratings</a> (Updated Note 3 to include current limit).</p> <p>Updated <a href="#">Electrical Characteristics</a> (Removed "L" version of CY62148E, changed typical value of I<sub>CC</sub> parameter from 1.5 mA to 2 mA at f = 1 MHz, changed maximum value of I<sub>CC</sub> parameter from 2 mA to 2.5 mA at f = 1 MHz, changed typical value of I<sub>CC</sub> parameter from 12 mA to 15 mA at f = f<sub>max</sub>, removed I<sub>SB1</sub> parameter and its details, changed typical value of I<sub>SB2</sub> parameter from 0.7 μA to 1 μA and maximum value of I<sub>SB2</sub> parameter from 2.5 μA to 7 μA).</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a> (Changed the AC test load capacitance from 100 pF to 30 pF in Figure 2, changed test load parameters R<sub>1</sub>, R<sub>2</sub>, R<sub>TH</sub> and V<sub>TH</sub> from 1838 Ω, 994 Ω, 645 Ω and 1.75 V to 1800 Ω, 990 Ω, 639 Ω and 1.77 V).</p> <p>Updated <a href="#">Data Retention Characteristics</a> (Changed maximum value of I<sub>CCDR</sub> parameter from 2.5 μA to 7 μA, Added typical value for I<sub>CCDR</sub> parameter).</p> <p>Updated <a href="#">Switching Characteristics</a> (Removed 35 ns speed bin, changed minimum value of t<sub>LZOE</sub> parameter from 3 ns to 5 ns, changed minimum value of t<sub>LZCE</sub> and t<sub>LZWE</sub> parameters from 6 ns to 10 ns, changed maximum value of t<sub>HZCE</sub> parameter from 22 ns to 18 ns, changed minimum value of t<sub>PWE</sub> parameter from 30 ns to 35 ns, changed minimum value of t<sub>SD</sub> parameter from 22 ns to 25 ns).</p> <p>Updated <a href="#">Ordering Information</a> (Updated ordering codes and replaced Package Name column with Package Diagram).</p>

**Document History Page** (continued)

Document Title: CY62148E MoBL <sup>®</sup> , 4-Mbit (512 K × 8) Static RAM Document Number: 38-05442				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C	464503	NXR	See ECN	Updated <a href="#">Product Portfolio</a> (Included Automotive Range). Updated <a href="#">Operating Range</a> (Included Automotive Range). Updated <a href="#">Electrical Characteristics</a> (Included Automotive Range). Updated <a href="#">Data Retention Characteristics</a> (Included Automotive Range). Updated <a href="#">Switching Characteristics</a> (Included Automotive Range). Updated <a href="#">Ordering Information</a> (Updated ordering codes (Included Automotive parts and their related information)).
*D	485639	VKN	See ECN	Updated <a href="#">Operating Range</a> (Updated $V_{CC}$ to 4.5 V to 5.5 V).
*E	833080	VKN	See ECN	Updated <a href="#">Electrical Characteristics</a> (Added $V_{IL}$ parameter for SOIC package, added Note 9 and referred the same note in $V_{IL}$ parameter for SOIC package).
*F	890962	VKN	See ECN	Updated <a href="#">Pin Configurations</a> (Added Note 1 related to SOIC package). Updated <a href="#">Product Portfolio</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Operating Range</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Electrical Characteristics</a> (Included Automotive-A range and removed Automotive-E range, added Note 10 related to $I_{SB2}$ and referred the same note in $I_{SB2}$ parameter). Updated <a href="#">Data Retention Characteristics</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Switching Characteristics</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Ordering Information</a> (Updated ordering codes (Added Automotive-A part and its related information, removed Automotive-E part and its related information)).
*G	2947039	VKN	06/10/2010	Updated <a href="#">Truth Table</a> (Added Note 29 and referred the same note in $\overline{CE}$ column). Updated <a href="#">Ordering Information</a> (Added "CY62148ELL-45ZSXA" part number). Updated <a href="#">Package Diagrams</a> . Added <a href="#">Sales, Solutions, and Legal Information</a> .
*H	3006318	AJU	08/23/10	Updated <a href="#">Data Retention Characteristics</a> (Added note 13 and referred the same note in $I_{CCDR}$ parameter). Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated in new template.
*I	3235744	RAME	04/20/2011	Updated <a href="#">Functional Description</a> (Removed the line "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines"). Updated <a href="#">Package Diagrams</a> .
*J	3302815	RAME	07/14/2011	Updated in new template.
*K	3539544	TAVA	03/01/2012	Updated <a href="#">Electrical Characteristics</a> (Updated Note 9). Updated <a href="#">Package Diagrams</a> .
*L	3992135	MEMJ	05/06/2013	Updated <a href="#">Functional Description</a> .  Updated <a href="#">Electrical Characteristics</a> (Added one more Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA" for $V_{OH}$ parameter and its corresponding values).  Updated <a href="#">Package Diagrams</a> : spec 51-85081 – Changed revision from *D to *E.  Completing Sunset Review.



## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

<a href="#">Automotive</a>	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
<a href="#">Memory</a>	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
<a href="#">Optical &amp; Image Sensing</a>	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
<a href="#">PSoC</a>	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

---

© Cypress Semiconductor Corporation, 2004-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.