

2-Mbit (256 K × 8) Static RAM

Features

■ Very high-speed: 45 ns

■ Temperature ranges

☐ Industrial: –40 °C to 85 °C ☐ Automotive-A: –40 °C to 85 °C

■ Wide voltage range: 2.20 V to 3.60 V

■ Pin compatible with CY62138CV25/30/33

■ Ultra low standby power

Typical standby current: 1 μA

Maximum standby current: 5 μA

■ Ultra low active power

□ Typical active current: 1.6 mA at f = 1 MHz

■ Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features

■ Automatic power down when deselected

■ Complementary metal oxide semiconductor (CMOS) for Optimum speed and power

■ Offered in Pb-free 36-ball VFBGA, 32-pin TSOP II, 32-pin SOIC, 32-pin TSOP I and 32-pin STSOP packages

Functional Description

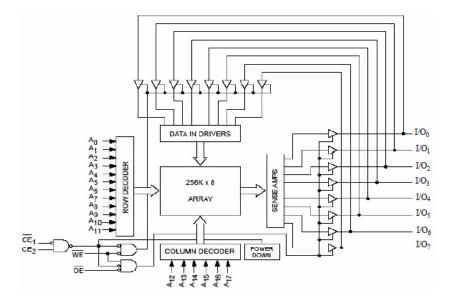
The CY62138FV30 is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery $\mathsf{Life}^\mathsf{TM}$ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Place the device into sta ndby mode reducing power consumption when deselected (CE_1 HIGH or CE_2 LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, ta<u>ke</u> Chip Enable (CE₁ LOW and CE₂ $\underline{\text{HIGH}}$) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O $_0$ through I/O $_7$) are placed in a high impedance state when the device is deselected ($\overline{\text{CE}}_1$ HIGH or $\overline{\text{CE}}_2$ LOW), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}_1$ LOW and $\overline{\text{CE}}_2$ HIGH and WE LOW).

Logic Block Diagram







Contents

Pin Configuration	3
Product Portfolio	3
Maximum Ratings	4
Operating Range	4
Electrical Characteristics	
Capacitance	5
Thermal Resistance	5
AC Test Loads and Waveforms	5
Data Retention Characteristics	6
Data Retention Waveform	
Switching Characteristics	7
Switching Waveforms	

Truth Table	9
Ordering Information	10
Ordering Code Definitions	
Package Diagrams	11
Acronyms	16
Document Conventions	16
Units of Measure	16
Document History Page	17
Sales, Solutions, and Legal Information	18
Worldwide Sales and Design Support	18
Products	18
DCoC Colutions	10



Pin Configuration

Figure 1. 36-ball VFBGA (Top View) [1]

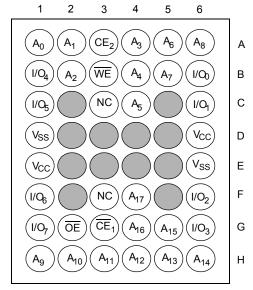


Figure 3. 32-pin TSOP I (Top View)

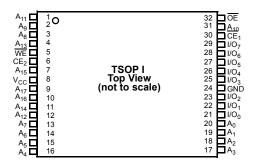


Figure 2. 32-pin SOIC/TSOP II (Top View)

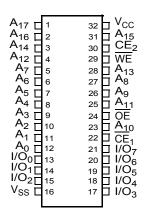
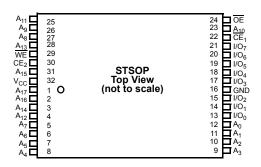


Figure 4. 32-pin STSOP (Top View)



Product Portfolio

		V _{CC} Range (V)				Power Dissipation					
Product	Range				Speed	peed		Operating I _{CC} (mA)			Standby I _{SB2}
Floudet	Range				(ns)	f = 1 MHz		f = 1 MHz		(μ A)	
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62138FV30LL	Industrial / Automotive-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5

Notes

NC pins are not connected on the die.

^{2.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested. Storage temperature-65 °C to +150 °C Ambient temperature with Supply voltage to ground potential-0.3 V to 3.9 V DC voltage applied to outputs in High Z State $^{[3,\ 4]}$ -0.3 V to 3.9 V

DC input voltage [3, 4]	0.3 V to 3.9 V
Output current into outputs (LOW)	20 mA
Static Discharge Voltage(MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Product	Range	Ambient Temperature	V _{CC} ^[5]
CY62138FV30LL	Industrial / Automotive-A		2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

	B	T	45 ns (Industrial / Automotive-A)			
Parameter	Description	Test Conditions	Min	Typ ^[6]	Max	Unit
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	2.0	_	_	V
		$I_{OH} = -1.0 \text{ mA}, V_{CC} \ge 2.70 \text{ V}$	2.4	_	_	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	-	-	0.4	V
		I _{OL} = 2.1 mA, V _{CC} ≥ 2.70 V		-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7 V	1.8	-	V _{CC} + 0.3 V	V
		V _{CC} = 2.7 V to 3.6 V	2.2	-	V _{CC} + 0.3 V	V
V _{IL}	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V For BGA package	-0.3	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-0.3	-	0.8	V
		V _{CC} = 2.2 V to 3.6 V For other packages	-0.3	-	0.6	V
I _{IX}	Input leakage current	$GND \le V_1 \le V_{CC}$	-1	-	+1	μΑ
I _{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, output disabled	-1	_	+1	μА
I _{CC}	V _{CC} Operating supply current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC_{max}}$	_	13	18	mA
		f = 1 MHz	_	1.6	2.5	
I _{SB1} ^[7]	Automatic CE Power-down current–CMOS inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V or CE}_2 \le 0.2 \text{ V},$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \text{V}_{\text{IN}} \le 0.2 \text{ V},$ $\text{f} = \text{f}_{\text{max}} \text{ (address and data only)},$ $\text{f} = 0 (\overline{\text{OE}}, \text{ and } \overline{\text{WE}}), \text{V}_{\text{CC}} = 3.60 \text{ V}$	_	1	5	μА
I _{SB2} ^[7]	Automatic CE Power-down current–CMOS inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V or CE}_2 \le 0.2 \text{ V},$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V or V}_{\text{IN}} \le 0.2 \text{ V},$ $\text{f} = 0, \text{V}_{\text{CC}} = 3.60 \text{ V}$	_	1	5	μА

- 3. $V_{IL(min)} = -2.0 \text{ V}$ for pulse durations less than 20 ns.

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
 V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
 Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



Capacitance

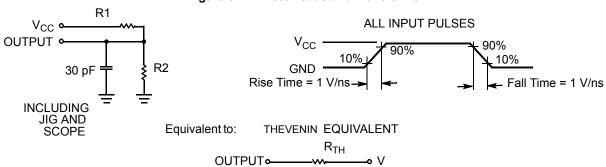
Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_A = 25 ^{\circ}\text{C}$, $f = 1 \text{MHz}$, $V_{CC} = V_{CC(typ.)}$	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Ī	Parameter ^[8]	Description	Test Conditions	32-pin SOIC	36-ball VFBGA	32-pin TSOP II	32-pin STSOP	32-pin TSOP I	Unit
	Θ_{JA}		Still air, soldered on a 3 × 4.5 inch, two layer printed circuit	44.53	38.49	44.16	59.72	50.19	°C/W
	$\Theta_{\sf JC}$	Thermal resistance (Junction to Case)	board	24.05	17.66	11.97	15.38	14.59	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



Parameter 2.5 V (2.2 V to 2.7 V)		3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.



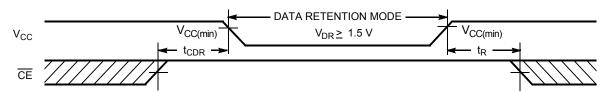
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit	
V_{DR}	V _{CC} for data retention		1.5	_	_	V	
I _{CCDR} [10]	Data retention current	$V_{CC} = 1.5 \text{ V}, \overline{CE}_1 \ge V_{CC} - 0.2 \text{ V}$ or $CE_2 \le 0.2 \text{ V}, V_{IN} \ge V_{CC} - 0.2 \text{ V}$ or $V_{IN} \le 0.2 \text{ V}$	Industrial / Automotive-A	-	1	4	μА
t _{CDR} [11]	Chip deselect to data retention time			0	_	_	ns
t _R ^[12]	Operation recovery time			45	_	_	ns

Data Retention Waveform

Figure 6. Data Retention Waveform [13]



Notes

^{9.} Typical values <u>are</u> included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.

10. Chip enables (CE₁ and CE₂) must be at CMOS level to meet the l_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

11. Tested initially and after any design or process changes that may affect these parameters.

12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.

13. CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.



Switching Characteristics

Over the Operating Range

Parameter [14]	Description	45 ns (Ir Autom	ndustrial/ otive-A)	Unit
	·	Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45	_	ns
t _{AA}	Address to data valid	-	45	ns
t _{OHA}	Data hold from address change	10	-	ns
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to data valid	-	45	ns
t _{DOE}	OE LOW to data valid	_	22	ns
t _{LZOE}	OE LOW to Low Z [15]	5	-	ns
t _{HZOE}	OE HIGH to High Z [15, 16]	-	18	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low Z ^[15]	10	_	ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High Z [15, 16]	-	18	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to Power-up	0	-	ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power-down	-	45	ns
Write Cycle [17	i	1		
t _{WC}	Write cycle time	45	_	ns
t _{SCE}	CE₁ LOW and CE₂ HIGH to write end	35	_	ns
t _{AW}	Address setup to write end	35	-	ns
t _{HA}	Address hold from write end	0	_	ns
t _{SA}	Address setup to Write Start	0	_	ns
t _{PWE}	WE pulse Width	35	-	ns
t _{SD}	Data setup to write end	25	-	ns
t _{HD}	Data hold from write end	0	-	ns
t _{HZWE}	WE LOW to High Z ^[15, 16]	-	18	ns
t _{LZWE}	WE HIGH to Low Z [15]	10	_	ns

^{14.} Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZCE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
17. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.



Switching Waveforms

Figure 7. Read Cycle 1 (Address transition controlled) [18, 19]

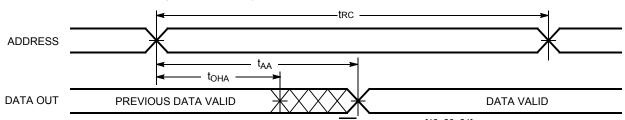


Figure 8. Read Cycle No. 2 (OE controlled) [19, 20, 21]

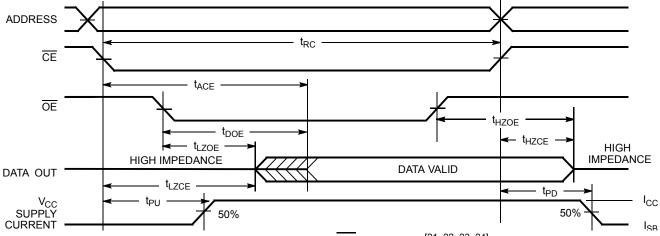
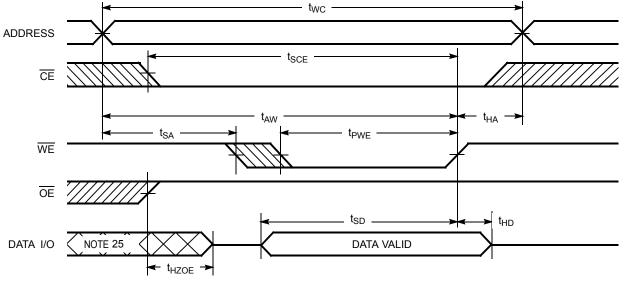


Figure 9. Write Cycle No. 1 (WE controlled) [21, 22, 23, 24]



- 18. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 19. WE is HIGH for read cycle.
- 20. Address valid before or similar to $\overline{\text{CE}}_1$ transition LOW and CE_2 transition HIGH.
- 21. CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.

 22. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
- 24. If $\overline{\text{CE}}_1$ goes $\overline{\text{HIGH}}$ or $\overline{\text{CE}}_2$ goes LOW simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.
- 25. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 (CE1 or CE2 controlled) [26, 27, 28, 29]

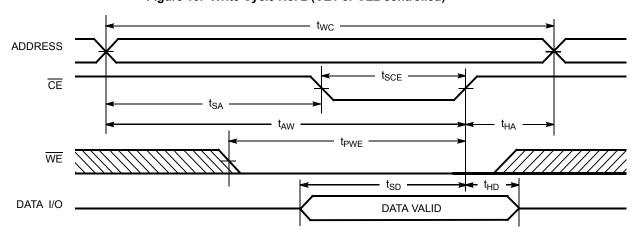
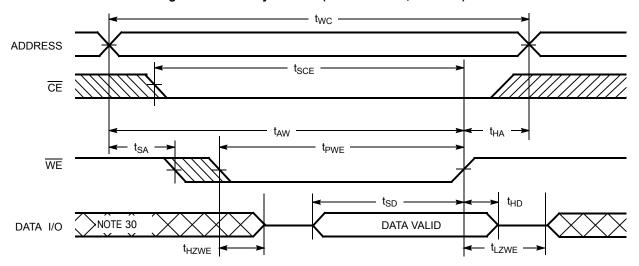


Figure 11. Write Cycle No. 3 (WE controlled, OE LOW) [26, 29]



Truth Table

CE ₁	CE ₂	WE	OE	Inputs/Outputs	Mode	Power
Н	X ^[31]	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	L	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	Data out	Read	Active (I _{CC})
L	Н	Н	Н	High Z	Output disabled	Active (I _{CC})
L	Н	L	Х	Data in	Write	Active (I _{CC})

- 26. CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.

 27. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.

 28. Data I/O is high impedance if OE = V_{IH}.

 29. If CE₁ goes HIGH or CE₂ goes LOW simultaneously with WE HIGH, the output remains iin high impedance state.

- 30. During this period, the I/Os are in output state. Do not apply input signals.

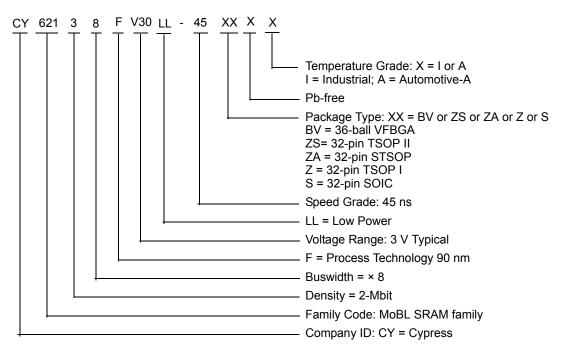
 31. The 'X' (Don't care) state for the Chip enables (CE₁ and CE₂) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	Industrial
	CY62138FV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
	CY62138FV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62138FV30LL-45ZXI	51-85056	32-pin TSOP I (Pb-free)	
	CY62138FV30LL-45SXI	51-85081	32-pin SOIC (Pb-free)	
	CY62138FV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

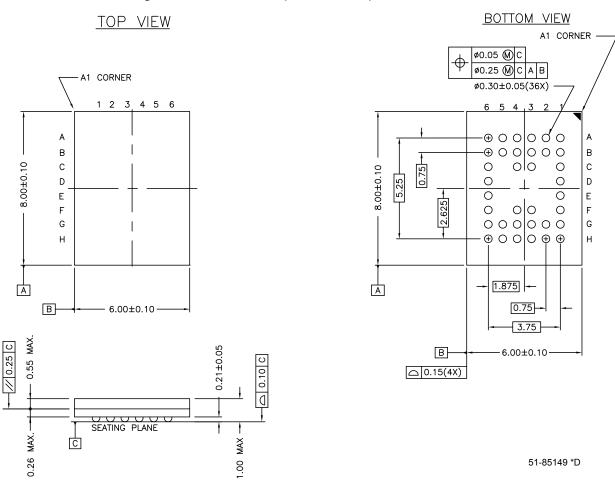
Ordering Code Definitions





Package Diagrams

Figure 12. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A, 51-85149





0.12 0.21 SEE DETAIL "A" **①** DIMENSIONS IN MILLIMETERS $\frac{\text{MIN.}}{\text{MAX.}}$ 10.03 10.29 TOP VIEW 0.95 1.05 0° MIN.-R. 0.12 MIN. 1.27 BSC --R. 0.12/0.25 0.25 1.20 MAX. 0.100 GAUGE PLANE

SEATING PLANE 0.05 0.15

0.40 0.60

DETAIL 'A'

Figure 13. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32, 51-85095

51-85095 *B

0*-5*

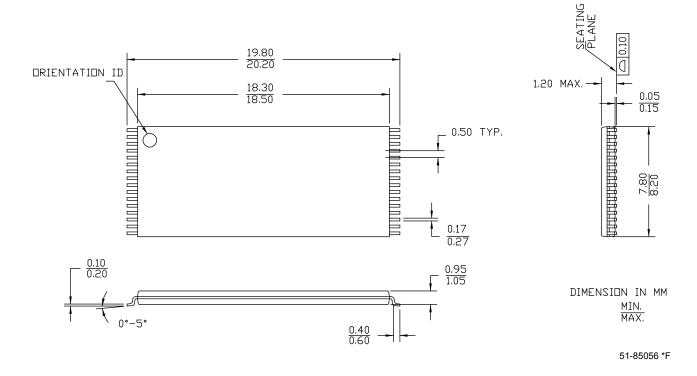


DIMENSIONS IN INCHES[MM] MIN. 0 MAX. PACKAGE WEIGHT 1.42gms 0.546[13.868] 0.566[14.376] PART #
S32.45 STANDARD PKG.
SZ32.45 LEAD FREE PKG. 32 0.006[0.152] 0.012[0.304] 0.793[20.142] 0.817[20.751] 0.101[2.565] 0.111[2.819] 0.118[2.997] | MAX. 0.047[1.193] 0.063[1.600] 0.004[0.102] 0.004[0.102] 0.050[1.270] _ MIN. BSC. 0.014[0.355] 0.020[0.508] SEATING PLANE-51-85081 *C

Figure 14. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45, 51-85081



Figure 15. 32-pin TSOP I (8 × 20 ×1.0 mm) Z32, 51-85056





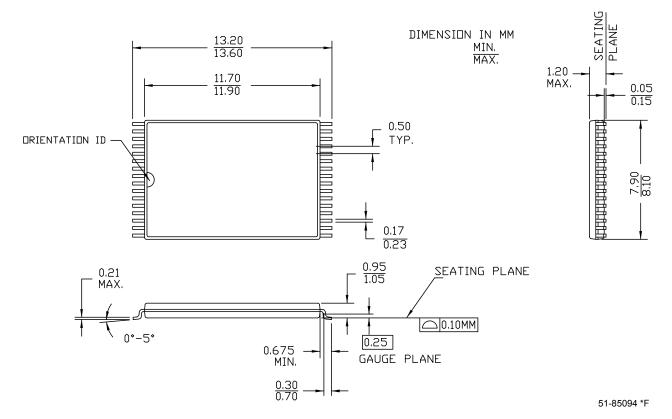


Figure 16. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32, 51-85094



Acronyms

Acronym	Description			
BGA	ball grid array			
CMOS	complementary metal oxide semiconductor			
I/O	input/output			
OE	output enable			
SOIC	small-outline integrated circuit			
SRAM	static random access memory			
STSOP	small thin small outline package			
TSOP	thin small outline package			
VFBGA	very fine-pitch ball grid array			
WE	write enable			

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
MHz	Mega Hertz		
μΑ	micro Amperes		
μS	micro seconds		
mA	milli Amperes		
mm	milli meter		
ns	nano seconds		
Ω	ohms		
%	percent		
pF	pico Farads		
V	Volts		
W	Watts		



Document History Page

Docum Docum	Document Title: CY62138FV30 MoBL [®] , 2-Mbit (256 K × 8) Static RAM Document Number: 001-08029					
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change		
**	463660	See ECN	NXR	New data sheet		
*A	467351	See ECN	NXR	Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages Changed ball A3 from NC to $\rm CE_2$ in 36-ball FBGA pin out		
*B	566724	See ECN	NXR	Converted from Preliminary to Final Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE $_1$ to OE and pin 22 from CE to CE $_1$) Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the $I_{SB2(typ)}$ value from 0.5 μ A to 1 μ A Changed the $I_{SB2(max)}$ value from 2.5 μ A to 5 μ A Changed the $I_{CCDR(typ)}$ value from 0.5 μ A to 1 μ A and $I_{CCDR(max)}$ value from 2.5 μ A to 4 μ A		
*C	797956	See ECN	VKN	Added 32-pin SOIC package Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table		
*D	809101	See ECN	VKN	Corrected typo in the Ordering Information table		
*E	940341	See ECN	VKN	Added footnote #7 related to I _{SB2} and I _{CCDR}		
*F	2769239	09/25/09	VKN/AESA	Included Automotive-A information		
*G	3055119	10/12/2010	RAME	Updated and converted all tablenotes into Footnote Added Acronyms and Units of Measure table Added Updated All Package Diagrams. Updated datasheet as per new template.		
*H	3061313	10/15/2010	RAME	Minor changes: Corrected "IO" to "I/O"		
*	3078557	11/04/2010	RAME	Corrected 55 C to -55C in Ambient Temperature with Power applied in Maximum Ratings Section		
*J	3235744	04/20/2011	RAME	Removed the note "For best practice recommendations, refer to the Cypress application Note "System Design Guidelines" at http://www.cypress.com " in page 1 and its reference in Functional Description. Updated Package Diagrams.		
*K	3285093	06/16/2011	RAME	Updated in new template.		



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

Wireless/RF

Automotive cypress.com/go/automotive Clocks & Buffers cypress.com/go/clocks Interface cypress.com/go/interface cypress.com/go/powerpsoc

cypress.com/go/plc
Memory cypress.com/go/memory
Optical & Image Sensing cypress.com/go/image
PSoC cypress.com/go/psoc
Touch Sensing cypress.com/go/touch
USB Controllers cypress.com/go/USB

cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document #: 001-08029 Rev. *K

Revised June 16, 2011

Page 18 of 18