- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced $V_{OH}$ (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **3-State Outputs**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Separation Controls for Data Flow in Each Direction**
- **Back-to-Back Latches for Storage**
- **CY54FCT543T**
  - **48-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT543T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**

**CY54FCT543T . . . D PACKAGE**
**CY74FCT543T . . . Q OR SO PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{LEBA}$ | 1 | 24 | $V_{CC}$ |
| $\overline{OEBA}$ | 2 | 23 | $\overline{CEBA}$ |
| $A_0$ | 3 | 22 | $B_0$ |
| $A_1$ | 4 | 21 | $B_1$ |
| $A_2$ | 5 | 20 | $B_2$ |
| $A_3$ | 6 | 19 | $B_3$ |
| $A_4$ | 7 | 18 | $B_4$ |
| $A_5$ | 8 | 17 | $B_5$ |
| $A_6$ | 9 | 16 | $B_6$ |
| $A_7$ | 10 | 15 | $B_7$ |
| $\overline{CEAB}$ | 11 | 14 | $\overline{LEAB}$ |
| GND | 12 | 13 | $\overline{OEAB}$ |
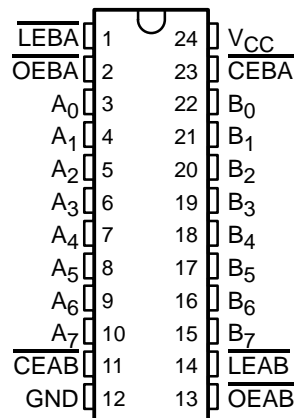
## description

The 'FCT543T octal latched transceivers contain two sets of eight D-type latches with separate latch-enable ($\overline{LEAB}$, $\overline{LEBA}$) and output-enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs for each set to permit independent control of input and output in either direction of data flow. For data flow from A to B, for example, the A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to take data from B, as indicated in the function table. With $\overline{CEAB}$ low, a low signal on the A-to-B latch-enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ low, the 3-state B-output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TEXAS INSTRUMENTS**

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### PIN DESCRIPTION

| NAME | DESCRIPTION |
|------|-------------|
| $\overline{\text{OEAB}}$ | A-to-B output-enable input (active low) |
| $\overline{\text{OEBA}}$ | B-to-A output-enable input (active low) |
| $\overline{\text{CEAB}}$ | A-to-B enable input (active low) |
| $\overline{\text{CEBA}}$ | B-to-A enable input (active low) |
| $\overline{\text{LEAB}}$ | A-to-B latch-enable input (active low) |
| $\overline{\text{LEBA}}$ | B-to-A latch-enable input (active low) |
| A | A-to-B data inputs or B-to-A 3-state outputs |
| B | B-to-A data inputs or A-to-B 3-state outputs |

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------|----------|--|------------|-----------------------|------------------|
| −40°C to 85°C | QSOP – Q | Tape and reel | 5.3 | CY74FCT543CTQCT | FCT543C |
| | SOIC – SO | Tube | 5.3 | CY74FCT543CTSOC | FCT543C |
| | | Tape and reel | 5.3 | CY74FCT543CTSOCT | |
| | QSOP – Q | Tape and reel | 6.5 | CY74FCT543ATQCT | FCT543A |
| | SOIC – SO | Tube | 6.5 | CY74FCT543ATSOC | FCT543A |
| | | Tape and reel | 6.5 | CY74FCT543ATSOCT | |
| | QSOP – Q | Tape and reel | 8.5 | CY74FCT543TQCT | FCT543 |
| | SOIC – SO | Tube | 8.5 | CY74FCT543TSOC | FCT543 |
| | | Tape and reel | 8.5 | CY74FCT543TSOCT | |
| −55°C to 125°C | CDIP – D | Tube | 10 | CY54FCT543TDMB | |
| | | Tube | 10 | CY54FCT543TLMB | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### FUNCTION TABLE‡

| INPUTS | | | LATCH A TO B§ | OUTPUT B |
|--------|--|--|----------------|----------|
| $\overline{\text{CEAB}}$ | $\overline{\text{LEAB}}$ | $\overline{\text{OEAB}}$ | | |
| H | X | X | Storing | Z |
| X | H | X | Storing | X |
| X | X | H | X | Z |
| L | L | L | Transparent | Current A inputs |
| L | H | L | Storing | Previous A inputs |

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state

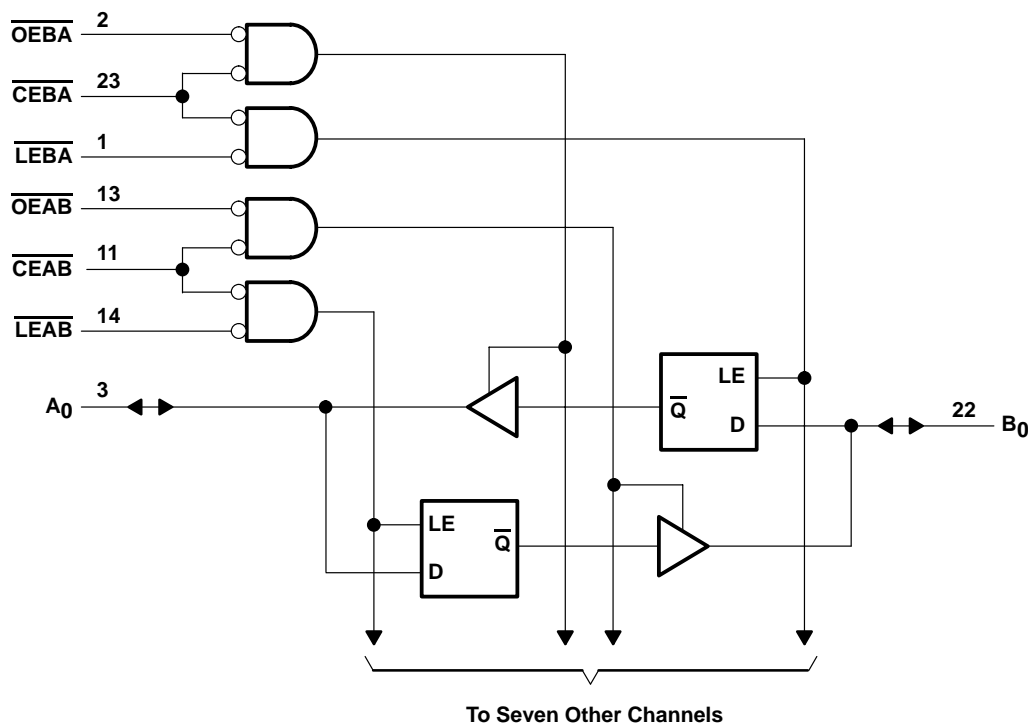‡ A-to-B data flow shown; B-to-A flow control is the same, except uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

§ Before $\overline{\text{LEAB}}$ low-to-high transition

**TEXAS INSTRUMENTS**

## logic diagram (positive logic)



To Seven Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range to ground potential | −0.5 V to 7 V |
| DC input voltage range | −0.5 V to 7 V |
| DC output voltage range | −0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package | 61°C/W |
| SO package | 46°C/W |
| Ambient temperature range with power applied, $T_A$ | −65°C to 135°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 2)

| | | CY54FCT543T | | | CY74FCT543T | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −12 | | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | −40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.

# CY54FCT543T, CY74FCT543T
## 8-BIT LATCHED REGISTERED TRANSCEIVERS
## WITH 3-STATE OUTPUTS

SCCS030A – MAY 1994 – REVISED OCTOBER 2001

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | | CY54FCT543T | | | CY74FCT543T | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_{IN}$ = −18 mA | | −0.7 | −1.2 | | | | V |
| | $V_{CC}$ = 4.75 V, | $I_{IN}$ = −18 mA | | | | | −0.7 | −1.2 | |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −12 mA | 2.4 | 3.3 | | | | | V |
| | $V_{CC}$ = 4.75 V | $I_{OH}$ = −32 mA | | | | 2 | | | |
| | | $I_{OH}$ = −15 mA | | | | 2.4 | 3.3 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.3 | 0.55 | | | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 64 mA | | | | | 0.3 | 0.55 | |
| $V_{hys}$ | All inputs | | | 0.2 | | | 0.2 | | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_{IN}$ = $V_{CC}$ | | | 5 | | | | μA |
| | $V_{CC}$ = 5.25 V, | $V_{IN}$ = $V_{CC}$ | | | | | | 5 | |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_{IN}$ = 2.7 V | | | ±1 | | | | μA |
| | $V_{CC}$ = 5.25 V, | $V_{IN}$ = 2.7 V | | | | | | ±1 | |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_{IN}$ = 0.5 V | | | ±1 | | | | μA |
| | $V_{CC}$ = 5.25 V, | $V_{IN}$ = 0.5 V | | | | | | ±1 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_{OUT}$ = 2.7 V | | | 10 | | | | μA |
| | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 2.7 V | | | | | | 10 | |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_{OUT}$ = 0.5 V | | | −10 | | | | μA |
| | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0.5 V | | | | | | −10 | |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_{OUT}$ = 0 V | −60 | −120 | −225 | | | | mA |
| | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0 V | | | | −60 | −120 | −225 | |
| $I_{off}$ | $V_{CC}$ = 0 V, | $V_{OUT}$ = 4.5 V | | | ±1 | | | ±1 | μA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $V_{IN} \le$ 0.2 V, $V_{IN} \ge V_{CC}$ − 0.2 V | | | 0.1 | 0.2 | | | | mA |
| | $V_{CC}$ = 5.25 V, $V_{IN} \le$ 0.2 V, $V_{IN} \ge V_{CC}$ − 0.2 V | | | | | | 0.1 | 0.2 | |
| $\Delta I_{CC}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 3.4 V§, $f_1$ = 0, Outputs open | | | 0.5 | 2 | | | | mA |
| | $V_{CC}$ = 5.25 V, $V_{IN}$ = 3.4 V§, $f_1$ = 0, Outputs open | | | | | | 0.5 | 2 | |
| $I_{CCD}$¶ | $V_{CC}$ = 5.5 V, Outputs open, One input switching at 50% duty cycle, $\overline{CEAB}$ and $\overline{OEAB}$ = low, $\overline{CEBA}$ = high, $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ − 0.2 V | | | 0.06 | 0.12 | | | | mA/ MHz |
| | $V_{CC}$ = 5.25 V, Outputs open, One input switching at 50% duty cycle, $\overline{CEAB}$ and $\overline{OEAB}$ = low, $\overline{CEBA}$ = high, $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ − 0.2 V | | | | | | 0.06 | 0.12 | |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

§ Per TTL-driven input ($V_{IN}$ = 3.4 V); all other inputs at $V_{CC}$ or GND

¶ This parameter is derived for use in total power-supply calculations.

**TEXAS INSTRUMENTS**

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

| PARAMETER | TEST CONDITIONS | | | CY54FCT543T | | | CY74FCT543T | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $I_C$# | $V_{CC}$ = 5.5 V, $f_0$ = 10 MHz, Outputs open, $\overline{CEAB}$ and $\overline{OEAB}$ = low, $\overline{CEBA}$ = high, $f_0 = \overline{LEAB}$ = 10 MHz | One bit switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V | | 0.7 | 1.4 | | | | mA |
| | | | $V_{IN}$ = 3.4 V or GND | | 1.2 | 3.4 | | | | |
| | | Eight bits switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V | | 2.8 | 5.6‖ | | | | |
| | | | $V_{IN}$ = 3.4 V or GND | | 5.1 | 14.6‖ | | | | |
| | $V_{CC}$ = 5.25 V, $f_0$ = 10 MHz, Outputs open, $\overline{CEAB}$ and $\overline{OEAB}$ = low, $\overline{CEBA}$ = high, $f_0 = \overline{LEAB}$ = 10 MHz | One bit switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V | | | | | 0.7 | 1.4 | |
| | | | $V_{IN}$ = 3.4 V or GND | | | | | 1.2 | 3.4 | |
| | | Eight bits switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V | | | | | 2.8 | 5.6‖ | |
| | | | $V_{IN}$ = 3.4 V or GND | | | | | 5.1 | 14.6‖ | |
| $C_i$ | | | | | 5 | 10 | | 5 | 10 | pF |
| $C_o$ | | | | | 9 | 12 | | 9 | 12 | pF |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

\# $I_C$ $= I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$

$I_{CC}$ = Quiescent current with CMOS input levels

$\Delta I_{CC}$ = Power-supply current for a TTL high input ($V_{IN}$ = 3.4 V)

$D_H$ = Duty cycle for TTL inputs high

$N_T$ = Number of TTL inputs at $D_H$

$I_{CCD}$ = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$ = Clock frequency for registered devices, otherwise zero

$f_1$ = Input signal frequency

$N_1$ = Number of inputs changing at $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the $I_{CC}$ formula.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| | PARAMETER | CY54FCT543T | | CY74FCT543T | | CY74FCT543AT | | CY74FCT543CT | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before $\overline{LEAB}\downarrow$ or $\overline{LEBA}\downarrow$ | 3 | | 2 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after $\overline{LEAB}\downarrow$ or $\overline{LEBA}\downarrow$ | 2 | | 2 | | 2 | | 2 | | ns |

**TEXAS INSTRUMENTS**

**switching characteristics over operating free-air temperature range (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY54FCT543T | | CY74FCT543T | | CY74FCT543AT | | CY74FCT543CT | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2 | 10 | 2.5 | 8.5 | 2.5 | 6.5 | 2.5 | 5.3 | ns |
| $t_{PHL}$ | | | 2 | 10 | 2.5 | 8.5 | 2.5 | 6.5 | 2.5 | 5.3 | |
| $t_{PLH}$ | $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$ | A or B | 2.5 | 14 | 2.5 | 12.5 | 2.5 | 8 | 2.5 | 7 | ns |
| $t_{PHL}$ | | | 2.5 | 14 | 2.5 | 12.5 | 2.5 | 8 | 2.5 | 7 | |
| $t_{PZH}$ | $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ | A or B | 2 | 14 | 2 | 12 | 2 | 9 | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 14 | 2 | 12 | 2 | 9 | 2 | 8 | |
| $t_{PZH}$ | $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ | A or B | 2 | 14 | 2 | 12 | 2 | 9 | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 14 | 2 | 12 | 2 | 9 | 2 | 8 | |
| $t_{PHZ}$ | $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ | A or B | 2 | 13 | 2 | 9 | 2 | 7.5 | 2 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 13 | 2 | 9 | 2 | 7.5 | 2 | 6.5 | |
| $t_{PHZ}$ | $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ | A or B | 2 | 13 | 2 | 9 | 2 | 7.5 | 2 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 13 | 2 | 9 | 2 | 7.5 | 2 | 6.5 | |

**TEXAS INSTRUMENTS**

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## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

**LOAD CIRCUIT FOR**
**TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR**
**3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS**
**PULSE DURATION**

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**
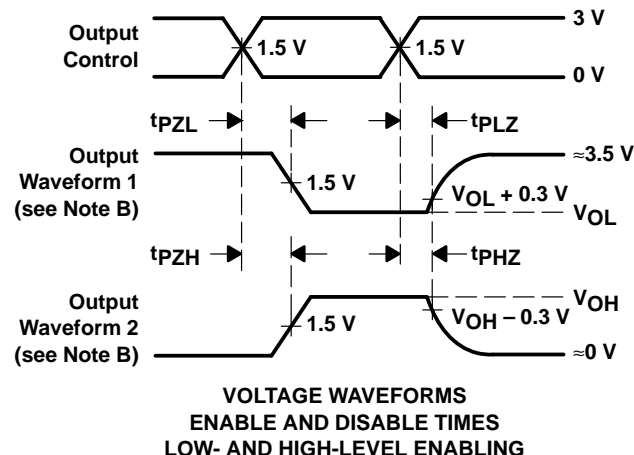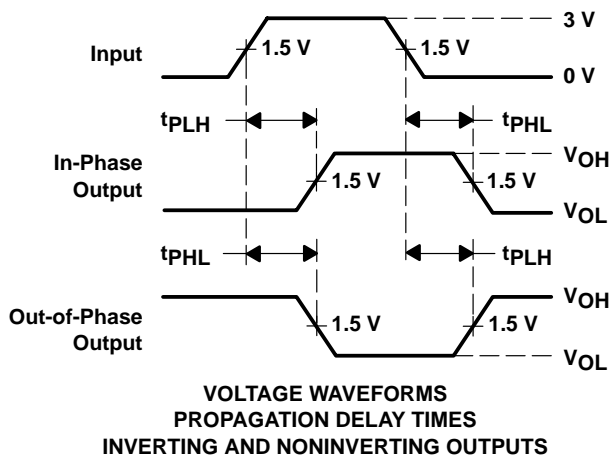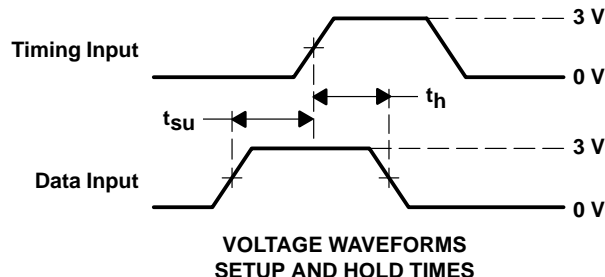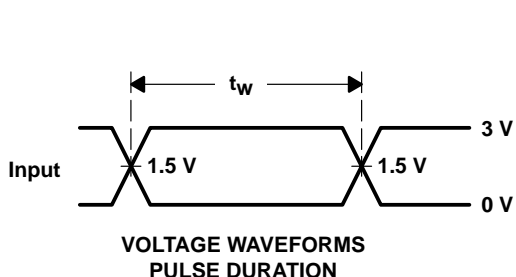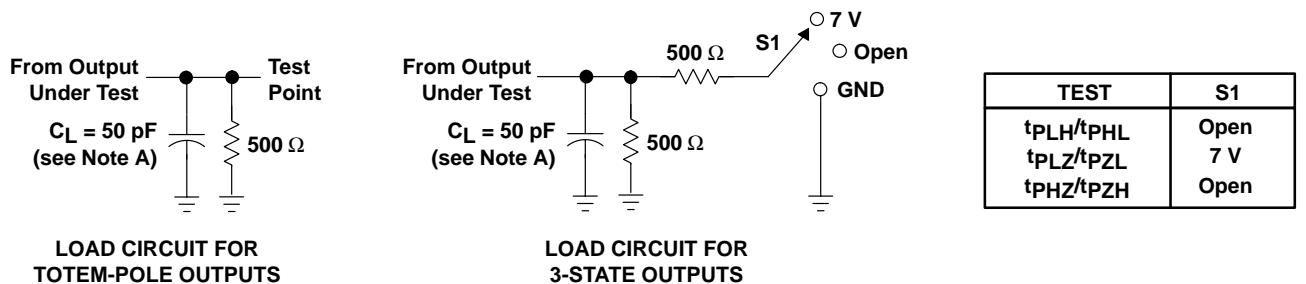
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 5962-9222101M3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9222101MLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CY54FCT543TDMB | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CY54FCT543TLMB | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| CY74FCT543ATQCT | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543ATQCTE4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543ATQCTG4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543ATSOC | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543ATSOCE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543ATSOCG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543ATSOCT | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543ATSOCTE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543ATSOCTG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTQCT | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543CTQCTE4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543CTQCTG4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543CTSOC | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTSOCE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTSOCG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTSOCT | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTSOCTE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543CTSOCTG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543TQCT | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543TQCTE4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543TQCTG4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT543TSOC | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543TSOCE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| CY74FCT543TSOCG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543TSOCT | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543TSOCTE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CY74FCT543TSOCTG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

**[1]** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**[2]** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**[3]** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CY74FCT543ATQCT | SSOP/ QSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT543ATSOCT | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CY74FCT543CTQCT | SSOP/ QSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT543CTSOCT | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CY74FCT543TQCT | SSOP/ QSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT543TSOCT | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CY74FCT543ATQCT | SSOP/QSOP | DBQ | 24 | 2500 | 346.0 | 346.0 | 33.0 |
| CY74FCT543ATSOCT | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |
| CY74FCT543CTQCT | SSOP/QSOP | DBQ | 24 | 2500 | 346.0 | 346.0 | 33.0 |
| CY74FCT543CTSOCT | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |
| CY74FCT543TQCT | SSOP/QSOP | DBQ | 24 | 2500 | 346.0 | 346.0 | 33.0 |
| CY74FCT543TSOCT | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |

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