

1:10 Clock Fanout Buffer

Features

- Low voltage operation
- Full range support:
 - 3.3V
 - 2.5V
 - 1.8V
- Over voltage tolerant input hot swappable
- 1:10 Fanout
- Drives either a 50-Ohm or 75-Ohm load
- Low input capacitance
- Low output skew
- Low propagation delay
- Typical (t_{pd} less than 4 ns)
- High speed operation:
 - 200 MHz at 1.8V
 - 650 MHz at 2.5V and 3.3V
- Industrial versions available
- Available packages include: SOIC, SSOP

Description

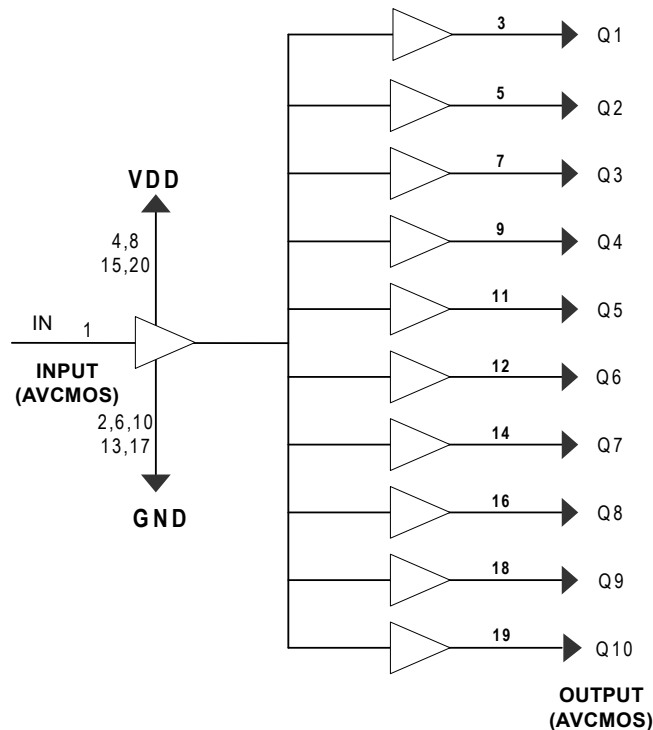
The Cypress series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC910 fanout buffer features one input and 10 outputs. It is ideal for conversion from and to 3.3V, 2.5V, and 1.8V

Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

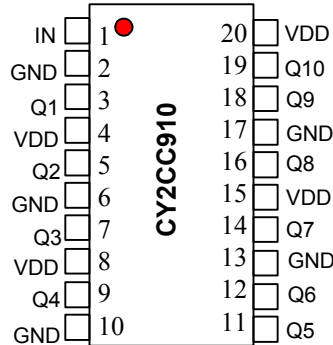
Cypress employs the unique AVCMOS type outputs VOI (Variable Output Impedance) that dynamically adjust for variable impedance matching, eliminate the need for series damping resistors, and reduce overall noise.

Logic Block Diagram



Pin Configuration

Figure 1. 20-Pin SOIP-SSOP



20 pin SOIC/SSOP

Pin Description

Pin Number	Pin Name	Description
1	IN	Input
2,6,10,13,17	GND	Ground
4,8,15,20	V _{DD}	Power Supply
3,5,7,9,11,12,14,16,18,19	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10	Output

Maximum Ratings^[1]

Storage Temperature: -65°C to +150°C
 Ambient Temperature: -40°C to +85°C
 Supply Voltage to Ground Potential
 V_{CC} -0.5V to 4.6V
 Input -0.5V to 5.8V

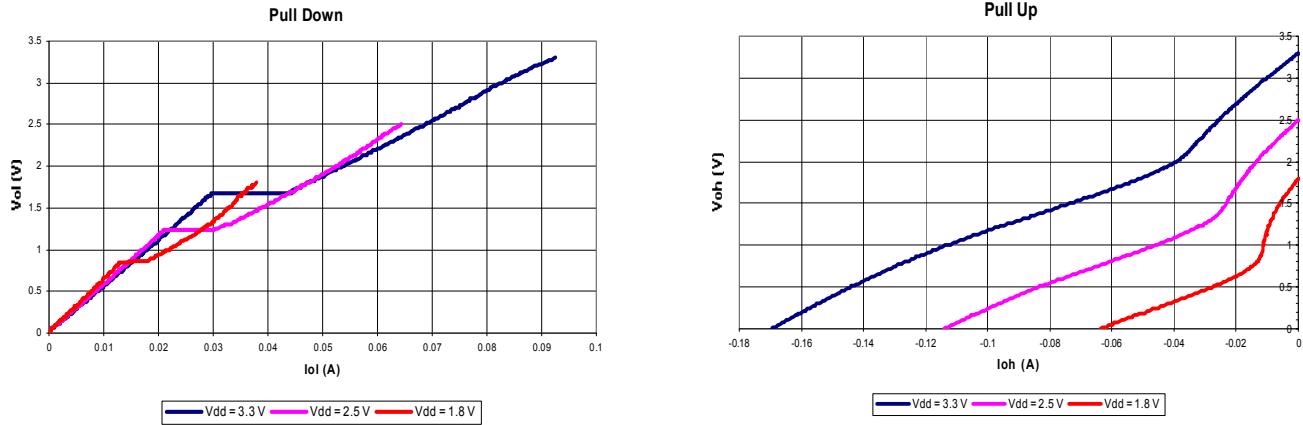
Supply Voltage to Ground Potential
 (Outputs only) -0.5V to V_{DD} + 1V
 DC Output Voltage -0.5V to V_{DD} + 1V
 Power Dissipation 0.75W

Note

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Variable Output Impedance Control (VOI)

Figure 2. Output Voltage versus Output Current ($T_A = 25^\circ\text{C}$)



DC Electrical Characteristics

At 3.3V (See Figure 3)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -12 mA	2.3	3.3		V
V _{OL}	Output Low Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA		0.2	0.5	V
V _{IH}	Input High Voltage	Guaranteed Logic High Level	2		5.8	V
V _{IL}	Input Low Voltage	Guaranteed Logic Low Level			0.8	V
I _{IH}	Input High Current	V _{DD} = Max. V _{IN} = 2.7V			1	μA
I _{IL}	Input Low Current	V _{DD} = Max. V _{IN} = 0.5V			-1	μA
I _I	Input High Current	V _{DD} = Max., V _{IN} = V _{DD} (Max.)			20	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OK}	Continuous Clamp Current	V _{DD} = Max., V _{OUT} = GND			-50	mA
O _{OFF}	Power-down Disable	V _{DD} = GND, V _{OUT} = < 4.5V			100	μA
V _H	Input Hysteresis			80		mV

At 2.5V (See [Figure 3](#))

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -7 mA	1.8		V
			I _{OH} = 12 mA	1.6		V
V _{OL}	Output Low Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}			0.65	V
V _{IH}	Input High Voltage	Guaranteed Logic High Level	1.6		5.0	V
V _{IL}	Input Low Voltage	Guaranteed Logic Low Level			0.8	V
I _{IH}	Input High Current	V _{DD} = Max.			1	μA
I _{IL}	Input Low Current	V _{DD} = Max.			-1	μA
I _I	Input High Current	V _{DD} = Max., V _{IN} = V _{DD} (Max.)			20	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OK}	Continuous Clamp Current	V _{DD} = Max., V _{OUT} = GND			-50	mA
O _{OFF}	Power Down Disable	V _{DD} = GND, V _{OUT} = < 4.5V			100	μA
V _H	Input Hysteresis			80		mV

At 1.8V (See [Figure 7](#))

Parameter	Description	Test Condition ^[2]	Min	Max	Unit
V _{DD}	Supply Voltage		1.71	1.89	V
V _{IH}	Input High Voltage		0.65V _{DD} [1.1]	4.3	V
V _{IL}	Input Low Voltage		-0.3	0.35 V _{DD} [0.6]	V
V _{OH}	Output High Voltage	I _{OH} = -2 mA	V _{DD} - 0.45[1.2]		V
V _{OL}	Output Low Voltage	I _{OH} = 2 mA		0.45	V

Capacitance

Parameter	Description	Test Conditions	Typ	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	2.5		pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5		pF

Power Supply Characteristics (See [Figure 3](#))

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
ΔI _{CC}	Delta I _{CC} Quiescent Power Supply Current	(I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD}) - (I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD} - 0.6V)			50	μA
I _{CCD}	Dynamic Power Supply Current	V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/ MHZ
I _C	Total Power Supply Current	V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open f _L = 40 MHZ			25	mA

Note

2. Test load conditions: 500-Ohm to ground with approximately 6-pF total loading and 200-MHz maximum frequency.

High Frequency Parametrics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
D _J	Jitter, Deterministic	50% duty cycle t _W (50–50) The “point to point load circuit” Output Jitter – Input Jitter			20	ps
F _{max} 3.3V	Maximum frequency V _{DD} = 3.3V	50% duty cycle t _W (50–50) Standard Load Circuit.			160	MHz
		50% duty cycle t _W (50–50) The “point to point load circuit”			650	
F _{max} 2.5V	Maximum frequency V _{DD} = 2.5V	The “point-to-point load circuit” V _{IN} = 2.4V/0.0V V _{OUT} = 1.7V/0.7V			200	MHz
F _{max} 1.8V	Maximum frequency V _{DD} = 1.8V	The “6-pF load circuit” V _{IN} = 1.7/0.0V V _{OUT} = 1.2V/0.4V			200	MHz
F _{max(20)}	Maximum frequency V _{DD} = 3.3V	20% duty cycle t _W (20–80) The “point to point load circuit” V _{IN} = 3.0V/0.0V V _{OUT} = 2.3V/0.4V			250	MHz
t _W 3.3V	Minimum pulse V _{DD} = 3.3V	The “point-to-point load circuit” V _{IN} = 3.0V/0.0V F = 100 MHz V _{OUT} = 2.0V/0.8V	1			ns
t _W 2.5V	Minimum pulse V _{DD} = 2.5V	The “point-to-point load circuit” V _{IN} = 2.4V/0.0V F = 100 MHz V _{OUT} = 1.7V/0.7V	1			ns
t _W 1.8V	Minimum pulse V _{DD} = 1.8V	The “6-pF load circuit” V _{IN} = 1.7V/0.0V V _{OUT} = 1.2V/0.4V	1			ns

AC Switching Characteristics

At 3.3V (V_{DD} = 3.3V ± 5%, Temperature = –40°C to +85°C)

Parameter	Description	Min	Typ	Max	Unit	
t _{PLH}	Propagation Delay – Low to High	See Figure 4	1.5	2.7	3.5	ns
t _{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	ns
t _R	Output Rise Time			0.8		V/ns
t _F	Output Fall Time			0.8		V/ns
t _{SK(0)}	Output Skew: Skew between outputs of the same package (in phase).	See Figure 11		0.2	ns	
t _{SK(p)}	Pulse Skew: Skew between opposite transitions of the same output (t _{PHL} – t _{PLH}).	See Figure 10		0.2	ns	
t _{SK(t)}	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 12		0.4	ns	

At 2.5V (V_{DD} = 2.5V ± 5%, Temperature = –40°C to +85°C)

Parameter	Description	Min	Typ	Max	Unit	
t _{PLH}	Propagation Delay – Low to High	See Figure 4	1.5	2.7	3.5	ns
t _{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	ns
t _R	Output Rise Time			0.8		V/ns
t _F	Output Fall Time			0.8		V/ns
t _{SK(0)}	Output Skew: Skew between outputs of the same package (in phase).	See Figure 11		0.2	ns	
t _{SK(p)}	Pulse Skew: Skew between opposite transitions of the same output (t _{PHL} – t _{PLH}).	See Figure 10		0.2	ns	
t _{SK(t)}	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 12		0.4	ns	

AC Switching Characteristics

At 1.8V ($V_{DD} = 1.8V \pm 5\%$, Temperature = $-40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Description	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay – Low to High	1.5	2.7	3.5	ns
t_{PHL}	Propagation Delay – High to Low	1.5	2.7	3.5	ns
t_R	Output Rise Time 20 – 80%	0.2		1.5	ns
t_F	Output Fall Time 20 – 80%	0.2		1.5	ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase).			0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$).			0.2	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.			0.4	ns

Parameter Measurement Information: V_{DD} at 3.3V to 2.5V

Figure 3. Load Circuit [3,4,5]

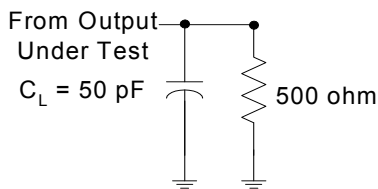


Figure 5. Point to Point Load Circuit [3,4,5]

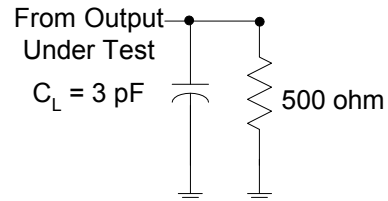


Figure 4. Voltage Waveforms Propagation Delay Times [6]

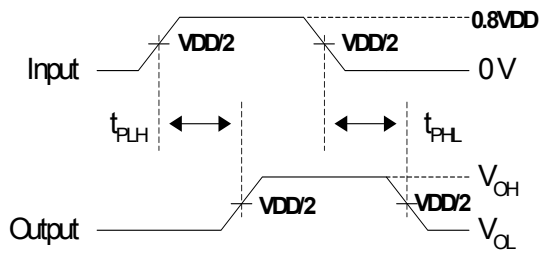
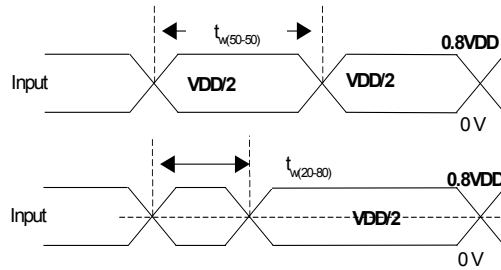


Figure 6. Voltage Waveforms – Pulse Duration [4]



Parameter Measurement Information: V_{DD} at 8V

Figure 7. Load Circuit [3,4,5]

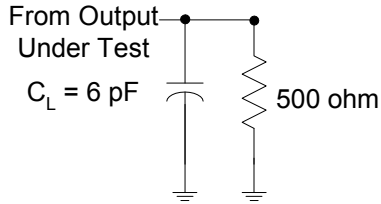


Figure 8. Voltage Waveforms Propagation

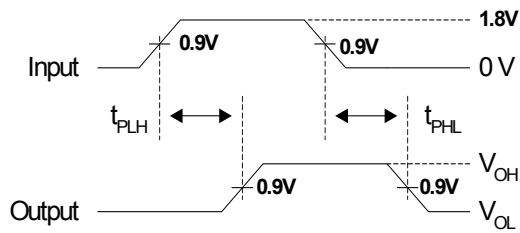


Figure 9. Voltage Waveforms – Pulse Duration [4]

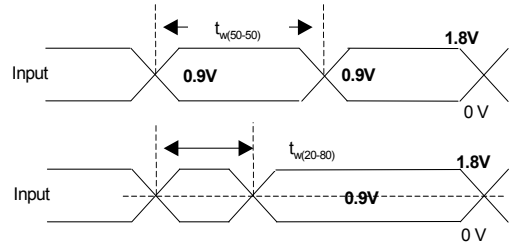


Figure 10. Pulse Skew - $tsk_{(p)}$

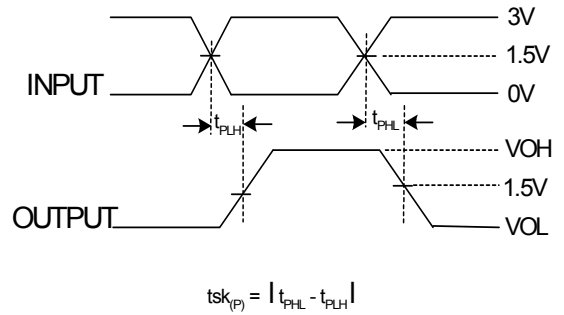
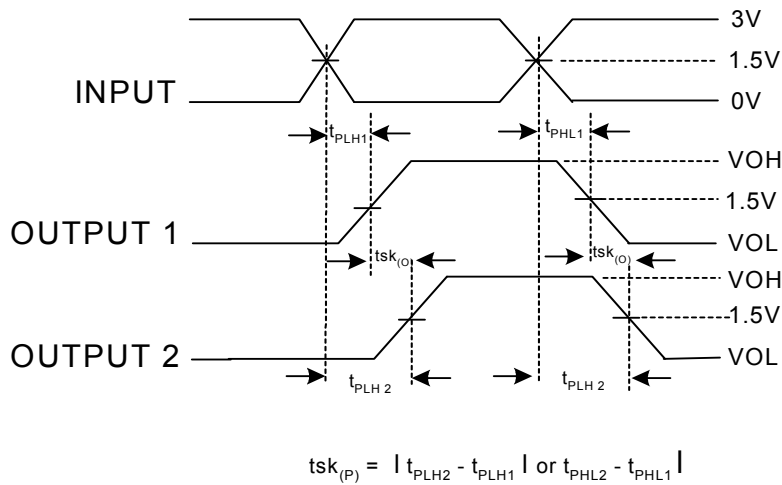


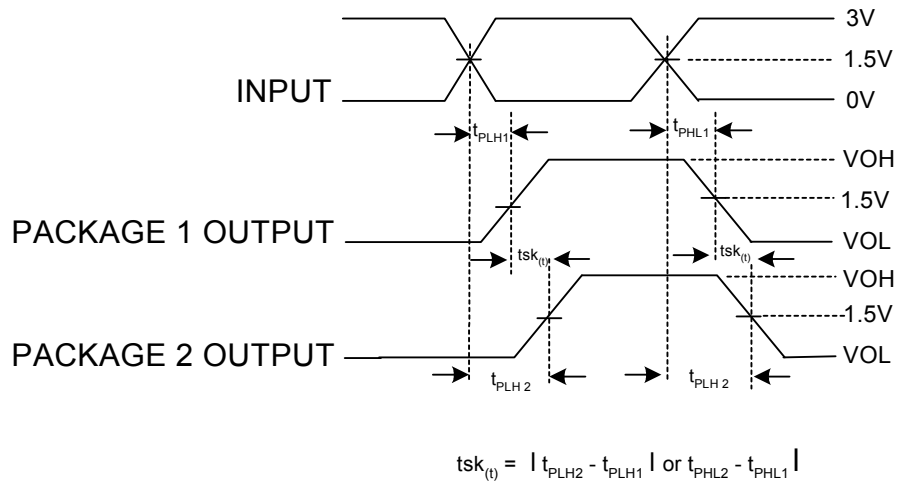
Figure 11. Output Skew - $tsk_{(o)}$



Notes

3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, $Z_0 = 50\Omega$, $t_R < 2.5 \text{ ns}$, $t_F < 2.5 \text{ ns}$.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd} .

Figure 12. Package Skew - $tsk_{(t)}$

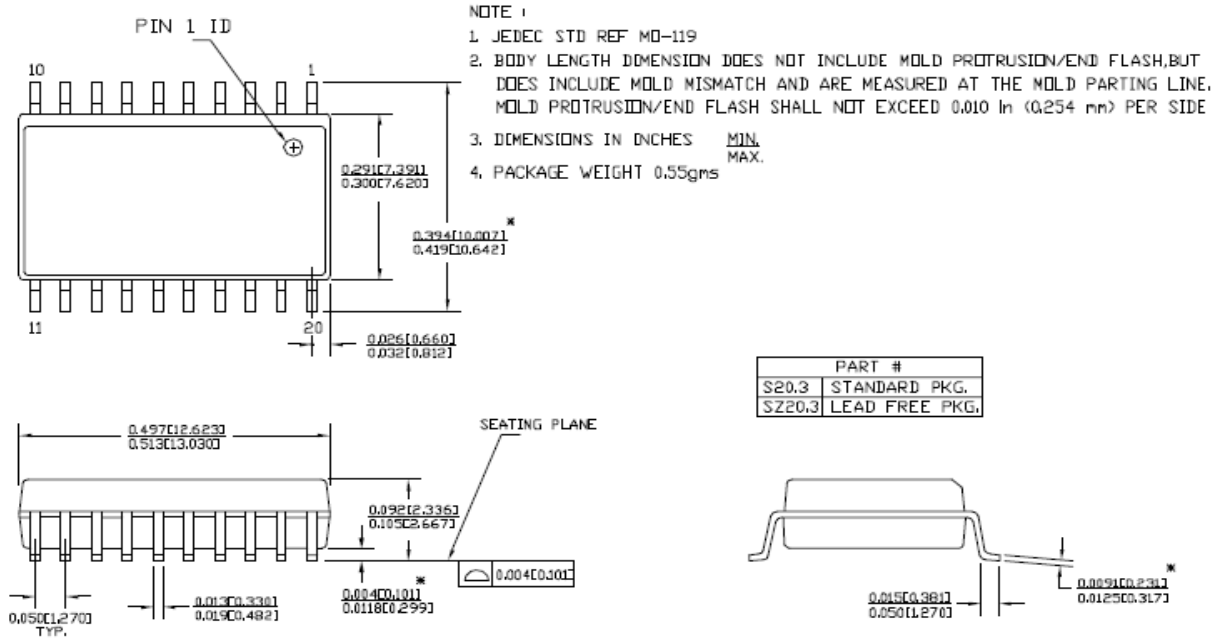


Ordering Information

Part Number	Package Type	Product Flow	Status
CY2CC910SI	20-pin SOIC	Industrial, -40° to 85°C	Obsolete
CY2CC910SIT	20-pin SOIC-Tape and Reel	Industrial, -40° to 85°C	Obsolete
CY2CC910SC	20-pin SOIC	Commercial, 0°C to 70°C	Obsolete
CY2CC910SCT	20-pin SOIC-Tape and Reel	Commercial, 0°C to 70°C	Obsolete
CY2CC910OI	20-pin SSOP	Industrial, -40° to 85°C	Obsolete
CY2CC910OIT	20-pin SSOP-Tape and Reel	Industrial, -40° to 85°C	Obsolete
CY2CC910OC	20-pin SSOP	Commercial, 0°C to 70°C	Obsolete
CY2CC910OCT	20-pin SSOP-Tape and Reel	Commercial, 0°C to 70°C	Obsolete
Pb-free			
CY2CC910OXI	20-pin SSOP	Industrial, -40° to 85°C	Active
CY2CC910OXIT	20-pin SSOP-Tape and Reel	Industrial, -40° to 85°C	Active
CY2CC910OXC	20-pin SSOP	Commercial, 0°C to 70°C	Active
CY2CC910OXCT	20-pin SSOP-Tape and Reel	Commercial, 0°C to 70°C	Active

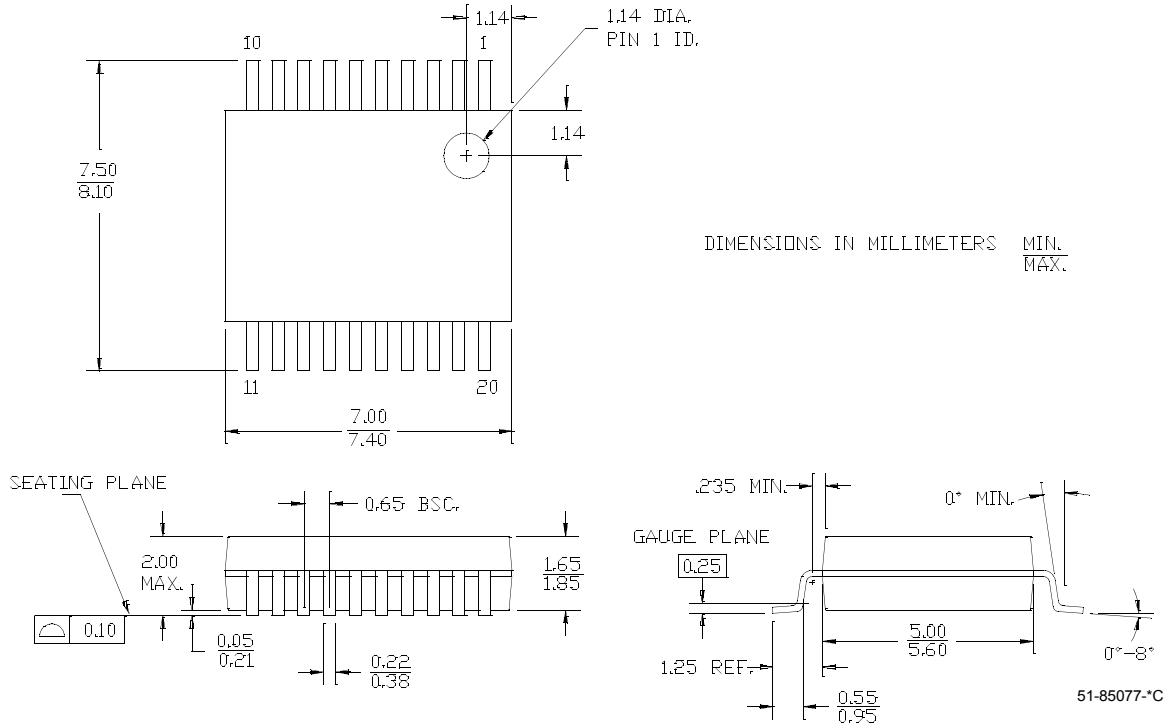
Package Drawing and Dimensions

Figure 13. 20-Pin (300-Mil) SOIC S5 (51-85024)



51-85024 *C

Figure 14. 20-Pin Shrunk Small Outline Package O20



Document History Page

Document Title: CY2CC910 1:10 Clock Fanout Buffer Document No: 38-07348				
Rev.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	114318	TSM	05/10/02	New Data Sheet
*A	119148	RGL	10/07/02	Added 5.8 as the Max. value for V_{IH} in the DC Electrical Characteristics @3.3V table. Changed the Max. value of V_{IH} from 5.8 to 5.0 in the DC Electrical Characteristics @2.5V table. Changed the value of V_{IH} from $V_{DD}+0.3$ [2.25] to 4.3 in the DC Electrical Characteristics @1.8V table.
*B	404287	RGL	See ECN	Added Lead-free devices for SSOP
*C	2595534	CXQ/PYRS	10/23/08	Added "Status" column to Ordering Information table Updated Package Diagram 51-85024 Updated template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2002-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.