

2.5 V or 3.3 V, 200-MHz, 1:10 Clock Distribution Buffer

Features

- 2.5 V or 3.3 V operation
- 200-MHz clock support
- Two LVCMOS-/LVTTTL-compatible inputs
- Ten clock outputs: drive up to 20 clock lines
- 1× or 1/2× configurable outputs
- Output three-state control
- 250-ps max output-to-output skew
- Pin-compatible with MPC946, MPC9446
- Available in commercial and industrial temperature range
- 32-pin TQFP package

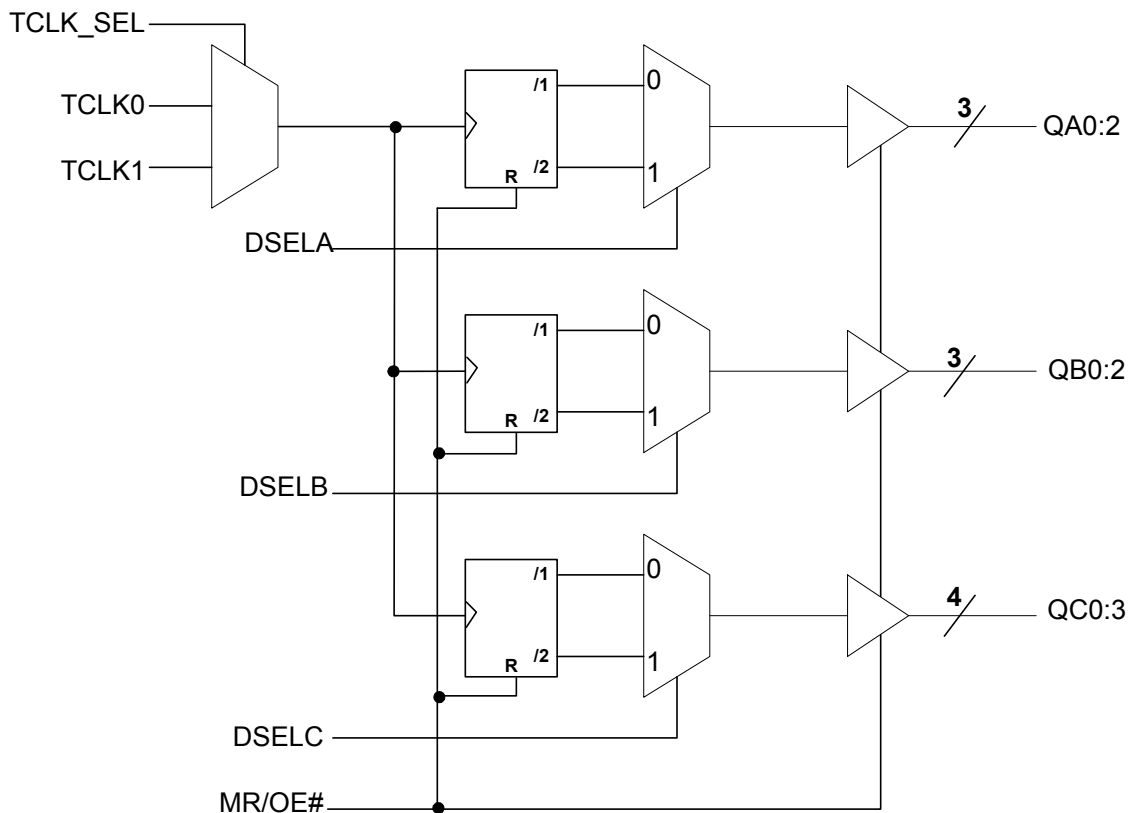
Description

The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTTL compatible. The 10 outputs are LVCMOS or LVTTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

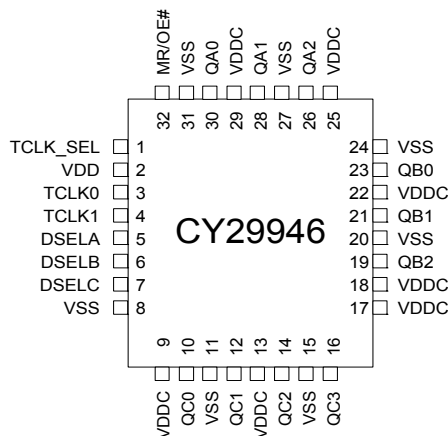
The CY29946 is capable of generating 1× and 1/2× signals from a 1× source. These signals are generated and retimed internally to ensure minimal skew between the 1× and 1/2× signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1× to 1/2× outputs.

The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description^[1]

Pin	Name	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 Bank is being used in /2 Mode, a reset must be performed (MR/OE# Asserted High) after power-up to ensure all internal flip-flops are set to the same state.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5 V or 3.3 V Power Supply for Output Clock Buffers
2	VDD			2.5 V or 3.3 V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

Note

1. PD = Internal pull-down. PU = Internal pull-up.

Absolute Maximum Conditions^[2]

Maximum Input Voltage Relative to V_{SS} $V_{SS} - 0.3$ V
 Maximum Input Voltage Relative to V_{DD} $V_{DD} + 0.3$ V
 Storage Temperature -65 °C to $+150$ °C
 Operating Temperature..... -40 °C to $+85$ °C
 Maximum ESD protection..... 2 kV
 Maximum Power Supply..... 5.5 V
 Maximum Input Current..... ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

$V_{DD} = V_{DDC} = 3.3$ V $\pm 10\%$ or 2.5 V $\pm 5\%$, over the specified temperature range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		V_{SS}	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low Current ^[3]		–	–	–100	μ A
I_{IH}	Input High Current ^[3]		–	–	100	μ A
V_{OL}	Output Low Voltage ^[4]	$I_{OL} = 20$ mA	–	–	0.4	V
V_{OH}	Output High Voltage ^[4]	$I_{OH} = -20$ mA, $V_{DD} = 3.3$ V	2.5	–	–	V
		$I_{OH} = -20$ mA, $V_{DD} = 2.5$ V	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	$V_{DD} = 3.3$ V, Outputs @ 100 MHz, CL = 30 pF	–	130	–	mA
		$V_{DD} = 3.3$ V, Outputs @ 160 MHz, CL = 30 pF	–	225	–	
		$V_{DD} = 2.5$ V, Outputs @ 100 MHz, CL = 30 pF	–	95	–	
		$V_{DD} = 2.5$ V, Outputs @ 160 MHz, CL = 30 pF	–	160	–	
Z_{Out}	Output Impedance	$V_{DD} = 3.3$ V	12	15	18	W
		$V_{DD} = 2.5$ V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Notes

- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.

AC Electrical Specifications

$V_{DD} = V_{DDC} = 3.3\text{ V} \pm 10\%$ or $2.5\text{ V} \pm 5\%$, over the specified temperature range^[5]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{max}	Input Frequency ^[6]	$V_{DD} = 3.3\text{ V}$	–	–	200	MHz
		$V_{DD} = 2.5\text{ V}$	–	–	170	
T_{pd}	TTL_CLK To Q Delay ^[6]		5.0	–	11.5	ns
F_{outDC}	Output Duty Cycle ^[6, 7]	Measured at $V_{DD}/2$	45	–	55	%
t_{pZL}, t_{pZH}	Output enable time (all outputs)		2	–	10	ns
t_{pLZ}, t_{pHZ}	Output disable time (all outputs)		2	–	10	ns
T_{skew}	Output-to-Output Skew ^[6, 8]		–	150	250	ps
$T_{skew(pp)}$	Part-to-Part Skew ^[9]		–	2.0	4.5	ns
T_r/T_f	Output Clocks Rise/Fall Time ^[8]	0.8 V to 2.0 V, $V_{DD} = 3.3\text{ V}$	0.10	–	1.0	ns
		0.6 V to 1.8 V, $V_{DD} = 2.5\text{ V}$	0.10	–	1.3	

Notes

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. 50% input duty cycle.
8. See [Figure 1 on page 5](#).
9. Part-to-Part skew at a given temperature and voltage.

Figure 1. LVCMOS_CLK CY29946 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

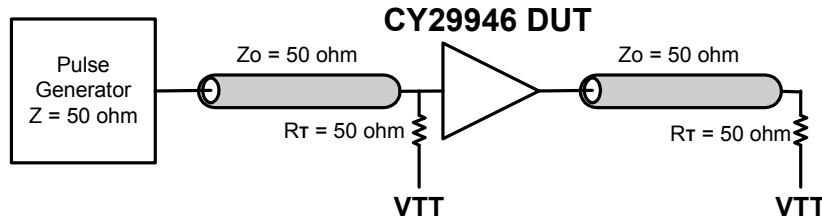


Figure 2. LVCMOS Propagation Delay (T_{PD}) Test Reference

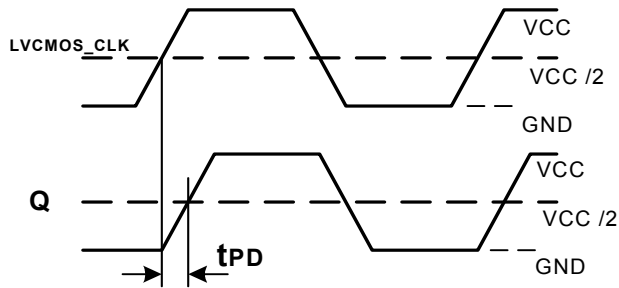


Figure 3. Output Duty Cycle (F_{outDC})

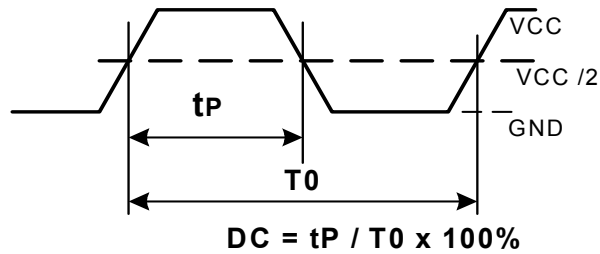
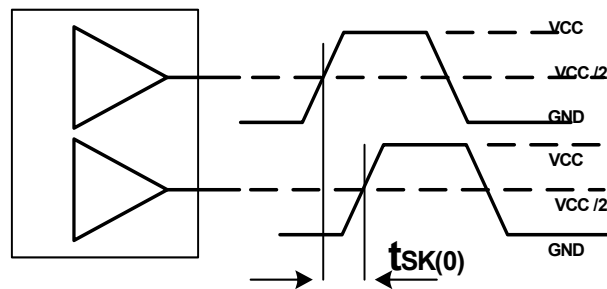


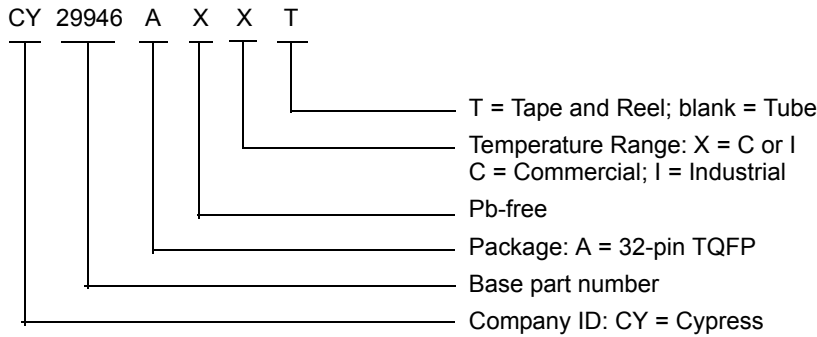
Figure 4. Output-to-Output Skew $t_{sk(0)}$



Ordering Information

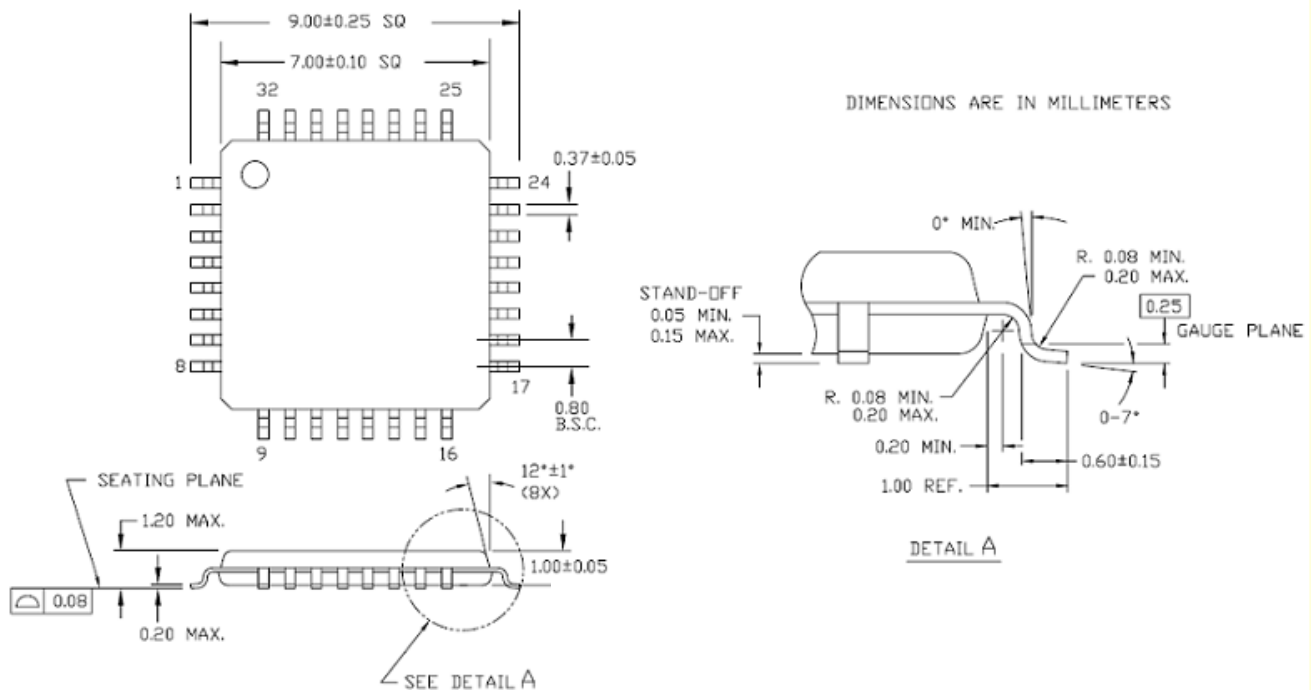
Part Number	Package Type	Production Flow
CY29946AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29946AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to +70 °C
CY29946AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29946AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to +85 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 5. 32-pin TQFP 7 × 7 × 1.0 mm A3210



51-85063 °C

Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
LVC MOS	low voltage complementary metal oxide semiconductor
LV TTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts

Document History Page

Document Title: CY29946, 2.5 V or 3.3 V, 200-MHz, 1:10 Clock Distribution Buffer				
Document Number: 38-07286				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111097	02/07/02	BRK	New data sheet
*A	116780	08/15/02	HWT	Added the commercial temperature range in the Ordering Information
*B	122878	12/22/02	RBI	Added power-up requirements to Maximum Ratings
*C	130007	10/15/03	RGL	Fixed the block diagram. Fixed the MK/OE# description in the pin description table.
*D	131375	11/21/03	RGL	Updated document history page (revision *C) to reflect changes that were not listed.
*E	221587	See ECN	RGL	Minor Change: Moved up the word Block Diagram in the first page.
*F	2899714	03/26/10	BRIJ/CXQ	Removed inactive parts from the ordering table. Updated package diagram
*G	3254185	05/11/2011	CXQ	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2002-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.