Three-PLL General-Purpose EPROM Programmable Clock Generator

Features

- **Three integrated phase-locked loops**
- **EPROM programmability**
- **Factory-programmable (CY2292) or field-programmable (CY2292F) device options**
- **Low-skew, low-jitter, high-accuracy outputs**
- **Power-management options (Shutdown, OE, Suspend)**
- **Frequency select option**
- **Smooth slewing on CPUCLK**
- **Configurable 3.3V or 5V operation**
- **16-pin SOIC Package (TSSOP: F only)**

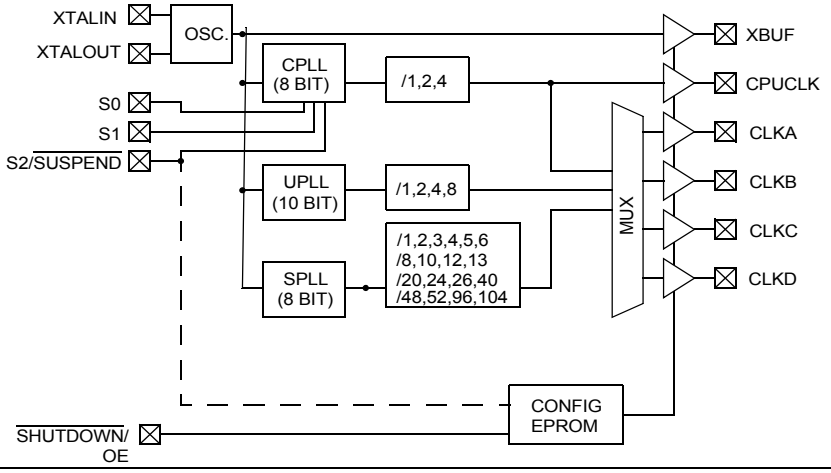
Benefits

- **Generates up to three custom frequencies from external sources**
- **Easy customization and fast turnaround**
- **Programming support available for all opportunities**
- **Meets critical industry standard timing requirements**
- **Supports low-power applications**
- **Eight user-selectable frequencies on CPU PLL**
- **Allows downstream PLLs to stay locked on CPUCLK output**
- **Enables application compatibility**
- **Industry-standard packaging saves on board space**

Selector Guide

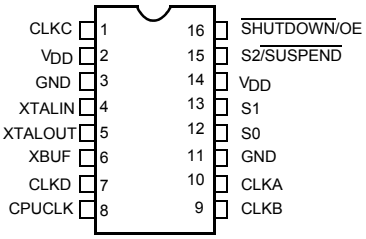
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2292	6	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2292I	6	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2292F	6	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V)	***Field Programmable*** Commercial Temperature
CY2292FI	6	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–80 MHz (5V) 76.923 kHz–60.0 MHz (3.3V)	***Field Programmable*** Industrial Temperature
CY2292FZ	6	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V)	***Field Programmable*** Commercial Temperature

Logic Block Diagram



Pin Configurations

CY2292
16-pin SOIC



Pin Summary

Name	Pin Number CY2292	Description
CLKC	1	Configurable clock output C.
V_{DD}	2, 14	Voltage supply.
GND	3, 11	Ground.
XTALIN[1]	4	Reference crystal input or external reference clock input.
XTALOUT[1, 2]	5	Reference crystal feedback.
XBUF	6	Buffered reference clock output.
CLKD	7	Configurable clock output D.
CPUCLK	8	CPU frequency clock output.
CLKB	9	Configurable clock output B.
CLKA	10	Configurable clock output A.
S0	12	CPU clock select input, bit 0.
S1	13	CPU clock select input, bit 1.
S2/SUSPEND	15	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.[3]
SHUTDOWN/OE	16	Places outputs in three-state[4] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[4] condition and does not shut down chip when LOW.

Operation

The CY2292 is a third-generation family of clock generators. The CY2292 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock generation needs of modern motherboards and other synchronous systems.

All parts provide a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs (CLKA–CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related[3] frequencies will have low ($\leq$ 500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2292 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator has been designed for 10-MHz to 25-MHz crystals, providing additional flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

Output Configuration

The CY2292 has four independent frequency sources on-chip. These are the reference oscillator, and three Phase-Locked Loops (PLLs). Each PLL has a specific function. The System PLL (SPLL) provides fixed output frequencies on the configurable outputs. The SPLL offers the most output frequency divider options. The CPU PLL (CPLL) is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The Utility PLL (UPLL) provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times. Please refer to the application note *Understanding the CY2291, CY2292, and CY2295* for information on configuring the part.

Notes:
1. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF or 18 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
3. Please refer to application note “Understanding the CY2291, CY2292 and CY2295” for more information.
4. The CY2292 has weak pull-downs on all outputs. Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Power-Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 50 μA (for commercial temperature or 100 μA for industrial temperature). After leaving shutdown mode, the PLLs will have to relock. All outputs have a weak pull-down so that the outputs do not float when three-stated.[4]

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[3]

The CPUCLK can slew (transition) smoothly between 20 MHz and the maximum output frequency (100 MHz at 5V/80 MHz at 3.3V for Commercial Temp. parts or 90 MHz at 5V/66.6 MHz at 3.3V for Industrial Temp. and for field-programmed parts). This feature is extremely useful in “Green” PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium® processor slewing requirements.

CyClocks Software

CyClocks™ is an easy-to-use application that allows you to configure any one of the EPROM-programmable clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. CyClocks also has a power calculation feature that allows you to see the power consumption of your specific configuration. You can download a copy of CyClocks for free on Cypress’s web site at www.cypress.com.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmer is a portable programmer designed to custom program our family of EPROM Field Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Custom Configuration Request Procedure

The CY229x are EPROM-programmable devices that may be configured in the factory or in the field by a Cypress Field Application Engineer (FAE). The output frequencies requested will be matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress FAE or sales representative. The method to use to request custom configurations is:

Use CyClocks software. This software automatically calculates the output frequencies that can be generated by the CY229x devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free of charge from the Cypress web site (http://www.cypress.com) or from your local sales representative.

Once the custom request has been processed you will receive a part number with a 3-digit extension (e.g., CY2292SC-128) specific to the frequencies and pinout of your device. This will be the part number used for samples requests and production orders.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... 260°C

Junction Temperature ..... 150°C

Package Power Dissipation ..... 750 mW

Static Discharge Voltage ..... ≤ 2000V (per MIL-STD-883, Method 3015)

Operating Conditions[5]

Parameter	Description	Part Numbers	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V operation	All	4.5	5.5	V
V_{DD}	Supply Voltage, 3.3V operation	All	3.0	3.6	V
T_A	Commercial Operating Temperature, Ambient	CY2292/CY2292F	0	+70	°C
	Industrial Operating Temperature, Ambient	CY2292I/CY2292FI	–40	+85	°C
C_{LOAD}	Max. Load Capacitance 5.0V Operation	All		25	pF
C_{LOAD}	Max. Load Capacitance 3.3V Operation	All		15	pF
f_{REF}	External Reference Crystal	All	10.0	25.0	MHz
	External Reference Clock[6, 7, 8]	All	1	30	MHz

Electrical Characteristics, Commercial 5.0V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V			<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Commercial	V_{DD} = V_{DD} max., 5V operation			75	100	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active	CY2292/CY2292F		10	50	µA

Electrical Characteristics, Commercial 3.3V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V			< 1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Commercial	V_{DD} = V_{DD} Max., 3.3V operation			50	65	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active	CY2292/CY2292F		10	50	µA

Notes:

5. Electrical parameters are guaranteed by design with these operating conditions, unless otherwise noted.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
7. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
8. The oscillator circuit is optimized for a crystal reference and for external reference clocks up to 20 MHz. For external reference clocks above 20 MHz, it is recommended that a 150Ω pull-up resistor to V_{DD} be connected to the Xout pin.
9. Xtal inputs have CMOS thresholds.
10. Load = Max., V_{IN} = 0V or V_{DD}, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06•(F_{CPLL}+F_{UPLL}+2•F_{SPLL})+0.27•(F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPUCLK}+F_{XBUF})$.

Electrical Characteristics, Industrial 5.0V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD} – 0.5V$			<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Industrial	$V_{DD} = V_{DD}$ Max., 5V operation			75	110	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active	CY2292I/CY2292FI		10	100	µA

Electrical Characteristics, Industrial 3.3V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD} – 0.5V$			<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Industrial	$V_{DD} = V_{DD}$ Max., 3.3V operation			50	70	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active	CY2292I/CY2292FI		10	100	µA

Switching Characteristics, Commercial 5.0V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	CY2292	10 (100 MHz)		13000 (76.923 kHz)	ns
			CY2292F	11.1 (90 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHz		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHz		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 14]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ms

Notes:
11. XBUF duty cycle depends on XTALIN duty cycle.
12. Measured at 1.4V.
13. Measured between 0.4V and 2.4V.
14. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the application note: *Jitter in PLL-Based Systems*.

Switching Characteristics, Commercial 5.0V (continued)

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)			<250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2292	20		100	MHz
			CY2292F	20		90	MHz

Switching Characteristics, Commercial 3.3V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 3.3V operation	CY2292	12.5 (80 MHz)		13000 (76.923 kHz)	ns
			CY2292F	15 (66.6 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq$ 66 MHz		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] f_{OUT} < 66 MHz		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 14]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)			< 0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			< 0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			< 400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)			< 250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-up			< 25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-up			< 0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2292	20		80	MHz
			CY2292F	20		66.6	MHz

Switching Characteristics, Industrial 5.0V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	CY2292I	11.1 (90 MHz)		13000 (76.923 kHz)	ns
			CY2292FI	12.5 (80 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHz		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHz		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 14]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)			< 0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			< 0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			< 400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter ($f_{OUT} > 50$ MHz)			< 250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2292I	20		90	MHz
			CY2292FI	20		80	MHz

Switching Characteristics, Industrial 3.3V

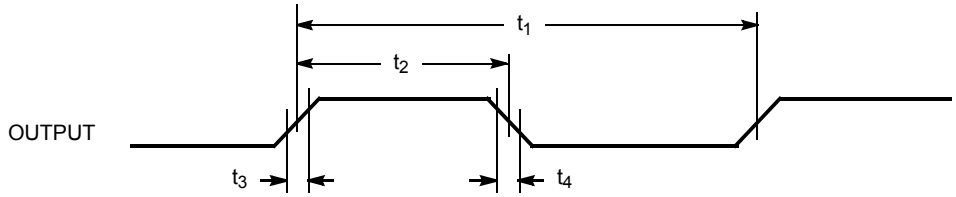
Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 3.3V operation	CY2292I	15 (66.6 MHz)		13000 (76.923 kHz)	ns
			CY2292FI	16.66 (60 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHz		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHz		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 14]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ms

Switching Characteristics, Industrial 3.3V (continued)

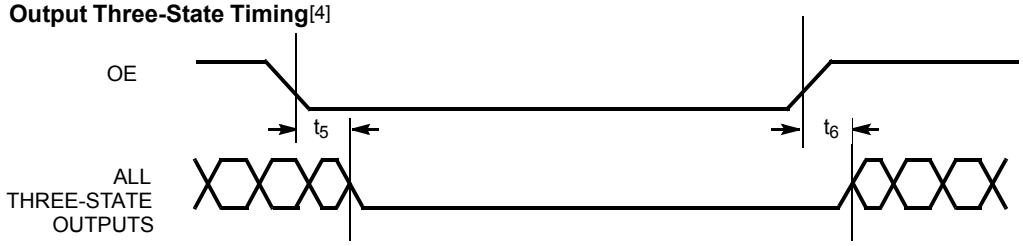
Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)			< 0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			< 0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			< 400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)			< 250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-up			< 25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-up			< 0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2292I	20		66.6	MHz
			CY2292FI	20		60	MHz

Switching Waveforms

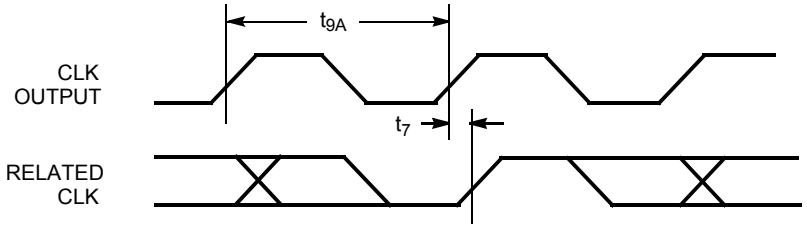
All Outputs, Duty Cycle and Rise/Fall Time



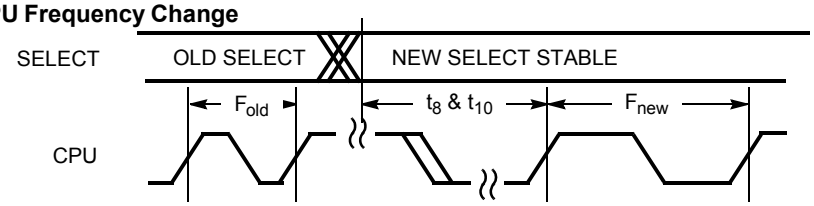
Output Three-State Timing[4]



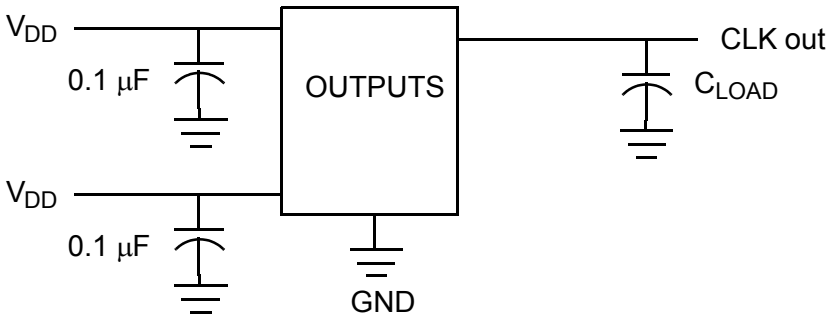
CLK Outputs Jitter and Skew



CPU Frequency Change



Test Circuit



Package Characteristics

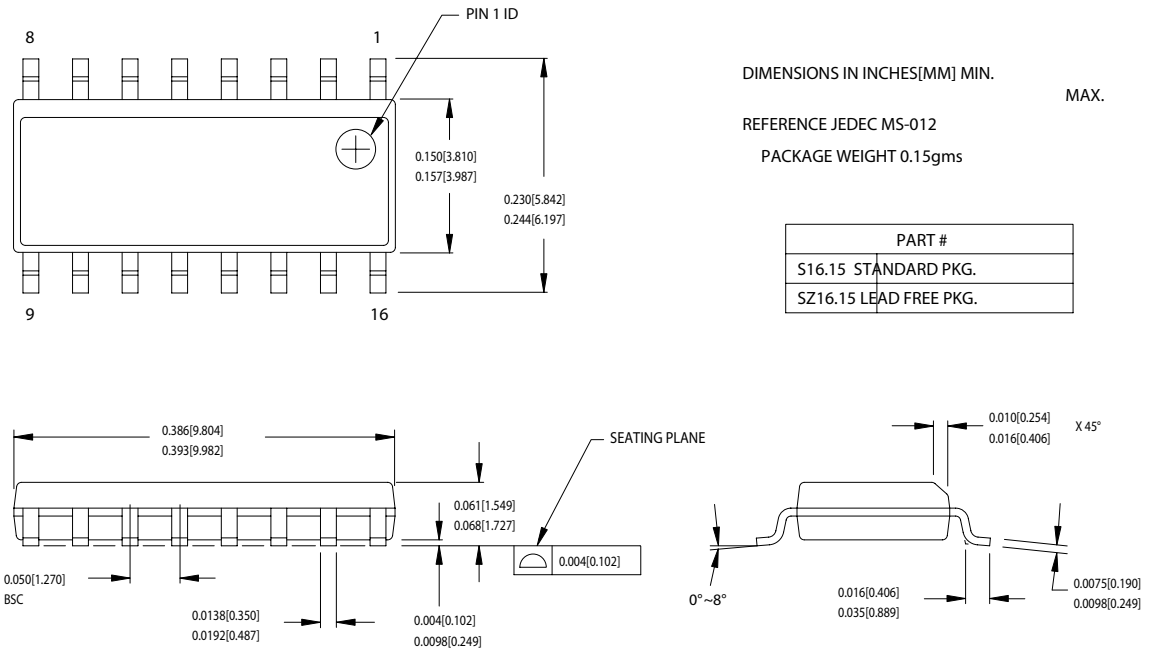
Package	θ_{JA} (C/W)	θ_{JC} (C/W)	Transistor Count
16-pin SOIC	83	19	9271

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY2292SC–XXX	16-Pin SOIC	Commercial	5.0V
CY2292SC–XXXT	16-Pin SOIC – Tape and Reel	Commercial	5.0V
CY2292SL–XXX	16-Pin SOIC	Commercial	3.3V
CY2292SL–XXXT	16-Pin SOIC – Tape and Reel	Commercial	3.3V
CY2292F	16-Pin SOIC	Commercial	3.3V or 5.0V
CY2292FT	16-Pin SOIC – Tape and Reel	Commercial	3.3V or 5.0V
CY2292SI–XXX	16-Pin SOIC	Industrial	3.3V or 5.0V
CY2292SI–XXXT	16-Pin SOIC – Tape and Reel	Industrial	3.3V or 5.0V
CY2292FI	16-Pin SOIC	Industrial	3.3V or 5.0V
CY2292FIT	16-Pin SOIC – Tape and Reel	Industrial	3.3V or 5.0V
CY2292FZ	16-Pin TSSOP	Commercial	3.3V or 5.0V
CY2292FZT	16-Pin TSSOP – Tape and Reel	Commercial	3.3V or 5.0V
Lead-Free			
CY2292SXC–XXX	16-Pin SOIC	Commercial	5.0V
CY2292SXC–XXXT	16-Pin SOIC – Tape and Reel	Commercial	5.0V
CY2292SXL–XXX	16-Pin SOIC	Commercial	3.3V
CY2292SXL–XXXT	16-Pin SOIC – Tape and Reel	Commercial	3.3V
CY2292FXC	16-Pin SOIC	Commercial	3.3V or 5.0V
CY2292FXCT	16-Pin SOIC – Tape and Reel	Commercial	3.3V or 5.0V
CY2292SXI–XXX	16-Pin SOIC	Industrial	3.3V or 5.0V
CY2292SXI–XXXT	16-Pin SOIC – Tape and Reel	Industrial	3.3V or 5.0V
CY2292FXI	16-Pin SOIC	Industrial	3.3V or 5.0V
CY2292FXIT	16-Pin SOIC – Tape and Reel	Industrial	3.3V or 5.0V
CY2292FZX	16-Pin TSSOP	Commercial	3.3V or 5.0V
CY2292FZXT	16-Pin TSSOP – Tape and Reel	Commercial	3.3V or 5.0V

Package Diagrams

16-Lead (150-Mil) SOIC S16.15



DIMENSIONS IN INCHES[MM] MIN.
MAX.

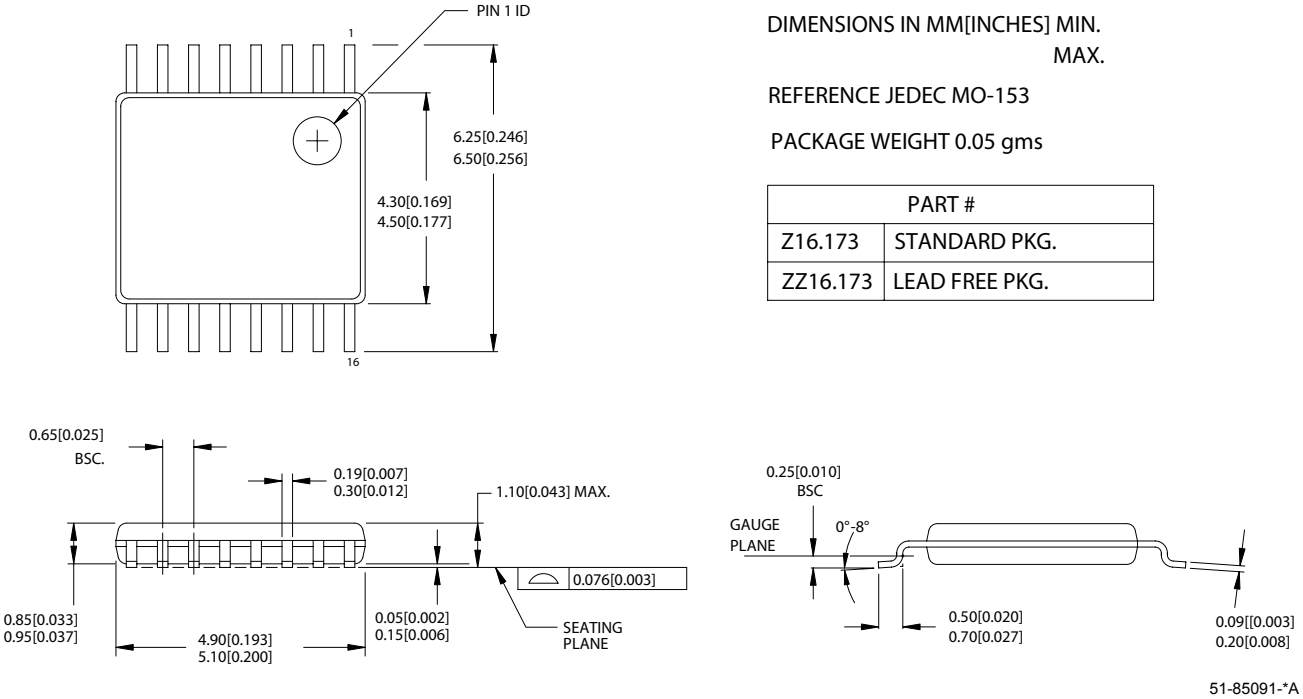
REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.

51-85068-*B

16-lead TSSOP 4.40 MM Body Z16.173



DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.

51-85091-*A

Document History Page

Document Title: CY2292 Three-PLL General-Purpose EPROM Programmable Clock Generator Document Number: 38-07449				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116993	07/01/02	DSG	Changed from Spec number: 38-00946 to 38-07449
*A	119639	12/05/02	CKN	Changed 8 MHz to 20 MHz in Power-saving Features
*B	277130	See ECN	RGL	Added Lead-free Devices
*C	395808	See ECN	RGL	Minor Change: fixed the typo in the ordering code